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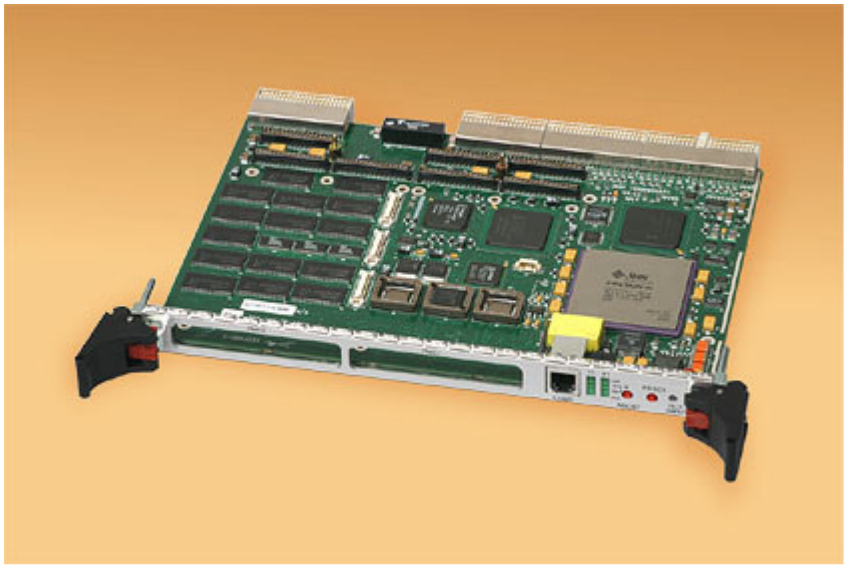
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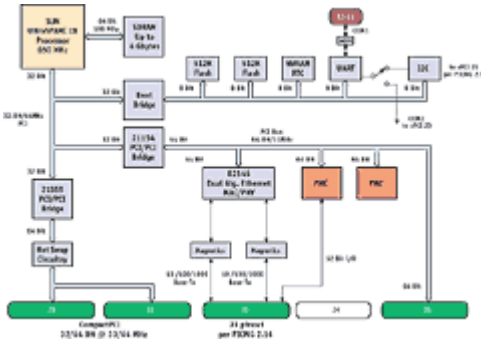
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Gigabit Ethernet for PICMG 2.16, High Performance, Low Power, 2 PMC Slots



A CompactPCI 6U form factor Single Board Computer that is designed for high performance embedded applications. It utilizes the Sun Microsystems UltraSPARC-IIi+ processor and supports up to 4 Gbytes of SDRAM Memory.



Larger View of Block Diagram

Occupies a single system or non-system slot in a standard CompactPCI chassis. The board automatically detects whether it is installed in a system or non-system slot and configures itself accordingly.

The board has two Gigabit Ethernet (copper) ports implementing PICMG 2.16, and has a full 64-bit PCI interface to a rear I/O module for virtually unlimited I/O capability. Two PMC slots are provided for user hardware expansion, one with rear I/O PIM support.

Feature Set

• SUN Microsystems UltraSPARC-IIi + (V9 architecture with VIS instruction set) operating at 650 MHz. The CPU has 16 Kbytes of L1 instruction cache, 16 Kbytes of L1 data cache, and an internal 512 Kbytes L2 unified cache (all caches 4-way set associative).
• Single slot 6U CompactPCI (PICMG 2.0 R3.0) board supporting auto-sensing of system or

non-system slot functionality.
• Hot Swappable (PICMG 2.1 R2.0).
• BMC or Standard Node capability per PICMG 2.9 R1.0 System Management Specification.
• Temperature and voltage sensors provide real time feed back for critical applications.
• 2 level Watchdog timer.
• Compact PCI connector J4 not populated to avoid conflict with H.110 Computer Telephony bus.
• Open boot firmware.
• Power on Self-Test (POST).
• One LED for POST results and one user controlled LED.
• Solaris version 2.8

Memory and Storage:

• Up to 4 Gbytes SDRAM with ECC running at 108 MHz. 1-2 Gbytes SDRAM are soldered directly to the baseboard. An additional 1-2 Gbytes SDRAM can be added with a Momentum Expansion Memory Module (MEMM). (The MEMM module shares its location with one of the two PMC slots: see below).
• Two socketed 512K byte Flash PROMs. Both are selectable as boot device via a jumper. One is reserved for Open Firmware; the other is free for user data, programs or NVRAM data backup.
• 32 Kbytes of NVRAM and Real Time Clock.

Versatile I/O:

on main board:

• Two 10/100/1000 BaseT Gigabit Ethernet ports routed to PICMG 2.16 packet switched backplane connection on J3.
• Two 64-bit, 33 MHz, PMC slots (IEEE P1386 / P1386.1)1. One PMC slot has rear I/O PIM support. The other PMC slot shares its location with the memory mezzanine so going beyond 2G of SDRAM prevents the use of the second PMC slot.
• 64-bit PCI interface to rear I/O module for virtually unlimited I/O options. *Rear I/O modules are currently available with SCSI, Ethernet and serial ports.*
• RS-232 communication port interfaces to front panel RJ11 connector or cPCI J3 for rear I/O.

Version *with 500 MHz UltraSPARC IIe*:

Also available with the UltraSPARC IIe running at 500 MHz. This version has 256 Kbytes of L2 cache and supports 2 Gbytes of SDRAM: 1 Gbyte on the baseboard plus a 1 Gbyte SDRAM mezzanine. With the 500 MHz UltraSPARC-IIe, the SDRAM runs at 100 MHz.

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