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CPIP5430 Single Board Computer and Transition Module

Installation and Use

CPIP5430A/IH2

June 2004 Edition

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Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. If the equipment is supplied with a three-conductor AC power cable, the power cable must be plugged into an approved three-contact electrical outlet, with the grounding wire (green/yellow) reliably connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards and local electrical regulatory codes.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in any explosive atmosphere such as in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment could result in an explosion and cause injury or damage.

Keep Away From Live Circuits Inside the Equipment.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Service personnel should not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, such personnel should always disconnect power and discharge circuits before touching components.

Use Caution When Exposing or Handling a CRT.

Breakage of a Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, do not handle the CRT and avoid rough handling or jarring of the equipment. Handling of a CRT should be done only by qualified service personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that all safety features are maintained.

Observe Warnings in Manual.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.



Warning

To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

Flammability

All Motorola PWBs (printed wiring boards) are manufactured with a flammability rating of 94V-0 by UL-recognized manufacturers.

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This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used with adequate EMI protection.

Lithium Battery Caution

This product contains a lithium battery to power the clock and calendar circuitry.



Danger of explosion if battery is replaced incorrectly. Replace battery only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to the manufacturer's instructions.



Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabricant.



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About This Manual

The *CPIP5430 Single Board Computer Installation and Use* manual provides the information you will need to install and configure your CPIP5430 board and the CPIP5430-RTM01 rear transition module. It provides specific preparation and installation information, and data applicable to the board.

As of the printing date of this manual, the CPIP5430 supports the models listed below.

Model Number	Description
CPIP5430-2131-K CPIP5430-2131-F	Intel Pentium 4 CPU, 2.16 I/O, 1.7GHz, 1GB (2x512MB) memory
CPIP5430-2232-K CPIP5430-2232-F	Intel Pentium 4 CPU, 2.16 I/O, 1.7GHz, 1GB (2x512MB) memory, 1HDD
CPIP5430-2241-K CPIP5430-2241-F	Intel Pentium 4 CPU, 2.16 I/O, 1.7GHz, 2GB (2x1GB) memory
CPIP5430-2242-K CPIP5430-2242-F	Intel Pentium 4 CPU, 2.16 I/O, 1.7GHz, 2GB (2x1GB) memory, 1HDD
CPIP5430-4231-K CPIP5430-4231-F	Intel Pentium 4 CPU, 2.16 I/O, 2.2GHz, 1GB (2x512MB) memory
CPIP5430-4232-K CPIP5430-4232-F	Intel Pentium 4 CPU, 2.16 I/O, 2.2GHz, 1GB (2x512MB) memory, 1HDD
CPIP5430-4241-K CPIP5430-4241-F	Intel Pentium 4 CPU, 2.16 I/O, 2.2GHz, 2GB (2x1GB) memory
CPIP5430-4242-K CPIP5430-4242-F	Intel Pentium 4 CPU, 2.16 I/O, 2.2GHz, 2GB (2x1GB) memory, 1HDD
CPIP5430-4251-K CPIP5430-4251-F	Intel Pentium 4 CPU, 2.16 I/O, 2.2GHz, 4GB (2x2GB) memory

Model Number	Description
CPIP5430-4452-K CPIP5430-4452-F	Intel Pentium 4 CPU, 2.16 I/O, 2.2GHz, 4GB (2x2GB) memory, 1HDD
CPIP5430-MEM1-K	Memory, 512MB: Max 2 per CPIP5430
CPIP5430-MEM2-K	Memory, 1.0GB: Max 2 per CPIP5430
CPIP5430-MEM3-K	Memory, 2.0GB: Max 2 per CPIP5430

Summary of Changes

This manual has been revised and should replace any previous editions. Below is a history of the changes affecting this manual.

Date	Change
June 2004	Updated BIOS screens to include ATAPI CDROM, SM-CDU5211 Drive, and MITSUMI USB FDD removeable drive. Added a note to alert user that the front panel USB port is used for maintenance only.

Overview of Contents

This manual is divided into the following chapters and appendices:

Chapter 1, *Hardware Preparation and Installation*, includes a description of the product, list of features, I/O interfaces, block diagram, required tools and equipment, jumper settings, and installation instructions for the memory module, the PMC or disk drive, and installation of the SBC in an MXP series chassis.

Chapter 2, *Startup and Operation*, provides the power-up procedure, identifies the switches and indicators, and explains how to generate a soft reset on the CPIP5430.

Chapter 3, *BIOS*, provides a description of the BIOS on the CPIP5430.

Chapter 4, *Functional Description*, describes the CPIP5430 on a block diagram level.

Chapter 5, *Rear Transition Module for CPIP5430*, describes the rear transition module which provides additional I/O and includes information for installing and configuring the CPIP5430-RTM1.

Chapter 6, *Connector Pin Assignments*, provides pin assignments for the connectors on the CPIP5430 single-board computer and CPIP5430-RTM01.

Appendix A, *Specifications*, provides environmental and mechanical specifications, as well as power requirements for the CPIP5430.

Appendix B, *Thermal Validation*, provides information to conduct thermal evaluations and identifies thermally significant components along with their maximum allowable operating temperatures.

Appendix C, *Memory Maps*, provides memory maps for the CPIP5430.

Appendix D, *IPMI Commands*, provides commands that may be used by a host device driver and/or application software to communicate with the Zircon, sensors, and other management controllers in the system.

Appendix E, *Related Documentation*, provides a listing of related Motorola manuals, vendor documentation, and industry specifications.

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Conventions Used in This Manual

The following typographical conventions are used in this document:

bold

is used for user input that you type just as it appears; it is also used for commands, options and arguments to commands, and names of programs, directories and files.

italic

is used for names of variables to which you assign values, for function parameters, and for structure names and fields. Italic is also used for comments in screen displays and examples, and to introduce new terms.

`courier`

is used for system output (for example, screen displays, reports), examples, and system prompts.

<Enter>, **<Return>** or **<CR>**

represents the carriage return or Enter key.

Ctrl

represents the Control key. Execute control characters by pressing the Ctrl key and the letter simultaneously, for example, Ctrl-d.

Hardware Preparation and Installation

1

Description

The CPIP5430 is a high performance, hot swappable peripheral slot board. It complies with PICMG 2.1, 2.9, and 2.16 specifications for 6U single slot form factor modules. Major features include: Intel Pentium Mobile P4 processor family, Intel 875P chipset with 6300 ESB, up to 4GB PC2100, dual Gigabit Ethernet interfaces for payload, separate Gigabit Ethernet interface for management, dual PMC sites, optional 2.5 inch hard drive, up to two COM ports, and up to three USB ports when used with the Rear Transition Module (RTM).

The controller features a single Mobile P4 Processor-M with 512KB L2 cache, 400 MHz to 800 MHz Front Side Bus (FSB) speed, and 266 MHz to 400 MHz DDR via two SODIMM sockets.

The CPIP5430 features both an Intel® 82547 Gigabit Ethernet (GbE) controller that can be configured for either front panel or rear transition module access and an Intel® 82546EB dual port Gigabit Ethernet (GbE) controller. These dual GbE connections are routed to the PICMG 2.16 compliant backplane.

In addition to high computing performance and communication capability, the CPIP5430 supports Intelligent Platform Management (IPMI) protocols based on PICMG 2.9 specifications for applications that require high reliability and serviceability. The CPIP5430 does not interface to the PCI bus common in CompactPCI backplanes.

Equipment Required

A typical CPIP5430 environment requires the following additional equipment:

- ❏ System enclosure, or available PICMG 2.16 slot in a system
- ❏ VGA monitor, VGA PMC, and USB keyboard, or serial terminal
- ❏ Operating system (may only require a kernel)
- ❏ Optional disk drive
- ❏ Optional CPIP5430-RTM1 Rear Transition Module
- ❏ USB mouse, floppy drive and/or CD/DVD drive, or IDE CD/DVD drive
- ❏ Connecting cables

Overview of Startup Procedures

The following table lists the things you will need to do before you can use this board and tells where to find the information you need to perform each step. Be sure to read this entire chapter, including all Caution and Warning notes, before you begin.

Table 1-1. Startup Overview

What you need to do...	Refer to...
Unpack the hardware.	*Unpacking Guidelines* on page 1-3
Prepare the hardware for insertion into a chassis.	*Hardware Preparation* on page 1-4
Ensure memory mezzanines are properly installed on the board	*Memory Module Installation* on page 1-9

Table 1-1. Startup Overview (continued)

What you need to do...	Refer to...
Install hard disk drive (if required)	*2.5-inch HDD Installation* on page 1-11
Install PMC module (if required)	*PCI Mezzanine Card Installation* on page 1-13
Install the CPIP5430 in the chassis	*Installing a Board* on page 1-15
Install transition module into chassis (optional).	*Installing the RTM* on page 5-7

Unpacking Guidelines

Unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Verify that the coin cell battery is in its holder and inserted correctly. Save the packing material for storing and reshipping of equipment.

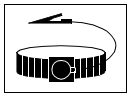
Note If the shipping carton is damaged upon receipt, request that the carrier's agent be present during the unpacking and inspection of the equipment.



Caution

Avoid touching areas of integrated circuitry; static discharge can damage circuits.

Use ESD



Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules can be extremely sensitive to electrostatic discharge (ESD). After removing the component from its protective wrapper or from the system, place the component flat on a grounded, static-free surface (and, in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an active electrical ground. Note that a system chassis may not be grounded if it is unplugged.



Caution Inserting or removing modules with power applied may result in damage to module components.



Warning Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

Hardware Preparation

The CPIP5430 is designed to PICMG (2.1, 2.9, 2.16) specifications and as such, is a general-purpose, universal slot card. Before using this card, you should review the specifications of any chassis and backplane intended to house the CPIP5430 to determine the presence of, and any limitations of, the IPMI bus, switched Ethernet, and user defined pinouts. As an example, some chassis backplanes route certain I/O pins to internal resources such as alarm cards, drive resources, or route PCI signals to failover circuitry or extension bridges.

The CPIP5430 is intended for chassis/backplanes where J5 connectors are all pass-through connections to a rear transition module and J3 connections are to a switched Ethernet fabric and pass-through connections to a rear transition module. Also, J3 and J5 provide power from the CPIP5430 to the rear transition module. It is your responsibility to verify this system compatibility. Failure to do so could result in improper operation or equipment damage.

Note The CPIP5430 is intended for use within the Motorola Computer Group MXP Series Platforms.

Most options on the CPIP5430 are software configurable. Configuration changes are made by setting bits in control registers after the board is installed in a system.

Figure 1-1 illustrates the placement of the jumpers, headers, connectors, and various other components on the CPIP5430. Connectors and configurable headers are listed in the following table.

Table 1-2. CPIP5430 Connectors and Headers

Reference Designator	Description
J1	Backplane connector, power, CPCI control, IPMI, ground
J2	Backplane connector, ground, CPCI control
J3	Backplane connector, User I/O
J5	Backplane connector, User I/O
J18	IDE connector, 44-pin
J17	Serial COM1 connector, RJ45, 8-pin
J16	Ethernet connector, RJ45 8-pin connector
J14	USB connector, 4-pin (for development, service, and setup operations only)
J13	Reserved
J12	Reserved
J11	PCI mezzanine connector, 64-pin
J10	PCI mezzanine connector, 64-pin
J9	PCI mezzanine connector, 64-pin
J8	PCI mezzanine connector, 64-pin
J7	PCI mezzanine connector, 64-pin

Table 1-2. CPIP5430 Connectors and Headers (continued)

Reference Designator	Description
J6	PCI mezzanine connector, 64-pin
J5	PCI mezzanine connector, 64-pin
E4	Ethernet signal header, 4-pin
E1	12V power for RTM USB control

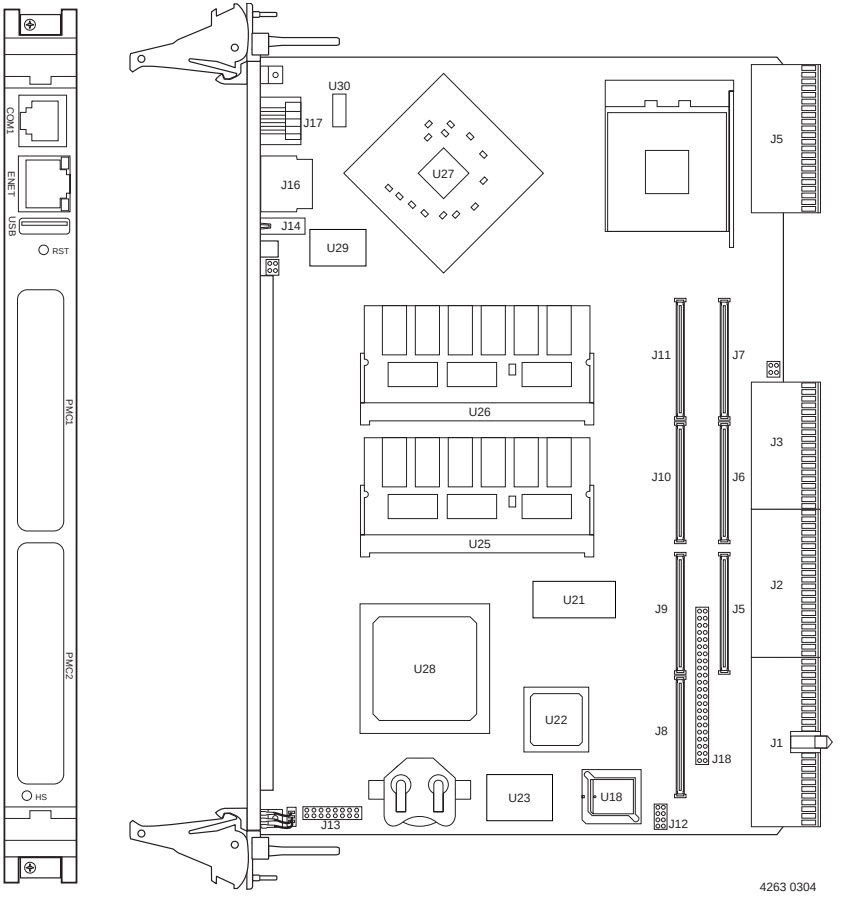


Figure 1-1. CPIP5430 Layout without Heat Sink

Hot Swap Considerations

The CPIP5430 is a CompactPCI form factor single board computer with hot swap capabilities. This allows insertion or removal of the board from a powered chassis without damage, with proper pin staging on the backplane. It does not employ a PCI bridge and can therefore be installed in a payload slot in an MXP3000 Series Platform chassis.

Insertion

The CPIP5430 supports live insertion. Live insertion makes on-board reset logic cause a reset. The reset signal routes directly into the board reset logic and ensures proper bootup.

- ✓ The chassis is powered up.
- ✓ The CPIP5430 is inserted into the MXP payload slot on the backplane. The blue LED is illuminated. When fully seated the ejector levers are closed, at which point the blue LED should go off after a short delay due to the IPMI controller.
- ✓ The system starts to boot.

Extraction

Following are the stages of extraction for a CPIP5430:

- ✓ When the ejector lever is opened, the IPMI control circuitry is signalled.
- ✓ The IPMI satellite controller communicates with the BMC and/or the resident OS. If software exists to interpret the ejector open event, it may communicate with the resident OS causing the board to properly shut down. If software exists to monitor the shutdown, it may also illuminate the blue LED to indicate that the board can safely be removed.

  Note While the IPMI controller will extinguish the blue LED when the ejector lever is closed upon insertion, it is the responsibility of software to illuminate the blue LED during extraction.

Hardware Installation

The following sections discuss the installation of memory modules, hard drives, and mezzanine cards on the CPIP5430 base board, the installation of the complete assembly into a chassis, and the system considerations relevant to installation. Before installing the CPIP5430, make sure that the serial ports and all jumpers are properly configured.

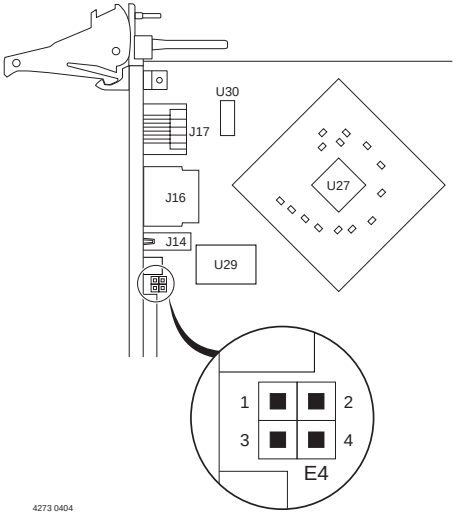
In most cases, memory modules and hard drives are already in place on the base board. The user-configured jumper, E4, is not easily accessible with a module installed. If you need to place a jumper, removing the module may be necessary.

Should it be necessary to install modules on the base board, refer to *PCI Mezzanine Card Installation* for a description of the procedure.

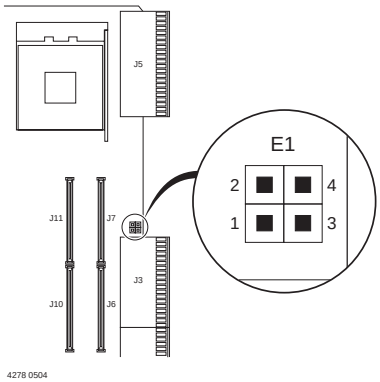
Configuring Headers

The following headers that can be configured are the Ethernet signal header (E4) and the 12 volt power for USB control to the RTM (E1). Please refer to the following figures and the next table for jumpering information.

Jumpering Diagram for Header E4



Jumpering Diagram for Header E1



Note The USB port on the front panel of the SBC is used for maintenance only. For data transfer in an end application, USB ports are available via the RTM.

Apply the jumpers according to the following table.

Jumper	Function	Setting
E4	Reserved Routes Ethernet signal to the RTM Routes Ethernet signal to the CPIP5430 front panel	[1-2] jumper off [3-4] jumper on [3-4] jumper off
E1	Default Standalone operation +12V power to RTM for USB control	{1-2, 3-4] no jumper [1-2] jumper on [3-4] jumper on

Memory Module Installation

The CPIP5430 depends upon a proprietary memory module and specialized signal routing to obtain densities of 2GB per SODIMM socket. All standard DDR SODIMM modules are compatible, however, 2GB is only achievable with the purchase of a special memory module.

The CPIP5430 SBC supports up to two slots of 144-pin, DDR2100 registered ECC SO-DIMMs. The maximum memory capacity is 4GB. The chipset supports 64MB, 128MB, 256MB, 512MB, 1GB, and 2GB memory module sizes. The supported DRAM types are listed in the following table. All standard 128-Mb, 256-Mb and 512-Mb technologies and addressing are supported for x16 and x8 devices.

The DDR speed, type and size can be determined from the BIOS reading the DIMM Serial Presence Detect (SPD) bits on the SMBus. The DDR timing register, which provides the DDR speed control for the entire array, must be programmed to use the parameters of the slowest installed DDRs. The DDR interface supports 128Mb, 256Mb, and 512Mb technology, which allows up to 1GB per double-sided SODIMM. The CPIP5430 supports up to 4GB of SDRAM memory with two 144-pin SO-DIMMs. The memory configurations are summarized in the following table.

Model Number	**CPIP5430-2231/4231 CPIP5430-2232/4232**	**CPIP5430-2241/4241 CPIP5430-2242/4242**	**CPIP5430-4251-4452**
Memory Sockets	2	2	2
Max. Memory	1GB	2GB	4GB
SODIMM Size	512MB	1GB	2GB
SODIMM Quantity	2	2	2
PMC slots	2:1	2:1	2:1
IDE Hard Drives	0:1	0:1	0:1

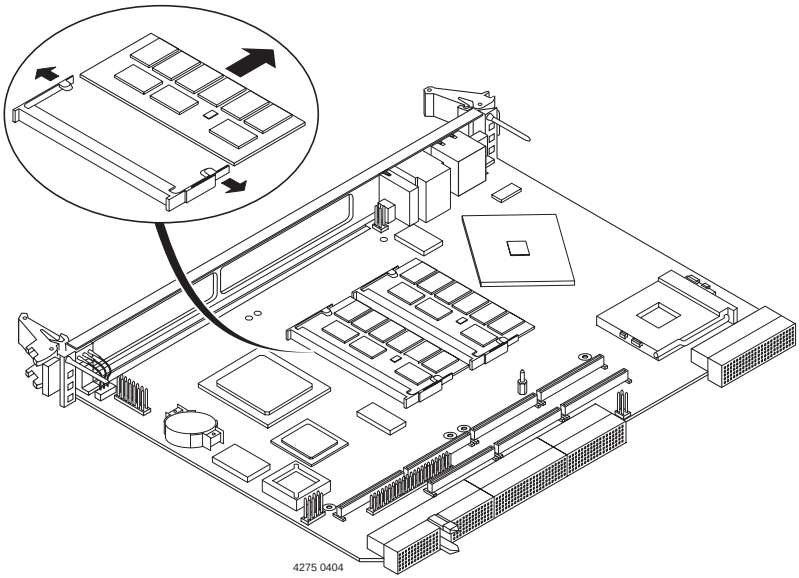
The CPIP5430 has been tested with 128MB, 256MB, 512MB, 1GB, and 2GB registered, ECC SODIMM modules.

To install the memory module, follow these steps.

1. Remove the CPIP5430 from the chassis and place it on a static free surface.

   Note The following illustration may not represent the exact board you are using, it is meant for illustration purposes only.

2. Insert a vendor-approved DIMM into one of the slots located on the top side of the board.
3. Press firmly until the DIMM is seated into the slot. It should click into place.



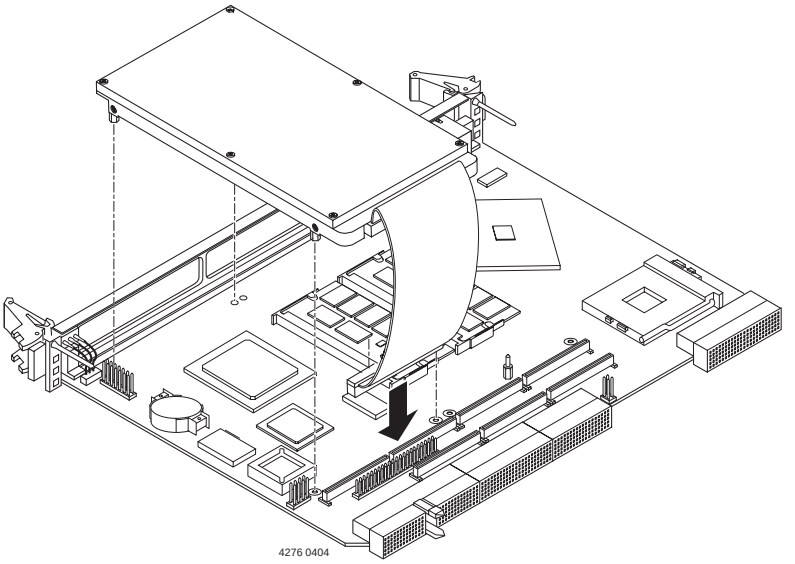
2.5-inch HDD Installation

One slim-line 2.5-inch HDD can be installed on the CPIP5430 controller instead of a standard PMC, if not already installed from the factory.

The following procedure describes how to mount a 2.5 inch hard disk drive on one of the PMC sites of the CPIP5430. If the CPIP5430 is currently installed in a system chassis, perform the following steps.

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. Keep the ESD secured throughout this procedure.
2. Shut down the operating system.
3. Remove the chassis or system cover(s) as necessary.

4. Carefully remove the CPIP5430 from its slot and lay it flat, with connectors J1 through J5 facing you.
5. Remove the PMC key-bolts of the second PMC slot.



6. Bolt the carrier rails onto the sides of the 2.5" HDD. The flange on each rail should be facing away from the drive.
7. Attach the 44-pin IDE cable to the drive.
8. Install the drive assembly onto the top side of the board and tighten the four screws from the bottom side of the board to secure the drive firmly (avoid overtightening).
9. Connect the 44-pin IDE cable to the J18 IDE connector on board.

PCI Mezzanine Card Installation

You can mount one +3.3V or Universal PCI Mezzanine Card (PMC) on each PMC site of the CPIP5430, presuming a hard drive has not been installed in PMC slot 2, either from the factory or by following the procedure previously outlined in this document.

The board's PMC sites are keyed for a +3.3V PCI bus interface and will not accept other PMCs with different voltage requirements. Removing the key may be necessary when attaching +3.3v or **universal** PMCs with components that cover the key location (such as hard drive/controller modules); removing the key DOES NOT CHANGE the bus voltage. To install a PMC on a CPIP5430 that is currently installed in a chassis, refer to the figure on page 1-14 and perform the following steps. If you are installing a PMC on a board that has not yet been installed in a chassis, begin with step 6.

Some devices, such as IDE connector components may restrict proper seating of PMCs that populate the PMC1 site. If this occurs, do not attempt to install a PMC on that site.

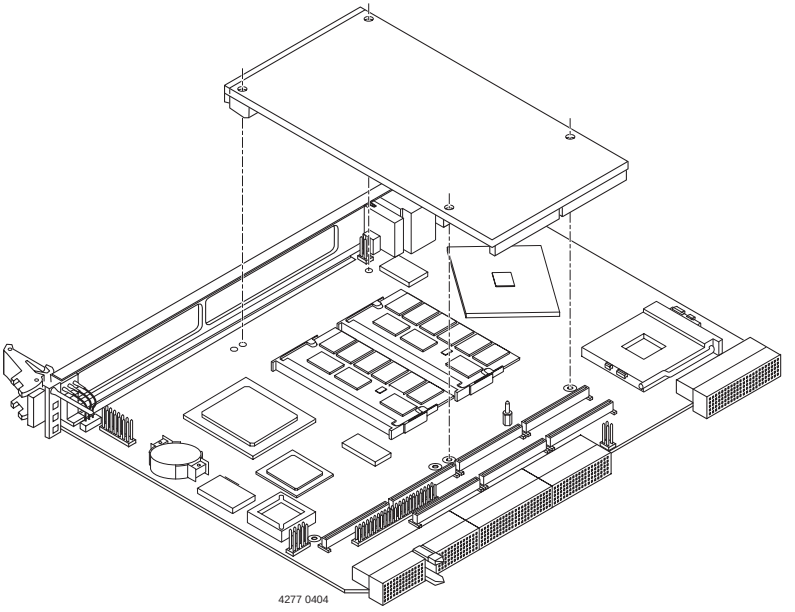
1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. Keep the ESD secured throughout this procedure.
2. Shut down the operating system.
3. Remove the chassis or system cover(s) as necessary.
4. Carefully remove the CPIP5430 from its slot and lay it flat, with connectors J1 through J5 facing you.
5. Avoid touching areas of integrated circuitry. Electrostatic discharge can damage these circuits.
6. Remove the PMC filler(s) from the front panel.

   Note The following illustration may not represent the exact board you are using, it is meant for illustration purposes only.

7. From behind the front panel, slide the edge connector of the PMC module into the PMC 1 front panel opening and place the PMC

module on top of the base board. The four PMC connectors on the underside of the PMC module should then connect smoothly with the corresponding PMC connectors on the CPIP5430 and properly align the PMC VIO keying pin.

8. Insert the four screws through the holes on the bottom side of the CPIP5430 and tighten the screws.



9. Reinstall the CPIP5430 in its proper slot. Be sure the module is well seated in the backplane connectors.

10. If necessary, connect the system to its AC or DC power source and turn the power on.

Note The rear I/O signals on the J6 pins of the PMC 1 slot are routed to the J3 connector on the CPIP5430 baseboard. Verify pin compatibility with the backplane prior to using.

The rear I/O routing is unique and only compatible with the RTM for the CPIP5430 SBC.

If you mount the HDD on the main board, the HDD will occupy the second PMC slot connector. Refer to *2.5-inch HDD Installation* on page 1-11 in this chapter.

Before You Install a Board

All payload boards used in the MXP3000 Series Platforms are 6U x 160mm and 4HP wide and are compliant with the IEEE1101.1, IEEE1101.10, and CompactPCI 2.0 specifications. These specifications define the placement of all mechanical components including connectors, front panel and alignment features, injector / ejector handle feature, and component outlines.

Caution

Carefully inspect your board prior to installation for both pin and component integrity. When installing payload boards we recommend that you start at the left of the cardcage and work to the right. Installation into a fully populated chassis should be performed with caution to avoid damage to the pins and components located on the front or back sides of the board, especially when installing the final boards.

Installing a Board

MCG and our suppliers take significant steps to ensure there are no bent pins on the backplane or connector damage to the boards prior to leaving our factory. Bent pins caused by improper installation or by boards with damaged connectors could void the MCG warranty for the backplane or boards. If a system contains one or more crushed pins, power off the system and contact your local sales representative to schedule delivery of a replacement chassis assembly.

Caution

Prevent possible damage to module components by verifying the proper MXP slot usage for your configuration.

Card cage rail guide description for MXP:
Switch Slot = Red
AMC Slots = Tan
Payload Slots = Black

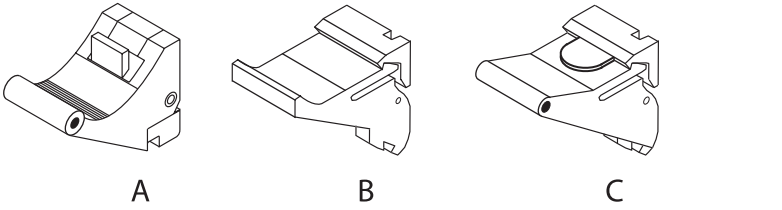
Caution

Insert the board by holding the ejector lever—do not exert unnecessary pressure on the faceplate.

You can remove hot-swap modules without removing the system's power.

Depending on your platform configuration, the modules you install may have different ejector handles and latching mechanisms. The following illustration shows the typical board ejector handles used with the MXP platform. A: Elma Latching, B: Rittal Type II, C: Rittal Type IV.

All handles are compliant with the CompactPCI specification and are designed to meet the IEEE1101.10 standards.

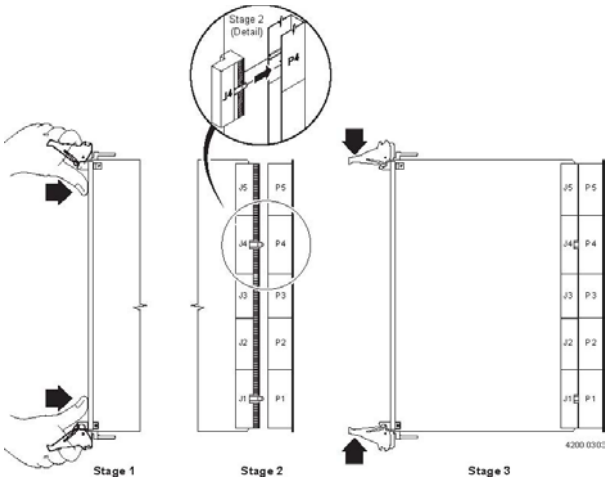


To reduce the risk of pin damage, refer to the following illustration and perform these steps when installing modules.

Note The following illustration may not represent the exact board you are using, it is meant for illustration purposes only.

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to an electrical ground (refer to *Unpacking Guidelines* on page 1-3). The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Remove any filler panel that might fill that slot.

3. Ensure that the two handles are in the outward position.The CPIP5430 ejector handle is a Rittal Type IV (C) and has a red tab or button on the lever. Push the red button and press the ejector lever outward.



4. Verify the proper slot for the module you are inserting. Orient the board and align it with the black card cage rail guides.

5. Insert the board by holding the ejector lever — you may need to gently press on the upper faceplate to help insert the board in its slot.

   Apply equal and steady pressure using your thumb if necessary to carefully slide the module into the card cage rail guides. Continue to gently push until the prealignment guide pegs engage in the backplane connector receptacles (Stage 2) and the ejector handle makes contact with the chassis rails. DO NOT FORCE THE BOARD INTO THE BACKPLANE SLOT.

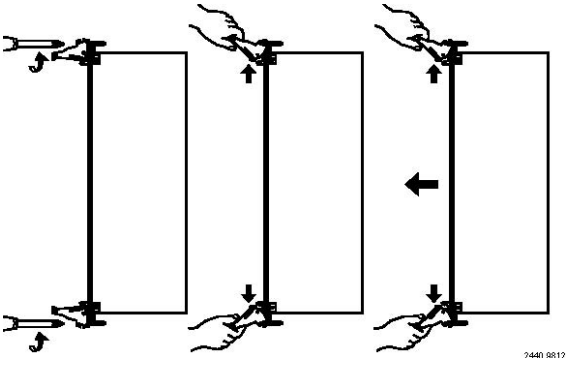
6. Use the ejector lever to seat the module in the slot by closing the lever inward until it is in the horizontal, locked position (Stage 3). There should be a “click” upon successful insertion. If the handles do not completely latch, remove module from chassis and visually inspect the slot to ensure there are no bent pins.

7. When the module you are installing is completely latched, secure it by tightening the captive screws at the top and bottom of the panel.

CPIP5430 Hot Swap Module Removal

Depending on your system configuration, you may need to manually shut down software on your module prior to removal to prevent data corruption. If system software exists to do so, shutdown may occur automatically after Step 2 is performed. Likewise, if system software is configured to illuminate the blue LED on the front of the module, ensure this has occurred before proceeding to Step 3. Once it illuminates, you may continue to remove the module.

1. Loosen the module's captive screws
2. Press the red button on the ejector levers to unlock.
3. Move the ejector levers in an outward direction to disengage the backplane connectors.
4. Pull the module from the chassis.



Startup and Operation 2

Applying Power to the System

After you verify that all necessary hardware preparation is complete and all connections are made correctly, you can apply power to the system and/or insert the board.

Prior to applying power, first verify that the chassis power supply voltage setting matches the voltage present in your location (if your power supply is not autosensing). When you power-on the chassis or insert the board, the CPIP5430 displays the BIOS banner and then runs a memory test.

Indicators

There are three LEDs and one reset switch on the front panel of the CPIP5430.

Front Panel Indicators	Description
Ethernet	Two LEDs
Hot swap	One blue LED
Reset	One recessed push button switch

Each indicator is described in the following sections.

LEDs for Gigabit Ethernet Port

Two LED indicators on the Ethernet connector show status of the gigabit Ethernet port. The yellow LED indicates speed and when illuminated it shows that the port has negotiated a 1000Mbps data rate. The green LED indicates link activity and when illuminated, the port is linked. When the green LED is blinking it means the port is actively transferring data.

Hot-Swap LED

The blue LED on the bottom of the panel is the hot-swap LED. When illuminated it indicates that it is safe to remove the board from the slot. The IPMI firmware automatically extinguishes the hot-swap LED shortly after insertion and ejector lock (or shortly after system power-up if the board is already inserted and locked). Note that system software is responsible for re-illuminating the LED once it has been extinguished by the IPMI subsystem.

Soft Reset

A soft reset can be generated from the Watchdog Timer. The two-stage, watchdog timer is built into the 6300 ESB ICH, it is programmable from 1 microsecond to 10 minutes.The system host CPU deactivates the PCI-to-PCI bridge before implementing the reset function. The BIOS preserves as much of the system memory state as possible.

PXE Boot

Use the following steps to boot the CPIP5430 from a PreBoot Execution Environment (PXE) server.

Note This explanation is only the sequence to get you into the PXE server environment. For an explanation on how to use the PXE server/software refer to the Intel web site and download the appropriate software:

http://www.intel.com/support/network/adapter/pro100/bootagent

To begin:

1. Press the <F2> or S key during system startup to enter the BIOS setup engine.
2. From the main **Setup** menu choose **Peripherals**.
3. Enable the gigabit controller that you want to boot from and enable the corresponding gigabit Boot ROM. If the controller and Boot ROM were enabled prior to entering **Setup**, go to Step 6.

4. Save changes and exit **Setup**. The board will reboot.
5. Enter **Setup** again, using either <F2> or the S key.
6. Choose **Boot Order** from the main **Setup** menu.
7. Under BOOT DEVICE PRIORITY select the **First Boot Device** option and press the Enter key.
8. Choose IBA GE Slot XXYZ, where XXYZ is the PCI identification of the network controller to boot from.

   There may be 1, 2 or 3 choices. If there is only one choice, this is the management (front panel or RTM) port. If there are two or more choices, two will have the same XX value. These are the backplane 2.16 ports, the other is the management port. For the 2.16 interfaces:

   Z = the port # (0 or 1)

   Port 0 connects to switch 1 and port 1 connects to switch 2
9. Save changes and exit **Setup**. the board will reboot.

Once the board completes POST it will boot to the PXE server. When the boot is successful the PXE server menu will appear on the screen.

BIOS 3

This chapter provides a description of the BIOS on the CPIP5430.

- *BIOS Setup Utility*
- *System Summary*
- *System Setup*
- *Hard Disk Setup*
- *Boot Order*
- *Peripherals*
- *USB Configuration*
- *Misc Configuration*
- *Event Logging*
- *Security/Virus*
- *Exit*

CPIP5430 BIOS Overview

The CPIP5430 BIOS software supports all of the IBM /AT standard functions and several board-specific functions and features. Features of the CPIP5430 BIOS include an easy-to-navigate setup engine and help windows.

Upon initial power up or after a hardware reset the processor begins executing code out of the onboard BIOS. The BIOS contains all of the software needed to boot the board to a working state so an operating system can be loaded. The first order of business for the BIOS is to initialize crucial system components, such as timers and chipset parts. The BIOS then performs basic component checks to ensure their presence and then sets them to a default state. Next, the cache and memory controllers must be initialized and configured for the type and configuration of the cache and memory found in the system. Once the memory has been

configured, the compressed portions of the BIOS are decompressed into RAM to allow the remainder of the BIOS tasks to be executed very quickly. The BIOS can now scan for and initialize other interfaces such as I/O devices and items on the PCI or ISA busses.

If a video adapter is in the system it is located and initialized. The video adapter will sign-on and its manufacturer, chip type, and creation date will appear on the screen. The BIOS will then display its sign-on information giving copyright information, the board name, and the version of the BIOS present in the system. At this point the following message appears at the bottom of the screen giving the hotkey that will invoke the setup engine.

```
F2 or s Enter Setup
<SPACE> Skip Memory
<ESC> BOOT Menu
```

If the F2 or <s> key is pressed, the message below will be displayed and the BIOS Setup Engine will be entered after the option ROM scan.

```
Entering SETUP . . .
```

The BIOS now starts to size and clear all system memory and display its progress on the screen. The BIOS now signs-on any option ROMs found on devices in the system. Also, the BIOS will scan for USB devices connected to the system. The BIOS then checks to see if the F2 or <s> key was pressed during POST. If it was, the BIOS Setup Engine will be executed.

Boot Menu

During POST display, the ESC key can be pressed to invoke the multi-boot menu. The menu appears near the end of POST, before the system summary screen is displayed, and after the option ROMs have signed on. The multi-boot menu allows interactive selection of the boot device. The list is typically in the following order:

```
Please select boot device:

USB 2.0 FLOPPY DRIVE
PM-WDC WD32BVA0
PS-CDU5211
IBA FE Slot 0328 v4110

↑ and ↓ to move selection
ENTER to select boot device
ESC to boot using defaults
```

The up and down arrows on the keyboard can be used to highlight the boot device you want to use. Press Enter to boot from it. Hard drives are any fixed disk (IDE, SCSI) in the system. Other devices may appear in the list, such as Ethernet boot ROMs from either integrated networking components or add-in cards. To change the boot order of devices within a category (such as to boot from IDE hard drive instead of SCSI) or to permanently change the boot order, you will have to enter SETUP and change the boot options.

If any errors are detected up to this point they will be displayed on the screen along with the following prompt to direct further actions. Pressing F1 ignores the errors and continues with the boot process. The F2 or s key can be pressed to enter the BIOS SETUP and possibly resolve any configuration error that may have been made.

Press **F2** or **s** to Run SETUP
Press **F1** to load default values and continue

If the F2 key was not pressed and no errors were detected, the SYSTEM SUMMARY SCREEN is displayed (if enabled). After 10 seconds or upon pressing a key, the BIOS attempts to boot the installed operating system.

The System BIOS is compatible with the Plug-and-Play Specification Version 1.0A. Two areas addressed by the System BIOS are Resource Management and Runtime Services.

Resource Management provides the ability to manage the fundamental system resources which include DMA, Interrupt Request Lines (IRQs), I/O and Memory Addresses. The Resource Manager takes on the responsibility for configuring Plug-and-Play (PnP) cards, as well as system board devices during the power up phase. After the Power-On Self Test (POST) process is complete, control of the Plug-and-Play device configuration passes from the system BIOS to the system software. The BIOS does, however, provide configuration services for system board devices even after the POST process is complete. These services are known as Runtime Services.

Runtime Services provide a mechanism whereby a Plug-and-Play operating system, such as Windows 2000, may perform resource allocation dynamically at runtime. The operating system may directly manipulate the configuration of devices that have traditionally been considered static.

BIOS Setup Utility

The BIOS Setup Utility is a menu-driven interface that is used to configure the board. The function of each category is briefly described below. Battery backed CMOS RAM is used to store the configuration/setup parameters selected in the BIOS Setup. On power-up the CMOS RAM parameters are used to configure the system. If the CMOS RAM is corrupt, default parameters stored in ROM are used to configure the system. If no errors occurred during the POST, the System Configuration Summary Screen will be displayed, see Table 3-1. Otherwise, BIOS configuration errors detected during the POST are displayed and the default values loaded. As each BIOS section is selected the contents of the category will be displayed. This allows you to view the current settings of each category without having to actually enter the category. To execute a specific category, using the up/down arrow keys, move the highlighted bar onto it and press **Enter**.

If you select **Go To Subscreen**, notice that there is a different navigational menu that allows you to **Select Item** (using the up/down arrows) and **Change Option** (using the up/down arrows or the +- keys).

Table 3-1. BIOS Setup Utility Screen

SYSTEM SUMMARY	Displays various information about the system installed
SYSTEM SETUP	Configures the time and date, as well as general BIOS features
HARD DISK SETUP	Configures the IDE interface and IDE storage devices
BOOT ORDER	Specifies boot device ordering
PERIPHERALS	Configures onboard peripherals
USB CONFIG	Configures USB devices
MISC CONFIG	Configures PCI, Plug n Play, and power options
EVENT LOGGING	Configures the system event log
SECURITY/VIRUS	Configures BIOS passwords and anti-virus options
EXIT	Exits ROM utilities, with options to save or discard changes

System Summary

The System Configuration Summary utility provides valuable information about the system. The information supplied can also be useful in determining items that are present in the system and how they are configured.

System Configuration Summary Screen

The System Configuration Summary screen is shown below, followed by a brief description of information supplied.

SYSTEM CONFIGURATION SUMMARY

SYSTEM SUMMARY SYSTEM SETUP HARD DISK SETUP BOOT ORDER PERIPHERALS USB CONFIG MISC. CONFIG EVENT LOGGING SECURITY/VIRUS EXIT	Motorola. - CPIP5430 CPU Type : Mobile Pentium(R) 4 - M CPU 2.20GHz CPU Speed : 2.20GHz IDE Drive 0: Not Detected Base RAM:632KB IDE Drive 1: Not Detected Extended RAM : 1024MB IDE Drive 2: Not Detected Cache Size : 512KB IDE Drive 3: Not Detected BIOS Date : 04/16/04 COM Ports : 3F8 2F8 BIOS Core : 08.00.10 LPT Ports : None Memory Mode : 266 MHz Single Channel with ECC PMC Mode : PCI 66 MHz USB Devices : None ↑ ↓ Select Screen Enter Go to Sub Screen F1 General Help Esc Exit
Motorola CPIP5430 BIOS v1.00 Beta-M	

System Summary Descriptions

CPU	Displays the type and speed of processor installed.
Base RAM	Displays the amount of installed system RAM up to 640KB.
Extended RAM	Displays the amount of installed extended RAM beyond 1024KB.
Cache Size	Displays the amount of L2 cache detected.
BIOS Date	Displays the date on which the BIOS was generated.
BIOS Core	Displays the core version that this BIOS was built upon.
IDE Drive 0 - 3	Displays the drive type selected for each directly or RTM-attached IDE drive (connected to on-board IDE controller).
COM Ports	Displays the I/O addresses of all installed serial ports.
LPT Ports	Displays the I/O addresses of all installed parallel ports.
Memory Mode	Displays the operating mode for the system memory.
PMC Mode	Displays the PCI mode that the PMC slots are currently operating in.
USB Device	Displays the USB devices detected by the BIOS. Under some circumstances, such as legacy USB support being set to POST-Only, some USB devices might not be displayed.

System Setup

The System Setup Configuration Utility is used to configure the system time/date. It is also used to customize the way the BIOS operates.

SYSTEM SETUP CONFIGURATION UTILITY		
SYSTEM SUMMARY		
	DATE/TIME OPTIONS	
SYSTEM SETUP	System Time	13:49:05
	System Date	Tue 4/27/2004
HARD DISK SETUP		
	BIOS OPTIONS	
BOOT ORDER	Quick Boot	Disabled
	Summary Screen At Boot	Disabled
PERIPHERALS	Boot Failure Retry	Auto
	AddOn ROM Display Mode	Force BIOS
USB CONFIG	AddOn ROM Display Delay	Disabled
	Pause on POST Errors	Disabled
MISC. CONFIG	SETUP Prompt During Post	Enabled
	Bootup Num-Lock	On
EVENT LOGGING		
	SYSTEM OPTIONS	
SECURITY/VIRUS	CPU Speed	Fast
	MPS Revision	1.4
EXIT	Spread Spectrum	Off
	↑ ↓ Select Screen Enter Go to Sub Screen	
	F1 General Help Esc Exit	
Motorola CPIP5430 BIOS v1.00 Beta-M		

Date / Time Descriptions

System Time	A new time is set by typing in the HOUR, MINUTE, and SECONDS each followed by pressing < ENTER >. The time is displayed in 24 hour format; therefore, AM hours range from 0 through 11 and the PM hours range from 12 through 23. Invalid times cannot be entered.
System Date	A new date is set by tying in the MONTH, DAY, and YEAR each followed by pressing < ENTER >. If one of the parameters is out of range, the new date will not be entered.

BIOS Options Descriptions

Quick	Allows the BIOS to skip certain tests while booting. This decreases the amount of time needed to boot the system.
Summary Screen At Boot	When this option is enabled, the system summary information will be displayed before the system boots.
Boot Failure Retry	Allows BIOS to automatically reattempt to boot if all detected boot devices fail.
AddOn ROM Display Mode	Selects the display mode used by the BIOS when signing on option ROMs.
AddOn ROM Display Delay	When this item is enabled, the BIOS will insert a brief pause after each option ROM signs on. This is useful to allow viewing any errors or messages that may otherwise be missed
Pause On Post Errors	This option determines whether the POST will pause and wait for user input when an error occurs.
Prompt During Post	When this option is enabled, the prompt that displays the key needed to enter SETUP will be displayed during the POST.

Keyboard Options Descriptions

Bootup Num-Lock	Specifies the state of the Num-Lock key to be set when the system boots.

System Options Descriptions

CPU Speed	Selects the CPU speed. This option applies only to processors that support SpeedStep technology. Processors that do not support SpeedStep will run at their rated speed.
MPS Revision	Selects the MultiProcessor Specification version to which the BIOS conforms. The default of 1.4 is recommended unless an OS reports a MPS error.
Spread Spectrum	Controls the spread spectrum behavior of the system clock generator. Enabling this may reduce EMI emissions.

Hard Disk Setup

For purposes of BIOS configuration, S-ATA refers to Serial ATA connectivity and P-ATA refers to Parallel ATA connectivity. The Hard Drive Configuration Utility is used to configure the hard drive controller and interface properties for the system. It is also used to configure the parameters for each directly attached drive in the system.

HARD DRIVE CONFIGURATION UTILITY	
SYSTEM SUMMARY SYSTEM SETUP **HARD DISK SETUP** BOOT ORDER PERIPHERALS USB CONFIG MISC. CONFIG EVENT LOGGING SECURITY/VIRUS EXIT	❏ IDE CONFIG ❏ PRIMARY MASTER Not Detected ❏ PRIMARY SLAVE Not Detected ❏ SECONDARY MASTER Not Detected ❏ SECONDARY SLAVE Not Detected ↑ ↓ Select Screen Enter Go to Sub Screen F1 General Help Esc Exit
Motorola CPIP5430 BIOS v1.00 Beta-M	

IDE Configuration Utility

The following sections describe the configuration options for the IDE controller.

IDE CONFIGURATION UTILITY	
IDE CONFIG PRIMARY MASTER PRIMARY SLAVE SECONDARY MASTER SECONDARY SLAVE	IDE Configuration P-ATA only P-ATA Channel Selection Both Hard Disk Write Protect Disabled IDE Detect Time Out (Sec) 35 Onboard IDE Drive Pin Count 40 ↑ ↓ Select Screen ↑ ↓/+- Change Option F1 General Help Esc Exit
Motorola CPIP5430 BIOS v1.00 Beta-M	

IDE Configuration Descriptions

IDE Configuration	Selects the configuration for the onboard parallel and serial IDE controllers.
Combined Mode Option	Selects which IDE connectors are active. When set to P-ATA Primary, the on-board parallel drive is set as the primary master, and the serial ATA connector on the Rear I/O board is set to secondary master. The parallel ATA connector on the Rear I/O is disabled in this mode. When set to S-ATA primary, the serial ATA connector on the Rear I/O is set to primary master, and the parallel ATA connector on the Rear I/O is set to the secondary master/slave. The onboard parallel drive is disabled in this mode.
Hard Disk Write Protect	When this item is enabled, the BIOS protects the IDE drives from write accesses. This is only effective for operating systems that access the hard drives using BIOS interfaces.

IDE Detect Time Out	This item specifies the maximum amount of time that the BIOS will attempt to search for IDE devices.
Onboard IDE Drive Pin Count	Selects the cable type that the onboard IDE drive reports. 80-pin mode may allow faster data rates to be achieved. This should be set to 40-pin if problems are encountered in 80-pin mode.

Primary Master Configuration Summary

```
                PRIMARY MASTER CONFIGURATION SUMMARY

IDE CONFIG          Device          :Hard Disk
                    Vendor          :WDC WD360GD-00FNVA0
PRIMARY MASTER      Size            : 37.0GB
                    LBA Mode        : Supported
PRIMARY SLAVE       Block Mode      : 16 Sectors
                    PIO Mode        : 4
SECONDARY MASTER    Async DMA       : MultiWord DMA-2
                    Ultra DMA       : Ultra DMA-2
SECONDARY SLAVE     S.M.A.R.T.      : Supported

                    Type                                    Auto
                    LBA/LARGE MODE                          Auto
                    Block(Multi-Sector Transfer)Mode        Auto
                    PIO MODE                                Auto
                    DMA MODE                                Auto
                    S.M.A.R.T.                              Auto
                    32-Bit Data Transfer                 Disabled
                    ARMD Emulation Type                     Auto

                    ↑ ↓ Select Screen EnterGo to Sub Screen
                    F1  General Help    Esc    Exit

                Motorola CPIP5430 BIOS v1.00 Beta-M
```

Hard Drive Setup Descriptions

The configuration options described below work identically for HARD DRIVES 0 - 3.

Device	Displays the type of IDE device currently installed. Type choices include Not Installed, Hard Disk, ATAPI CDROM, and ARMD.
Vendor	Displays the manufacturer device identification information.
Size	Displays the storage capacity of the device.
LBA Mode	Displays support for Logical Block Accessing. LBA uses 28-bit addressing of the hard disk instead of CHS (Cylinder/Head/Sector) addressing for supporting drives up to 137GB.
Block Mode	Displays the maximum Block Mode transfer for the device.
PIO Mode	Displays the maximum PIO supported by the device.
Async DMA	Displays the highest support Asynchronous DMA Mode.
Ultra DMA	Displays the highest support Synchronous DMA Mode.
S.M.A.R.T.	Displays device support for Self-Monitoring Analysis and Reporting Technology. This protocol allows detection of drive errors.
Type	Selects the type of IDE device. Type choices include Not Installed, Auto, CDROM, and ARMD.

If AUTO type is selected, the hard drive parameters are read during boot-up and are configured automatically. The hard drive information, such as manufacturer and model number, is displayed during POST. The CDROM type will enable bootable CD-ROM support for an IDE CDROM drive attached as a master or slave. An IDE CD-ROM can be made the boot device through the BOOT OPTIONS screen. The ARMD type is selected when an ATAPI Removable Media Device is present. This includes drives for high capacity floppies that can be formatted as floppies or hard disks, such as LS120, IOMega Zip, Fujitsu MO, and certain flash devices.

32BIT Data Transfer	Controls support for 32-Bit IDE transfers.
ARMD Emulation Type	Specifies the type of emulation used.

Boot Order

The Boot Order Configuration Utility is used to determine the order in which the BIOS attempts to boot from devices. The BIOS attempts to boot from the devices at the top of the list first. If the device is not bootable, then the next item down in the list is tried. Removable devices and hard disks have further ordering within their category. The following page describes the configuration options. The ESC key can be pressed during POST to display a boot device menu. This will override the boot order chosen in the CMOS Setup Utility and boot from the device selected.

BOOT ORDER CONFIGURATION SUMMARY	
SYSTEM SUMMARY SYSTEM SETUP HARD DISK SETUP **BOOT ORDER** PERIPHERALS USB CONFIG MISC. CONFIG EVENT LOGGING SECURITY/VIRUS EXIT	Boot Device Priority 1st Boot Device IBA GE Slot 0210 v1 2nd Boot Device IBA GE Slot 0211 v1 3rd Boot Device Ultra D0 IC25N020AT 4th Boot Device ATAPI CDROM ATAPI CDROM Drives 1st Drive SM-CDU5211 Hard Disk Drives 1st Drive Ultra D0 IC25N020AT Removable Devices 1st Drive MITSUMI USB FDD ↑ ↓ Select Screen Enter Go to Sub Screen F1 General Help Esc Exit
Motorola CPIP5430 BIOS v1.00 Beta-M	

Boot Order Descriptions

Boot Device Priority	Selects the boot order for installed boot devices. The BIOS attempts to boot from items at the top of the list first.
Removable Devices	Boot from legacy floppy diskette, removable LS-120, or ZIP drives. The desired removable device must be selected.
Hard Disk Devices	Boot from hard disk drive. The desired hard drive must be selected through Hard Disk Drives.
ATAPI CDROM Drives	Boot from an IDE CDROM.

Peripherals

PERIPHERAL CONFIGURATION UTILITY	
SYSTEM SUMMARY SYSTEM SETUP HARD DISK SETUP BOOT ORDER **PERIPHERALS** USB CONFIG MISC. CONFIG EVENT LOGGING SECURITY/VIRUS EXIT	ONBOARD PERIPHERAL CONTROL Single CSA Gigabit Enabled (*see note*) CSA Gigabit Boot ROM Disabled Dual PCI-X Gigabit Enabled PCI-X Gigabit Boot ROM Enabled I/O PORT CONTROL Serial Port 1 Address 3F8/IRQ4 Serial Port 2 Address 2F8/IRQ3 CONSOLE REDIRECTION BIOS Console Redirection Enabled Serial Port COM1 Serial Port Mode 19200 8,n,1 Flow Control None Redirection After BIOS POST Always Terminal Type ANSI VT-UTF8 Combo Key Support Disabled ↑ ↓ Select Screen Enter Go to Sub Screen F1 General Help Esc Exit
Motorola CPIP5430 BIOS v1.00 Beta-M	

Note If you change the CSA gigabit port from the disabled state to an enabled state, you must power cycle the board after the change is made.

Peripherals Descriptions

Single CSA Gigabit	This item controls the onboard 82547 CSA gigabit chip. (See Note for the Peripheral Configuration Utility on page 3-17.)
CSA Gigabit Boot ROM	Controls the boot ROM allowing for remote network booting with the 82547.
Dual PCI-X Gigabit	This item controls the onboard 82546 PCI-X gigabit chip.
PCI-X Gigabit Boot ROM	Controls the boot ROM allowing for remote network booting with the 82546.
Serial Port 1 & 2 Address	The two serial ports can be configured to one of four possible settings or disabled.

I/O Address	**Interrupt**	**COM Port**
3F8h	IRQ4	COM1
2F8h	IRQ3	COM2
3E8h	IRQ4	COM3
2E8h	IRQ3	COM4

Console Redirection Descriptions

BIOS Console Redirection	This item allows serial console redirection to be enabled. This allows all video output to be redirected through the serial port during the POST and DOS. In addition, input through the serial port will be used through the POST and DOS. The default setting is enabled.
Serial Port	Specifies the serial port to be used for console redirection.
Serial Port Mode	Selects the baud rate for console redirection. The possible baud rates are 9600, 19200, 38400, 57600, and 115200.
Flow Control	This item allows flow control to be used to prevent data overruns. If the cable supports hardware handshaking, then the hardware option should be selected. Otherwise, software handshaking should be selected.
Redirection After BIOS Post	Control if console redirection is to be used after POST.
Terminal Type	Selects between ANSI and VT100 terminal types.
VT-UTF8 Combo Key Support	Controls VT-UTF8 combination key support for ANSI and VT100 terminals.

USB Configuration

3

USB CONFIGURATION UTILITY	
SYSTEM SUMMARY SYSTEM SETUP HARD DISK SETUP BOOT ORDER PERIPHERALS **USB CONFIG** MISC. CONFIG EVENT LOGGING SECURITY/VIRUS EXIT	USB CONTROL USB Function Front and Rear USB 2.0 Controller Enabled Legacy USB Support Always Legacy USB Speed Full Speed USB MASS STORAGE CONFIG USB Mass Storage Reset Delay 20 Sec No USB Mass Storage device detected ↑ ↓ Select Screen Enter Go to Sub Screen F1 General Help Esc Exit
Motorola CPIP5430 BIOS v1.00 Beta-M	

USB Control Descriptions

USB Function	This item controls the onboard USB functions. The USB ports are not usable when this item is disabled.
USB 2.0 Controller	Controls the USB 2.0 controller. When enabled, the system will support high-speed (480 Mbps) USB devices, provided the OS loads a driver for the 2.0 controller.
Legacy USB Support	Controls whether USB devices are available after POST. When set to POST Only, the USB keyboard may be used during POST. Storage devices are not applicable in POST Only mode since they do not need to be accessed. When set to Always, USB devices including drives, CD-ROMs, keyboards, and mice can be accessed after POST has completed.
Legacy USB Speed	Selects the maximum operating speed for USB devices running in legacy mode.

USB Mass Storage Configuration Descriptions

USB Mass Storage Reset Delay	Number of seconds to wait for a USB mass storage device after sending the start unit command.
Emulation Type	Specifies the method used to determine the type of USB mass storage devices connected.

Misc Configuration

The Miscellaneous Configuration Utility allows configuration of the PCI bus, PnP options, and ACPI related items.

PCI and PNP Configuration Summary

MISC. CONFIGURATION SUMMARY		
SYSTEM SUMMARY	PCI OPTIONS	
	PCI Latency Timer	64
SYSTEM SETUP	Interrupt 19 Capture	Disabled
	Reserved Memory Size	Disabled
HARD DISK SETUP		
	PNP OPTIONS	
BOOT ORDER	Plug & Play O/S	No
	Reset Config Data	No
PERIPHERALS		
	POWER OPTIONS	
USB CONFIG	ACPI 2.0 Support	No
	ACPI APIC Support	Enabled
MISC. CONFIG	Headless Mode	Disabled
	ACPI Console Redirection	Disabled
EVENT LOGGING		
SECURITY/VIRUS	↑ ↓ Select Screen Enter Go to Sub Screen F1 General Help Esc Exit	
EXIT		
Motorola CPIP5430 BIOS v1.00 Beta-M		

PCI Options Descriptions

PCI Latency Timer	This option is used to set the desired PCI latency for all devices on the PCI bus.
Interrupt 19 Capture	This item allows option ROMs to capture interrupt 19 for use in booting.
Reserved Memory	This section is used to reserve upper memory blocks (UMBs) for use by non-PnP cards. A block can be reserved in 16K increments from C000h to DFFFh. This is not needed for PCI devices, but may be needed for legacy devices that are behind an add-on PCI card.

PnP Options Descriptions

Plug and Play O/S	If disabled (default), the BIOS will set up all PnP devices. If enabled, the BIOS configures only the devices critical for booting, and the operating system is assumed to configure all other PnP devices. Even when set to disabled, a PnP operating system may be used.
Reset Configuration Data	If set to “Yes”, the PnP configuration is reset after leaving SETUP and reconfigured on the next boot. This option is automatically reset to **No** after rebooting.

ACPI Options Descriptions

ACPI 2.0 Support	If this item is enabled, the BIOS builds the ACPI tables to comply with the ACPI 2.0 specification. When disabled, the BIOS is ACPI 1.0b compliant.
ACPI APIC Support	Enables or disables the ACPI support for the APIC. When enabled, a pointer to the APIC table is integrated into the RSDT pointer list.
Headless Mode	If this item is enabled, information about headless support is included in the ACPI FACP table.
ACPI Console Redirection	Lets an ACPI OS know if it should use console redirection. If enabled, the BIOS informs the OS which port it should use, what data parameters to use, and the terminal emulation to use.

Event Logging

The Event Logging Configuration Utility is used to configure and view system events that have been logged.

EVENT LOGGING CONFIGURATION UTILITY	
SYSTEM SUMMARY SYSTEM SETUP HARD DISK SETUP BOOT ORDER PERIPHERALS USB CONFIG MISC. CONFIG **EVENT LOGGING** SECURITY/VIRUS EXIT	View Event Log Mark All Events As Read Clear Event Log Event Log Statistics Disabled ↑ ↓ Select Screen Enter Go to Sub Screen F1 General Help Esc Exit
Motorola CPIP5430 BIOS v1.00 Beta-M	

Event Logging Descriptions

View Event Log	This item is used to open a window containing a list of the currently logged system events.
Mark All Events As Read	This item is used the mark all system events in the log as read.
Clear Event Log	This item is used to erase all events from the system log.
Event Log Statistics	This item is used to view statistics about the system event log

Security/Virus

The Security and Anti-Virus Configuration Utility is used to set system passwords and control system anti-virus items.

SECURITY AND ANTI-VIRUS CONFIGURATION UTILITY	
SYSTEM SUMMARY SYSTEM SETUP HARD DISK SETUP BOOT ORDER PERIPHERALS USB CONFIG MISC. CONFIG EVENT LOGGING **SECURITY/VIRUS** EXIT	Supervisor Password : Not Installed User Password : Not Installed Change Supervisor Password Change User Password Clear User Password Boot Sector Virus Protection Disabled ↑ ↓ Select Screen Enter Go to Sub Screen F1 General Help Esc Exit
Motorola CPIP5430 BIOS v1.00 Beta-M	

Security/Virus Descriptions

Supervisor Password	This item indicates whether a supervisor password has been set.
User Password	This item indicates whether a user password has been set.
Change Supervisor Password	This item allows setting the supervisor password.
Change User Password	This item allows setting the user password.
Clear User Password	This item is used to clear the user password.
Boot Sector Virus Protection	When this item is enabled, a warning message is displayed before any program tries to access the boot sector.

Exit

The Exit Menu provides a way to exit setup and save or discard changes. It also provides a way to load the default settings stored in the BIOS.

EXIT MENU	
SYSTEM SUMMARY SYSTEM SETUP HARD DISK SETUP BOOT ORDER PERIPHERALS USB CONFIG MISC. CONFIG EVENT LOGGING SECURITY/VIRUS **EXIT**	Save Changes and Exit Discard Changes and Exit Load Defaults Discard Changes Save Custom Defaults ↑ ↓ Select Screen Enter Go to Sub Screen F1 General Help Esc Exit
Motorola CPIP5430 BIOS v1.00 Beta-M	

Exit Descriptions

Save Changes and Exit	Exits SETUP and saves all changes to CMOS.
Discard Changes and Exit	Exits SETUP and discards any changes.
Load Defaults	Loads the SETUP factory default values.
Discard Changes	Discard any changes made during SETUP.
Save Custom Defaults	Allows you to make a backup of the current CMOS settings to NVRAM.
Load Custom Defaults	Loads the SETUP Custom Defaults. If custom defaults have been saved, they will automatically be loaded if CMOS becomes corrupted instead of the manufacturing defaults.
Clear Custom Defaults	Erases the Custom Defaults from NVRAM.

Functional Description

4

Introduction

The CPIP5430 series products include the following features. The processor(s) are socketed PGA devices. The amount of memory available and the availability of the PMC slots vary, based on the specific model. The Hard Disk Drive (HDD), if installed, occupies one PMC site. The Rear Transition Module, CPIP5430-RTM1, is an optional item.

The following table lists the features of the CPIP5430.

Table 4-1. CPIP5430 Features Summary

Feature	Description
Form Factor	6U board (233.35, +0.0/-0.3mm x 160.0, +0.0/-0.3mm) 1-slot width Supports rear I/O through J3 and J5
CPU/Cache	Supports Intel Mobile Pentium 4 Processor-M processor with 512KB on-die L2 cache at full core speed and 400 MHz FSB
Chipset	Intel 875P MCH with 6300 ESB ICH Supports up to 4GB of DDR memory Supports ECC, on-memory bus 64-bit, 33/66 MHz, on board, PCI bus interface
System Memory	Supports 266 MHz to 400 MHz DDR Supports two onboard SO-DIMM sockets Supports memory size up to 4GB Supports 144-pin registered SO-DIMMs ECC supported
IDE Port	Supports one (secondary) EIDE channel through J5 rear I/O for up to two IDE devices An onboard 44-pin IDE pin header for optional 2.5" hard drive or Disk-on-Module on front controller (primary channel).
On-Board Super I/O	The function of the SIO is to provide legacy serial port controller functionality (16550 compatible).

Table 4-1. CPIP5430 Features Summary (continued)

Feature	Description
USB Interface	Supports one port (USB0 - type A connector) on front panel for development, service, and setup operations only Supports two ports (USB1 & USB2 - type A connector) on RTM USB Specification Rev. 2.0 compliant Over-current protection on each USB port
Watchdog Timer	The 2-stage, watchdog timer is built into the 6300 ESB ICH, it is programmable from 1 microsecond to 10 minutes.
On-board Ethernet (PICMG 2.16 compliant)	Two Ethernet ports on rear I/O connector (RTM) are provided by one Intel 82546EB dual-port Gigabit Ethernet controller On 64-bit/66 MHz PCI bus IEEE 802.3x compliant flow control support EEE 802.3ab compliant 10/100/1000 Mbps auto-negotiation
On-board Ethernet (Management Port)	One Ethernet port on front panel (COM1) provided by one Intel 82547EI Gigabit Ethernet controller On Communication Streaming Architecture (CSA) bus IEEE 802.3x compliant flow control support IEEE 802.3ab compliant 10/100/1000 Mbps auto-negotiation Front panel Ethernet port can be routed to the RTM
System Management Interface	QLogic Zircon Peripheral Management Controller with 14KB internal SRAM Supports PICMG 2.9 secondary system managing bus and implements IPMI functions as defined in the IPMI Specification v 1.0 Monitors onboard voltages, temperatures Supports external 16-bit flash ROM up to 1MB (protected boot block required) Two-stage watchdog timer, externally programmable via IPMI
OS Compatibility	Red Hat Linux versions with 2.4.20 and newer kernels

Table 4-1. CPIP5430 Features Summary (continued)

Feature	Description
Busses	No external PCI bus support (no PCI connections on J1 and J2) Two onboard PMC expansion slots supporting up to 64-bit/66 MHz PCI interface
BIOS: AMI PnP BIOS	Quick Boot Multi-Boot Peripheral Enable/Disable Console Redirection Legacy USB Support - Keyboard, Mouse and Mass Storage Device ACPI 1.0 and 2.0 Plug and Play PCI 2.2 Compliant Enhanced IDE Support - PIO, DMA, and Ultra DMA IDE S.M.A.R.T Support Custom CMOS (Save to Flash Security
General Features	PCI Rev. 2.1 compliant PICMG 2.1 CompactPCI Hot-swap specification Rev. 1.0 compliant PICMG 2.9 CompactPCI System Management Bus Rev. 1.0 compliant PICMG 2.16 CompactPCI Packet Switching Backplane Rev. 1.0 compliant
Front Panel LEDs and Switches	Front panel LED to indicate Hot-Swap status Front panel LED to indicate Management Ethernet status including speed (yellow) and link/activity (green) Recessed switch for system reset

For information on the environmental, mechanical, and power specifications, as well as reliability and compliance statements, refer to Appendix A, *Specifications*.

Block Diagram

Figure 4-1 shows a block diagram of the overall board architecture.

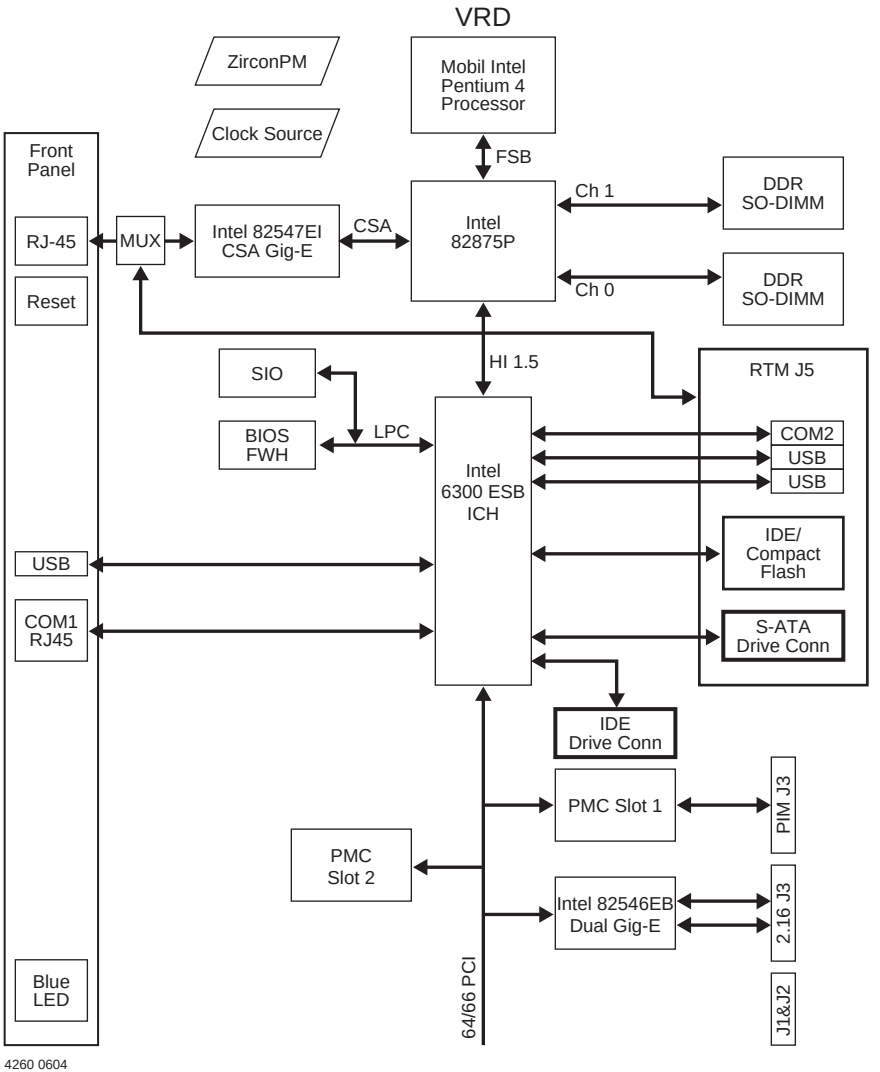


Figure 4-1. CPIP5430 Block Diagram

Serial EEPROMs

The CPIP5430 provides two serial EEPROMs to store the SEL and FRU information. Each SEL record uses 16 bytes providing 500 records for SEL storage, the 64KB FRU is used to store the VPD data.

- ❏ The slave address for SEL is 0xAC
- ❏ The slave address for FRU is 0xAE

QLogic and MCG provide a firmware suite supporting the Intelligent Platform Management Interface (IPMI) specification v 1.0, including the Intelligent Platform Management Bus (IPMB). For a list of commands used to communicate with the management controllers in the system, refer to Appendix C, *IPMI Commands*.

Asynchronous Serial Ports

Two serial ports are supported on the CPIP5430. The EIA232 drivers and receivers reside on board the CPIP5430. COM1 is resides on the board and is available via an RJ45 connector on the front panel. COM2 resides on the RTM and is available via an RJ45 connector on the RTM front panel. By default, the BIOS configures the primary port, COM1, for use by Remote Access, which allows console access to BIOS Setup. The default port configuration is:

- ❏ 19200 baud
- ❏ 8 data bits
- ❏ no parity
- ❏ 1 stop bit
- ❏ CTS/RTS flow control

ANSI is the default console type for the BIOS.

If you experience difficulty connecting with these settings, try a different flow control setting. If you still can’t connect, or if Remote Access becomes disabled, you may need to connect a video monitor and a USB

keyboard to access BIOS Setup to correct the settings. The supported baud rates are 1200, 2400, 4800, 9600, 19200, 38400, 57600, and 115200 bps.

Table 4-2. Serial Port Characteristics

Serial Port	Connector Type	Base Address	Interrupt Address
COM1	RJ45 on CPIP5430	3F8h	IRQ4
COM2	RJ45 on RTM	2F8h	IRQ3

Real-Time Clock and Nonvolatile Memory

The real time clock is built into the 6300 ESB ICH. It is supported by a 256 byte battery backed RAM.

Watchdog Timer (SIO Chip)

The 6300 ESB ICH provides a two-stage watchdog timer with independent count values for each stage. The first stage generates an INT or SMI. The second stage drives an external pin active until it is cleared by system reset or a power cycle. It is configurable for granularity from 1us to 10 min.

IPMI Controller

The Zircon Peripheral Management Controller from QLogic is used to manage the CPIP5430 system boards. The features are summarized below:

- ARM7/TDMI controller with internal 14KB SRAM
- Six channel A-to-D converter for voltage monitoring, 10-bit resolution
- Heartbeat/watchdog (two-stage) timer
- Three I^2C buses
- I2C bus with bus master capability (use I^2C bus #0)
- LPMI interface (using SMBus I^2C bus #1)
- Supports onboard hardware monitor (via I^2C #2)
- Three serial EEPROMs for boot and runtime firmware, SEL, FRU, and customer use

QLogic provides a firmware suite that supports the Intelligent Platform Management Interface (IPMI) specification, including the Intelligent Platform Management Bus (IPMB). The supporting firmware features are summarized as follows:

- IPMI version 1.0
- Online firmware update (via IPMI standard command)
- Dynamic IPMB address allocation with compact PCI GA input
- FRU commands
- IPMB message bridging functions
- SDR and sensor reading

PCI Arbitration

The following tables show the PCI arbitration assignments for PCI Bus 1. This bus hosts the two PMC sites and the on-board 82546EB Gigabit Ethernet controller.

PCI Bus 1

The PCI request/arbitration assignments for the PCI bus 1 are as follows:

Table 4-3. PCI Bus 1 Arbitration Assignments

PCI Bus Request	PCI Master(s)
Request 0	Onboard LAN 82546EB
Request 1	PMC slot 1 (1st REQ)
Request 2	PMC slot 1 (2nd REQ)
Request 3	PMC slot 2
Request 4	None
Request 5	None

Rear Transition Module for CPIP5430

5

This chapter includes information for installing and configuring the CPIP5430-RTM1 transition module, which is designed to work in conjunction with the CPIP5430 series of CompactPCI controller boards.

The sections include the following:

- *Features*
- *Block Diagram*
- *Functional Descriptions*
- *Preparing the RTM*
- *Installing the RTM*
- *Pin Assignments*

Features

The CPIP5430-RTM1 provides additional I/O capabilities to the CPIP5430 SBC. It is a 6U x 80mm form factor and is installed directly in the MXP backplane in the rear transition board slot of the chassis and interfaces with the CPIP5430 board through the J3 and J5 connectors. This RTM does not support hot swap and it can be serviced if the front CPIP5430 SBC is removed or powered off.

Rear panel connectors include:

- One RJ45 connector for 10/100 /1000 Base-Tx Ethernet
- Two USB ports
- One RJ45 connector for asynchronous serial port COM2

An additional IDE channel and Serial ATA are available on J3 and J5 from the CPIP5430. Connections for the IDE include CompactFlash socket or IDE hard drive. Connection for the optional Serial ATA hard drive is also provided. There is also support for IPMI VPD via the J15 header.

The CPIP5430-RTM1 supports one single-wide (74mm wide by 69mm long) PMC I/O module. I/O pins 1 through 64 for PMC slot 1 on the CPIP5430 board are routed from the J3 connector to the PMC I/O module.

Block Diagram

Figure 5-1 shows a block diagram of the overall RTM architecture.

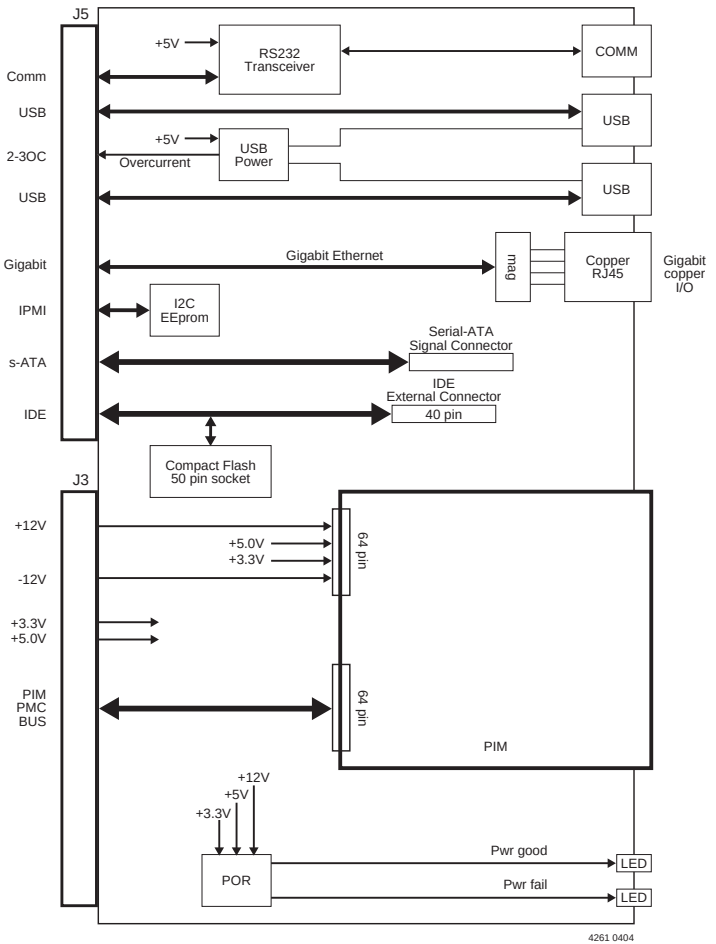


Figure 5-1. CPIP5430-RTM1 Block Diagram

Functional Descriptions

The CPIP5430-RTM1 is designed to match the signal pinouts of the CPIP5430 SBC when installed in a MXP chassis. The interface connection between the CPIP5430-RTM1 and the CPIP5430 is one-to-one pins through the backplane.

The CPIP5430 provides four bus interfaces to the CPIP5430-RTM1. The Serial-ATA bus, routed to a on-board connector on the CPIP5430-RTM1 allows for Serial-ATA drives to be interfaced externally from the CPIP5430-RTM1. The PMC I/O bus on the RTM provides one PIM location with access though the CPIP5430-RTM1 front panel. The IDE bus on the CPIP5430-RTM1 provides one CompactFlash media socket and a 40-pin external IDE connector interface for an optional hard drive. The IPMI/I^2C bus provides for IPMI review of the CPIP5430-RTM1 build Vital Product Data (VPD).

The CPIP5430-RTM1 indicates FAIL and GOOD power status via a LED on the front panel.

The CPIP5430-RTM1 uses +5V and +3.3V supplied from the CPIP5430 for control and buffering functions. The CPIP5430 also supplies the PIM with +5V, +3.3V,+12V and -12V.

Gigabit Ethernet Interface

The CPIP5430 SBC provides one 10/100/1000 Base-TX Ethernet interface through the J5 connector to the CPIP5430-RTM1.

An 8-pin RJ45 connector is available on the front panel of the CPIP5430-RTM1 and is used with Ethernet twisted pair links with a RJ45 plug on each end. Pin assignments are found in Table 5-10

Serial Port COM2

One serial port, COM2, is supported on the CPIP5430-RTM1 and is accessed via an RJ45 connector on the front panel of the RTM. The EIA232 drivers and receivers reside on board the CPIP5430. Refer to *Asynchronous Serial Ports* on page 4-5 for configuration information of the serial ports. Pin assignments are found in Table 5-8

USB Interface

The CPIP5430-RTM1 provides two USB ports on the rear panel. USB capability allows for the easy addition of peripherals, such as a mouse, keyboard, or speakers. The USB interface transfers signal and power over a four-wire cable. The signaling occurs over two wires on each point-to-point segment. There are three data rates:

- ❏ The USB high-speed signaling bit rate is 480 Mb/s.
- ❏ The USB full-speed signaling bit rate is 12 Mb/s
- ❏ A limited capability low-speed signaling mode is 1.5 Mb/s

The CPIP5430-RTM1 provides the standard power resource of 0.5A at 5V to the peripherals. The power to each port is protected. Pin assignments are found in Table 5-9.

IDE Interface

The CPIP5430-RTM1 supports a single IDE channel for external storage devices. This IDE channel is routed to the J5 I/O connector. One 50-pin Type II CompactFlash card header connector provides the IDE interface to one CompactFlash plug-in module. The CompactFlash connector is not accessible through the rear panel. The CPIP5430-RTM1 must be removed in order to install a CompactFlash memory card. Pin assignments are found in Table 5-7.

I2C Interface

The CPIP5430-RTM1 contains a 256 x 8 Serial EEPROM. The Serial EEPROM provides for storage of the transition module configuration information. The default I2C address for this EEPROM is $A6h.

Preparing the RTM

Figure 5-2 illustrates the placement of the jumpers, headers, connectors, and various other components on the CPIP5430-RTM1. The configurable headers are listed in the following table.

For pin assignments on the CPIP5430-RTM1, refer to *Pin Assignments* on page 5-9.

Table 5-1. RTM Jumper Settings

Jumper	Function	Setting
J15	Enable VPD Write	[2-3]
J16	Sets the CompactFlash card as Slave device of the IDE channel. Sets the Compact Flash card as Master device of the IDE channel.	[No jumper] [1-2]

Note Items in brackets are factory default settings.

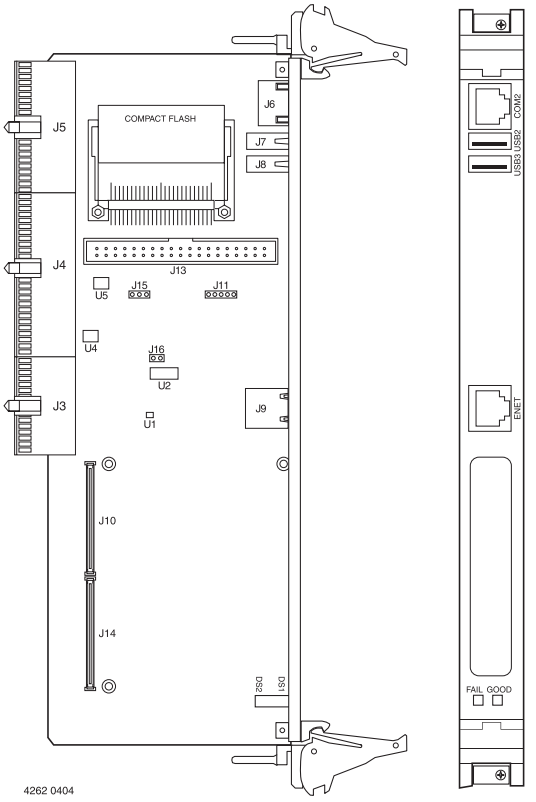


Figure 5-2. CPIP5430-RTM1 Layout

Table 5-2. Connector Reference

Reference Designator	Connector Function
J3	User I/O. Refer to Table 5-4 for pin assignments
J4	For alignment purposes only.
J5	User I/O. Refer to Table 5-3 for pin assignments
J6	COM2
J7	USB
J8	USB
J9	1GB Ethernet

Table 5-2. Connector Reference (continued)

Reference Designator	Connector Function
J10	PMC (power)
J11	Serial ATA (signal)
J12	CompactFlash
J13	IDE Hard Drive Header
J14	PMC (signal)
J15	VPD Write
J16	IDE master/slave

Installing the RTM

Before installing the CPIP5430-RTM1, you should install the CompactFlash memory card.

CPIP5430-RTM Transition Module Installation

Use the following steps to install the CPIP5430-RTM1 into your computer chassis.

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. Keep the ESD secured throughout this procedure.
2. Shut down the operating system.
3. Turn AC or DC power off and remove the AC cord or DC power lines from the system, or power down or remove the CPIP5430.
4. Remove the chassis or system cover(s) as necessary for access to the chassis backplane.
5. Locate the desired peripheral slot.
6. Remove any filler panel (or existing board) that might fill that slot.

7. With the CPIP5430-RTM1 in the correct vertical position that matches the pin positioning of the backplane, and the levers of the two injector/ejector handles in the outward position, carefully slide the transition module into the appropriate slot and seat tightly into the backplane.
8. Simultaneously move the injector/ejector levers in an inward direction so they lock in place.
9. Secure in place with the screws provided on the outside edge of each injector/ejector lever. Be sure the screws make good contact with the transverse mounting rails to minimize RF emissions.
10. Connect the appropriate cables to the rear of the transition module.
11. Replace the chassis or system cover(s), reconnect the system to the AC or DC power source, and turn the equipment power on, or if hot swapping, you may now install the CPIP5430 SBC.

Pin Assignments

The following subsections include pin assignment information for the major connectors on the CPIP5430-RTM1 rear transition module.

User I/O Connector (J5)

Connector J3 and J5 are 110-pin AMP Z-pack 2mm hard metric type B connectors. The pin assignments for these CompactPCI connectors can be found in Chapter 6, *Connector Pin Assignments*. Connector J4 on the RTM is for alignment purposes only.

Table 5-3. J5 User I/O Connector

POS	Row A	Row B	Row C	Row D	Row E	Row F
22	DA2	CS1_L	CS3_L	DA1	DACTV_L	GND
21	DIOW_L	DMACK_L	DIOR_L	PDIA_L	DA0	GND
20	DD0	DD15	INTRQ	DMARQ	IORDY	GND
19	DD12	DD2	DD13	DD1	DD14	GND
18	DD5	DD10	DD4	DD11	DD3	GND
17	DRESET_L	DD7	DD8	DD6	DD9	GND
16	RSVD	RSVD	GND	RSVD	RSVD	GND
15	RSVD	GND	RSVD	GND	RSVD	GND
14	RSVD	RSVD	RSVD	RSVD	RSVD	GND
13	+5.0V_IN	+5.0V_IN	+12V	+3.3V_IN	+3.3V_IN	GND
12	DDCCLK	DDCDAT	GND	GND	GND	GND
11	VSYNC	HSYNC	BLUE	GREEN	RED	GND
10	USB_2+	USB_2-	GND	USB_3+	USB_3-	GND
9	MDIO_0+	MDIO_0-	GND	MDIO_1+	MDIO_1-	GND
8	MDIO_2+	MDIO_2-	GND	MDIO_3+	MDIO_3-	GND
7	SATA_0TX-	SATA_0RX-	COM2_DTR_L	COM2_RI_L	COM2_DSR_L	GND

Table 5-3. J5 User I/O Connector (continued)

POS	Row A	Row B	Row C	Row D	Row E	Row F
6	SATA_0TX+	SATA_0RX+	COM2_TXD	COM2_RXD	COM2_CTS_L	GND
5				COM2_RTS_L	COM2_DCD_L	GND
4						GND
3						GND
2	RSVD	RSVD	RSVD	RSVD	RSVD	GND
1	IPMB_CLK	IPMB_DATA	IPMB_PWR	USB_CTRL	USB_OC2/3	GND

Table 5-4. J3 User I/O Connector

POS	Row A	Row B	Row C	Row D	Row E	Row F
19	GND	+12V	GND	-12V	GND	GND
18		LP_A_DA0-	GND	LP_A_DC0+	LP_A_DC0-	GND
17	LP_A_DB0+	LP_A_DB0-	GND	LP_A_DD0+	LP_A_DD0-	GND
16	LP_B_DA1+	LP_B_DA1-	GND	LP_B_DC1+	LP_B_DC1-	GND
15	LP_B_DB1+	LP_B_DB1-	GND	LP_B_DD1+	LP_B_DD1-	GND
14	+3.3V_IN	+3.3V_IN	+3.3V_IN	+5.0V_IN	+5.0V_IN	GND
13	PMCIO53	PMCIO28	PMCIO27	PMCIO2	PMCIO1	GND
12	PMCIO54	PMCIO30	PMCIO29	PMCIO4	PMCIO3	GND
11	PMCIO55	PMCIO32	PMCIO31	PMCIO6	PMCIO5	GND
10	PMCIO56	PMCIO34	PMCIO33	PMCIO8	PMCIO7	GND
9	PMCIO57	PMCIO36	PMCIO35	PMCIO10	PMCIO9	GND
8	PMCIO58	PMCIO38	PMCIO37	PMCIO12	PMCIO11	GND
7	PMCIO59	PMCIO40	PMCIO39	PMCIO14	PMCIO13	GND
6	PMCIO60	PMCIO42	PMCIO41	PMCIO16	PMCIO15	GND
5	PMCIO61	PMCIO44	PMCIO43	PMCIO18	PMCIO17	GND

Table 5-4. J3 User I/O Connector (continued)

POS	Row A	Row B	Row C	Row D	Row E	Row F
4	PMCIO62	PMCIO46	PMCIO45	PMCIO20	PMCIO19	GND
3	PMCIO63	PMCIO48	PMCIO47	PMCIO22	PMCIO21	GND
2	PMCIO64	PMCIO50	PMCIO49	PMCIO24	PMCIO23	GND
1	_5V_IN	PMCIO52	PMCIO51	PMCIO26	PMCIO25	GND

PMC Connectors

Two 64-pin surface mount connectors on CPIP5430-RTM1 provide an interface for an optional add-on PMC I/O module. All serial port signals are at TTL levels.

Table 5-5. PMC Connector J10 Pin Assignments

Pin	Signal	Signal	Pin
1	PMCIO1	PMCIO2	2
3	PMCIO3	PMCIO4	4
5	PMCIO5	PMCIO6	6
7	PMCIO7	PMCIO8	8
9	PMCIO9	PMCIO10	10
11	PMCIO11	PMCIO12	12
13	PMCIO13	PMCIO14	14
15	PMCIO15	PMCIO16	16
17	PMCIO17	PMCIO18	18
19	PMCIO19	PMCIO20	20
21	PMCIO21	PMCIO22	22
23	PMCIO23	PMCIO24	24
25	PMCIO25	PMCIO26	26
27	PMCIO27	PMCIO28	28

Table 5-5. PMC Connector J10 Pin Assignments

Pin	Signal	Signal	Pin
29	PMCIO29	PMCIO30	30
31	PMCIO31	PMCIO32	32
33	PMCIO33	PMCIO34	34
35	PMCIO35	PMCIO36	36
37	PMCIO37	PMCIO38	38
39	PMCIO39	PMCIO40	40
41	PMCIO41	PMCIO42	42
43	PMCIO43	PMCIO44	44
45	PMCIO45	PMCIO46	46
47	PMCIO47	PMCIO48	48
49	PMCIO49	PMCIO50	50
51	PMCIO51	PMCIO52	52
53	PMCIO53	PMCIO54	54
55	PMCIO55	PMCIO56	56
57	PMCIO57	PMCIO58	58
59	PMCIO59	PMCIO60	60
61	PMCIO61	PMCIO62	62
63	PMCIO63	PMCIO64	64

Table 5-6. J14 PMC (Power) Pin Assignments

Pin	Signal	Signal	Pin
1	Signal (reserved)	+12V	2
3	Signal (reserved)	Signal (reserved)	4
5	+5V	Signal (reserved)	6
7	Signal (reserved)	Signal (reserved)	8

Table 5-6. J14 PMC (Power) Pin Assignments (continued)

Pin	Signal	Signal	Pin
9	Signal (reserved)	+3.3V	10
11	Signal (reserved)	Signal (reserved)	12
13	GND	Signal (reserved)	14
15	Signal (reserved)	Signal (reserved)	16
17	Signal (reserved)	GND	18
19	Signal (reserved)	Signal (reserved)	20
21	+5V	Signal (reserved)	22
23	Signal (reserved)	Signal (reserved)	24
25	Signal (reserved)	+3.3V	26
27	Signal (reserved)	Signal (reserved)	28
29	GND	Signal (reserved)	30
31	Signal (reserved)	Signal (reserved)	32
33	Signal (reserved)	GND	34
35	Signal (reserved)	Signal (reserved)	36
37	+5V	Signal (reserved)	38
39	Signal (reserved)	Signal (reserved)	40
41	Signal (reserved)	+3.3V	42
43	Signal (reserved)	Signal (reserved)	44
45	GND	Signal (reserved)	46
47	Signal (reserved)	Signal (reserved)	48
49	Signal (reserved)	GND	50
51	Signal (reserved)	Signal (reserved)	52
53	+5V	Signal (reserved)	54
55	Signal (reserved)	Signal (reserved)	56

Table 5-6. J14 PMC (Power) Pin Assignments (continued)

Pin	Signal	Signal	Pin
57	Signal (reserved)	+3.3V	58
59	Signal (reserved)	Signal (reserved)	60
61	-12V	Signal (reserved)	62
63	Signal (reserved)	Signal (reserved)	64

40-Pin IDE Connector

The following pinout applies to the 40-pin IDE connector on the CPIP5430-RTM1.

Table 5-7. IDE Connect Pin Assignment

Pin	Signal	Signal	Pin
1	Reset-	Gnd	2
3	D7	D8	4
5	D6	D9	6
7	D5	D10	8
9	D4	D11	10
11	D3	D12	12
13	D2	D13	14
15	D1	D14	16
17	D0	D15	18
19	Gnd	Key	20
21	21	Gnd	22
23	IOW-	Gnd	24
25	IOR-	Gnd	26
27	IOCHRDY-	SPSYNC/ALE	28

Table 5-7. IDE Connect Pin Assignment (continued)

Pin	Signal	Signal	Pin
29	reserved	Gnd	30
31	INTRQ	IOCS16-	32
33	ADDR1	PDIAG-	34
35	ADDR0	ADDR2	36
37	CS!FX-	CS3FX-	38
39	DASP-	Gnd	40

IDE port	TTL levels
DMARQ	DMA request
DMACK_L	DMA acknowledge
DIOR_L	I/O read
DIOW_L	I/O write
IORDY	indicates drive ready for I/O
DD(15:0)	data lines
DRESET_L	reset signal to drive
CS1FX_L	chip select drive 0 or command register block select
CS3FX_L	chip select drive 1 or command register block select
DA(2:0)	drive register and data port address lines
INTRQ	drive interrupt request

COM2

The following pin assignments apply to the COM2 port on the CPIP5430RTM1.

Table 5-8. RTM COM2 Pin Assignments

Pin	Signal	Function
1	DCD#	Data Carrier Detect
2	RTS#	Request to Send
3	GND	Ground
4	TXD	Transmit Data
5	RXD	Receive Data
6	GND	Ground
7	CTS#	Clear to Send
8	DTR#	Data Terminal Ready

USB Port 2

The following pin assignments apply to the USB2 pinouts on the rear panel of the CPIP5430-RTM1. External cabling also carries VBUS and GND wires on each segment to deliver power to devices. VBUS is nominally +5 V at the source. VBUS is protected against external faults by a resetable fuse. Control of the USB output power is controlled by the host board.

Table 5-9. RTM USB Port 2 Pin Assignments

Pin	Signal	Function
1	VBUS	Current limited USB power
2	Data (-)	USB serial communication differential pair
3	Data (+)	USB serial communication differential pair
4	Ground	USB port common

Ethernet Connector

The following connector pinouts apply to the CPIP5430-RTM1. The RTM supports 10/100/1000Base-T Ethernet signals.The RTM has no status LEDs. When the RTM Ethernet port is selected, the CPIP5430 Ethernet ports (RJ45) provide the status LEDs for the RTM.

Table 5-10. RTM Ethernet Connector Pin Assignments

Pin	1000 Mb/s	10/100 Mb/s
1	MDIO_0+	TD+
2	MDIO_0-	TD-
3	MDIO_1+	RD+
4	MDIO_2+	Not Used
5	MDIO_2-	Not Used
6	MDIO_1-	RD-
7	MDIO_3+	Not Used
8	MDIO_3-	Not Used

CompactFlash

The following pin assignments apply to the Type II 50-pin CompactFlash connector on the CPIP5430-RTM1.

Table 5-11. CompactFlash Connector

Pin	Signal	Signal	Pin
1	GND	DD3	2
3	DD4	DD5	4
5	DD6	DD7	6
7	DCS1_L	GND	8
9	GND	GND	10

Table 5-11. CompactFlash Connector (continued)

Pin	Signal	Signal	Pin
11	GND	GND	12
13	+5.0V	GND	14
15	GND	GND	16
17	GND	DA2	18
19	DA1	DA0	20
21	DD0	DD1	22
23	DD2	NC	24
25	NC	NC	26
27	DD11	DD12	28
29	DD13	DD14	30
31	DD15	DC3_L	32
33	NC	SDIOR_L	34
35	DIOW_L	+5.0V	36
37	IRQ	+5.0V	38
39	CSEL_L	NC	40
41	BRSTDRV_L	DIORDY	42
43	DREQ	DACK_L	44
45	DASP_L	PDIAG_L	46
47	DD8	DD9	48
49	DD10	GND	50

Serial ATA

A Serial ATA hard drive can be connected to the CPIP5430-RTM1 via a cable, where the hard drive signal connector connects with the signal cable receptacle and the other end of the cable is inserted into the RTM on-board signal connector. The signal cable wire consists of two twinax sections in a common outer sheath.

In addition to the signal cable, there is a separate power cable for the cabled connection. The RTM will not provide the Serial ATA power cable connection.

Signal Segment Key			
Signal segment	S1	Gnd	2nd mate
	S2	A+	Differential signal pair A from Phy
	S3	A-	
	S4	Gnd	2nd mate
	S5	B-	Differential signal pair B from Phy
	S6	B+	
	S7	Gnd	2nd mate
Signal Segment "L"			
Central Connector Polarizer			
Power Segment "L"			
Power segment	P1	V_{33}	3.3 V power
	P2	V_{33}	3.3 V power
	P3	V_{33}	3.3 V power, pre-charge, 2nd mate
	P4	Gnd	1st mate
	P5	Gnd	2nd mate
	P6	Gnd	2nd mate
	P7	V_5	5 V power, pre-charge, 2nd mate
	P8	V_5	5 V power
	P9	V_5	5 V power
	P10	Gnd	2nd mate
	P11	Reserved	1. The pin corresponding to P11 in the backplane receptacle connector is also reserved 2. The corresponding pin to be mated with P11 in the power cable receptacle connector shall always be grounded
	P12	Gnd	1st mate
	P13	V_{12}	12 V power, pre-charge, 2nd mate
	P14	V_{12}	12 V power
	P15	V_{12}	12 V power
Power Segment Key			

Figure 5-3. Serial ATA Connection Pin Assignment

Signal	Description
IO_SATA_Tx(15:0)	Differential SATA signal pair that originates at the I/O controller (Tx) and is received by the SATA disk drive (Rx). These signals must be 100 ohms differential characteristic impedance as per the Serial-ATA 1.0 specification.
IO_SATA_Rx(15:0)	Differential SATA signal pair that originates at the SATA disk drive (Tx) and is received by the I/O controller (Rx). These signals must be 100 ohms differential characteristic impedance. As per the Serial-ATA 1.0 specification.

Connector Pin Assignments

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This chapter provides connector pin assignments for the CPIP5430 series processor boards. For pin assignments on the transition module, refer to Chapter 5, *Rear Transition Module for CPIP5430*.

PCI Mezzanine (PMC) Connectors (J9/11, J8/J10, J5/J7, J6)

The following tables list the PMC bus signal pinouts for the PMC connectors on theCPIP5430. The PMC bus connects to the internal PCI bus (bus 1), which is 64-bits wide.

There are four, 64-pin EIA E700 AAAB SMT connectors for the first 64-bit PMC slot with feature connector (for PIM pinout), and there are three, 64-pin EIA E700 AAAB SMT connectors for the second 64-bit PMC slot (without feature connector) on the CPIP5430.

Note For all PMC Connectors, PCI_RSVD = PCI Reserved Pin

Table 6-1. PMC Connector J9, J11 Pin Assignments

Pin	Signal	Signal	Pin
1	TCK	–12V	2
3	GND	INTA#	4
5	INTB#	INTC#	6
7	PRESENT#	+5V	8
9	INTD#	PCI_RSVD	10
11	GND	+3.3Vaux	12
13	CLK	GND	14
15	GND	GNT#	16
17	REQ#	+5V	18

Table 6-1. PMC Connector J9, J11 Pin Assignments

Pin	Signal	Signal	Pin
19	VIO	AD31	20
21	AD28	AD27	22
23	AD25	GND	24
25	GND	C/BE3#	26
27	AD22	AD21	28
29	AD19	+5V	30
31	VIO	AD17	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	GND	LOCK#	40
41	PCI_RSVD	PCI_RSVD	42
43	PAR	GND	44
45	VIO	AD15	46
47	AD12	AD11	48
49	AD09	+5V	50
51	GND	C/BE0#	52
53	AD06	AD05	54
55	AD04	GND	56
57	VIO	AD03	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	REQ64#	64

Table 6-2. PMC Connector J5/J7 Pin Assignments

Pin	Signal	Signal	Pin
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	PCI_RSVD	8
9	PCI_RSVD	PCI_RSVD	10
11	PRESENT#	+3.3V	12
13	PCI_RRESET#	PRESENT#	14
15	+3.3V	PRESENT#	16
17	PME#	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	+3.3V	24
25	IDSEL	AD23	26
27	+3.3V	AD20	28
29	AD18	GND	30
31	AD16	C/BE2#	32
33	GND	PMC_RSVD1	34
35	TRDY#	+3.3V	36
37	GND	STOP#	38
39	PERR#	GND	40
41	+3.3V	SERR#	42
43	C/BE1#	GND	44
45	AD14	AD13	46
47	M66EN	AD10	48
49	AD8	+3.3V	50

Table 6-2. PMC Connector J5/J7 Pin Assignments

Pin	Signal	Signal	Pin
51	AD7	PMC_RSVD2	52
53	+3.3V	PMC_RSVD3	54
55	PCI_RSVD	GND	56
57	PCI_RSVD	PCI_RSVD	58
59	GND	PCI_RSVD	60
61	ACK64#	+3.3V	62
63	GND	PCI_RSVD	64

Note

1:	J7	2nd IDSEL
2:	J7	2nd PCI REQ#
3:	J7	2nd PCI GNT#

Table 6-3. PMC Connector J8/J10 Pin Assignments

Pin	Signal	Signal	Pin
1	PCI_RSVD	GND	2
3	GND	C/BE7#	4
5	C/BE6#	C/BE5#	6
7	C/BE4#	GND	8
9	VIO	PAR64	10
11	AD63	AD62	12
13	AD61	GND	14
15	GND	AD60	16
17	AD59	AD58	18
19	AD57	GND	20
21	VIO	AD56	22
23	AD55	AD54	24
25	AD53	GND	26
27	GND	AD52	28
29	AD51	AD50	30
31	AD49	GND	32
33	GND	AD48	34
35	AD47	AD46	36
37	AD45	GND	38
39	VIO	AD44	40
41	AD43	AD42	42
43	AD41	GND	44
45	GND	AD40	46
47	AD39	AD38	48

Table 6-3. PMC Connector J8/J10 Pin Assignments

Pin	Signal	Signal	Pin
49	AD37	GND	50
51	GND	AD36	52
53	AD35	AD34	54
55	D33	GND	56
57	VIO	AD32	58
59	PCI_RSVD	PCI_RSVD	60
61	PCI_RSVD	GND	62
63	GND	PCI_RSVD	64

Table 6-4. PMC Connector J6 Pin Assignments

Pin	Signal	Signal	Pin
1	PMCIO1	PMCIO2	2
3	PMCIO3	PMCIO4	4
5	PMCIO5	PMCIO6	6
7	PMCIO7	PMCIO8	8
9	PMCIO9	PMCIO10	10
11	PMCIO11	PMCIO12	12
13	PMCIO13	PMCIO14	14
15	PMCIO15	PMCIO16	16
17	PMCIO17	PMCIO18	18
19	PMCIO19	PMCIO20	20
21	PMCIO21	PMCIO22	22
23	PMCIO23	PMCIO24	24
25	PMCIO25	PMCIO26	26
27	PMCIO27	PMCIO28	28
29	PMCIO29	PMCIO30	30
31	PMCIO31	PMCIO32	32
33	PMCIO33	PMCIO34	34
35	PMCIO35	PMCIO36	36
37	PMCIO37	PMCIO38	38
39	PMCIO39	PMCIO40	40
41	PMCIO41	PMCIO42	42
43	PMCIO43	PMCIO44	44
45	PMCIO45	PMCIO46	46
47	PMCIO47	PMCIO48	48

Table 6-4. PMC Connector J6 Pin Assignments

Pin	Signal	Signal	Pin
49	PMCIO49	PMCIO50	50
51	PMCIO51	PMCIO52	52
53	PMCIO53	PMCIO54	54
55	PMCIO55	PMCIO56	56
57	PMCIO57	PMCIO58	58
59	PMCIO59	PMCIO60	60
61	PMCIO61	PMCIO62	62
63	PMCIO63	PMCIO64	64

Notes

1. The VIO signals are default-connected to +3.3V via a resistor. Please do not apply any “+5V only” PMC module on the PMC sockets.
2. The J6 signals are connected to the CompactPCI J3 connector. To use those signals, the RTM needs to be custom designed for special purpose or to have a PIM connector on board.

Backplane Connectors

The CPIP5430 does not utilize the PCI bus on the backplane. The only connections made are power and ground connections via J1/J2. This section describes only the connections that the CPIP5430 makes to the backplane.

Table 6-5. Power Connector J1 Pin Assignments

Pin	Z	A	B	C	D	E	F
25	GND	+5.0V		ENUM#	+3.3V	+5.0V	GND
24	GND		+5.0V	V(IO)[1]			GND
23	GND	+3.3V			+5.0V[1]		GND
22	GND		GND	+3.3V[1]			GND
21	GND	+3.3V					GND
20	GND		GND	V(IO)			GND
19	GND	+3.3V			GND[1]		GND
18	GND		GND	+3.3V			GND
17	GND	+3.3V	IPMB_SCL	IPMB_SDL	GND[1]		GND
16	GND		GND	V(IO)			GND
15	GND	+3.3V			BDSEL#		GND
KEY	GND						GND
11	GND				GND[1]		GND
10	GND		GND	+3.3V			GND
9	GND				GND[1]		GND
8	GND		GND	V(IO)			GND
7	GND				GND[1]		GND
6	GND		RSVD	+3.3V[1]			GND
5	GND			CPCI_PRST#	GND[1]		GND

Table 6-5. Power Connector J1 Pin Assignments (continued)

Pin	Z	A	B	C	D	E	F
4	GND	IPMB_PWR	HEALTHY#	V(IO)[1]			GND
3	GND				+5.0V[1]		GND
2	GND		+5.0V				GND
1	GND	+5.0V	-12V		+12V	+5.0V	GND

Note 1. Early power pins.

Table 6-6. Ground Connector J2 Pin Assignments

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND		GND				GND
20	GND		GND		GND		GND
19	GND		GND				GND
18	GND				GND		GND
17	GND		GND				GND
16	GND			RSVD	GND		GND
15	GND		GND	RSVD			GND
14	GND				GND		GND
13	GND		GND	V(IO)			GND
12	GND				GND		GND
11	GND		GND	V(IO)			GND
10	GND				GND		GND
9	GND		GND	V(IO)			GND
8	GND				GND		GND
7	GND		GND	V(IO)			GND
6	GND				GND		GND

Table 6-6. Ground Connector J2 Pin Assignments (continued)

Pin	Z	A	B	C	D	E	F
5	GND		GND	V(IO)			GND
4	GND	V(IO)			GND		GND
3	GND		GND				GND
2	GND			SYS_SLOT#			GND
1	GND		GND				GND

Table 6-7. User I/OJ3 Connector Pin Assignments

Pin	Z	A	B	C	D	E	F
19	GND	GND	+12V	GND	-12V	GND	GND
18	GND	LPa_DA0+	LPa_DA0-	GND	LPa_DC0+	LPa_DC0-	GND
17	GND	LPa_DB0+	LPa_DB0-	GND	LPa_DD0+	LPa_DD0-	GND
16	GND	LPb_DA1+	LPb_DA1-	GND	LPb_DC1+	LPb_DC1-	GND
15	GND	LPb_DB1+	LPb_DB1-	GND	LPb_DD1+	LPb_DD1-	GND
14	GND	+3.3V	+3.3V	+3.3V	+5V	+5V	GND
13	GND	PMCIO53	PMCIO28	PMCIO27	PMCIO2	PMCIO1	GND
12	GND	PMCIO54	PMCIO30	PMCIO29	PMCIO4	PMCIO3	GND
11	GND	PMCIO55	PMCIO32	PMCIO31	PMCIO6	PMCIO5	GND
10	GND	PMCIO56	PMCIO34	PMCIO33	PMCIO8	PMCIO7	GND
9	GND	PMCIO57	PMCIO36	PMCIO35	PMCIO10	PMCIO9	GND
8	GND	PMCIO58	PMCIO38	PMCIO37	PMCIO12	PMCIO11	GND
7	GND	PMCIO59	PMCIO40	PMCIO39	PMCIO14	PMCIO13	GND
6	GND	PMCIO60	PMCIO42	PMCIO41	PMCIO16	PMCIO15	GND
5	GND	PMCIO61	PMCIO44	PMCIO43	PMCIO18	PMCIO17	GND

Table 6-7. User I/OJ3 Connector Pin Assignments (continued)

Pin	Z	A	B	C	D	E	F
4	GND	PMCIO62	PMCIO46	PMCIO45	PMCIO20	PMCIO19	GND
3	GND	PMCIO63	PMCIO48	PMCIO47	PMCIO22	PMCIO21	GND
2	GND	PMCIO64	PMCIO50	PMCIO49	PMCIO24	PMCIO23	GND
1	GND	VIO(+3.3V)	PMCIO52	PMCIO51	PMCIO26	PMCIO25	GND

Table 6-8. User I/O J5 Connector Pin Assignments

Pin	Z	A	B	C	D	E	F
22	GND	DA2	CS1-	CS3-	DA1	DACTV-	GND
21	GND	DIOW-	DMACK-	DIOR-	PDIAG-	DA0	GND
20	GND	DD0	DD15	INTRQ	DMARQ	IORDY	GND
19	GND	DD12	DD2	DD13	DD1	DD14	GND
18	GND	DD5	DD10	DD4	DD11	DD3	GND
17	GND	DRESET-	DD7	DD8	DD6	DD9	GND
16	GND	RSVD	RSVD	GND	RSVD	RSVD	GND
15	GND	RSVD	GND	RSVD	GND	RSVD	GND
14	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
13	GND	+5V	+5V	+5V	+3.3V	+3.3V	GND
12	GND	RSVD	RSVD	GND	GND	GND	GND
11	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
10	GND	USB-2+	USB-2-	GND	USB-3+	USB-3-	GND
9[1]	GND	BI-DA+	BI-DA-	GND	BI-DB+	BI-DB-	GND
8	GND	BI-DC+	BI-DC-	GND	BI-DD+	BI-DD-	GND
7	GND	SATA0_TX-	SATA0_RX-	DTR	RI	DSR	GND
6	GND	SATA0_TX	SATA0_RX	TXD	RXD	CTS	GND
5	GND				RTS	DCD	GND

Table 6-8. User I/O J5 Connector Pin Assignments (continued)

Pin	Z	A	B	C	D	E	F
4	GND						GND
3	GND						GND
2	GND	RSVD	RSVD	RSVD	RSVD	RSVD	GND
1	GND	IPMB_CLK	IPMB_DAT	IPMB_PWR	USB_CTRL[2]	USB_OC	GND

Notes

1. **BI-Dx+/-**

   J5 Row 9 pins arranged to provide backward compatibility to 5385 100BaseTX interface vs. std. arrangement as in J3 Rows 15-16 and 17-18.

2. **USB_CTRL**

   +12V via SBC jumper header for backward compatibility with RTM.

USB Connector

The CPIP5430 does not have a keyboard or mouse connector. Use a USB connection on the CPIP5430-RTM1 The USB port on the front panel of the CPIP5430 SBC is for development, service, and setup operations only.

Table 6-9. Front USB J14 Connector Pin Assignments

Pin	Signal
1	VCC
2	DATA-
3	DATA+
4	GND

Serial Port COM1 Connector

the CPIP5430 has one serial port RJ45 connector on the front panel with the following pin assignments. It is configured as DTE.

Table 6-10. COM1 J17 Pin Assignments

	Signal	Direction
1	DCD	Input
2	RTS	Output
3	GNDC	N/A
4	TXD	Output
5	RXD	Input
6	GNDC	N/A
7	CTS	Input
8	DTR	Output

Management Ethernet Port Connector

The CPIP5430 has one front panel Gigabit Ethernet connector. It is an industry standard RJ45 connector with the following pin assignments.

Table 6-11. 10/100/1000Mb/s J16 Connector Pin Assignments

Pin	1000 Mbit/s	10/100 Mbit/s
1	MDIO0+	TD+
2	MDIO0-	TD-
3	MDIO1+	RD+
4	MDIO2+	Not Used
5	MDIO2-	Not Used
6	MDIO1-	RD-
7	MDIO3+	Not Used
8	MDIO3-	Not Used

IDE Port

The following pinout information applies to the 44-pin primary IDE connector on the CPIP5430 at J18.

Table 6-12. IDE Port J18 Connector Pin Assignments

Pin	Signal	Function	Pin	Signal	Function
1	BRSTDRVJ	Reset	2	GND	Ground
3	DD7	Data7	4	DD8	Data8
5	DD6	Data6	6	DD9	Data9
7	DD5	Data5	8	DD10	Data10
9	DD4	Data4	10	DD11	Data11
11	DD3	Data3	12	DD12	Data12
13	DD2	Data2	14	DD13	Data13
15	DD1	Data1	16	DD14	Data14
17	DD0	Data0	18	DD15	Data15
19	GND	Ground	20	NC (key pin)	-
21	DDREQ	Request	22	GND	Ground
23	DIOWJ	I/O Write	24	GND	Ground
25	DIORJ	I/O Read	26	GND	Ground
27	IORDY	I/O Ready	28	CSEL	Cable Select
29	DDACKJ	DMA Acknowledge	30	GND	Ground
31	IRQ14	Interrupt Request	32	NC	No Connect
33	DA1	Device Address 1	34	NC	No Connect
35	DA0	Device Address 0	36	DA2	Device Address 2
37	CS1PJ	Chip Select 1	38	CS3PJ	Chip Select 3
39	IDEACTPJ	Device Active	40	GND	Ground
41	+5V	+5V	42	+5V	+5V
43	GND	Ground	44	NC	No Connect

Specifications A

Environmental

This appendix contains the environmental and mechanical specifications for the CPIP5430 single board computer and CPIP5430-RTM01 transition module. For information on thermal validation and testing, refer to Appendix B, *Thermal Validation*.

Table A-1. CPIP5430 Environmental Specifications

Condition	Range or Value
Temperature Range	32°F (0°C) to 137°F (55°C) operating (*see note below*)
	-4°F (-20°C) to 176°F (80°C) nonoperating
	(derated 1°C per 1000 ft. or 305 m. above sea level)
	Note For a 2.2 GHz CPU board with 500 LFM airflow or less, the CPU performance will reduce if the chassis ambient temperature exceeds 50°C.
Humidity (Operating)	5% to 95% @ 104°F (40°C), noncondensed
Humidity (Nonoperating)	0% to 95% @ 104°F (40°C), noncondensed
Operating Altitude	16,404 ft. (5,000 meters) maximum
Storage Altitude (shipping)	40,000 feet (12195 meters)
Maximum wet bulb	82°F (28°C) operating
	90°F (32°C) nonoperating
Minimum dew point	36°F (2°F) operating
Cooling	250 LFM (operating)
Vibration	1.88G rms, 5-500Hz, 3 axis, 30 min./axis, nonoperating
	0.5G rms, 5-500Hz, 3 axis, 1 hr/axis, operating

Table A-1. CPIP5430 Environmental Specifications (continued)

Condition	Range or Value
Shock	15G peak-to-peak, 11ms duration, 3 axis, 3 times/axis, nonoperating
Reliability	
MTBF	139,000 hours for CPU with 1.5GB memory at 25°C
(MIL-HDBK-217F)	
Compliance	CE, FCC Class A
	Designed to meet NEBs 3.0 requirements
Materials	All plastic, PCB and battery material are UL-94V0 certified

Table A-2. CPIP5430 SBC and RTM Power Requirements

Configurations	+5V (+/-5%)		+3.3V (+/-5%)		+12V (+/-5%)		-12V (+/-5%)	
	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.
CPIP5430-2121 1.7 GHz	4.93A	6.01A	2.52A	2.63A	3mA	0.51A	0mA	0.50A
CPIP5430-4241 2.2 GHz	6.13A	6.97A	2.62A	2.72A	3mA	0.26A	0mA	0.25A

Note Although measurements were taken in conjunction with a PMC, the standard IEEE1386.1 PCI Mezzanine Interface is used, which requires +3.3V, +5V, +12V and -12V with a maximum specification stated power requirement of 7.5 W.

Mechanical

The CPIP5430 family of boards are 6U, 4HP wide (233 mm x 160 mm x 20 mm) and conform to PICMG 2.0 CompactPCI (rev. 2.1) and PCI SIG 2.1 specifications (based on model selected).

EMC Compliance

The CPIP5430 controller was tested in an EMC-compliant chassis and meets the requirements for EN55022 Class A equipment. Compliance was achieved under the following conditions:

- ❏ Shielded cables on all external I/O ports
- ❏ Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel
- ❏ Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground
- ❏ Front panel screws properly tightened

For minimum RF emissions, it is essential that the conditions above be implemented. Failure to do so could compromise the EMC compliance of the equipment containing the module.

Thermal Validation

B

Board component temperatures are affected by ambient temperature, air flow, board electrical operation, and software operation. In order to evaluate the thermal performance of a circuit board assembly, it is necessary to test the board under actual operating conditions. These operating conditions vary depending on system design.

While Motorola Computer Group performs thermal analysis in a representative system to verify operation within specified ranges (see Appendix A, *Specifications*), you should evaluate the thermal performance of the board in your application.

This appendix provides systems integrators with information which can be used to conduct thermal evaluations of the board in their specific system configuration. It identifies thermally significant components and lists the corresponding maximum allowable component operating temperatures. It also provides example procedures for component-level temperature measurements.

Thermally Significant Components

The following table summarizes components that exhibit significant temperature rises. These are the components that should be monitored in order to assess thermal performance. The table also supplies the component reference designator and the maximum allowable operating temperature.

You can find components on the board by their reference designators as shown in Figure B-1. Versions of the board that are not fully populated may not contain some of these components.

The preferred measurement location for a component may be *junction*, *case*, or *air* as specified in the table. Junction temperature refers to the temperature measured by an on-chip thermal device. Case temperature

refers to the temperature at the top, center surface of the component. Air temperature refers to the ambient temperature near the component.

Table B-1. Thermally Significant Components

Reference Designator	Generic Description	Max. Allowable Component Temperature (deg. C)	Measurement Location
U8	Perntium-4 Mobile CPU	100° C (Tj)	U8
U27	875P MCH	95° C (Tj)	U27

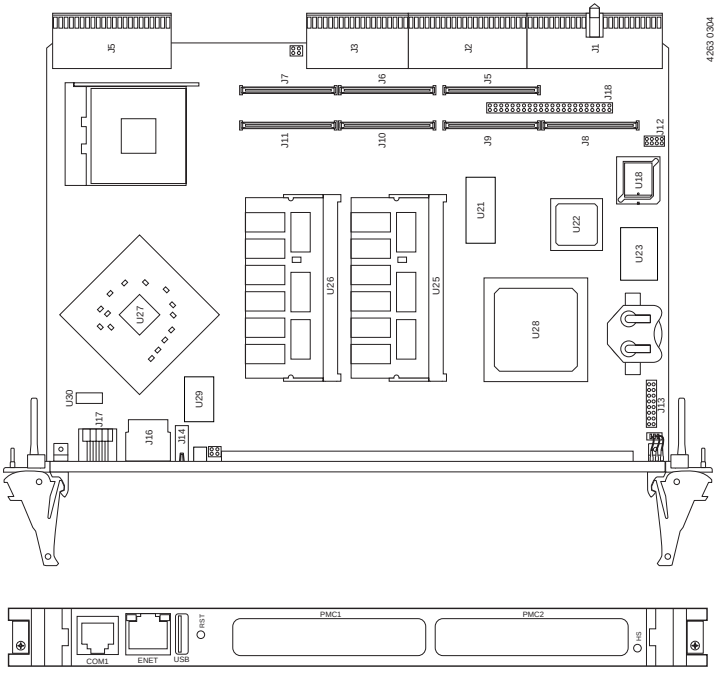


Figure B-1. Thermally Significant Components—Primary Side

Component Temperature Measurement

The following sections outline general temperature measurement methods. For the specific types of measurements required for thermal evaluation of this board, see Table B-1.

Preparation

We recommend 40 AWG (American wire gauge) thermocouples for all thermal measurements. Larger gauge thermocouples can wick heat away from the components and disturb air flowing past the board.

Allow the board to reach thermal equilibrium before taking measurements. Most circuit boards will reach thermal equilibrium within 30 minutes. After the warm up period, monitor a small number of components over time to assure that equilibrium has been reached.

Measuring Junction Temperature

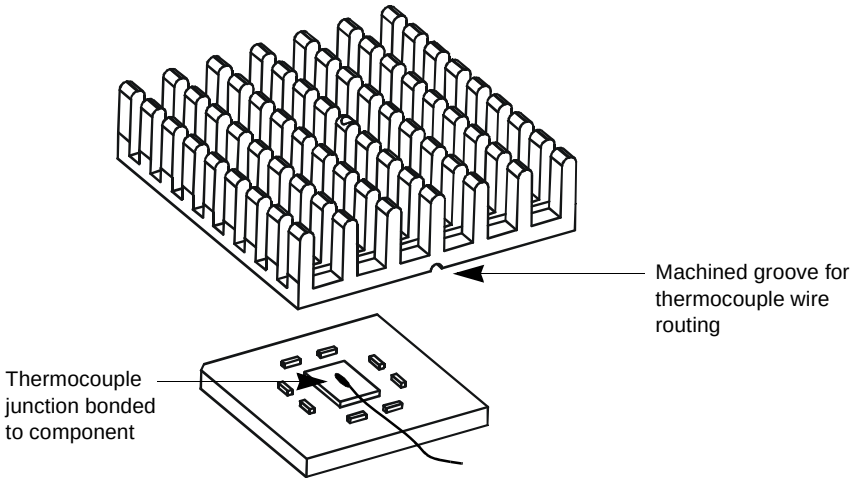
Some components have an on-chip thermal measuring device such as a thermal diode. For instructions on measuring temperatures using the on-board device, refer to the component manufacturer's documentation listed in Appendix E, *Related Documentation*.

Measuring Case Temperature

Measure the case temperature at the center of the top of the component. Make sure there is good thermal contact between the thermocouple junction and the component. We recommend you use a thermally conductive adhesive such as Loctite 384.

If components are covered by mechanical parts such as heatsinks, you will need to machine these parts to route the thermocouple wire. Make sure that the thermocouple junction contacts *only* the electrical component. Also make sure that heatsinks lay flat on electrical components. The following figure shows one method of machining a heatsink base to provide a thermocouple routing path.

Note Machining a heatsink base reduces the contact area between the heatsink and the electrical component. You can partially compensate for this effect by filling the machined areas with thermal grease. The grease should not contact the thermocouple junction.



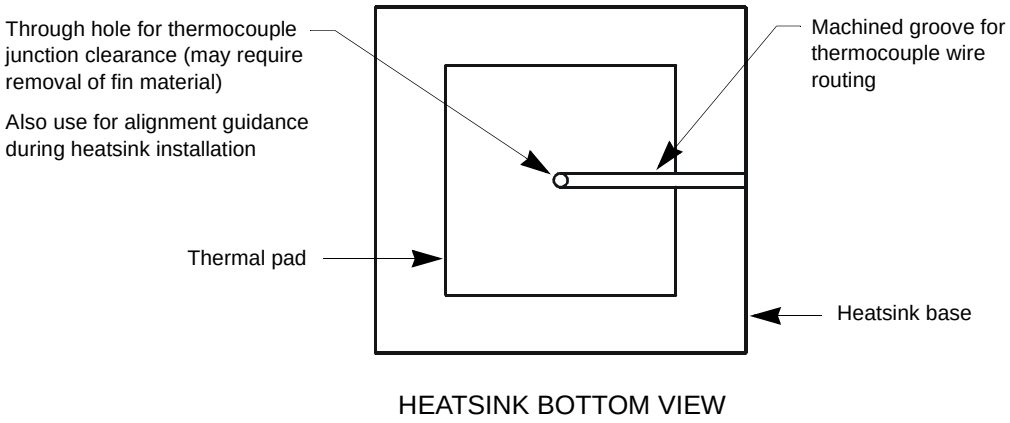


Figure B-2. Mounting a Thermocouple Under a Heatsink

B

Measuring Local Air Temperature

Measure local component ambient temperature by placing the thermocouple downstream of the component. This method is conservative since it includes heating of the air by the component. The following figure illustrates one method of mounting the thermocouple.

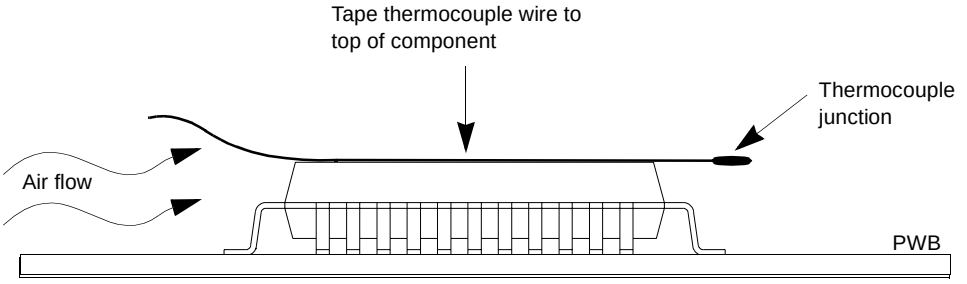


Figure B-3. Measuring Local Air Temperature

Memory Maps

The following table lists the current memory map for the CPIP5430.

Table C-1. CPIP5430 Memory Maps

Descriptor #	Start Address	Address Length	Address Type
0	0000 0000	9FC00	1
1	0009 FC00	400	2
2	000E 0000	20000	2
3	0010 0000	1FEF 0000	1
4	1FFF 0000	F000	3 (ACPI)
5	1FFF FC00	1000	4
6	FEC0 0000	100000	2
7	FEE0 0000	1000	2
8	FFB0 0000	500000	2

PCI Configuration Mapping

The PCI configuration mapping is shown in the following table.

Table C-2. PCI Configuration Mapping

PCI Bus	Device Number Field	PCI Address Line	Function Number	IDSEL Connection (Functions)
0	15	AD31	0	6300ESB
0	15	AD31	1	IDE Controller
0	15	AD31	2	USB Controller
0	15	AD31	3	LPC Function (subtractive decoding)
1	1	AD18	0	Onboard LAN 82546EB
1	2	AD24	0	PMC Slot 1 (1st ID)
1	3	AD25	0	PMC Slot 1 (2nd ID)
1	3	AD26	0	PMC Slot 2

SMBUS Address Map

The following table provides the address and mapping for various devices on the SMBUS.

Table C-3. SMBUS Address Map

Address	Function	Device
A0h	SO-DIMM ID	SO-DIMM
00h	Temperature Monitor	MAX1617
A0h	Boot/FRU data storage (IPMI)	24C256
A2h	Runtime data storage (IPMI	24C512
AAh	BIOS CMOS storage	24C02
A4h	VPD data storage (IPMI)	24C64

Note ID of SO-DIMM 1-4 are selected by two GPIO from CSB SO-DIMM selection table

GPIO13	GPIO12	DIMM
0	0	1
0	1	2
1	0	3
1	1	4

IPMB Address Map

The following IPMB address map is defined based on the controller's slot location.

Table C-4. CompactPCI Peripheral Address Map

Geo. Addr.	IPMB Addr.	Geo. Addr.	IPMB Addr.
0	Disabled	16	D0h
1	B0h	17	D2h
2	B2h	18	D4h
3	B4h	19	D6h
4	B6h	20	D8h
5	B8h	21	DAh
6	BAh	22	DCh
7	BCh	23	DEh
8	BEh	24	E0h
9	C0h	25	E2h
10	C4h	26	E4h
11	C6h	27	E6h
12	C8h	28	E8h
13	CAh	29	EAh
14	CCh	30	ECh
15	CEh	31	Disabled

PCI Interrupt Connections

The following table provides interrupt connections to various devices on the CPIP5430.

Table C-5. PCI Interrupt Connections

Device	PCI Slot Interrupt INTA#	PCI Slot Interrupt INTB#	PCI Slot Interrupt INTC#	PCI Slot Interrupt INTD#	IOAPIC#	IOAPIC PIN#
LAN82546EB	INTG	INTG	INTG	INTG	2 2 2 2	2 3 0 1
PMC Slot 1	INTG	INTG	INTG	INTG	2 2 2 2	0 1 2 3
PMC Slot 2	INTG	INTG	INTG	INTG	2 2 2 2	2 3 0 1
IDE	INTC				1	18
SMBUS		INTB			1	17
USB1	INTA				1	16
USB2		INTD			1	19
Watchdog					2	10
USB 2.0				INTH	1	23
Intel82547	INTC				1	18

Sensor Data Record

The CPIP5430 controller has predefined SDRs such as voltages and system temperature that are indicated by the following table.

Table C-6. Sensor Data Record List

Sensor Number	Sensor Name	Device	Normal Reading	Remark
0x20	Vcore	Zircon	1.3V	
0x21	5V	Zircon	5V	
0x22	3.3V	Zircon	3.3V	
0x24	12V	Zircon	12V	
0x11	Int temp	MAX1617	30° C	Temp inside MAX1617
0x13	CPU temp	MAX1617	45° C	

IPMI Commands

D

Introduction

For other supported IPMI commands (listed below) refer to the *MXP IPMI Subsystem Reference Manual* and the IPMI 1.0 specification for a complete description of these commands. These documents are listed in Appendix E, *Related Documentation*.

- ❏ IPM Device Global Commands
- ❏ PMC Watchdog Timer Commands
- ❏ Event Commands
- ❏ Chassis Commands
- ❏ SEL Device Commands
- ❏ FRU Inventory Commands

The following IPMI commands are implemented in this release of the CPIP5430. These commands may be used by a host device driver and/or application software to communicate with the Zircon, sensors, and other management controllers in the system.

SDR (Sensor Data Record) Device Commands

Zircon firmware supports only the repository updates. During SDR update only (also called modal mode) the commands listed below are supported. Commands not supported during update mode will be responded to with a completion code of SDR Repository Update in progress.

ENTER SDR REPOSITORY UPDATE MODE

Used to enter SDR Repository Update Mode.

EXIT SDR REPOSITORY UPDATE MODE

Used to exit the SDR Repository Update Mode.

Related Documentation

E

Motorola Computer Group Documents

You can obtain the most up-to-date product information in PDF or HTML format by:

- ❏ Contacting your local Motorola sales office
- ❏ Visiting Motorola Computer Group's World Wide Web literature site, http://www.motorola.com/computer literature

Table E-1. Related Documents

Document Title	Part Number
MXP IPMI Subsystem Reference Manual	MXPIPMIA/RM
MXP IPMI Library Reference Manual	MXPAPIA/RM

Related Specifications

For additional information, refer to the following table for related specifications. For your convenience, a source for the listed document is also provided. It is important to note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Table E-2. Related Specifications

Document Title and Source	Source/Publication Number
Intel Corporation http://www.intel.com/design/servers/ipmi	
IPMI Spec v1.5, Document Revision 1.1, February 20, 2002	Intel Corporation, Hewlett-Packard, DEC, NEC

Table E-2. Related Specifications (continued)

Document Title and Source	Source/Publication Number
IEEE http://standards.ieee.org/catalog/	
IEEE Standard for Compact Embedded PC Modules	IEEE P996.1
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc.	P1386.1 Draft 2.0
PCI Industrial Manufacturers Group (PICMG) http://www.picmg.com/	
Compact PCI Specification 2.0, Revision 3.0	PICMG 2.0 R 3.0 Dated 10/1/99
PCI Local Bus Specification, Revision 2.2	PICMG 2.2 Dated 12/8/98
CompactPCI Hot Swap Specification, 2.1, Revision 2.0	PICMG 2.1 R2.0 Dated 1/17/01
CompactPCI Computer Telephony Specification, 2.5, Revision 1.0	PICMG 2.5 R1.0
CompactPCI System Management Bus Specification 2.9, Revision 1.0	PICMG 2.9 R1.0 Rev. 2.0 Dated 2/2/00
CompactPCI Packet Backplane Specification 2.16, D0.9.1	PICMG 2.16 D0.4 Dated 4/10/01

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