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CompactPCI® CPN5360 Single Board Computer and Transition Module

Installation and Reference Guide

CPN5360A/IH1

August 25, 2000 Edition

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Motorola, Inc.
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Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. If the equipment is supplied with a three-conductor AC power cable, the power cable must be plugged into an approved three-contact electrical outlet, with the grounding wire (green/yellow) reliably connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable must meet International Electrotechnical Commission (IEC) safety standards and local electrical regulatory codes.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in any explosive stmosphere such as in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment could result in an explosion and cause injury or damage.

Keep Away From Live Circuits Inside the Equipment.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Service personnel should not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, such personnel should always disconnect power and discharge circuits before touching components.

Use Caution When Exposing or Handling the CRT.

Breakage of a Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, do not handle the CRT and avoid rough handling or jarring of the equipment. Handling of a CRT should be done only by qualified service personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that safety features are maintained.

Observe Warnings in Manual.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.



Warning

To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

Flammability

All Motorola PWBs (printed wiring boards) are manufactured with a flammability rating of 94V-0 by UL-recognized manufacturers.

EMI Caution

Caution

This equipment generates, uses, and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used with adequate EMI protection.

CE Notice (European Community)

Warning

This is a Class A product. In a domestic environment, this product may cause radio interference, in which case the user may be required to take adequate measures.

Motorola Computer Group products with the CE marking comply with the EMC Directive (89/336/EEC). Compliance with this directive implies conformity to the following European Norms:

> EN55022 “Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment”; this product tested to Equipment Class A
>
> EN50082-1:1997 “Electromagnetic Compatibility--Generic Immunity Standard, Part 1, Residential, Commercial and Light Industry”.

System products also fulfill EN60950 (product safety) which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

Board products are tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a CE-marked system will maintain the required EMC/safety performance.

In accordance with European Community directives, a “Declaration of Conformity” has been made and is on file within the European Union. The “Declaration of Conformity” is available on request. Please contact your sales representative.

Lithium Battery Caution

This product contains a lithium battery to power the clock and calendar circuitry.



Caution

Danger of explosion if battery is replaced incorrectly. Replace battery only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to the manufacturer's instructions.



Attention

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabricant.



Vorsicht

Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch denselben oder einen vom Hersteller empfohlenen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.

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About This Manual

This CompactPCI® CPN5360 Single Board Computer (SBC) Installation and Reference Guide describes the installation, components, and configurations of the CPN5360 SBC and Transition Module. Use this guide for general and technical information about the CPN5360 CompactPCI System CPU.

Model Numbers	Description
CPN5360-266	CompactPCI Single Board Computer with 266 MHz processor and 128 or 256MB SDRAM
CPN5360-333	CompactPCI Single Board Computer with 333 MHz processor and 128 or 256MB SDRAM with or without hard drive and J4 connector
CPN5360-500	CompactPCI Single Board Computer with 500MHz processor and 128 or 256MB SDRAM with or without hard drive and J4 connector
CPN5360TM	CompactPCI Transition Module with one or two PIM sites, key/board mouse, USB, CompactFlash, EIDE, floppy, serial, parallel Ethernet, video

Summary of Changes

This table summarizes revisions to this manual.

Date:	Change:
August 25, 2000	Added section, “About this Manual.”
	Revised Chapter 1, for CPN5360 models for use with H.110 bus.
	Revised Table 1-1, for floppy access information on the CPN5360 and CPN5360T.
	Removed “System Management Bus (SMBUS) Alert Signal” from “Special Functions”, “Advanced System Monitoring” in Chapter 1.
	Revised “Remote Setup” in Chapter 4.
	Added “PCI Mezzanine Card Limitations” in Chapter 4.
	Added note to “Using the CPN5360 in a Host Slot” section in Chapter 4.
	Revised Table 4-5, under “Device 00h System” to 00 Status.
	Revised Table A-1, Appendix A.
	Added cooling specification to Table A-4, Appendix A.
	Revised temperature specifications for “Operating” and “Non-operating” conditions in, Table A-4, Appendix A.

Overview of Contents

This section contains a short description of the content of each chapter and appendix in this manual.

This Chapter or Appendix:	Gives you:
Chapter 1, “CPN5360 Single Board Computer and Transition Module Overview”	a detailed CPN5360 product description, information about input/output interfaces, a CPN5360 SBC block diagram and information about special functions.
Chapter 2, "Getting Started"	information about ESD, board installation and power up, replacement of lithium batteries, locations of connectors and indicators.
Chapter 3, "Components on the CPN5360"	the location of major components on the CPN5360 SBC and CPN5360TM80 Transition Module.
Chapter 4, “Functional Description”	a functional description including information about the PCI Bus, host and non-host slot mounting, the watchdog timer, memory address mapping, the I/O address map and the FPGA registers.
Chapter 5, “Pin Assignments”	pin assignments for the SBC and transition module
Appendix A, "Specifications"	board specifications
Appendix B, "WindowsNT 4.0 Installation Error"	information about a potential error in the event viewer log during WindowsNT 4.0 installation
Appendix C, "Related Documentation"	information about related Motorola Computer Group documents, other related documents and URLs for access to more information.

Who Should Use This Guide

The information in this guide is written for system installers, original equipment manufacturers (OEM) and technicians. The procedures assume familiarity with the safety practices and regulatory compliance required for using and modifying electronic equipment. Personnel who install CompactPCI systems should be trained and experienced with the installation of computers and computer equipment.

Comments and Suggestions

We welcome and appreciate your comments on our documentation. We want to know what you think about our manuals and how we can make them better. Mail comments to:

Motorola Computer Group
Reader Comments DW164
2900 S. Diablo Way
Tempe, Arizona 85282

You can also submit comments to the following e-mail address: reader-comments@mcg.mot.com

In all your correspondence, please list your name, position, and company. Be sure to include the title and part number of the manual and tell how you used it. Then tell us your feelings about its strengths and weaknesses and any recommendations for improvements.

CPN5360 Single Board Computer and Transition Module Overview

1

Introduction

The CPN5360 Single Board Computer (SBC) is a hot swap, single-slot, CompactPCI® (Compact Peripheral Communication Interface) compliant computer. It is powered by a Pentium® II processor Low Power module. It can serve either as a standard CompactPCI peripheral CPU or as a system controller. Some models of the CPN5360 SBC work in H.110 systems. These models are the same as other versions except that the J4 connector is removed.

The highly integrated processor gives you a 16MB on-board solid-state disk, USB, PCI EIDE, accelerated graphics, dual Fast Ethernet controllers, and standard PC I/O plus two PMC sites for additional expansion.

An optional Transition Module gives you backplane I/O for PMC sites and on-board devices.

The CPN5360 meets the needs of embedded application developers. Typical applications include broadband data or intelligent network switching, CTI server, industrial control and automation, military and aerospace, and medical, scientific, or imaging products.

Additional Features

The CPN5360 gives you these features:

- Pentium II processor Low Power module for high end embedded applications
- Up to 256MB on-board 3.3V SDRAM memory
- Accelerated 2D graphics with 2MB video memory
- Dual Fast Ethernet controllers for monitoring and telecom applications

- Hot Swap compatibility allowing insertion or removal of the CPN5360 and other peripheral CPU slot boards while the chassis is powered up
- An array of on-board I/O available from the front panel of the CPN5360 and/or the rear panel via the CPN5360TM80 Transition Module
- Models available for H.110 interface

The CPN5360TM80 Transition Module gives you these features:

- rear panel connections for:
  - PS/2 keyboard/mouse
  - video
  - COM2 (serial port)
  - Ethernet 1 and 2
  - PIM 1
- on-board connectors for:
  - PS/2 keyboard/mouse
  - floppy
  - USB0 and USB1
  - primary and secondary IDE

Input/Output Interfaces

Refer to Table 1-1 for brief descriptions of the input/output interfaces on the CPN5360 Single Board Computer and CPN5360TM80 Transition Module. Do not use the rear panel connectors and internal connectors at the same time.

Note When the identical function is available through the CPN5360's front panel and the rear transition module, you can use either the front or the rear, **not both.**

Table 1-1. Input/Output Interfaces on the CPN5360 Single Board Computer and the CPN5360TM80 Transition Module

Function	CPN5360		CPN5360TM80 Transition Module	
	Front Panel	On-board	Rear Panel	On-board
Ethernet 1	RJ-45	-	RJ-45	-
Ethernet 2	-	-	RJ-45	-
COM1 (Serial Port 1)	RJ-45	-	-	10-pin shrouded
COM2 (Serial Port 2)	-	-	9-pin D-sub	-
PMC Panel	PMC 1 Device	-	PMC 1 Device	-
PMC Panel	PMC 2 Device	-	-	-
Keyboard/Mouse	-	-	6-pin mini-DIN	12-pin connector
Floppy [1]	-	-	-	34-pin connector
Parallel	-	-	-	26-pin shrouded
USB 0 and USB 1	-	-	-	two - stacked 4-pin connectors
Video	-	-	15-pin D-sub	-
Primary IDE	-	-	-	40-pin connector
Secondary IDE	-	-	-	40-pin connector
CompactFlash	-	-	-	50-pin connector

[1] The CPN5360 Single Board Computer does not offer front panel or on-board access to a floppy connector. The floppy interface routes through the J4 connector on the CPN5360. This connector is not on telephony (T) versions of the board. Driver updates on the CPN5360T must be done over the network.

Refer to Figure 1-1 for a block diagram of the CPN5360 Single Board Computer.

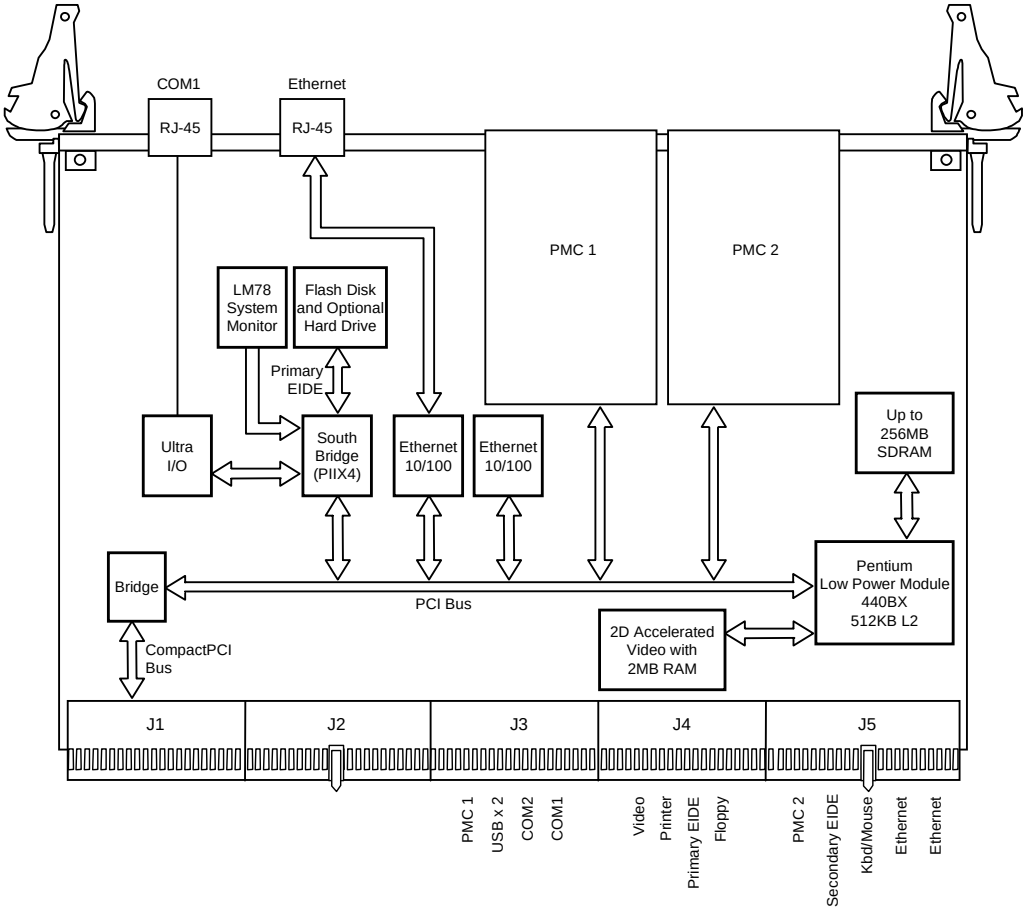


Figure 1-1. Block Diagram of the CPN5360 Single Board Computer

Special Functions

The CPN5360 uses these functions designed for use in certain applications. Refer to Chapter 4 for programmer's reference information.

- Watchdog Timer

  The watchdog timer can operate in four modes:

  - Disabled
  - Sets the timeout flag in the Watchdog Strobe/Status port in ISA I/O memory map
  - Sets the timeout flag in the Watchdog Strobe/Status port in ISA I/O memory map + Assert a selectable interrupt (ISA IRQ)
  - Sets the timeout flag in the Watchdog Strobe/Status port in ISA I/O memory map + Assert NMI followed by a system Reset or Soft Reset

  You can program the watchdog timer via registers in the ISA I/O memory map. The watchdog timer is protected from being accidentally enabled. The timer supports a range of count down time-outs up to eight minutes.

- Advanced System Monitoring

  The CPN5360 monitors the following system events:

  - On-card temperature
  - MMC2 thermal fault
  - On-card voltages +5V, +3.3V, +/-12V and the processor core voltage
  - Chassis power supply loss of regulation

Getting Started 2

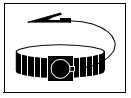
This chapter gives you:

- basic installation information for the CPN5360 Single Board Computer (SBC) and Transition Module
- information about lithium battery replacement
- information about front and rear panel connectors on the SBC and transition module

Note This document treats the CPN5360 SBC as a component of a system, and assumes that you install it in a CompactPCI backplane that is PICMG compliant.

Antistatic Precautions

Use ESD



Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to electrostatic discharge (ESD). After removing the component from its protective wrapper or from the system, place the component flat on a grounded, static-free surface (and, in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an active electrical ground. Note that a system chassis may not be grounded if it is unplugged.

2

Before Installing the CPN5360

After removing the CPN5360 from its packaging:

- Check for obvious physical damage.
- Verify that the coin cell battery is in its holder and inserted correctly.

Make sure that you disconnect the chassis from the main power supply before you continue.

Installing the CPN5360

Use these steps to install the CPN5360 into your computer chassis. Refer to Figure 2-1.

1. Follow the instructions in your chassis user manual to remove any outer cover.
2. Locate the desired peripheral slot.
3. Remove any filler panel (or existing board) that might fill that slot.
4. Install the top and bottom edge of the CPN5360 in the guides of the chassis.
5. Ensure that the levers of the two injector/ejectors are in the inward position.
6. Slide the CPN5360 into the chassis until resistance is felt.
7. Simultaneously move the injector/ejector levers in an outward direction.
8. Verify that the CPN5360 is properly seated and secure it to the chassis using the two screws located adjacent to the injector/ejector levers.
9. Connect the appropriate cables to the CPN5360.

10. Repeat steps 3 through 9 for installing the transition module.

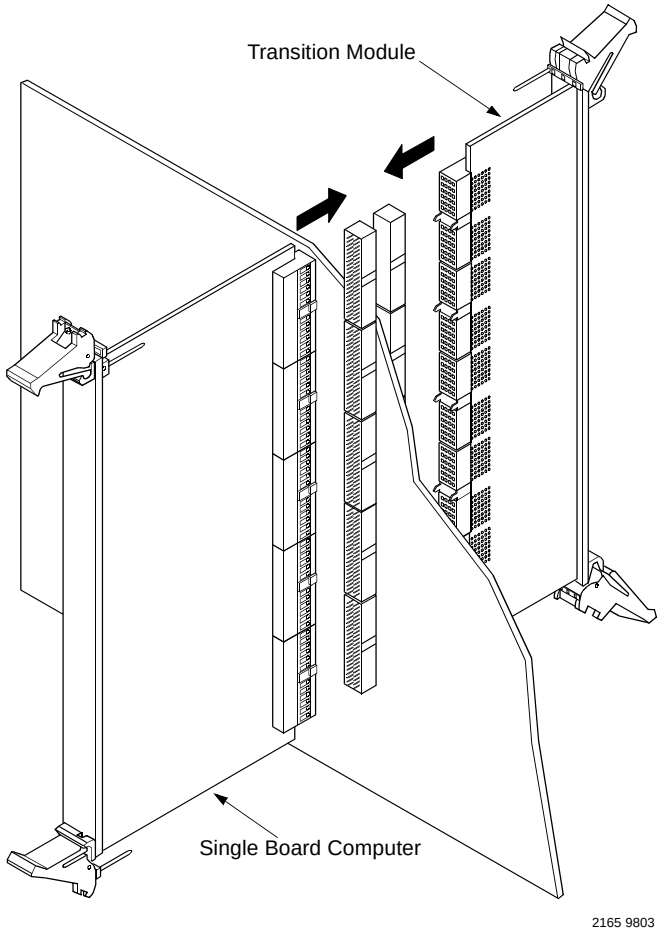


Figure 2-1. Installing the CPN5360 Single Board Computer and Transition Module in Your Computer Chassis

2

Powering up the CPN5360

When you are ready to power up the CPN5360:

- Verify that the chassis power supply voltage setting matches the voltage present in the country of use (if the power supply in your system is not auto-sensing).
- On powering up, the CPN5360 displays the PhoenixBIOS banner and then runs a memory test.

Replacing Lithium Batteries

Follow these safety rules for proper battery operation and to reduce equipment and personal injury hazards when handling lithium batteries. Use the battery for its intended application only.

Note **Do not** recharge, open, puncture or crush, incinerate, expose to high temperatures or dispose of in your general trash collection.

To replace the lithium battery, observe the following guidelines and follow the steps below.

Note When replacing the battery, you must apply power to the board to prevent data loss.



Warning

To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

Warning

Lithium batteries incorporate flammable materials such as lithium and organic solvents. If lithium batteries are short-circuited or exposed to high temperature or pressure, they may burst open and ignite, possibly resulting in injury and/or fire. When dealing with lithium batteries, carefully follow the precautions listed below to prevent accidents.

- ❏ Do not short-circuit.
- ❏ Do not disassemble, deform or apply excessive pressure.
- ❏ Do not heat or incinerate.
- ❏ Do not apply solder directly.
- ❏ Do not use different models, or new and old batteries together.
- ❏ Do not charge.
- ❏ Always check proper polarity.

To replace the on-board backup battery, follow the steps below.

Caution

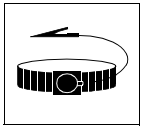
Danger of explosion if battery is replaced incorrectly.

Replace only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage circuits.

Use ESD



Wrist Strap

Attach an ESD strap to your wrist. Attach the other end of the ESD strap to an electrical ground. (Note that the system chassis may not be grounded if it is unplugged.) Secure the ESD strap to your wrist and to ground throughout the procedure.

1. To remove the battery from the module, carefully pull the battery from the socket.
2. Before installing a new battery, make sure that the battery pins are clean.

3. Not the battery polarity and press the new battery into the socket.

Note No soldering is required when the battery is in the socket.

4. Recycle or dispose of the old battery according to local regulations and manufacturer's instructions.

Front Panel Connectors and Indicators on the CPN5360

The CPN5360's front panel has connectors for:

- Ethernet 1 (RJ-45)
- COM1 serial port (RJ-45)
- two PMC Panels (PMC1 and PMC2)

LED Indicator lights on the front panel display of the CPN5360 include:

- Hot Swap status (Blue LED)
- Power (Green LED)

Refer to Figure 2-2 for front panel connectors and LEDs on the CPN5360.

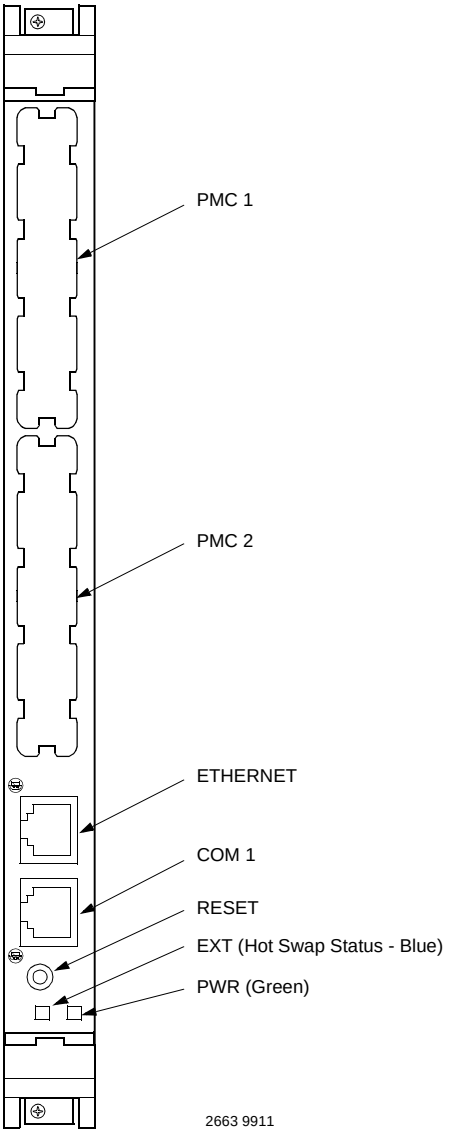


Figure 2-2. Front Panel Connectors and LEDs on the CPN5360 Single Board Computer

Rear Panel Connectors on the CPN5360TM80 Transition Module

The CPN5360 Transition Module has connectors on the rear panel for:

- keyboard/mouse (PS/2)
- Ethernet 1 and Ethernet 2 (RJ45)
- COM2 (serial port) (9 pin D-sub)
- video (15 pin high density D-sub)

Refer to Figure 2-3 for rear panel connectors on the CPN5360 Transition Module.

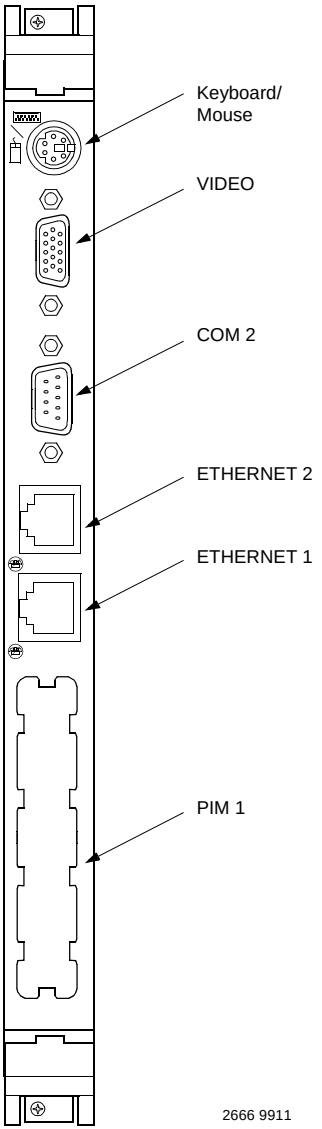


Figure 2-3. Rear Panel Connectors on the CPN5360 Transition Module

Components on the CPN5360

3

Components on the CPN5360 Single Board Computer

The CPN5360 Single Board Computer (SBC) carries components on both sides. Figure 3-1 shows the location of the on-board connectors. There are no on-board jumpers.

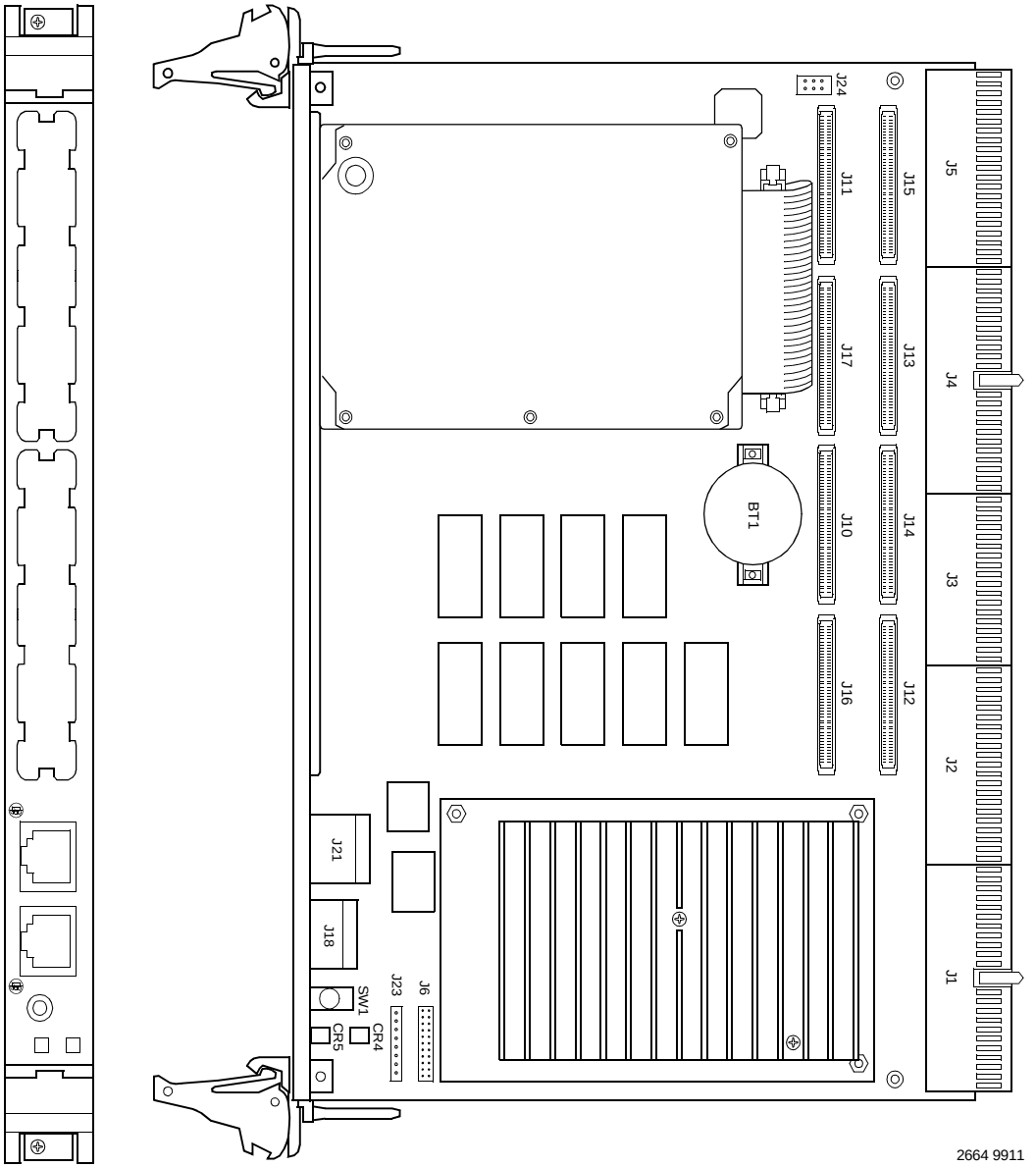


Figure 3-1. Location of Major Components on the CPN5360 Single Board Computer

Table 3-1 lists the connectors available to support devices on the CPN5360. Refer to Figure 3-1. Refer to Chapter 5 for connector pin assignment.

Table 3-1. List of Front Panel Connectors, Board Connectors and Components for the CPN5360 Single Board Computer

Connector	Description
J1	CompactPCI Bus Connector
J2	CompactPCI Bus Connector
J3	Rear I/O CompactPCI Connector
J4	Rear I/O CompactPCI Connector
J5	Rear I/O CompactPCI Connector
J6	Debug Port
J10	PMC2 bus signal connector
J11	PMC1 bus signal connector
J12	PMC2 I/O connector
J13	PMC1 I/O connector
J14	PMC2 bus signal connector
J15	PMC1 bus signal connector
J16	PCI 64 bit PCI extension on PMC2 connector
J17	PCI 64 bit PCI extension on PMC1 connector
J18	COM1 (serial port - RJ45 connector)
J21	Ethernet connector (RJ-45)

Components on the CPN5360TM80 Transition Module

Figure 3-2 shows major components on the CPN5360TM80 Transition Module.

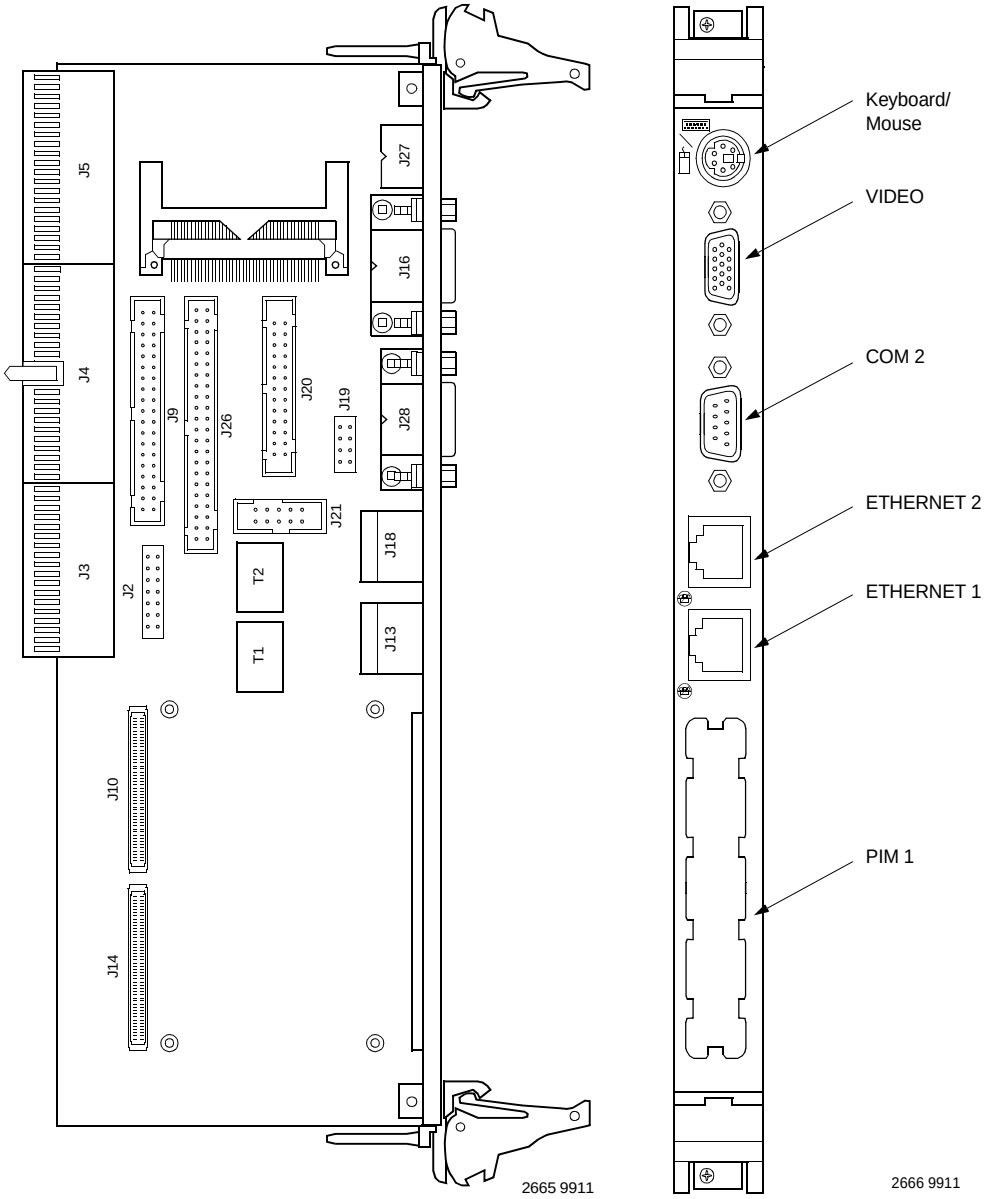


Figure 3-2. Major Components on the CPN5360TM80 Transition Module

Table 3-2 lists the connectors available to support devices on the CPN5360TM80 Transition Module. Refer to Figure 3-2. Refer to Chapter 5 for connector pin assignment.

Table 3-2. List of Front Panel Connectors, Board Connectors and Components for the CPN5360TM80 Transition Module

Connector	Description
J2	Drive LED's, Reset
J3	Rear I/O CompactPCI Connector
J4	Rear I/O CompactPCI Connector
J5	Rear I/O CompactPCI Connector
J6	Keyboard/Mouse (internal)
J9	Floppy
J10	PIM connector (PMC I/O)
J13	Ethernet 1
J14	PIM connector (PMC I/O)
J15	PIM connector (PMC I/O)
J16	Video
J18	Ethernet 2
J19	USB connector
J20	Parallel connector
J21	COM1 (serial port 1)
J26	IDE (secondary)
J27	Keyboard/Mouse (external)
J28	COM2 (serial port 2)

Connecting to Board Connectors

The CPN5360 Single Board Computer (SBC) and CPN5360TM80 Transition Module (TM) give you board connectors for attaching peripheral devices. Before installing the CPN5360 SBC or TM, you may want to connect your peripheral cables to the connectors. Refer to Chapter 5, *Connector Pin Assignments* for pin assignment information.

Note When the identical function is available through the CPN5360 SBC (front panel) and TM (rear panel), you can use either the front or the rear, not both.



Warning Always remove power from the system before connecting peripherals to the CPN5360 SBC or TM. To reduce the risk of personal injury, disconnect the power cord from the power source. Only qualified, experienced electronics personnel should access the interior of a chassis.



Caution The components of the CPN5360 SBC and TM are sensitive to static discharge. While out of the unit, place the modules on a static-dissipative surface or into a static-shielding bag.

CPU Speed Settings

You cannot configure the CPU speed settings.

Functional Description 4

Introduction

This chapter gives you information about:

- the Peripheral Component Interconnect (PCI) Bus
- host and non-host slot mounting
- the watchdog timer
- memory address mapping
- the I/O address map
- Field Programmable Gate Array (FPGA) registers

The CPN5360 BIOS is similar to the CPV5350 BIOS. Refer to *Related Documentation*, Table C-1 for information about how to access the "CPV5350 CompactPCI BIOS and Programmer's Reference Guide" (Motorola part number CPV5350A/PGx). Refer to *Jump to User Code in Alternate Flash Bank* on page 4-32 and *DEC21554 PCI-to-PCI Bridge Configuration* on page 4-32 for more information about the CPN5360 BIOS.

PhoenixBIOS Description

The CPN5360 uses the PhoenixBIOS to provide initial hardware configuration for local devices and local operating system boot.

Soft Reset

You can generate a "soft reset" from your keyboard, the watchdog timer, or the front panel push button in Soft Reset Mode. The BIOS preserves as much of the system memory state as possible.

A CPN5360 circuit monitors system power and provides the PWROK signal to the PIIX4E. The PIIX4E distributes the reset to the rest of the board by generating the CPU, PCI, and IDE resets. You can also reset the board using the front panel reset switch and the FPGA watchdog timer. You can program the Watchdog Timer and the front panel push button switch to generate a soft reset. Refer to *Field Programmable Gate Array Registers* on page 4-12 for programming information.

Headless Operation

The BIOS can operate with no keyboard or display. You do, however, need a keyboard and display to change setup options unless you use the remote setup feature.

Remote Setup

You can change setup options remotely through the BIOS Setup - Advanced Menu using the RJ45, COM1 port on the front panel of the CPN5360 Single Board Computer. The default settings for a serial console are 9600 baud, 1 stop bit, no parity, and no flow control.

Network Boot

We include the Intel PXE (Pre-boot Execution Environment) 82559 BIOS extension module to provide operating system boot via one of the 82559 ports. This module is built into the BIOS. You can enable the PXE for either port through the BIOS Setup-Advanced-PCI Configuration Menu.

Peripheral Component Interconnect (PCI) Local Bus Interface

The PCI local bus is a high-performance, 32-bit bus with multiplexed address and data lines. Use it as an interconnect mechanism between highly-integrated peripheral controller components, peripheral add-in boards and processor/memory systems.

The CPN5360 supports a 32-bit local PCI bus interface. On-board devices connect directly to the local PCI bus.

PCI Mezzanine Card Limitations

The CPN5360 Single Board Computer drives the Peripheral Component Interconnect (PCI) Mezzanine Card's (PMC) PCI Bus to 3.3V logic levels.



Caution

Driving the PCI bus to 5V logic levels could damage the PCI devices on the CPN5360.

PMCs used on the CPN5360 must support 3.3V or universal voltage PCI signaling. The CPN5360 is keyed to prevent installation of 5V PMCs.

CompactPCI Bus Interface

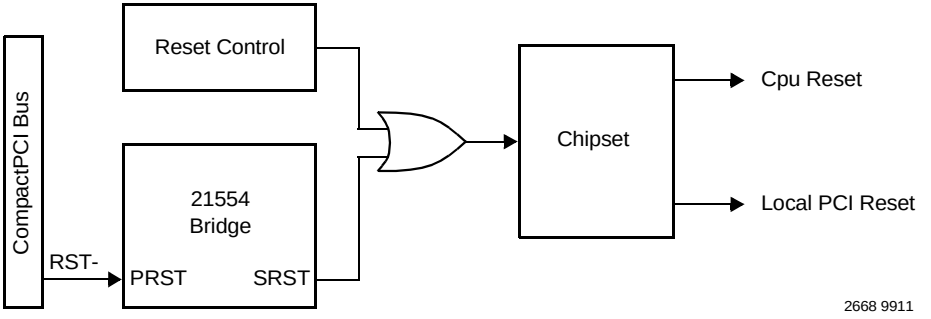
The CPN5360 supports a single 64-bit CompactPCI bus interface. You can insert the physical connector into a 64-bit High Availability CompactPCI backplane and make connection to off card CompactPCI peripherals through the PCI-PCI bridge.

Using the CPN5360 in a Non-Host Slot

The CPN5360 is intended for mounting in a non-host slot as a peripheral CPU. The module configures itself for peripheral mode when it plugs into a peripheral slot. The CompactPCI interface device is a non-transparent bridge (21554). The local CPU enumerates the local devices and sets up the bridge for configuration by the host CPU. The peripheral CPU can also configure itself onto the Compact PCI bus using a scheme allowing it to map itself to a particular area using the geographical addressing CPCI lines.You can read these lines through the FPGA. Refer to the FPGA register description for information about reading these bits.

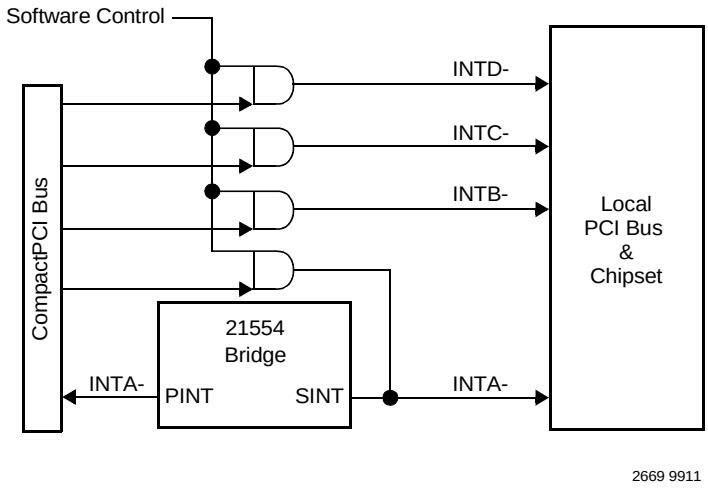
Peripheral Reset Function

In peripheral mode the PCI reset signal comes from the CompactPCI bus through the bridge to reset all on-card functions. You can reset the card independently without affecting other cards in the system.



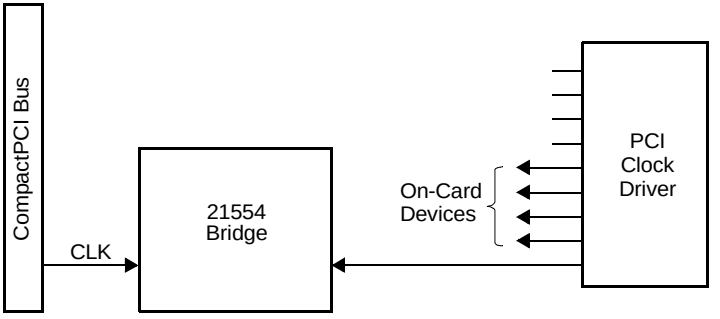
Peripheral PCI Interrupt Function

In peripheral mode the PCI interrupts route as shown below. The 21554 bridges primary interface can generate a system interrupt via the INTA- line on the CompactPCI bus. Local and host CPUs can generate an interrupt to the other CPU via the 21554's primary and secondary doorbell interrupts.



Peripheral PCI Clock Function

In peripheral mode the 21554's primary interface connects to the CompactPCI CLK (clock) signal. The secondary interface connects to an on-card PCI clock. In this configuration the bridge operates in asynchronous clocking mode.



Peripheral Hot Swap Function

The CPN5360 complies with the CompactPCI Hot Swap Specification in peripheral mode. You must, however, use a compliant backplane with proper pin staging.

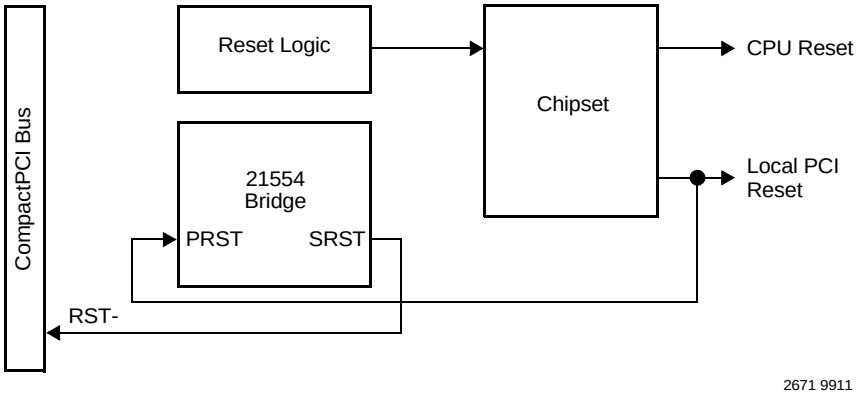
Using the CPN5360 in a Host Slot

The CPN5360 automatically provides host hardware functions (clocks and REQ/GNT arbitration) when plugged into the host slot. Bus configuration, however, is non-standard. This means you need special software drivers. Also, the BIOS does not support configuration past the bridge. You can read the SYSEN- CPCI line indicating the host mode through the FPGA. Refer to the FPGA register descriptions for information about how to read this bit.

Note The CPN5360 is designed mainly for use as a peripheral. The system may need additional CompactPCI bus termination and special software drivers if it is used as a host.

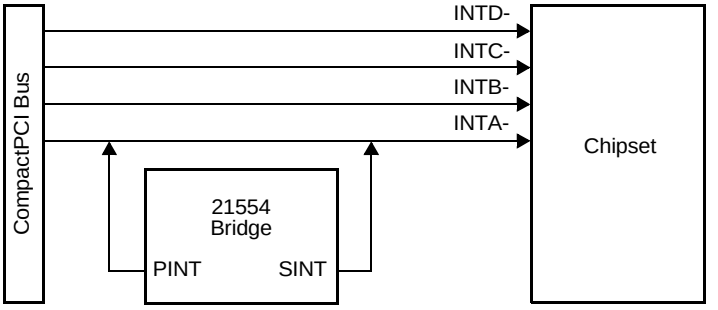
Host Reset Function

In host mode the on-board reset logic generates the reset. The PCI reset signal routes through the PCI bridge to the CompactPCI bus to reset the system.



Host PCI Interrupt Function

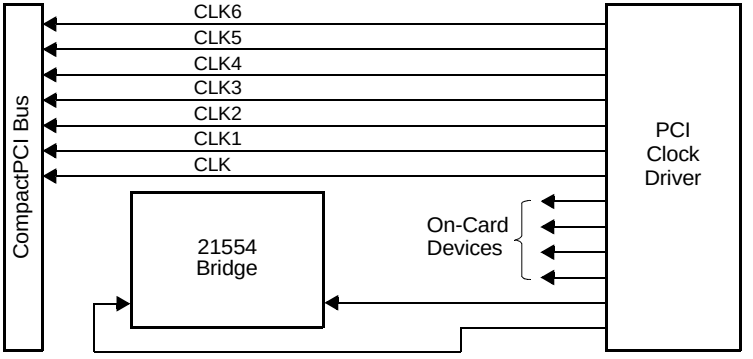
In host mode the PCI interrupts route as shown below. The on-card PCI interrupts connect to the CompactPCI bus in the standard way.



2672 9911

Host PCI Clock Function

In host mode all seven CompactPCI clock signals provide clocking for all peripheral slots.



2673 9911

Host Hot Swap Function

Host mode does not support the Hot Swap function. Bus arbitration and clock signals are lost if the board is removed. You can, however, remove the board under power without damage from a Hot Swap compliant backplane slot with proper pin staging.

Watchdog Timer

The Field Programmable Gate Array (FPGA) includes a watchdog timer. The watchdog timer has four modes of operation:

1. disabled
2. sets the timeout flag in the Watchdog Strobe/Status port in ISA I/O memory map
3. item 2 + assert a selectable interrupt (ISA IRQ)
4. item 2 + assert NMI followed by a system reset or soft reset

You can program the watchdog timer via registers in the ISA I/O memory map. The watchdog timer is protected from being accidentally enabled and can support a range of count down time-outs up to eight minutes.

Memory Address Mapping

Refer to Table 4-1 for memory address information.

Table 4-1. Memory Addresses and Descriptions

Address	Size	Description
FFF80000 - FFFFFFFF	512K	512K BIOS PROM Area
FEE01000 - FFF8FFFF	18M-128K-4K	18M-128K-4K PCI
FEE00000 - FEE00FFF	4K	Local APIC Configuration Space
40000000 - FEDFFFFF	3G-18M	PCI
00100000 - 3FFFFFFF	1023M	Extended Memory

Table 4-1. Memory Addresses and Descriptions (Continued)

Address	Size	Description
000F0000 - 000FFFFF	64K	System BIOS Area
000E0000 - 000EFFFF	64K	Extended System BIOS Area
000C0000 - 000DFFFF	128K	BIOS Option Expansion Area
000A0000 - 000BFFFF	128K	Video Buffer Area
00000000 - 0009FFFF	640K	DOS Application Area

I/O Address Map

Table 4-2 shows I/O addressing. You can use BIOS Setup or special utilities to enable or relocate these features from their default values.

Table 4-2. I/O Addresses and Descriptions

Address (hex)	Size	Description
0000 - 000F	16 bytes	PIIX4E DMA, channels 0 - 3
0020 - 0021	2 bytes	PIIX4E Interrupt Controller 1
0040 - 0043	4 bytes	PIIX4E - Timer 1
0050 - 0057 [1]	8 bytes	LM78 Hardware Monitor
0058 - 005F [2]	8 bytes	FPGA Functions (Watchdog Timer, ENUM)
0060	1 byte	Keyboard Controller
0061	1 byte	PIIX4E - NMI, Speaker Control
0064	1 byte	Keyboard Controller
0070 - 7	1 bit	PIIX4E NMI Enable
0070-6:0	7 bits	PIIX4E RTC
0071	1 byte	PIIX4E RTC
0072-0073	2 bytes	PIIX4E RTC (extended registers)
0080 - 008F	16 bytes	PIIX4E DMA Page Register
0092	1 byte	PIIX4E Port 92 Register
00A0 - 00A1	2 bytes	PIIX4E Interrupt Controller 2
00B2 - 00B3	2 bytes	APM reserved

Table 4-2. I/O Addresses and Descriptions (Continued)

Address (hex)	Size	Description
00C0 - 00DE	31 bytes	PIIX4E DMA, channels 4 - 7
00EA	1 byte	Ultra I/O General Purpose I/O Index Register
00EB	1 byte	Ultra I/O General Purpose I/O Data Register
00F0	1 byte	Reset Numeric Error
0170 - 0177	8 bytes	Secondary IDE Channel
01F0 - 01F7	8 bytes	Primary IDE Channel
02F8 - 02FF	8 bytes	COM2
0376	1 byte	Secondary IDE Channel Command Port
0377	1 byte	Secondary IDE Channel Status Port
0378 - 037F	8 bytes	LPT1
03F0 [3]	1 byte	Ultra I/O Configuration Index Register
03F1 [3]	1 byte	Ultra I/O Configuration Data Register
03F0 - 03F5	6 bytes	Floppy
03F6	1 byte	Primary IDE Channel Command Port
03F7-7	1 bit	Floppy Disk Change Channel 1
03F7-6:0	7 bits	Primary IDE Channel Status Port
03F7 (write)	1 byte	Floppy Channel 1 Command
03F8 - 03FF	8 bytes	COM 1
04D0 - 04D1	2 bytes	Interrupt Controller Edge/Level Register
0CF8 - 0CFB	4 bytes	PCI CONFADD (DWORD Access Only)
0CFC - 0CFF	4 bytes	PCI CONFDATA
0CF9	1 byte	PIIX4E Reset Control Register
FF00 - FF07	8 bytes	IDE Bus Master Register

Table 4-2. I/O Addresses and Descriptions (Continued)

Address (hex)	Size	Description
FFA0 - FFA7	8 bytes	Primary Bus Master IDE Registers
FFA8 - FFAF	8 bytes	Secondary Bus Master IDE Registers
FF80 - FF9F	32 bytes	USB

[1] This address range is selected by Programmable Chip Select 1 (PCS0-) on the PIIX4E and is reprogrammable. PCS0- is initially set by the BIOS.

[2] This address range is selected by Programmable Chip Select 2 (PCS1-) on the PIIX4E and is reprogrammable. PCS1- is initially set by the BIOS.

[3] These registers are shared with the Floppy registers. Refer to the Ultra I/O data sheet via “Related Documentation” at the end of this manual.

Field Programmable Gate Array Registers

The Field Programmable Gate Array (FPGA) is used for add-on features and control, and connects to the internal ISA bus. It consists of a group of I/O registers for control of features such as a Watchdog Timer, I/O switching control, NVRAM control and decoding, and system management functions.

When a system management event occurs, the input causing the event latches and remains latched until cleared by the system software. The system management hardware notifies the system of the event depending on the mode selected by the user. Refer to Table 4-3.

Table 4-3. System Management Modes

In:	an:
Alarm Mode	alarm generates - You can connect the signal to external alarm hardware. The front panel alarm status indicator also illuminates when an event occurs and alarm mode is selected.
IRQ Mode	ISA interrupt generates - You can set the interrupt by writing to the IRQ select register.
SCI Mode	SCI generates - The FPGA's SCI output connects to the PIIX4 Therm input GPI8.
NMI Mode	NMI generates

FPGA Register Descriptions

This section describes how to access the various FPGA register sets. The bit description tables below show bits 0 through 7 on the top line and bit functions on the second line.

You can access the FPGA registers by an index register at offset 05h from the base address of the FPGA (0x5Dh). The data register is located at offset 07h (0x5Fh). Refer to Table 4-4. To access an FPGA register, write to the index register first and then read/write from the data register. The BIOS sets the default FPGA Base address to 58h.

Table 4-4. Index and data register address and function

Port	Offset address	Function
Index	05h	Register Index Port - selects the device register
Data	07h	Data Port - read/write data to selected register
Watchdog Strobe/Status	03h	Watchdog Strobe and Status register

Refer to Table 4-5 for a map of the FPGA register set.

Table 4-5. Map of the FPGA register set

DEVICE 00h SYSTEM	DEVICE 10h LAN A Ctrl	DEVICE 11h LAN B Ctrl	DEVICE 14h FLASH Ctrl	DEVICE 15h SLOT Ctrl Port
00 Status				
	01 LAN A	01 LAN B	01 FLASH	01 SLOT Ctrl
02 EEPROM				
03 Watchdog				
04 INT Sel				
05 SCI Mask				
06 NMI Mask				
07 IRQ Mask				
08 Alm Mask				
09 FLT Latch				
0B Power On				
0F DEV SEL	0F DEV SEL	0F DEV SEL	0F DEV SEL	0F DEV SEL

Status Register

The Status Register (STAT) is a read only register. Reads of the unused bits produce indeterminate values. Writes have no effect. The Temp Alarm, Fan Alarm, Alarm B, and Alarm A are all latched when active. You must initiate a write to index register 09 (Fault Latch) to clear the latched signals. Refer to Table 4-6.

Table 4-6. Bit descriptions for the STAT register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ALARM	FAL-	DEG-	ENUM-	LM78 ALARM A	LM78 ALARM B	SMB ALERT	MMC2 TEMP ALARM

MMC2 TEMP ALARM (Bit 0)

This signal connects to the MMC2's thermal sensor alarm output (ATF). You can program it to trip at a specific temperature. The input is latched when active (low). You can clear this bit (0) via Index register 09h. A read of these bits returns the latched status of the input.

SMB ALERT (Bit 1)

This bit reflects the level of the SMBus Alert signal.

LM78 ALARM A (Bit 3) and LM78 ALARM B (Bit 2)

The LM78 output functions feed these signals. The input is latched when active. You can clear these bits (3 and 2) via Index register 09h.

ENUM (Bit 4)

ENUM comes from the CPCI bus and signals the insertion of a new device. The input is latched when active (low). You can clear this bit (4) via Index register 09h. A read of this bit returns the latched status of the input.

DEG (Bit 5)

DEG comes from the CPCI bus and signals a power condition. The backplane may or may not support this ATX type signal.

FAL (Bit 6)

This signal comes from the CPCI bus and signals a power condition. The backplane may or may not support this ATX type signal.

ALARM (Bit 7)

This signal comes from device 0 Index Register 08h Alarm Enable.

EEPROM Control Register

The EEPROM Control Register (ECTRL) lets you access the external serial configuration EEPROM. Refer to Table 4-7.

Table 4-7. Bit descriptions for the ECTRL register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
Unused	Unused	Unused	EEPRG Enbl	EERST	EEEN	EECLK	EEDTA

Bits 0 through 4 are reserved for programming the FPGA's on card serial EEPROM.

Watchdog Timer Register

Refer to Table 4-8 for Watchdog Timer Register bit descriptions.

Table 4-8. Bit descriptions for the Watchdog Timer register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
CLR_STATUS	ALARM_SET	SOFT_RST	WD1	WD0	SEL2	SEL1	SEL0

SEL0 (Bit 0), SEL1 (Bit 1) and SEL2 (Bit 2)

Use SEL0, SEL1 and SEL2 to select the watchdog timeout time. Writing to these bits does not clear or reset the watchdog timer. Refer to Table 4-9.

Table 4-9. Bit values for selecting watchdog timeout time

Period	SEL2	SEL1	SEL0
.46 seconds	0	0	0
.93 seconds	0	0	1
3.73seconds	0	1	0
14.91seconds	0	1	1
29.8 seconds	1	0	0
119 seconds, (1.99 minutes)	1	0	1
238 seconds, (3.97 minutes)	1	1	0
477 seconds, (7.95 minutes)	1	1	1

WD0 (Bit 3) and WD1 (Bit 4)

Use these bits to define the event that occurs on a watchdog timeout and to disable the watchdog timer. Reading these bits returns the last value written. Refer to Table 4-10.

Table 4-10. Bit values defining watchdog timeout and disabling

Name	WD1	WD0	Description
DISABLED	0	0	Resets watchdog. This mode disables the watchdog timer. No watchdog events occur.
POLLED	0	1	This mode sets the watchdog into polled mode. The Watchdog Strobe/Status port bit 2 polls for a watchdog event.
FPGA IRQX	1	0	This mode generates an IRQ on a watchdog timeout. Refer to the Interrupt select register for programming the particular interrupt.
NMI followed by Reset or Soft Reset	1	1	This mode first generates an NMI interrupt and then a reset or soft reset.

SOFT_RST (Bit 5)

Use this bit to change the Watchdog Reset function to Soft reset. Refer to Table 4-11. This bit clears on power-up reset.

Table 4-11. SOFT_RST bit 5 settings

Set bit to:	For:
0 (default)	hard reset
1	soft reset

ALARM_SET (Bit 6)

Use this bit to force the FPGA Alarm to go active.

- Write a logic 1 to force an FPGA Alarm.
- Write a logic 0 to return the FPGA Alarm to its previous state (active if watchdog or EXT_ALARM are active).
- Read this bit to return the last written value.

CLR_STATUS (Bit 7)

Use this bit to reset and enable the watchdog timer FPGA ALARM output latch.

- Write a logic 1 to hold the watchdog timer FPGA ALARM output latch in a reset state.
- Write a logic 0 to allow the watchdog timer FPGA ALARM output latch to latch a watchdog timeout.

Strobe the watchdog timer before enabling the latch to make sure that a watchdog timeout did not occur before the latch enabled.

Reading this bit returns the last written value.

Interrupt Select Register

Use the Interrupt Select Register to select the desired IRQ line. Refer to Table 4-12. This IRQ can then be generated by a watchdog Timeout or ENUM-.

Table 4-12. Bit descriptions for the INTUM register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
Unused	Unused	Unused	Unused	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0

IRQSEL0 (Bit 0), IRQSEL1 (Bit 1), IRQSEL2 (Bit 2) and IRQSEL3 (Bit 3)

These bits determine which IRQ is driven when an IRQ even triggers. Refer to Table 4-13.

Table 4-13. Bit values for determining driven IRQ lines

Interrupt Line	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0
No IRQ Selected	0	0	0	0
No IRQ Selected	0	0	0	1
No IRQ Selected	0	0	1	0
No IRQ Selected	0	0	1	1
No IRQ Selected	0	1	0	0
Select IRQ5	0	1	0	1
No IRQ Selected	0	1	1	0
Select IRQ7	0	1	1	1
No IRQ Selected	1	0	0	0
Select IRQ9	1	0	0	1
Select IRQ10	1	0	1	0
Select IRQ11	1	0	1	1
No IRQ Selected	1	1	0	0
No IRQ Selected	1	1	0	1
No IRQ Selected	1	1	1	0
No IRQ Selected	1	1	1	1

SCI Enable Register

The SCI Enable Register (SCIEN) defines the type of events that can generate an SCI. Refer to Table 4-14.

Table 4-14. Bit descriptions for the SCIEN register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENABLE	Unused	Unused	ENUM-	ALARM_A-	ALARM_B-	TEMP-	SMB_ALERT-

SMB_ALERT (Bit 0)

- Set to a logic 1 to allow generation of an SCI when SMB ALERT is active. SMB ALERT is active when logic 0.
- Write a logic 0 to this bit to disable an SCI for this event.

TEMP (Bit 1)

- Set to a logic 1 to allow generation of an SCI when TEMP is active. TEMP is the ATF signal from the MMC2 and is active when logic 0.
- Write a logic 0 to this bit to disable an SCI for this event.

ALARM_A (Bit 3) and ALARM_B (Bit 2)

- Set to a logic 1 to allow the generation of an SCI when the ALARM_A or ALARM_B go active. Alarm is active when logic 0.
- Write a logic 0 to these bits to disable an SCI for this event.

ENUM (Bit 4)

- Set to a logic 1 to allow generation of an SCI when the ENUM event occurs.
- Write a logic 0 to this bit to disable an SCI for this event.

ENABLE

- Set to a logic 1 to allow generation of an SCI by one of the events above.
- Write a logic 0 to prevent the events from generating an SCI.

NMI Enable Register

The NMI Enable Register (NMIEN) defines the events that can generate an NMI. Refer to Table 4-15.

Table 4-15. Bit descriptions for the NMIEN register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENABLE	Unused	Unused	ENUM	ALARM_A	ALARM_B	TEMP	SMB_ ALERT

SMB_ALERT (Bit 0)

- Set to a logic 1 to allow the generation of an NMI when the SMB Alert is active. SMB Alert is active when logic 0.
- Write a logic 0 to this bit to disable an NMI for this event.

TEMP (Bit 1)

- Set to a logic 1 to allow the generation of an NMI when TEMP is active. TEMP is active when logic 0.
- Write a logic 0 to this bit to disable an NMI for this event.

ALARM_A (Bit 3) and ALARM_B (Bit 2)

- Set to a logic 1 to allow the generation of an NMI when the ALARM_A or ALARM_B go active. ALARM is active when logic 0.
- Write a logic 0 to this bit to disable an NMI for this event.

ENUM (Bit 4)

- Set to a logic 1 to allow the generation of an NMI when the ENUM event occurs.
- Write a logic 0 to this bit to disable an NMI for this event.

ENABLE (Bit 7)

- Set to a logic 1 to allow the listed events to generate an NMI.
- Write a logic 0 to prevent the events from generating an NMI.

IRQ Enable Register

The IRQ Enable Register (IRQEN) defines the events that can generate an IRQ. The IRQ generated is set by IRQ Select Register index04. Refer to Table 4-16.

Table 4-16. Bit descriptions for the IRQEN register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENABLE	Unused	Unused	ENUM	ALARM_A	ALARM_B	TEMP	SMB_ ALERT

SMB_ALERT (Bit 0)

- Set to a logic 1 to allow the generation of an IRQ when the SMB Alert is active. SMB Alert is active when logic 0.
- Write a logic 0 to this bit to disable an IRQ for this event.

TEMP (Bit 1)

- Set to a logic 1 to allow the generation of an IRQ when TEMP is active. TEMP is active when logic 0.
- Write a logic 0 to this bit to disable an IRQ for this event.

ALARM_A (Bit 3) and ALARM_B (Bit 2)

- Set to a logic 1 to allow the generation of an IRQ when the ALARM_A or ALARM_B go active. Alarm is active when logic 0.
- Write a logic 0 to this bit to disable an IRQ for this event.

ENUM (Bit 4)

- Set to a logic 1 to allow the generation of an IRQ when the ENUM event occurs.
- Write a logic 0 to this bit to disable an IRQ for this event.

ENABLE (Bit 7)

- Set to a logic 1 to allow the listed events to generate an IRQ.
- Write a logic 0 to prevent the events from generating an IRQ.

Alarm Enable Register

The Alarm Enable Register (ALEN) defines the events that generate an alarm output. Refer to Table 4-17.

Table 4-17. Bit descriptions for the ALEN register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENABLE	Unused	Unused	ENUM	ALARM_A	ALARM_B	TEMP	SMB_ ALERT

SMB ALERT (Bit 0)

- Set to a logic 1 to allow the generation of an Alarm when the SMB Alert is active. SMB Alert is active when logic 0.
- Write a logic 0 to this bit to disable an Alarm for this event

TEMP (Bit 1)

- Set to a logic 1 to allow the generation of an Alarm when TEMP is active. TEMP is active when logic 0.
- Write a logic 0 to this bit to disable an Alarm for this event.

ALARM_A (Bit 3) and ALARM_B (Bit 2)

- Set to a logic 1 to allow the generation of an Alarm when the ALARM_A or ALARM_B go active. ALARM is active when logic 0.
- Write a logic 0 to this bit to disable an Alarm for this event.

ENUM (Bit 4)

- Set to a logic 1 to allow the generation of an Alarm when the ENUM event occurs.
- Write a logic 0 to this bit to disable an Alarm for this event.

ENABLE (Bit 7)

- Set to a logic 1 to allow the listed events to generate an Alarm.
- Write a logic 0 to prevent the events from generating an Alarm.

Latch Enable Register

The Latch Enable Register (LEN) resets latches in the Field Programmable Gate Array (FPGA) for the SMB_ALERT, TEMP, ALARM_B and ALARM_B alarms. Refer to Table 4-18. This register is write only. Write a logic 1 to clear the latch. Writing a logic 0 has no effect on the latch.

Table 4-18. Bit descriptions for the LEN register

7 (most significant bit)	6	5	4	3	2	1	0
Unused	Unused	Unused	ENUM	ALARM_A	ALARM_B	TEMP	SMB_ ALERT

SMB Alert (Bit 0) - SMB Alert Signal

- Write a logic 1 to clear the SMB_ALERT input latch
- Writing a logic 0 has no effect

TEMP (Bit 1) - CPU Temperature Signal

- Write a logic 1 to clear the TEMP input latch
- Writing a logic 0 has no effect

ALARM_B (Bit 2) - LM78 Alarm B Signal

- Write a logic 1 to clear the ALARM_B input latch
- Writing a logic 0 has no effect

ALARM_A (Bit 3) - LM78 Alarm A Signal

- Write a logic 1 to clear the ALARM_A input latch
- Writing a logic 0 has no effect

ENUM (Bit 4) - Bus Enumeration Signal

- Write a logic 1 to clear the ENUM input latch
- Writing a logic 0 has no effect

Power-On Flag Register

The Power-On Flag Register checks for power-on condition. You can also read back written bits. Refer to Table 4-19.

Table 4-19. Bit descriptions for the Power-On Flag register

7 (most significant bit)	6	5	4	3	2	1	0
PBSOFT	Unused	Unused	Unused	FLAG1	FLAG0	PWRON1	PWRON0

PWRON0 (Bit 0) and PWRON1 (Bit 1)

The BIOS uses this bit to determine if it is booting from a power-up. After BIOS POST this bit reads as a 1. It clears at power-on only. The BIOS may set it to flag subsequent resets.

FLAG0 (Bit 2) and FLAG1 (Bit 3)

Applications use these bits to flag boot states to the BIOS on the next reset. These bits clear at power-on and are not affected by reset.

PBSOFT (Bit 7)

Use this bit to program the function of the reset pushbutton switch. By default the front panel pushbutton switch causes a hard reset. Set this bit to a 1 to cause a soft reset. Clear the bit to 0 to program the switch to cause a hard reset. The default state is 0.

LAN A Control Register

Use this register to control Ethernet LAN A. Bits written can also read back. Refer to Table 4-20.

Table 4-20. Bit descriptions for the LAN A register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
LAN A ENABLE	LAN A REAR	Unused	Unused	Unused	Unused	Unused	Unused

LAN A REAR (Bit 6)

The BIOS uses this bit to route LAN A signals to either the front or the rear connectors.

- Write a logic 0 to this bit to route LAN A signals to the front connector.
- Write a logic 1 to this bit to route LAN A signals to the rear connector.

The BIOS sets this bit according to setup settings.

LAN A ENABLE (Bit 7)

The BIOS uses this bit to enable LAN A.

- Write a logic 1 to this bit to enable LAN A.
- Write a logic 0 to this bit to disable LAN A.

The BIOS sets this bit according to setup settings.

LAN B Control Register

Use this register to control Ethernet LAN B. Bits written can also read back. Refer to Table 4-21.

Table 4-21. Bit descriptions for the LAN B register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
LAN B ENABLE	Unused	Unused	Unused	Unused	Unused	Unused	Unused

LAN B ENABLE (Bit 7)

The BIOS uses this bit to enable LAN B.

- Write a logic 1 to this bit to enable LAN B.
- Write a logic 0 to this bit to disable LAN B.

The BIOS sets this bit according to setup settings.

Flash BIOS Write Protect Control Register

Use this register to control the write protect line on the BIOS Flash memory. Bits written can also read back. Refer to Table 4-22.

Table 4-22. Bit descriptions for the Flash BIOS Write Protect Control register

7 (most significant bit)	6	5	4	3	2	1	0
WP-	Unused	Unused	Unused	Unused	BC2	BC1	BC0

BC0 (Bit 0), BC1 (Bit 1) and BC2 (Bit 2)

Use the Bank Control bits to control the Flash BIOS device. Reset selects Bank 0 as the default. Refer to Table 4-23 for Bank Control bit settings.

Table 4-23. Bit selections for the Flash BIOS Device Bank Control

512K BANK	Flash Offset	Window	BC2	BC1	BC0
Bank 0*	000000h	FFF80000h	0	0	0
Bank 1	080000h	FFF80000h	0	0	1
Bank 2	100000h	FFF80000h	0	1	0
Bank 3	180000h	FFF80000h	0	1	1
Bank 4	200000h	FFF80000h	1	0	0
Bank 5	280000h	FFF80000h	1	0	1
Bank 6	300000h	FFF80000h	1	1	0
Bank 7	380000h	FFF80000h	1	1	1
*Default Reset state					

WP (Bit 7)

Use this bit to enable the Flash BIOS for updating.

- Write a logic 1 to open the BIOS for writing

- Write a logic 0 to write protect the BIOS

Slot Control Port Register

Use this register to read the CompactPCI Slot address signals GA0, GA1, GA2, GA3, and GA4. Refer to Table 4-24.

Table 4-24. Bit descriptions for the Slot Control Port register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
SYSEN	TMPRSNT	INTIN	GA4	GA3	GA2	GA1	GA0

GA0 (Bit 0), GA1 (Bit 1), GA2 (Bit 2), GA3 (Bit 3), GA4 (Bit 4)

These bits are the CompactPCI Geographic Addressing Signals. These five signals identify the current slot location of the card. The value of these five bits read 0 to 31 and correspond to 32 possible slot positions in the system.

INTIN (Bit 5)

Use this bit to enable CompactPCI interrupts to the card.

- Write a logic 0 to this bit to disconnect CompactPCI interrupts.
- Write a logic 1 to this bit to enable all four CompactPCI interrupts.

TMPRSNT (Bit 6)

This bit indicates if a Transition Module is installed.

- A logic 0 indicates no Transition Module is installed.
- A logic 1 indicates a Transition Module is installed.

SYSEN (Bit 7)

This bit reflects the SYSEN (System Enable) pin from the CPCI bus.

- A logic 0 indicates the card is plugged into the system slot.

- A logic 1 indicates the card is plugged into a peripheral slot and is running in peripheral mode.

Jump to User Code in Alternate Flash Bank

The flash device for the BIOS is a 4MB part consisting of eight 512K banks. The BIOS occupies bank 0 only.

From the boot screen in the BIOS setup, you can select an alternate 512K flash bank to load and execute instead of booting from standard devices in the boot menu. If you select one of the alternate banks (banks 1 - 7), the BIOS looks for the five character signature "_MOT_" in the last five bytes of the selected 512K bank. If found, the BIOS disables interrupts, timers, and the watchdog. Then it reads the top 64K of the selected bank into segment 0F000h and jumps to 0F000:FFF0h. If the signature is not found, the BIOS proceeds normally and attempts to boot from standard floppy and hard drive devices.

Note When the bank switch and jump occurs, it happens very late in the Power-On Self Test (POST) after all hardware initializes.

DEC21554 PCI-to-PCI Bridge Configuration

From the Advanced, PCI screen, you can enter a configuration screen for the DEC21554 non-transparent PCI-to-PCI bridge. This screen contains five setup options.

1. Select "Advanced" from the menu bar on the Main Menu to display the Advanced menu.
2. Select "PCI Configuration" on the "Advanced" menu.
3. Select "DEC21554 PCI-to-PCI Bridge Setup" on the "PCI Configuration" menu.

Setup Option Number 1 - “BIOS Setup of DEC21554 Bridge”

This setup option enables at default. When enabled, the BIOS:

- configures the DEC21554’s command register, two upstream and two downstream pre-fetchable memory windows
- disables the DEC21554’s primary lockout.

Note We do not recommend selecting “Disabled”. If disabled, the BIOS does not alter the command register, re-size the upstream and downstream windows, or disable the primary lockout. It leaves the DEC21554’s settings at default or pre-loaded SROM values.

You can see this recommendation in the setting information displayed on the right side of the BIOS setup screen.

If the DEC21554’s primary lockout is left enabled, PCI configuration accesses to the DEC21554 from the primary bus result in approximately a two second target retry timeout for each attempted access. On power up or reset, a host processor may continue to attempt to access the DEC21554 and tie up the system for several minutes.

Setup Options 2, 3, 4, and 5

Setup options 2, 3, 4, and 5 on the DEC21554 configuration screen display only when BIOS setup of the bridge enables. These questions let you modify the pre-fetchable PCI memory window sizes of the two upstream and two downstream windows configured by the BIOS.

Sample Code for Accessing a Field Programmable Gate Array

Table 4-25 gives you a sample code example for accessing a field programmable gate array (FPGA) register within a device. This example shows how to modify the IRQ Mask register (device 0, index register 7).

Table 4-25. Sample Code for Accessing a Field Programmable Gate Array

Step	Instruction	Instruction Values		Description
1	mov out IODELAY	al 05Dh	0fh al	 ;select the FPGA devselect register
2	mov out IODELAY	al 05Fh	00h al	;device 00 ;select the System FPGA Device
3	mov out IODELAY	al 05Dh	07h al	;index 7, IRQ mask register ;IRQ mask register (DEV 0h)
4	mov out IODELAY	al 05Fh	??h al	;??=data to write to register

These steps describe the sample code in Table 4-25. The code:

1. writes a byte value of 15 (0xF hex) to port 0x5D hex. 0xF is the FPGA device register.
2. selects a system device (device 0) by writing a byte value of 0 to port 0x5F and then delays 1/2 to 1 microsecond.
3. selects the register to index (in this case the IRQ Mask register). To do this, it writes a byte value of 7 to port 0x5D, followed by another delay.

4. writes the desired value to the IRQ Mask register by writing the value (??= whatever byte value you require) to port 0x5F, followed by an I/O delay.

You could use a similar sequence to perform a read. To perform a read, replace step 4 in Table 4-25 with:

4	in mov IODELAY	al ah	05Fh al	;read IRQ Mask register contents ;save value read

Connector Pin Assignments

5

This chapter gives you connector pin assignments for CPN5360 Single Board Computer (SBC) and Transition Module (TM) connectors.

Ethernet Connectors

Refer to Table 5-1 for pin assignments for the:

- CPN5360 Single Board Computer
  - Ethernet (J21)
- CPN5360TM80 Transition Module
  - Ethernet 2 (J18)
  - Ethernet 1 (J13)

Table 5-1. Ethernet Connector Pin Assignments for the CPN5360 Single Board Computer and CPN5360TM80 Transition Module

Pin Number	Signal Mnemonic	Signal Description
1	TX+	Differential transmit lines
2	TX-	Differential transmit lines
3	RX+	Differential receive lines
4	-	-
5	-	-
6	RX-	Differential receive lines
7	-	-
8	-	-

Serial Port Connectors

Refer to Table 5-2 for pin assignments for the:

- CPN5360 Single Board Computer
  - COM 1 (Serial Port 1) (J18)

Refer to Table 5-3 and Table 5-4 for pin assignments for the:

- CPN5360TM80 Transition Module
  - COM 2 (Serial Port 2) (J28)
  - COM 1 (Serial Port 1) (J21)

Table 5-2. Serial Port Connector Pin Assignments for the CPN5360 Single Board Computer (RJ-45) (J18)

Pin Number	Single Mnemonic	Signal Description
1	DCD-	Data set has detected the data carrier
2	RTS-	Indicates to data set that UART is ready to exchange data
3	GND	Ground
4	TXD	Sends serial output to communications link
5	RXD	Receives serial data input from communications link
6	GND	Ground
7	CTS-	Indicates that data set is ready to exchange data
8	DTR-	Indicates that a data set is ready to establish a communications like

Table 5-3. Serial Port Connector Pin Assignments for the CPN5360TM80 Transition Module (COM2) (J28)

Pin Number	Single Mnemonic	Signal Description
1	DCD-	Data set has detected the data carrier
2	RX	Receives serial data input from communication link
3	TX	Sends serial output to communication link
4	DTR-	Indicates that a data set is ready to establish a communication link
5	GND	Ground
6	DSR-	Indicates that a data set is ready to establish a communication link
7	RTS-	Indicates to data set that UART is ready to exchange data
8	CTS-	Indicates that a data set is ready to exchange data
9	RI-	Indicates that a modem has received a telephone ringing signal

Table 5-4. Serial Port Connector Pin Assignments for the CPN5360TM80 Transition Module (COM1) (J21)

Pin Number	Signal Mnemonic	Signal Description	Pin Number	Signal Mnemonic	Signal Description
1	DCD-	Data set has detected the data carrier	2	DSR-	Data set is ready to establish a communications link
3	RX	Receives serial data input from communication link	4	RTS-	UART is ready to exchange data
5	TX	Sends serial data to communication link	6	CTS-	Data set is ready to exchange data
7	DTR-	Data set is ready to establish a communication link	8	RI-	Modem has received a telephone ringing signal
9	GND	Ground	10	CGND	Chassis ground

Video Connector for the CPN5360TM80 Transition Module

Table 5-5. Video Connector Pin Assignments for the CPN5360TM80 Transition Module (J16)

Pin Number	Signal Mnemonic	Signal Description
1	RED	Red signal
2	GREEN	Green signal
3	BLUE	Blue signal
4	NC	no connection
5	DACVSS	Video return
6	DACVSS	Video return
7	DACVSS	Video return
8	DACVSS	Video return
9	NC	no connection
10	DACVSS	Video return
11	NC	no connection
12	DDCDAT	Display Data Channel data signal for DDC2 support
13	HSYNC	Horizontal synchronization
14	VSYNC	Vertical synchronization
15	DDCCLK	Display Data Channel clock signal for DDC2 support

Keyboard/Mouse P/S2 Connector for the CPN5360TM80 Transition Module

Table 5-6. Keyboard/Mouse P/S2 Connector Pin Assignments for the CPN5360TM80 Transition Module

Pin	Signal Mnemonic	Signal Description
1	KBDDAT	Data line for keyboard
2	AUXDAT	Data line for mouse
3	GND	Ground
4	KBDVCC	Keyboard Power
5	KBDCLK	Clock for keyboard
6	AUXCLK	Clock for mouse
7	CGND	Common Ground

Keyboard/Mouse/Power LED Connector for the CPN5360TM80 Transition Module

Table 5-7. Keyboard/Mouse/Power LED Connector Pin Assignments for the CPN5360TM80 Transition Module

Pin	Signal Mnemonic	Signal Description	Pin	Signal Mnemonic	Signal Description
1	PWRLED	Power LED Indicator	2	KBDCLK	Clock for keyboard
3	GND	Ground	4	KBDDAT	Data line for keyboard
5	GND	Ground	6	AUXDAT	Data line for mouse
7	-	-	8	GND	Ground
9	GND	Ground	10	KBDVCC	Keyboard power
11	-	-	12	AUXCLK	Clock for mouse

USB Connectors for the CPN5360TM80 Transition Module

Table 5-8. USB Connector Pin Assignments for the CPN5360TM80 Transition Module

Pin	Signal Mnemonic	Signal Description	Pin	Signal Mnemonic	Signal Description
1	VCC	Current limited USB power	2	VCC	Current limited USB power
3	DATA1-	USB serial communication differential pair	4	DATA0-	USB serial communication differential pair
5	DATA1+	USB serial communication differential pair	6	DATA0+	USB serial communication differential pair
7	GND	USB port common	8	GND	USB port common

Parallel Connector for the CPN5360TM80 Transition Module

Table 5-9. Parallel Connector Pin Assignments for the CPN5360TM80 Transition Module

Pin	Signal Mnemonic	Signal Description	Pin	Signal Mnemonic	Signal Description
1	STROBE-	Indicates data at parallel port is valid	2	AFD-	Causes printer to add a line feed
3	D0	Parallel data lines	4	ERR-	Set low when an error is detected
5	D1	Parallel data lines	6	INIT-	Initializes the printer
7	D2	Parallel data lines	8	SLIN-	Selects the printer
9	D3	Parallel data lines	10	GND	Ground
11	D4	Parallel data lines	12	GND	Ground
13	D5	Parallel data lines	14	GND	Ground
15	D6	Parallel data lines	16	GND	Ground
17	D7	Parallel data lines	18	GND	Ground
19	ACK-	Input is pulsed by the peripheral to acknowledge data retrieval	20	GND	Ground
21	BUSY	Printer cannot accept any more data	22	GND	Ground
23	PE	Printer is out of paper	24	GND	Ground
25	SELECT	Set high when selected	26	-	-

EIDE Connector for the CPN 5360TM80 Transition Module

Table 5-10. EIDE Connector Pin Assignments for the CPN5360TM80 Transition Module

Pin	Signal Mnemonic	Signal Description	Pin	Signal Mnemonic	Signal Description
1	RESET-	Reset signal to drive	2	GND	Ground
3	DD7	Drive data line	4	DD8	Drive data line
5	DD6	Drive data line	6	DD9	Drive data line
7	DD5	Drive data line	8	DD10	Drive data line
9	DD4	Drive data line	10	DD11	Drive data line
11	DD3	Drive data line	12	DD12	Drive data line
13	DD2	Drive data line	14	DD13	Drive data line
15	DD1	Drive data line	16	DD14	Drive data line
17	DD0	Drive data line	18	DD15	Drive data line
19	GND	Drive data line	20	-	-
21	DMARQ	Drive DMA request	22	GND	Ground
23	IOW-	Drive I/O write	24	GND	Ground
25	IOR-	Drive I/O read	26	GND	Ground
27	IORDY	Drive is ready for I/O cycle(s)	28	CSEL-	Cable select
29	DMACK-	Drive DMA acknowledge	30	GND	Ground
31	INTRQ	Drive interrupt request	32	IOCS16-	Indicates a 16 bit register is decoded
33	DA1	Drive register and data port address line	34	PDIAG-	Output from drive 1 and monitored by drive 0
35	DA0	Drive register and data port address line	36	DA2	Drive register and data port address line
37	CS1-	Chip select drive 0, also command register block select	38	CS3-	Chip select drive 1, also command register block select
39	DASP-	Drive active/slave present	40	GND	Ground

CompactFlash Connector for the CPN5360TM80 Transition Module

Table 5-11. CompactFlash Connector Pin Assignments for the CPN5360TM Transition Module

Pin	Signal Mnemonic	Signal Description	Pin	Signal Mnemonic	Signal Description
1	GND	Ground	26	-	-
2	DD3	Drive data line	27	DD11	Drive data line
3	DD4	Drive data line	28	DD12	Drive data line
4	DD5	Drive data line	29	DD13	Drive data line
5	DD6	Drive data line	30	DD14	Drive data line
6	DD7	Drive data line	31	DD15	Drive data line
7	CS1-	Chip select drive 0, also command register block select	32	CS3-	Chip select drive 1, also command register block select
8	GND	Ground	33	-	-
9	GND	Ground	34	IOR-	Drive I/O read
10	GND	Ground	35	IOW-	Drive I/O write
11	GND	Ground	36	VCC	+5 Volts
12	GND	Ground	37	INTRQ	Drive interrupt request
13	VCC	+5 Volts	38	VCC	+5 Volts
14	GND	Ground	39	CSE:L-DD3	Cable select
15	GND	Ground	40	-	-
16	GND	Ground	41	RESET-	Reset signal to drive
17	GND	Ground	42	IORDY	Drive is ready for I/O cycle(s)
18	DA2	Drive register and data port address lines	43	-	-
19	DA1	Drive register and data port address lines	44	VCC	+5 Volts
20	DA0	Drive register and data port address lines	45	DASP-	Drive active/slave present

Table 5-11. CompactFlash Connector Pin Assignments for the CPN5360TM Transition Module (Continued)

Pin	Signal Mnemonic	Signal Description	Pin	Signal Mnemonic	Signal Description
21	DD0	Drive data line	46	PDIAG-	Output from drive 1 and monitored by drive 0
22	DD1	Drive data line	47	DD8	Drive data line
23	DD2	Drive data line	48	DD9	Drive data line
24	-	-	49	DD10	Drive data line
25	-	-	50	GND	Ground

Floppy Connector for the CPN5360TM80 Transition Module

Table 5-12. Floppy Connector Pin Assignments for the CPN5360TM80 Transition Module

Pin	Signal Mnemonic	Signal Description	Pin	Signal Mnemonic	Signal Description
1	GND	Drive Common	2	DRVDENS0	Disk density select communication
3	-	-	4	-	-
5	GND	Drive Common	6	DRVDENS1	Disk density select communication
7	GND	Drive Common	8	INDEX-	Indicates the beginning of a track
9	GND	Drive Common	10	MTR0-	Motor enable outputs
11	GND	Drive Common	12	DS1-	Drive select 1
13	GND	Drive Common	14	DS0-	Drive select 0
15	GND	Drive Common	16	MTR1-	Motor enable outputs
17	GND	Drive Common	18	DIR-	Controls the direction of the FDD head during seek operations
19	GND	Drive Common	20	STEP-	Supplies step pulses to move head during seek operations
21	GND	Drive Common	22	WDATA-	Writes serial data to disk drive
23	GND	Drive Common	24	WGATE-	Enables head of disk drive to write to disk
25	GND	Drive Common	26	TR0-	Indicates that head of FDD is at track 0

Table 5-12. Floppy Connector Pin Assignments for the CPN5360TM80 Transition Module (Continued)

Pin	Signal Mnemonic	Signal Description	Pin	Signal Mnemonic	Signal Description
27	GND	Drive Common	28	WPROT-	Indicates a disk is write protected
29	GND	Drive Common	30	RDATA-	Raw read data from disk drive
31	GND	Drive Common	32	HDSEL-	Determines side of the floppy disk being accessed
33	GND	Drive Common	34	DSKCHG-	Notifies the disk drive controller that the drive door is open

Indicator LED/Miscellaneous Connector for the CPN5360TM80 Transition Module

Table 5-13. Indicator LED/Miscellaneous Connector Pin Assignments for the CPN5360TM80 Transition Module (J2)

Pin	Signal Mnemonic	Signal Description	Pin	Signal Mnemonic	Signal Description
1	VCC	+5 Volt power	2	-	-
3	VCC	+5 Volt power	4	-	-
5	VCC	+5 Volt power	6	EIDE_LEDa	Secondary channel EIDE activity LED
7	VCC	+5 Volt power	8	EIDE_LEDb	Primary channel EIDE activity LED
9	VCC	+5 Volt power	10	-	-
11	GND	Ground	12	PBRESET	Pushbutton reset
13	GND	Ground	14	CSEL-	Tie this pin to ground to make the CompactFlash master

CPN5360 Single Board Computer, CompactPCI Bus Connectors (J1 and J2)

The CPN5360 Single Board Computer provides a 64 bit CompactPCI interface on connectors J1 and J2. Refer to Table 5-14 for J1 and Table 5-15 for J2 pin designations.

Table 5-14. CPN5360 Backplane Connector Pin Assignments (J1)

Pin Number	F	E	D	C	B	A
25	GND	VCC	VCC3	ENUM#	REQ64#	VCC
24	GND	ACK64#	AD[0]	VIO	VCC	AD[1]
23	GND	AD[2]	VCC	AD[3]	AD[4]	VCC3
22	GND	AD[5]	AD[6]	VCC3	GND	AD[7]
21	GND	C/BE[0]#	M66EN	AD[8]	AD[9]	VCC3
20	GND	AD[10]	AD[11]	VIO	GND	AD[12]
19	GND	AD[13]	GND	AD[14]	AD[15]	VCC3
18	GND	C/BE[1]#	PAR	VCC3	GND	SERR#
17	GND	PERR#	GND	SBO#	SDONE	VCC3
16	GND	LOCK#	STOP#	VIO	GND	DEVSEL#
15	GND	TRDY#	BD_SEL#	IRDY#	FRAME#	VCC3
KEY						
11	GND	C/BE[2#]	GND	AD[16]	AD[17]	AD[18]
10	GND	AD[19]	AD[20]	VCC3	GND	AD[21]
9	GND	AD[22]	GND	AD[23]	IDSEL	C/BE[3]#
8	GND	AD[24]	AD[25]	VIO	GND	AD[26]
7	GND	AD[27]	GND	AD[28]	AD[29]	AD[30]
6	GND	AD[31]	CLK	VCC3	GND	REQ#
5	GND	GNT#	GND	RST#	BRSVP1B5	BRSVP1A5
4	GND	INTS	INTP	VIO	HLTY	BRSVP1A4
3	GND	INTD#	VCC	INTC#	INTB#	INTA#
2	GND	TD1	TD0	TMS	VCC	TCK
1	GND	VCC	+12V	TRST#	-12V	VCC

Table 5-15. CPN5360 Backplane Connector Pin Assignments (J2)

Pin Number	F	E	D	C	B	A
22	GND	GA0	GA1	GA2	GA3	GA4
21	GND	RSV	RSV	RSV	GND	CLK6
20	GND	RSV	GND	RSV	GND	CLK5
19	GND	RSV	RSV	RSV	GND	GND
18	GND	BRSVP2E18	GND	BRSVP2C18	BRSVP2B18	BRSVP2A18
17	GND	GNT6#	REQ6#	PRST#	GND	BRSVP2A17
16	GND	BRSVP2E16	GND	DEG#	BRSVP2B16	BRSVP2A16
15	GND	GNT5#	REQ5#	FAL#	GND	BRSVP2A15
14	GND	AD[32]	GND	AD[33]	AD[34]	AD[35]
13	GND	AD[36]	AD[37]	VIO	GND	AD[38]
12	GND	AD[39]	GND	AD[40]	AD[41]	AD[42]
11	GND	AD[43]	AD[44]	VIO	GND	AD[45]
10	GND	AD[46]	GND	AD[47]	AD[48]	AD[49]
9	GND	AD[50]	AD[51]	VIO	GND	AD[52]
8	GND	AD[53]	GND	AD[54]	AD[55]	AD[56]
7	GND	AD[57]	AD[58]	VIO	GND	AD[59]
6	GND	AD[60]	GND	AD[61]	AD[62]	AD[63]
5	GND	PAR64	C/BE[4]#	VIO	GND	C/BE[5]#
4	GND	C/BE[6]#	GND	C/BE[7]#	BRSVP2B4	VIO
3	GND	GNT4#	REQ4#	GNT3#	GND	CLK4
2	GND	REQ3#	GNT2#	SYSEN#	CLK3	CLK2
1	GND	REQ2#	GNT1#	REQ1#	GND	CLK1

CPN5360 Single Board Computer, CompactPCI Rear I/O Connectors (J3, J4, and J5)

Table 5-16. CPN5360 Single Board Computer, Rear I/O Connector Pin Assignments (J3)

Pin Number	F	E	D	C	B	A
19	GND	-	USB0-	USB0+	USB1-	USB1+
18	GND	-	COM2_RI	COM2_DTR	COM1_RI	COM1_DTR
17	GND	-	COM2_DCD	COM2_DSR	COM1_DCD	COM1_DSR
16	GND	-	COM2_TxD	COM2_CTS	COM1_TxD	COM1_CTS
15	GND	-	COM2_RxD	COM2_RTS	COM1_RxD	COM1_RTS
14	GND	+5V	+5V	+3.3V	+3.3V	+3.3V
13	GND	PMC2IO1	PMC2IO2	PMC2IO3	PMC2IO4	PMC2IO5
12	GND	PMC2IO6	PMC2IO7	PMC2IO8	PMC2IO9	PMC2IO10
11	GND	PMC2IO11	PMC2IO12	PMC2IO13	PMC2IO14	PMC2IO15
10	GND	PMC2IO16	PMC2IO17	PMC2IO18	PMC2IO19	PMC2IO20
9	GND	PMC2IO21	PMC2IO22	PMC2IO23	PMC2IO24	PMC2IO25
8	GND	PMC2IO26	PMC2IO27	PMC2IO28	PMC2IO29	PMC2IO30
7	GND	PMC2IO31	PMC2IO32	PMC2IO33	PMC2IO34	PMC2IO35
6	GND	PMC2IO36	PMC2IO37	PMC2IO38	PMC2IO39	PMC2IO40
5	GND	PMC2IO41	PMC2IO42	PMC2IO43	PMC2IO44	PMC2IO45
4	GND	PMC2IO46	PMC2IO47	PMC2IO48	PMC2IO49	PMC2IO50
3	GND	PMC2IO51	PMC2IO52	PMC2IO53	PMC2IO54	PMC2IO55
2	GND	PMC2IO56	PMC2IO57	PMC2IO58	PMC2IO59	PMC2IO60
1	GND	PMC2IO61	PMC2IO62	PMC2IO63	PMC2IO64	VCC3

Table 5-17. Signal Descriptions for the CPN5360 Single Board Computer Backplane Connector (J3)

Signal	Signal Mnemonic	Signal Description
Universal Serial Bus (Channel 0 and Channel 1)	USB0+	(+) signal of differential data pair for USB channel 0
	USB0-	(-) signal of differential data pair for USB channel 0
	USB1+	(+) signal of differential data pair for USB channel 1
	USB1-	(-) signal of differential data pair for USB channel 1
Serial COM Ports (1 and 2)	COMx_CTS-	Clear to send
	COMx_DCD-	Data carrier detected
	COMx_DSR-	Data set ready
	COMx_DTR-	Data terminal ready
	COMx_RTS-	Request to send
	COMx_RXD	Serial receive data
	COMx_TXD	Serial transmit data
	COMx_RI	Ring Indicator
General	GND	ground plane
	+/-3.3V, +/-5V	power
PMC2 I/O	PMC2IO [1 to 64]	PMC channel 2 I/O signals 1 through 64

Connector J4 contains floppy, printer port and miscellaneous functions. J4 is an optionally installed connector. Refer to Table 5-18 and Table 5-19.

Table 5-18. CPN5360 Rear I/O Pin Assignments (J4)

Pin Number	F	E	D	C	B	A
25	GND		PRSTDRV-	PINTRQ	PCS1-	GND
24	GND	PDACK-	PCS3-	PIORDY	PDREQ	PIOW-
23	GND	PA2	PIOR-	PA1	PA0	PD15
22	GND	PD14	PD13	PD12	PD11	PD10
21	GND	PD9	PD8	PD7	PD6	PD5
20	GND	PD4	PD3	PD2	PD1	PD0
19	GND	GRN	RED		PDIAG	PDASP-
18	GND	BLU	GND			
17	GND	HSYNC	DDCCLK			
16	GND	VSYNC	DDCDAT			
15	GND					
Key						
11	GND					
10	GND					
9	GND					
8	GND					
7	GND	PD2	AFD-	STB-		
6	GND	PD6	PD0	ERR-	PD1	INIT-
5	GND	SLCT	SLIN-	PD3	PD4	PD5
4	GND	DRVDENS0	PD7	ACK-	BUSY	PE
3	GND	DSKCHG-	HDSEL-	RDATA-	WPROT-	TR0-
2	GND	WGATE-	WDATA-	STEP-	DIR-	MTR1-
1	GND	DS0-	DS1-	MTR0-	INDEX-	DRVDENS1

Table 5-19. Signal Descriptions for the CPN5360 Single Board Computer Backplane Connector (J4)

Signal	Signal Mnemonic	Signal Description
Floppy Disk Drive	DSKCHG-	Indicates drive door is open
	DIR-	Controls direction of the head during step operation
	DS[1:0]-	Drive selects
	HDSEL-	Selects top or bottom side head
	INDEX-	Indicates the beginning of a track
	MTR[1:0]	Motor enables
	RDATA-	Data read
	STEP-	Step, pulses move head in or out
	TR0-	Indicates that head is positioned above track 00
	WDATA-	Write data to drive
	WGATE-	Enables head write circuitry of drive
	WPROT-	Indicates a disk is write-protected
	DRVDENS[1:0]	Disk density select communication
	PDIAG-	Output from drive 1 and monitored by drive 0
	DASP-	Drive active/slave present
	ACK-	Pulsed by peripheral to acknowledge data sent
	BUSY	Indicates that printer cannot accept more data
	ERR-	Peripheral detected an error
	PD[7:0]	Parallel data lines, bits 7--0
	PE	Paper end, indicates the printer is out of paper
	AFD-	Auto feed, causes printer to line feed
	INIT-	Initializes the printer
	SLIN-	Select in, selects the printer
	STB-	Data strobe, indicates data is valid
	SLCT	Select, peripheral indicates it is selected
EIDE (ATA-2), Primary Channel	PDREQ-	Drive DMA request
	PDACK-	Drive DMA acknowledge
	PIOR-	Drive I/O read

Table 5-19. Signal Descriptions for the CPN5360 Single Board Computer Backplane Connector (J4) (Continued)

Signal	Signal Mnemonic	Signal Description
	PIOW-	Drive I/O write
	PIORDY-	Indicates drive is ready for I/O cycle(s)
	PD[15:0]	Drive data lines, bits 15 -- 0
	DRSTDRV	Reset signal to drive
	PCS1	Chip select drive 0, also command register block select
	PCS3	Chip select drive 1, also command register block select
	PA[2:0]	Drive register and data port address lines
	PINTRQ	Drive interrupt request
	PDASP	Drive active
	PDIAG	Drive inter-communication
Video Signals	RED	Red signal
	GRN	Green signal
	BLU	Blue Signal
	HSYNC	Horizontal synchronization
	VSYNC	Vertical synchronization
	DDCCLK	Display Data Channel clock signal for DDC2 support
	DDCDAT	Display Data Channel data signal for DDC2 support

Table 5-20. CPN5360 Rear I/O Pin Assignments (J5)

Pin Number	F	E	D	C	B	A
22	GND	SRSTDRV-	SINTRQ	KBDDAT	ERX0+	ETX0+
21	GND	SCS1-	SDACK-	KBDCLK	ERX0-	ETX0-
20	GND	SCS3-	SIORDY	RESET_IN	AUXVCC	GND
19	GND	SDREQ	SIOW-	MDAT	ERX1+	ETX1+
18	GND	SA2	SIOR-	MCLK	ERX1-	ETX1-
17	GND	SA1	SA0	SD15	AUXVCC	GND
16	GND	SD14	SD13	SD12	SD11	SD10
15	GND	SD9	SD8	SD7	SD6	SD5
14	GND	SD4	SD3	SD2	SD1	SD0
13	GND	PMC1IO1	PMC1IO2	PMC1IO3	PMC1IO4	PMC1IO5
12	GND	PMC1IO6	PMC1IO7	PMC1IO8	PMC1IO9	PMC1IO10
11	GND	PMC1IO11	PMC1IO12	PMC1IO13	PMC1IO14	PMC1IO15
10	GND	PMC1IO16	PMC1IO17	PMC1IO18	PMC1IO19	PMC1IO20
9	GND	PMC1IO21	PMC1IO22	PMC1IO23	PMC1IO24	PMC1IO25
8	GND	PMC1IO26	PMC1IO27	PMC1IO28	PMC1IO29	PMC1IO30
7	GND	PMC1IO31	PMC1IO32	PMC1IO33	PMC1IO34	PMC1IO35
6	GND	PMC1IO36	PMC1IO37	PMC1IO38	PMC1IO39	PMC1IO40
5	GND	PMC1IO41	PMC1IO42	PMC1IO43	PMC1IO44	PMC1IO45
4	GND	PMC1IO46	PMC1IO47	PMC1IO48	PMC1IO49	PMC1IO50
3	GND	PMC1IO51	PMC1IO52	PMC1IO53	PMC1IO54	PMC1IO55
2	GND	PMC1IO56	PMC1IO57	PMC1IO58	PMC1IO59	PMC1IO60
1	GND	PMC1IO61	PMC1IO62	PMC1IO63	PMC1IO64	TMPRSNT

Table 5-21. Signal Descriptions for the CPN5360 Single Board Computer Backplane Connector (J5)

Signal	Signal Mnemonic	Signal Description
Ethernet	ERX1+, ERX1-	Differential receive lines, Ethernet 1
	ETX1+, ETX1-	Differential transmit lines, Ethernet 1
	ERX2+, ERX2-	Differential receive lines, Ethernet 2
	ERX2+, ETX2-	Differential transmit lines, Ethernet 2
Keyboard/Mouse Device, TTL Levels	MCLK	Clock for PS/2 mouse
	MDAT	Serial data line for PS/2 mouse
	KBDCLK	Clock for PC/AT or PS/2 keyboard
	KBDDAT	Serial data line for PC/AT or PS/2 keyboard
Miscellaneous Signals	TMPRSNT	Indicates transition module is installed
	AUXVCC	Auxiliary VCC power
PMC1 I/O	PMC1IO [1 to 64]	PMC channel 1 I/O signals 1 through 64
EIDE (ATA-2), Secondary Channel, TTL levels	SDREQ-	Drive DMA request
	SDACK-	Drive DMA acknowledge
	SIOR-	Drive I/O read
	SIOW-	Drive I/O write
	SIORDY-	Indicates drive is ready for I/O cycle(s)
	SD[15:0]	Drive data lines, bits 15 -- 0
	SRSTDRV	Reset signal to drive
	SCS1	Chip select drive 0, also command register block select
	SCS3	Chip select drive 1, also command register block select
	SA[2:0]	Drive register and data port address lines
	SINTRQ	Drive interrupt request

Table 5-21. Signal Descriptions for the CPN5360 Single Board Computer Backplane Connector (J5) (Continued)

Signal	Signal Mnemonic	Signal Description
Video Signals	RED	Red signal
	GRN	Green signal
	BLU	Blue Signal
	HSYNC	Horizontal synchronization
	VSYNC	Vertical synchronization
	DDCCLK	Display Data Channel clock signal for DDC2 support
	DDCDAT	Display Data Channel data signal for DDC2 support

CPN5360TM80 Transition Module, Rear I/O Connectors (J3, J4, and J5)

Table 5-22 through Table 5-27 show J3, J4, and J5 connector pinouts and signal descriptions.

Table 5-22. CPN5360TM80 Transition Module, Rear I/O Connector Pin Assignments (J3)

Pin Number	F	E	D	C	B	A
19	GND		UDATA0-	UDATA0+	UDATA1-	UDATA1+
18	GND	+12V	RI2	DTR2	RI1	DTR1
17	GND	-12V	DCD2	DSR	DCD1	DSR1
16	GND		TxD2	CTS2	TxD1	CTS1
15	GND		RxD2	RTS2	RxD1	RTS1
14	GND	VCC	VCC	VCC3	VCC3	VCC3
13	GND	PMC1IO1	PMC1IO2	PMC1IO3	PMC1IO4	PMC1IO5
12	GND	PMC1IO6	PMC1IO7	PMC1IO8	PMC1IO9	PMC1IO10
11	GND	PMC1IO11	PMC1IO12	PMC1IO13	PMC1IO14	PMC1IO15
10	GND	PMC1IO16	PMC1IO17	PMC1IO18	PMC1IO19	PMC1IO20
9	GND	PMC1IO21	PMC1IO22	PMC1IO23	PMC1IO24	PMC1IO25
8	GND	PMC1IO26	PMC1IO27	PMC1IO28	PMC1IO29	PMC1IO30
7	GND	PMC1IO31	PMC1IO32	PMC1IO33	PMC1IO34	PMC1IO35
6	GND	PMC1IO36	PMC1IO37	PMC1IO38	PMC1IO39	PMC1IO40
5	GND	PMC1IO41	PMC1IO42	PMC1IO43	PMC1IO44	PMC1IO45
4	GND	PMC1IO46	PMC1IO47	PMC1IO48	PMC1IO49	PMC1IO50
3	GND	PMC1IO51	PMC1IO52	PMC1IO53	PMC1IO54	PMC1IO55
2	GND	PMC1IO56	PMC1IO57	PMC1IO58	PMC1IO59	PMC1IO60
1	GND	PMC1IO61	PMC1IO62	PMC1IO63	PMC1IO64	VCC3

Table 5-23. Signal Descriptions for the CPN5360TM80 Transition Module, Backplane Connector (J3)

Signal	Signal Mnemonic	Signal Description
Universal Serial Bus (Channel 0 and Channel 1)	USDATAn+	(+) signal of differential data pair for USB channel
	USDATAn-	(-) signal of differential data pair for USB channel
Serial COM Ports (1 and 2)	CTSn	Clear to send
	DCDn	Data carrier detected
	DSRn	Data set ready
	DTRn	Data terminal ready
	RIn	Ring indicator
	RTSn	Request to send
	RXDn	Serial receive data
	TXDn	Serial transmit data
General	GND	ground plane
	VCC	+5 Volt power
	VCC3	+3.3 Volt power
	+12V	+12 Volt power
	-12V	- 12 Volt power
PMC1 I/O	PMC1IO [1 to 64]	PMC channel 1 I/O signals 1 through 64

Table 5-24. CPN5360TM80 Transition Module, Rear I/O Connector Pin Assignments (J4)

Pin Number	F	E	D	C	B	A
25	GND					
24	GND					
23	GND					
22	GND					
21	GND					
20	GND					
19	GND	GRN	RED			
18	GND	BLU	GND			
17	GND	HSYNC	DDCCLK			
16	GND	VSYNC	DDCDAT			
15	GND					
Key						
11	GND					
10	GND					
9	GND					
8	GND					
7	GND	PD2	AFD-	STB-		
6	GND	PD6	PD0	ERR-	PD1	INIT-
5	GND	SLCT	SLIN-	PD3	PD4	PD5
4	GND	DRVDENS0	PD7	ACK-	BUSY	PE
3	GND	DSKCHG-	HDSEL-	RDATA-	WPROT-	TR0-
2	GND	WGATE-	WDATA-	STEP-	DIR-	MTR1-
1	GND	DS0	DS1-	MTR0-	INDEX-	DRVDENS1

Table 5-25. Signal Descriptions for the CPN5360TM80 Transition Module, Backplane Connector (J4)

Signal	Signal Mnemonic	Signal Description
Floppy Disk Drive	DSKCHG-	Indicates drive door is open
	DIR-	Controls direction of the head during step operations
	DRVDENS[1:0]	Disk density select communication
	DS[1:0]-	Drive selects
	HDSEL-	Selects top or bottom side head
	INDEX-	Indicates the beginning of a track
	MTR[1:0]-	Motor enables
	RDATA-	Data read
	STEP-	Step, pulses move head in or out
	TR0	Indicates that head is positioned above track 00
	WDATA-	Write data to drive
	WGATE-	Enables head write circuitry of drive
	WPROT-	Indicates a disk is write-protected
Parallel LPT Port	ACK-	Pulsed by peripheral to acknowledge data sent
	BUSY	Indicates that the printer cannot accept more data
	ERR-	Peripheral detected an error
	PD[7:0]	Parallel data lines, bits 7- 0
	PE	Paper end, indicates printer out of paper
	AFD-	Auto feed, causes printer to line feed
	INIT-	Initializes the printer
	SLIN-	Select in, selects the printer
	STB-	Data strobe, indicates data is valid
	SLCT	Select, peripheral indicates it is selected

Table 5-25. Signal Descriptions for the CPN5360TM80 Transition Module, Backplane Connector (J4) (Continued)

Signal	Signal Mnemonic	Signal Description
Video	RED	Red signal
	GRN	Green signal
	BLU	Blue signal
	HSYNC	Horizontal synchronization
	VSYNC	Vertical synchronization
	DDCCLK	Display Data Channel clock signal for DDC2 support
	DDCDAT	Display Data Channel data signal for DDC2 support

Table 5-26. CPN5360TM80 Transition Module, Rear I/O Connector Pin Assignments (J5)

Pin Number	F	E	D	C	B	A
22	GND	SDRESET-	SINTRQ	KBDDAT	RD1+	TD1+
21	GND	SCS1-	SDMACK-	KBDCLK	RD1-	TD1-
20	GND	SCS3-	SIORDY	RESET_IN	AUXVCC2	GND
19	GND	SDMARQ	SDIOW-	MDAT	RD2+	TD2+
18	GND	SDA2	SDIOR-	MCLK	RD2-	TD2-
17	GND	SDA1	SDA0	SDD15	AUXVCC1	GND
16	GND	SDD14	SDD13	SDD12	SDD11	SDD10
15	GND	SDD9	SDD8	SDD7	SDD6	SDD5
14	GND	SDD4	SDD3	SDD2	SDD1	SDD0
13	GND					
12	GND					
11	GND					
10	GND					
9	GND					
8	GND					
7	GND					
6	GND					
5	GND					
4	GND					
3	GND					
2	GND					
1	GND					GND

Table 5-27. Signal Descriptions for the CPN5360TM80 Transition Module, Backplane Connector (J5)

Signal	Signal Mnemonic	Signal Description
Miscellaneous	AUXVCCn	Auxiliary VCC power, fused at 0.75A maximum
	GND	Digital signal ground plane
EIDE (ATA-2), Secondary Channel	SDMARQ	Drive DMA request
	SDMACK-	Drive DMA acknowledge
	SDIOR-	Drive I/O read
	SDIOW-	Drive I/O write
	SIORDY	Indicates drive is ready for I/O cycle(s)
	SDD[15:0]	Drive data lines, bits 15- 0
	SDRESET-	Reset signal to drive
	SCS1-	Chip select drive 0, also command register block select
	SCS3-	Chip select drive 1, also command register block select
	SDA[2:0]	Drive register and data port address lines
	SINTRQ	Drive interrupt request
Ethernet	RDn+, RDn-	Differential receive lines
	TDn+, TDn-	Differential transmit lines
Keyboard/Mouse Device	MCLK	Clock for PS/2 mouse
	MDAT	Serial data line for PS/2 mouse
	KBDCLK	Clock for PC/AT or PS/2 keyboard
	KBDDAT	Serial data line for PC/AT or PS/2 keyboard

Specifications A

Refer to these tables for:

- input power requirements (Table A-1)
- physical characteristics (Table A-2
- lithium battery specifications (Table A-3)
- environmental specifications (Table A-4)

Table A-1. Power Requirements for the CPN5360 Single Board Computer and Transition Module

Input power [1, 2]	Clock speed
+5V @4A (20W)	266/333/500 MHz with 128 or 256MB SDRAM
+3.3V @ 2.5A (8.2W)	
+12V @ 100mA (1.2W)	
-12V @ 10mA (0W)	
[1] These values include the single board computer and the transition module [2] Total power = 29.4W	

Table A-2. Physical Characteristics of the CPN5360 Single Board Computer

Parameter	Description
Form Factor	CompactPCI Standard 6U (233mm x 160mm x 20mm) Conforms to PICMG 2.0, CompactPCI (rev. 2.1) and PCI SIG 2.1 specifications
Dimensions	4 HP (.8 inches) wide

Table A-3. Lithium Battery Specifications

Rating	Shelf Life
180mA/hour	2 years

This environmental specifications table does not include the on-board hard drive option.

Table A-4. Environmental Specifications

Parameter	Condition	Specification
Temperature	Operating	0°C to 55°C (32°F to 130°F)[1]
	Non-operating	-40°C to 65°C (°-40F to 150°F)
Humidity	Operating	5% to 90% @ 40°C, non-condensing
	Non-operating	5% to 95% @40°C, non-condensing
Shock	Operating	10G, 3 axis
	Non-operating	per ASTM 0775
Vibration	Operating	1.0 G RMS, 20 to 2000 Hz random
	Non-operating	6 Gs RMS, 20 to 2000 Hz random
Altitude	Operating	15,000 feet (4,572 m)
	Non-operating	40,000 feet (12,192 m)
Maximum wet bulb	Operating	28°C (82°F)
	Non-operating	32°C (90°F)
Cooling	na	35 CFM over the Single Board Computer
MTBF (MIL-HDBK-217F)	Operating	300,000 hours at 30°C 100,000 hours at 50°C

[1] Derate the maximum operating temperature by 1°F (1.8°C) per 3280 feet (1000m) above sea level.
[2] Environmental Specifications exclude the on-board hard drive option

Windows NT 4.0 Installation Error

B

After installing Windows NT 4.0, you may see an error in the Event Viewer log. The message references a system shutdown during the OEM installation of NT 4.0. The shutdown was orderly, but the Event Viewer logged the shutdown as unexpected.

Note Nothing is wrong with the system, or the installation. This message appears once, and does not appear on future restarts of the operating system.

Related Documentation C

Motorola Computer Group Documents

You can get more information about CompactPCI by looking at the publications in Table C-1. You can get paper or electronic copies of Motorola Computer Group publications by:

- Visiting Motorola Computer Group's World Wide Web literature site, http://www.motorola.com/computer/literature
- Contacting your local Motorola sales office

Table C-1. Motorola Computer Group Documents

Document Title	Motorola Publication Number
CPV5350 CompactPCI Single Board Computer and Transition Module Installation Guide	CPV5350A/IHx
CPV5350 CompactPCI BIOS and Programmer's Reference Guide	CPV5350A/PGx

To get the most up-to-date product information in PDF or HTML format, visit http://www.motorola.com/computer/literature.

URLs

The following URLs (uniform resource locators) may provide helpful sources of additional information about this product, related services, and development tools. Please note that, while these URLs are verified, they are subject to change without notice.

- Motorola Computer Group, http://www.motorola.com/computer
- Motorola Computer Group OEM Services, http://www.motorola.com/computer/support

C

- PCI Industrial Computer Manufacturer's Group (PICMG) Hot Swap Specification, http://www.picmg.org
- Standard Microsystems Corporation, Ultra I/O Data Sheet, http://www.smsc.com/main/catalog/fdc37c67x.html
- Wired for Management, PXE (Preboot Execution Environment), http://developer.intel.com/ial/wfm

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