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CompactPCI® CPV5300 Single Board Computer

BIOS and Programmer's Reference Guide

CPV5300A/PG2

November 3, 2000 Edition

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Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in any explosive atmosphere such as in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment could result in an explosion and cause injury or damage.

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Observe Warnings in Manual.

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Warning

To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

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All Motorola PWBs (printed wiring boards) are manufactured with a flammability rating of 94V-0 by UL-recognized manufacturers.

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CAUTION

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Lithium Battery Caution

This product contains a lithium battery to power the clock and calendar circuitry.



CAUTION

Danger of explosion if battery is replaced incorrectly. Replace battery only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to the manufacturer's instructions.



Attention

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabricant.



Vorsicht

Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch denselben oder einen vom Hersteller empfohlenen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.

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>
> EN50082-1:1997 “Electromagnetic Compatibility—Generic Immunity Standard, Part 1. Residential, Commercial and Light Industry”

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Table of Contents

CHAPTER 1 PhoenixBIOS Overview

What is a ROM BIOS? 1-1
ROM BIOS Functions 1-2
Power-on Self Test 1-3

CHAPTER 2 BIOS Setup

Using the Phoenix Setup Program 2-1
Starting Setup 2-1
The Setup Interface 2-2
The Menu Bar 2-3
The Legend Bar 2-3
The Field Help Window 2-4
The General Help Window 2-5
Main Menu Selections 2-6
Masters and Slaves 2-7
Advanced Hard Disk Features 2-9
The Advanced Menu 2-12
Saving Values 2-28
Exit Discarding Changes 2-29
Load Setup Defaults 2-29
Discard Changes 2-30
Save Changes 2-30

CHAPTER 3 Phoenix BIOS Messages

PhoenixBIOS Messages 3-1

CHAPTER 4 Power On Self-Tests

Recoverable Power On Self-Test (POST) Errors 4-1
POST Terminal Errors 4-2
Test Points and Beep Codes 4-2

CHAPTER 5 Functional Description

Introduction 5-1
Peripheral Component Interconnect (PCI) Local Bus 5-1

Watchdog Timer 5-2
Watchdog Timer Operation 5-3
Enabling the timer 5-3
I/O Address Map 5-4
Memory Address Mapping 5-6
Video Controller 5-7
Ultra SCSI Controller 5-7
EIDE Interface 5-10
Floppy Interface 5-10
Parallel Port 5-11
Serial Ports 5-11
USB 5-11
Keyboard/Mouse Interface 5-12
DMA Channels 5-12
Interrupts 5-13
Understanding the Programmable Logic Field Programmable Gate Array (PLFPGA) Registers 5-14
Register Descriptions 5-15
DEVNUM 5-17
STAT 5-18
ECTRL 5-19
WDCFG 5-20
INTUM 5-22
SCIEN 5-23
NMIEN 5-24
IRQEN 5-26
ALEN 5-27
LTCLR 5-28
ENMCFG 5-29
LNACTRL 5-30
LNBCTRL 5-31
SCSICTRL 5-32
USBCTRL 5-33
FLBCTRL 5-34

APPENDIX A Related Documentation

Motorola Computer Group Documents A-1

List of Figures

Figure 2-1. The basic setup screen 2-2
Figure 5-1. PLFPGA Watchdog Block Diagram 5-3
Figure 5-2. SCSI Termination 5-9
Figure 5-3. Block diagram for the PLFPGA 5-14

List of Tables

Table 1-1. PhoenixBIOS functions 1-2
Table 1-2. Fixed Disk Drive Values 1-5
Table 1-3. PhoenixBIOS special function keys 1-8
Table 2-1. PhoenixBIOS Main Menu Bar 2-3
Table 2-2. Legend Bar 2-4
Table 2-3. Scroll bar selections 2-6
Table 2-4. Main Menu Selections 2-6
Table 2-5. Features for Hard Disk Configuration 2-10
Table 2-6. Advanced Menu Selections 2-13
Table 2-7. Features for Configuring PCI Devices 2-16
Table 2-8. Configuring Ultra-I/O Devices on the CPV5300 2-19
Table 2-9. Configuring the System-Security Options 2-22
Table 2-10. Checking the Status Menu 2-24
Table 2-11. Selecting the Boot Options 2-25
Table 3-1. PhoenixBIOS Messages 3-2
Table 4-1. Checkpoint Codes and Beep Codes 4-3
Table 5-1. I/O Addresses 5-4
Table 5-2. Memory Address 5-6
Table 5-3. On-board drive options 5-10
Table 5-4. DMA channels 5-12
Table 5-5. Interrupt channels 5-13
Table 5-6. PLFPGA mapping for I/O ports 5-15
Table 5-7. PLFPGA register sets 5-16
Table 5-8. PLFPGA registers 5-16
Table 5-9. Bit descriptions for the FPGA register set 5-17
Table 5-10. Bit values for selecting register access 5-17
Table 5-11. Bit descriptions for the STAT register 5-18
Table 5-12. Bit descriptions for the ECTRL register 5-19
Table 5-13. Bit descriptions for the WDCFG register 5-20
Table 5-14. Bit values for selecting watchdog timeout time 5-20
Table 5-15. Bit values defining watchdog timeout and disabling 5-21
Table 5-16. Bit descriptions for the INTUM register 5-22
Table 5-17. Bit values for IRQ events 5-22
Table 5-18. Bit descriptions for the SCIEN register 5-23

Table 5-19. Bit descriptions for the NMIEN register 5-24
Table 5-20. Bit descriptions for the IRQEN register 5-26
Table 5-21. Bit descriptions for the ALEN register 5-27
Table 5-22. Bit descriptions for the LTCLR register 5-28
Table 5-23. Bit descriptions for the ENMCFG register 5-29
Table 5-24. Actions Taken for Each Value of ACT1 and ACT0 5-29
Table 5-25. Bit descriptions for the LNACTRL register 5-30
Table 5-26. Bit descriptions for the LNACTRL register 5-31
Table 5-27. Bit descriptions for the SCSICTRL register 5-32
Table 5-28. Bit descriptions for the USBCTRL register 5-33
Table 5-29. Bit descriptions for the FLBCTRL register 5-34
Table A-1. Motorola Computer Group Documents A-1

About This Manual

This CompactPCI® CPV5300 BIOS and Programmer's Reference Guide is based partly on the PhoenixBIOS 4.0 User's Manual and gives you instructions for configuring the PhoenixBIOS installed on the CPV5300 Single Board Computer. It also gives you instructions for using PhoenixBIOS utilities.

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CPV5300 Single Board Computer Model Numbers	Description
CPV5300-266	CompactPCI Single Board Computer with 266 MHz processor and 64 or 128MB SDRAM
CPV5300-333	CompactPCI Single Board Computer with 333 MHz processor and 64 or 128MB SDRAM

Summary of Changes

This table summarizes revisions to this manual.

Date:	Change:
November 3, 2000	Added “About This Manual”
	Revised “Understanding the PLFPGA Registers”, starting on page 5-14, for ENUM

Overview of Contents

This section contains a short description of the content of each chapter and appendix in this manual.

This Chapter or Appendix:	Gives you:
Chapter 1, “PhoenixBIOS Overview”	a detailed CPV5300 BIOS description.
Chapter 2, "BIOS Setup"	a description of the CPV5300 menu-driven PhoenixBIOS Setup program.
Chapter 3, "PhoenixBIOS Messages"	a list of messages that the BIOS can display.
Chapter 4, “Power On Self-Tests”	information to help you troubleshoot your system. It describes error reporting methods and beep codes.
Chapter 5, “Functional Description”	information about the PCI bus, watchdog timer, I/O address map, video and ultra SCSI controllers, EIDE and floppy drive interfaces and PLFPGA registers.
Appendix A, "Related Documentation"	information about related Motorola Computer Group documents and URLs for more information about this product, related services and development tools.

Who Should Use This Guide

The information in this guide is written for system installers, original equipment manufacturers (OEM) and technicians. The procedures assume familiarity with the safety practices and regulatory compliance required for using and modifying electronic equipment. Personnel who install CompactPCI systems should be trained and experienced with the installation of computers and computer equipment.

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PhoenixBIOS Overview 1

This chapter gives you a brief introduction and overview of the PhoenixBIOS software. It covers:

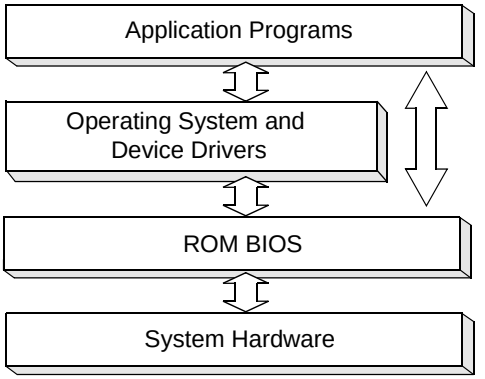
- a description of the ROM BIOS including ROM BIOS functions
- the power-on-self tests (POST)
- BIOS services
- system hardware requirements
- fixed disk drives
- function keys

What is a ROM BIOS?

A ROM BIOS (Basic Input/Output System) is a set of programs permanently stored in a ROM (Read-Only Memory) chip located on the computer motherboard. These programs micro-manage the hardware devices installed on your computer. When you turn on your computer, the ROM BIOS initializes and tests these devices. During run-time, the ROM BIOS provides the operating system and application programs with access to these devices. You can also use the BIOS Setup program to change your computer's hardware or behavior.

Software works best when it operates in layers. The ROM BIOS is the bottom-most software layer in the computer. It functions as the interface between the hardware layer in the computer. It functions as the interface between the hardware and the other layers of software, isolating them from the details of how the hardware works. This arrangement lets you change hardware devices without having to install a new operating system.

The following diagram shows how the ROM BIOS interfaces between the hardware and other layers of software.



ROM BIOS Functions

The PhoenixBIOS software performs these functions (Table 1-1):

Table 1-1. PhoenixBIOS functions

Function	Description
Configures Devices	Using the Setup program, you can enable, configure, and optimize the hardware devices in your system (clock, memory, disk drives).
Initializes Hardware at Boot	At power-on or reset, the BIOS performs Power-On-Self Test (POST) routines to test system resources and run the operating system.
Executes Run-Time Routines	The BIOS gives you access to basic hardware routines called from DOS and Windows applications.

Power-on Self Test

The first job of the ROM BIOS is to initialize and configure the computer hardware when you turn on your computer (system boot). It runs a series of complex programs called the Power-On Self Test (POST), which performs a number of tasks, including:

- Test Random Access Memory (RAM)
- Conduct an inventory of the hardware devices installed in the computer
- Configure hard and floppy disks, keyboard, monitor, and serial and parallel ports
- Configure other devices installed in the computer such as CD-ROM drives and sound cards
- Initialize computer hardware required for computer features such as plug and play and power management
- Run Setup if requested
- Load and run the Operating System (OS) such as DOS, OS/2, UNIX, or Windows NT

BIOS Services

The ROM BIOS gives the operating system, device drivers, and application programs access to the system hardware. It completes this task with a set of program routines, called BIOS Services. These program routines load into high memory at system boot.

The number of BIOS Services changes regularly. The BIOS Services give precise control of hardware devices such as disk drives, which require management and error checking. They also help manage new computer features such as power management, plug and play, and MultiBoot.

System Hardware Requirements

The PhoenixBIOS requires the following hardware components on the motherboard:

- CPU (486 or later)
- AT-compatible and MC146818 RTC-compatible chipset
- AT or PS/2-compatible Keyboard controller
- At least 1 MB of system RAM
- The power on self test (POST) of the BIOS initializes additional ROM BIOS extensions (Option ROMs) if they are accessible in the proper format. The following special requirements pertain to such adapter ROMs:
  - The code must reside in the address space between C0000H and F0000H.
  - The code must reside on a 2K boundary.
  - The first two bytes of the code must be 55H and AAH.
  - The third byte must contain the number of 512-byte blocks.
  - The fourth byte must contain a jump to the start of the initialization code.
  - The code must checksum to zero (byte sum).

Note The address space from C0000h to C8000h is reserved for external video adapters (for example; EGA, VGA). Part of the address space from D0000h to E0000h is typically used by expanded memory (EMS).

Fixed Disk Drives

The PhoenixBIOS supports up to four fixed-disk drives. For each drive, the BIOS supports 39 pre-defined drive types (1 through 39) and four user-defined types (40 through 43). Table 1-2 shows the pre-defined drive types and their default values.

You can modify the user-defined drive type for each fixed disk listed in Setup by using the menus of the Setup program. This feature eliminates the need for customized software for non-standard drives.

Table 1-2. Fixed Disk Drive Values

Type	Cylinders	Heads	Sectors	Wrt Pre	Landing
1	306	4	17	128	305
2	615	4	17	300	615
3	615	6	17	300	615
4	940	4	17	512	940
5	940	6	17	512	940
6	615	4	17	-1	615
7	462	8	17	256	511
8	733	5	17	-1	733
9	900	15	17	-1	901
10	820	3	17	-1	820
11	855	5	17	-1	855
12	855	7	17	-1	855
13	306	8	17	128	319
14	733	7	17	-1	733
15	Reserved				
16	612	4	17	0	633
17	977	5	17	300	977
18	977	7	17	-1	977
19	1024	7	17	512	1023
20	733	5	17	300	732

Table 1-2. Fixed Disk Drive Values (Continued)

Type	Cylinders	Heads	Sectors	Wrt Pre	Landing
21	733	7	17	300	732
22	733	5	17	300	733
23	306	4	17	0	336
24	612	4	17	305	663
25	612	2	17	300	612
26	614	4	17	-1	614
27	820	6	17	-1	820
28	977	5	17	-1	977
29	1218	15	36	-1	1218
30	1224	15	17	-1	1224
31	823	10	17	512	823
32	809	6	17	128	809
33	830	7	17	-1	830
34	830	10	17	-1	830
35	1024	5	17	-1	1024
36	1024	8	17	-1	1024
37	615	8	17	128	615
38	1024	8	26	-1	1024
39	925	9	17	-1	925
40	User Defined				
41	User Defined				
42	User Defined				
43	User Defined				

PhoenixBIOS Function Keys

PhoenixBIOS uses the following special function keys (Table 1-3):

Table 1-3. PhoenixBIOS special function keys

Key	Function
<F2>	Enter the Setup program during POST
<Esc>	Launch the Boot First menu
Ctrl-Alt-<->	Switch to slow CPU speed
Ctrl-Alt-<+>	Switch to fast CPU speed

BIOS Setup 2

Using the Phoenix Setup Program

This section describes the CPV5300 menu-driven PhoenixBIOS Setup program. This program lets you specify changes in the computer hardware (for example; add a new diskette drive) and optimize system performance. Setup maximizes your control over your system's features and performance.

With the PhoenixBIOS setup program, you can modify BIOS settings and control the special features of your CPV5300 Single Board Computer. The setup program uses a number of menus for making changes and turning special features on or off.

Note The menus shown in this chapter were in effect when the manual was printed. The actual menus displayed on your screen may be different and depend on the features and hardware installed in your computer.

Starting Setup

The PhoenixBIOS setup utility starts when you turn on or reboot your computer. It checks and configures the system through a power-on self test (POST). During POST, the following message appears at the bottom of the screen:

```
Press <F2> to enter SETUP
```

To start the PhoenixBIOS setup utility, press <F2>.

The BIOS Setup Utility starts and displays the Main Menu.

Note If POST finishes before you respond and you still want to enter Setup, restart the computer and try again.

2

The Setup Interface

The Setup program uses a menu-driven interface. Each Setup screen has a menu bar, a legend bar, and a field-specific help window as shown in Figure 2-1. An options window is also available for each field with predefined values.

Note When the “CPU Speed” is 333MHz the BIOS reports the “CPU Type” as “Celeron”. The BIOS should report the “CPU Type” as “Pentium II”.

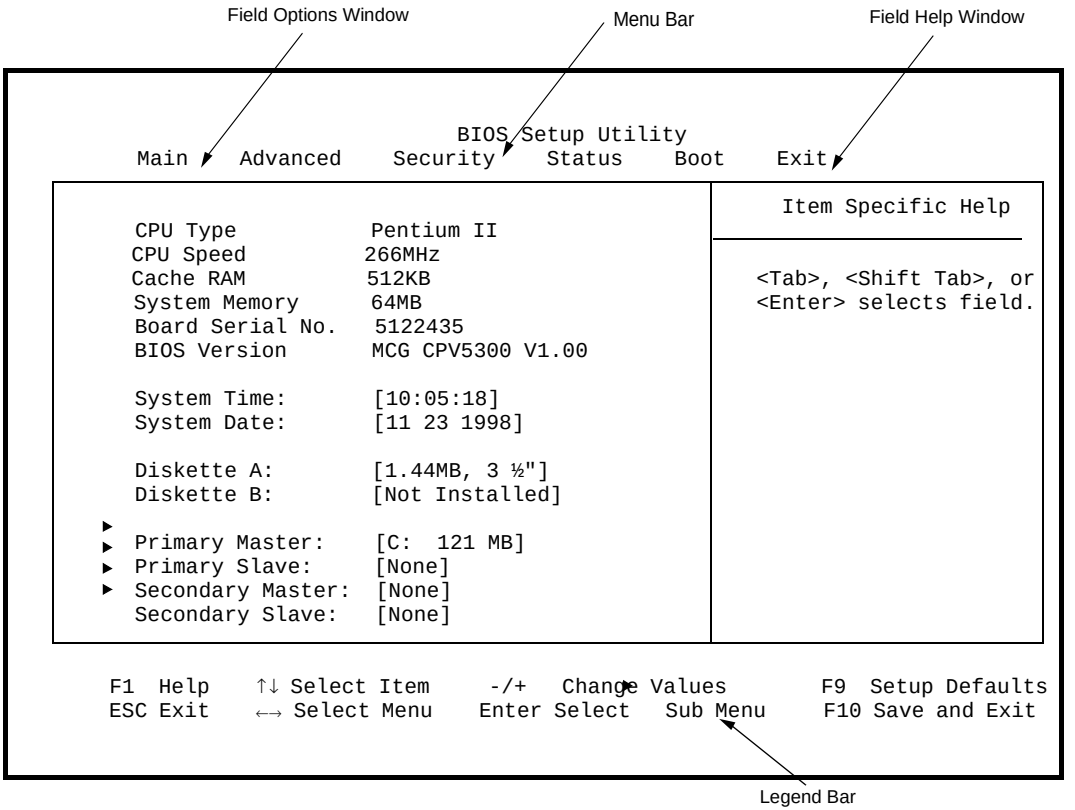


Figure 2-1. The basic setup screen

See Table 2-1 for a description of the fields on this menu.

The Menu Bar

The Menu Bar at the top of the window lists these selections. Refer to Table 2-1

Table 2-1. PhoenixBIOS Main Menu Bar

Use this menu bar selection:	For:
Main	basic system configuration
Advanced	setting the advanced features available on your system's chipset
Security	setting user and supervisor passwords and the backup and virus-check reminders
Status	viewing system temperature and power supply status
Boot	configuring system boot options
Exit	exiting the current menu/setup utility

Use the left/right arrow keys to make a selection.

See the section below, "exiting setup", for information about exiting the main menu.

The Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. Table 2-2 describes the legend keys and their alternates.

Table 2-2. Legend Bar

Use this key:	To:
<F1> or <Alt-H>	get general help
<Esc>	exit this menu
← or → arrow keys	select a different menu
↑ or ↓ arrow keys	move the cursor up and down
<Tab> or <Shift-Tab>	cycle the cursor up and down

Table 2-2. Legend Bar

Use this key:	To:
<Home> or <End>	move the cursor to the top or bottom of the window
<PgUp> or <PgDn>	move the cursor to the next or previous page
<F5> or <->	select the previous value for the field
<F6> or <+> or <Space>	select the next value for the field
<F9>	load the default configuration values for this menu
<F10>	save and exit
<Enter>	execute a command or select > a submenu
<Alt-R>	refresh the screen

To select an item, use the arrow keys to move the cursor to the field you want. Then use the plus and minus value keys to select a value for that field. The Save Value commands in the Exit Menu save the values currently displayed in all the menus.

To display a sub menu, use the arrow keys to move the cursor to the sub menu you want. Then press <Enter>. A pointer marks all sub menus.

The Field Help Window

The help window on the right side of each menu displays the help text for the currently selected field. It updates as you move the cursor to each field.

The General Help Window

Pressing <F1> or <Alt-H> on any menu brings up the General Help window that describes the legend keys and their alternates:

```
                        General Help

Setup changes system behavior by modifying the BIOS
configuration parameters.  Selecting incorrect values
may cause system boot failure; load Setup Default values
 to recover.

<Up/Down> arrows select fields in current menu.
<PgUp/PgDn> moves to previous/next page on scrollable menus.
<Home/End> moves to top/bottom item of current menu.

Within a field, <F5> or <-> selects next lower value and
<F6>, <+>, or <Space> selects next higher value.

<Left/Right> arrows select menus on menu bar.
<Enter> displays more options for items marked with a P.
<Enter> also displays an option list on some fields.

<F9> loads factory-installed Setup Default values.
<F10> restores previous values from CMOS.

<ESC> or <Alt-X> exits Setup; in sub-menus, pressing these
 keys returns to the previous menu.

<F1> or <Alt-H> displays General Help (this screen).
                                                          _


                        [Continue]
```

The scroll bar on the right of any window indicates that there is more than one page of information in the window. Refer to Table 2-3.

Table 2-3. Scroll bar selections

Use:	To:
<PgUp> and <PgDn>	display all the pages
<Home> and <End>	display the first and last page
<Enter>	display each page and then exit the window
<Esc>	to exit the current window

Main Menu Selections

You can make the following selections on the Main Menu itself. Refer to Table 2-4. Use the sub menus for other selections.

Table 2-4. Main Menu Selections

Feature	Options	Description
CPU Type	N/A	Displays the type of processor detected during bootup
CPU Speed	N/A	Displays the processor speed detected during bootup
Cache Ram	N/A	Displays the amount of level 2 cache detected during bootup
System Memory	N/A	Displays the amount of memory detected during bootup
Board Serial No.	N/A	Displays the serial number of the CPU board

Table 2-4. Main Menu Selections (Continued)

Feature	Options	Description
BIOS Version	N/A	Displays the BIOS version on the CPU board
System Time	HH:MM:SS	Sets the system time
System Date	MM/DD/YY	Sets the system date
Diskette A Diskette B	360KB, 5 1/4 inch 1.2MB, 5 1/4 inch 720 KB, 3 1/2 inch 1.44/1.25 MB, 3 1/2 inch 2.88 MB, 3 1/2 inch Not installed Disabled	Select the type of floppy-disk drive installed in your system. 1.25 MB is a Japanese media format that requires a 3 1/2 inch, 3-mode diskette drive.

You can set the boot sequence of the bootable drives by selecting Boot Sequence on the Main Menu or opening the Boot Menu.

Masters and Slaves

The master and slave settings on the Main Menu control these types of devices:

- hard-disk drives
- removable-disk drives
- CD-ROM drives

PhoenixBIOS supports up to two IDE disk adapters, called primary and secondary adapters. Each adapter supports one master drive and one optional slave drive in these possible combinations:

- 1 Master
- 1 Master, 1 Slave
- 2 Masters

- 2 Masters, 1 Slave
- 2 Masters, 2 Slaves

There is one IDE connector for each adapter on your machine, usually labelled “Primary IDE” and “Secondary IDE”. There are usually two connectors on each ribbon cable attached to each IDE connector. When you connect two drives to these connectors, the one on the end of the cable is the Master.

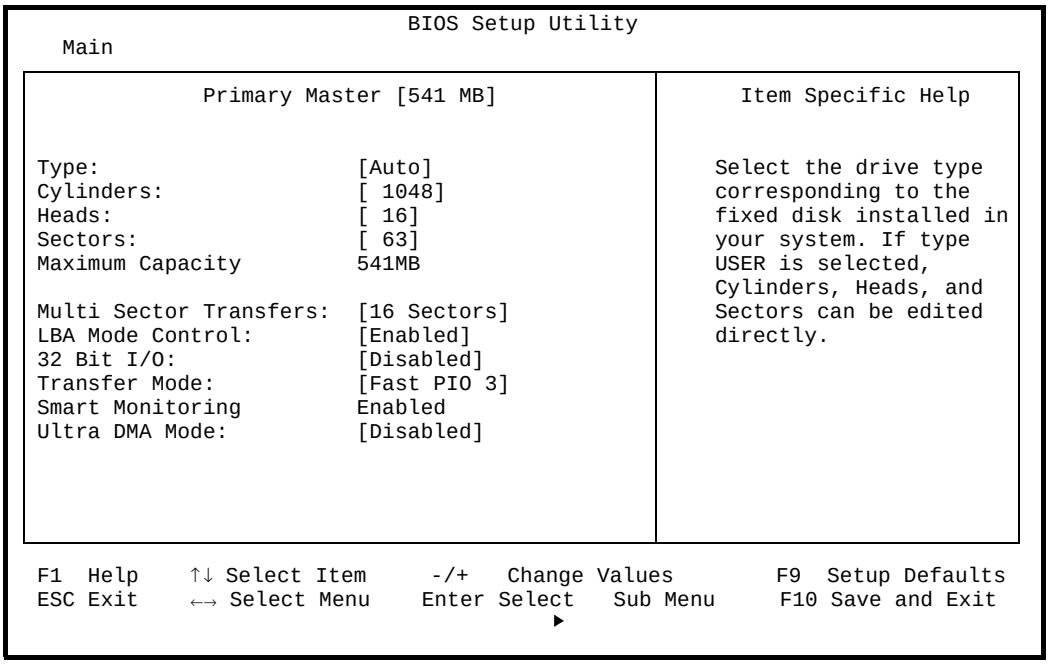
When you enter Setup, the Main Menu displays the results of Autotyping. Autotyping is the information each drive provides about its own size and other characteristics-and how they are arranged as Masters or Slaves on your machine.

Note Do not attempt to change these settings unless you have an installed drive that does not autotype properly (such as an older hard-disk drive that does not support autotyping).

If you need to change your drive settings, use one of the Master or Slave sub-menu as explained in the following.

Advanced Hard Disk Features

Selecting one of the Master or Slave sub-menus on the Main Menu displays a menu like this:



Use the legend keys listed on the bottom to make your selections and exit to the Main Menu.

Refer to Table 2-5 to configure the hard disk drive with Advanced Hard Disk Features:

Table 2-5. Features for Hard Disk Configuration

Feature	Options	Description
Type	None 1 to 39 User Auto IDE Removable CD-ROM ATAPI Removable	None = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed. 1 to 39 = fills in all remaining fields with values for predefined hard-disk type
Cylinders	1 to 65,536	Number of cylinders
Heads	1 to 16	Number of read/write heads
Sectors/Track	1 to 63	Numbers of sectors per track
Multi-Sector Transfers	Disabled Standard 2 sectors 4 sectors 8 sectors 16 sectors	Any selection except Disabled determines the number of sectors transferred per block. Standard is 1 sector per block.
LBA Mode Control	Enabled Disabled	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads and Sectors.

Table 2-5. Features for Hard Disk Configuration (Continued)

Feature	Options	Description
32-bit I/O	Enabled Disabled	Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus.
Transfer Mode	Standard Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4	Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.
Smart Monitoring	N/A	Displays whether or not SMART monitoring has been enabled for the drive.
Ultra DMA Mode	Disabled Mode 0 Mode 1 Mode 2	Selects the DMA method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.

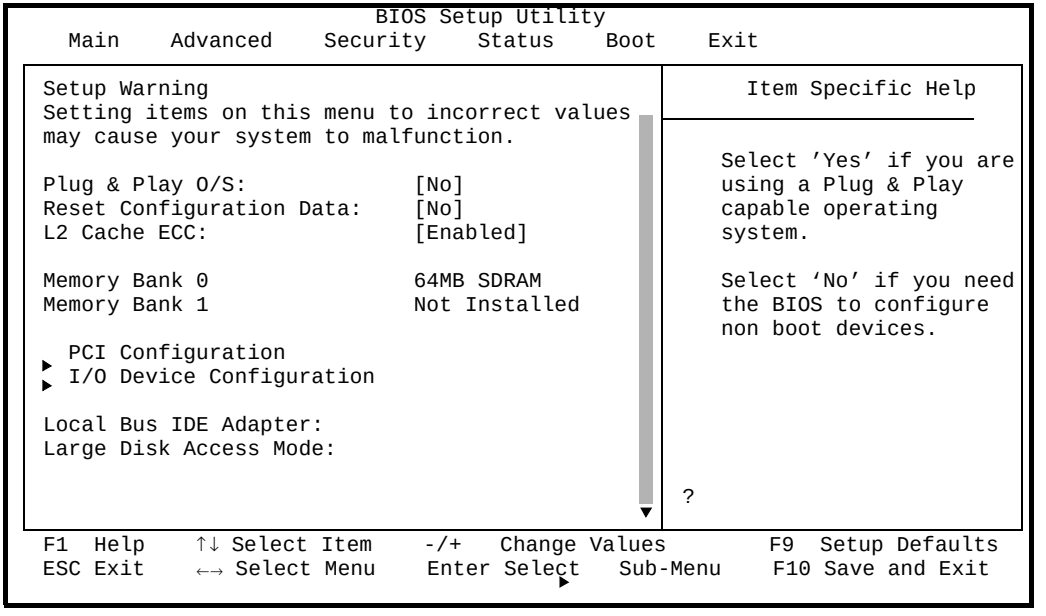
Warning

Incorrect settings can cause your system to malfunction.

2

The Advanced Menu

Select “Advanced” from the menu bar on the Main Menu to display this menu:



Use the legend keys to make your selections and exit to the Main Menu. Refer to Table 2-6 to make your selection.

Table 2-6. Advanced Menu Selections

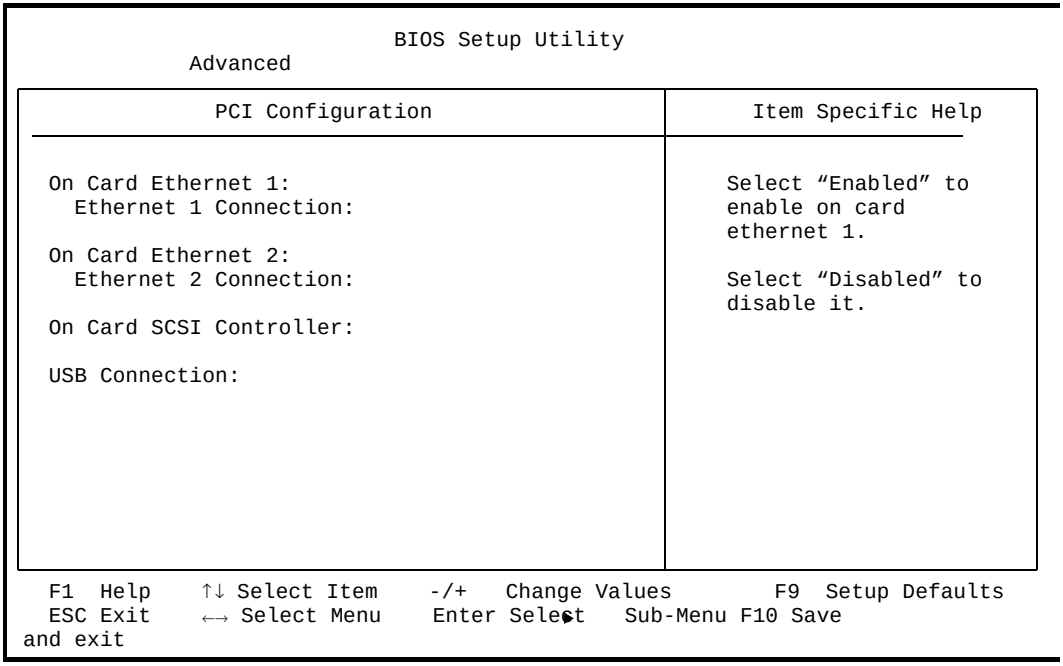
Feature	Options	Description
Plug and Play OS	Yes or No	If your system has a Plug and Play Operating System, Yes lets the Operating System configure Plug and Play devices not required for boot. No makes the BIOS configure them.
Reset Configuration Data	Yes or No	Yes erases all configuration data in ESCD, which stores the configuration settings for non-PnP plug-in devices. Select Yes when required to restore the manufacturer's defaults.
L2 Cache ECC	Enabled Disabled	Yes configures error correction of the L2 cache. No disables it.
Memory Bank 0 / Memory Bank 1	N/A	Displays the size and type of memory installed in CPU board

Table 2-6. Advanced Menu Selections (Continued)

Feature	Options	Description
Local Bus IDE	Both Primary Secondary Disabled	Configures the on-board IDE controllers. 'Both' enables both the primary and secondary controllers. 'Primary' enables only the primary controller. 'Secondary' enables only the secondary controller. 'Disabled' disables both controllers.
Large Disk Access Mode	DOS Other	Select DOS if you have DOS. Select Other if you have another operating system such as UNIX. A large disk is one that has more than 1024 cylinders, more than 16 heads, or more than 63 tracks per sector.
Legacy USB Support	Enabled Disabled	Select Enabled if you are using a USB keyboard or mouse. Select Disabled if you are not using a USB keyboard or mouse.
Serial Console	Enabled Disabled	'Enabled' allows all screen output to be sent to COM1 during the boot process. HOSTKEY.EXE can be used on another system to remotely view the boot and modify the setup. Select 'Disabled' if you are not using HOSTKEY.EXE.

PCI Configuration Menu

If the system has a PCI bus, select “PCI Configuration” from the menu bar on the Advanced menu, to display:



PCI Devices are devices equipped for operation with a PCI (Peripheral Component Interconnect) bus, a standardized hardware system that connects the CPU with other devices. Use this menu to configure the PCI devices installed on your CPU card.

Use the legend keys to make your selections and exit to the Advanced menu.

Refer to Table 2-7 when configuring the PCI devices:

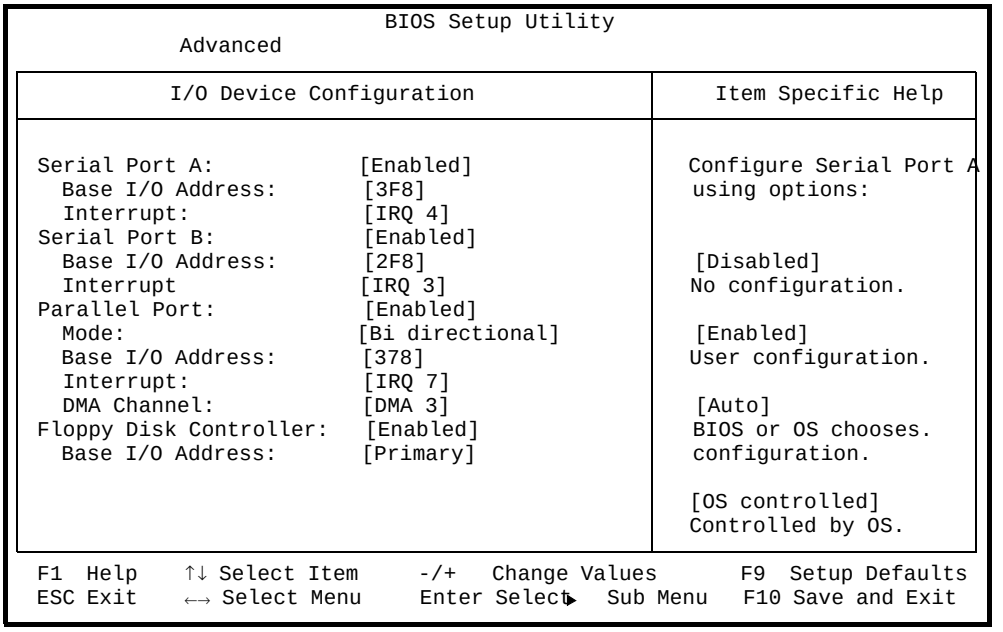
Table 2-7. Features for Configuring PCI Devices

Features	Options	Descriptions
On-Card Ethernet 1	Enabled or Disabled	'Enabled' enables the device and allows the BIOS or the operating system to configure and use it. 'Disabled' disables the device so that it is not accessible by the BIOS or operating system.
Ethernet 1 Connection	Front or Rear	'Front' connects the ethernet signals to the front panel of the CPU board. 'Rear' connects the ethernet signals to the connector on the rear transition module (if used).
On-Card Ethernet 2	Enabled or Disabled	'Enabled' enables the device and allows the BIOS or the operating system to configure and use it. 'Disabled' disables the device so that it is not accessible by the BIOS or operating system.
Ethernet 2 Connection	Front or Rear	'Front' connects the ethernet signals to the front panel of the CPU board. 'Rear' connects the ethernet signals to the connector on the rear transition module (if used).
On-Card SCSI Controller	Enabled or Disabled	'Enabled' enables the device and allows the BIOS or the operating system to configure and use it. 'Disabled' disables the device so that it is not accessible by the BIOS or operating system.
USB Connection	Front or Rear	'Front' connects the USB signals to the front panel of the CPU board. 'Rear' connects the USB signals to the connector on the rear transition module (if used).

2

I/O Device Configuration Menu

Select "I/O Device Configuration" on the Advanced Menu to display this menu and specify how you want to configure the Ultra-I/O Devices on the CPV5300.



Use the legend keys to make your selections and exit to the Main Menu.

Refer to Table 2-8 for information about how to configure the Input/Output settings.

Table 2-8. Configuring Ultra-I/O Devices on the CPV5300

Feature	Options	Description
Serial port A: Serial port B:	Disabled Enabled Auto OS Controlled	Disabled turns off the port. Enabled requires you to enter the base Input/Output address and the Interrupt number on the next line. Auto makes the BIOS configure the port automatically during POST. OS Controlled lets the PnP Operating System (such as Windows 95) configure the port after POST.
Base I/O Address/IRQ	3F8, IRQ 4 2F8, IRQ 3	If you select Enabled, choose one of these combinations.
Parallel Port	Disabled Enabled Auto OS Controlled	Disabled turns off the port. Enabled requires you to enter the base Input/Output address and the Interrupt number below. Auto makes the BIOS autoconfigure the port during POST. OS Controlled lets the PnP Operating System (such as Windows 95) configure the port after POST.
Mode	Output only Bi-directional	Output only is standard one-way protocol for a parallel device. Bi-directional uses two-way protocol of an Extended Capabilities Port (ECP).

Table 2-8. Configuring Ultra-I/O Devices on the CPV5300 (Continued)

Feature	Options	Description
Base I/O Address	378 278 3BC	If you select Enabled for the Parallel Port, choose one of these I/O addresses.
Interrupts	IRQ5 IRQ7	If you select Enabled for the Parallel Port, choose one of these interrupt options.
Floppy Disk Controller	Disabled Enabled	Enables the on-board diskette controller. Disabled turns off all diskette drives.
Base I/O Address	Primary Secondary	If you select Enabled for the Diskette Controller, choose Primary for one diskette drive installed or Secondary for two diskette drives installed.

Use this menu to specify how the I/O (Input and Output) ports are configured:

- ❏ manually
- ❏ automatically by the BIOS during POST
- ❏ automatically by a PnP Operating System such as Windows 95 after the Operating System boots.

Note

Note: If you choose the same I/O address or Interrupt for more than one port, the menu displays an asterisk (*) at the conflicting settings. It also displays this message at the bottom of the menu:

* Indicates a DMA, Interrupt, I/O or memory resource conflict with another device.

Resolve the conflict by selecting another setting for the devices.

The Security Menu

Selecting "Security" from the Main Menu displays a menu like this:

```
                        BIOS Setup Utility
  Main    Advanced    Security    Status    Boot    Exit

                                                Item Specific Help

User Password Is:           Set
Supervisor Password Is:     Set                 User password controls
                                                access to system at
Set User Passowrd           [Enter]             boot.
Set Supervisor Password     [Enter]

Clear User Password         [Enter]

Password On Boot:           [Disabled]

F1  Help    ↑↓ Select Item    -/+   Change Values        F9  Setup Defaults
ESC Exit    ←→ Select Menu    Enter Select   Sub-Menu     F10 Save and Exit
```

Use the legend keys to make your selections and exit to the Main Menu.

Enabling "Supervisor Password" requires a password for entering Setup. The passwords are not case sensitive.

Press <Enter> at either Set Supervisor Password or Set User Password to display a dialog box like this:

```
                Set Password

   Enter new password:  [        ]
  Confirm new password: [        ]
                Enter:Accept
```

Type the password and press <Enter>. Repeat.

Note: The User and Supervisor passwords are related. You cannot have a User password without first creating a Supervisor password.

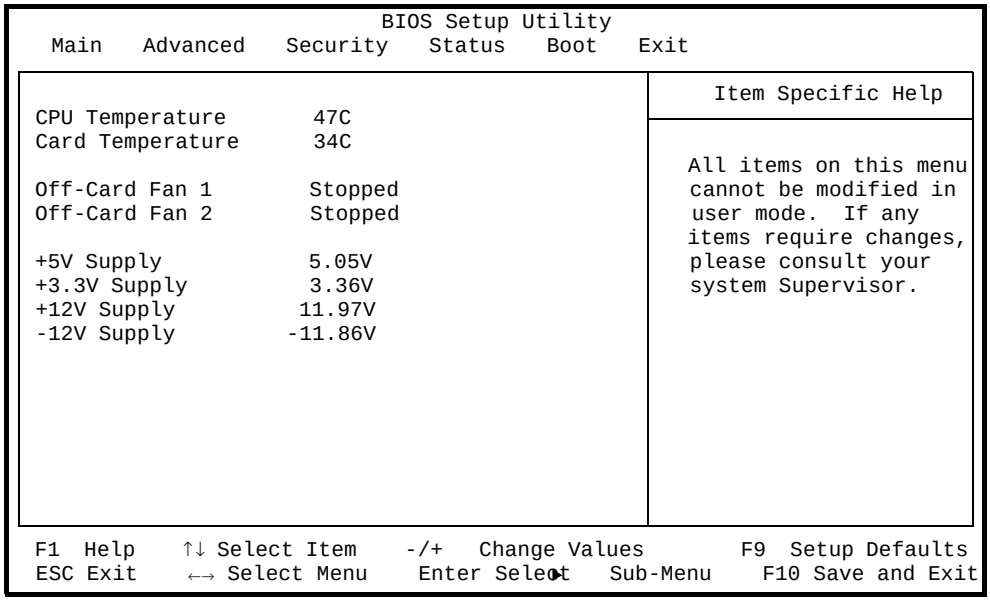
Refer to Table 2-9 to configure the system-security options.

Table 2-9. Configuring the System-Security Options

Feature	Options	Description
User Password Is	N/A	Displays whether or not the user password is set.
Supervisor Password Is	N/A	Displays whether or not the supervisor password is set
Set User Password	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives restricted access to SETUP menus.
Set Supervisor Password	Up to seven alphanumeric characters	Pressing <Enter> displays dialog box for entering the supervisor password. In related systems, this password gives full access to Setup menus.
Password on boot	Enabled Disabled	Enabled requires a password on boot. Requires prior setting of the Supervisor password. If supervisor password is set and this option disabled, BIOS assumes user is booting. Users may not boot from a floppy diskette.

Status Menu

Selecting "Status" from the Main Menu displays this menu:



Note You cannot change items on the status menu. They display as information only.

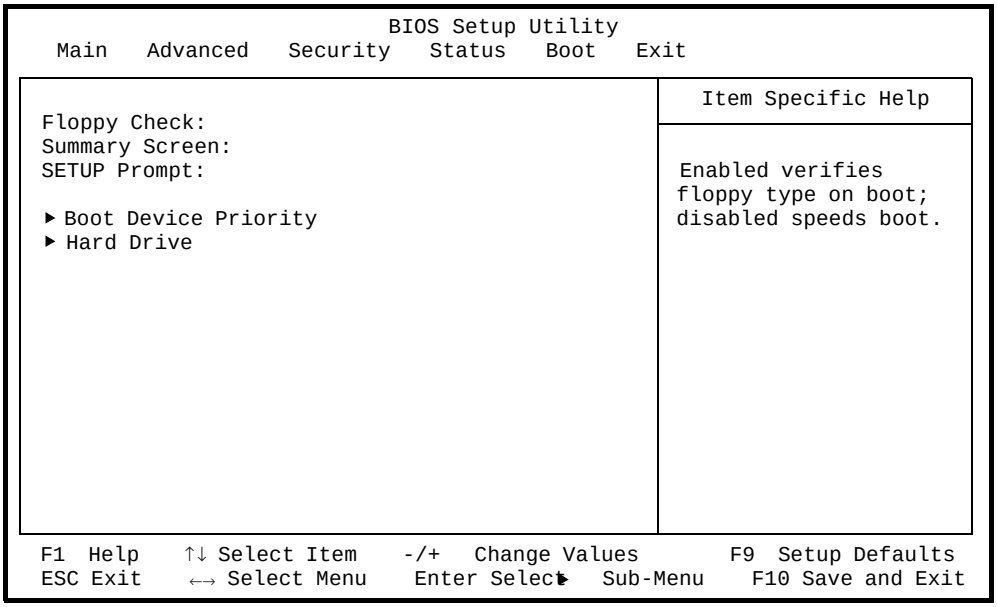
Refer to Table 2-10 for information about the Status Menu.

Table 2-10. Checking the Status Menu

Feature	Options	Description
CPU Temperature	N/A	Displays die temperature of the processor chip.
Card Temperature	N/A	Displays the temperature of the CPU card.
Off-Card Fan 1/ Off-Card Fan 2	N/A	Displays the speeds of any off-card fans that interface to the CPU card's tachometer inputs.
+5V Supply +3.3V Supply +12V Supply -12V Supply	N/A	Displays the voltages delivered to the CPU card from the system power supply.

Boot Menu

Selecting "Boot Menu" on the Main Menu displays the Boot Options menu.



Use the legend keys to make your selections and exit to the Main Menu.

Refer to Table 2-11 to select your boot options.

Table 2-11. Selecting the Boot Options

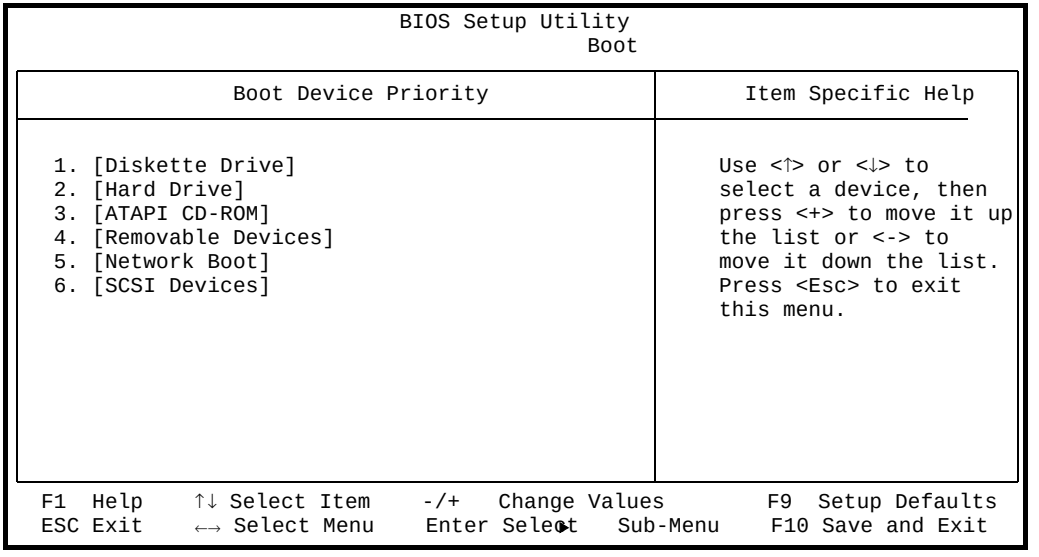
Features	Options	Description
Floppy Check	Enabled or Disabled	Seeks diskette drives during bootup. Disabling speeds boot time.
Summary Screen	Enabled or Disabled	Displays system summary screen during bootup.
POST errors	Enabled or Disabled	Displays "Press <F2> for Setup" during bootup.

Boot Device Priority

After you turn on your computer, it attempts to load the operating system (such as Windows 95) from the drive of your choice. If it cannot find the operating system on that drive, it attempts to load it from one or more other drives in the order specified in the Boot Device Priority Menu.

Note Specifying any drive as a boot drive on the Boot Menu requires the installation of an operating system on that drive. Using a drive as a potable drive may require you to install the operating system.

If you select "Boot Device Priority" the Boot Menu displays this menu:

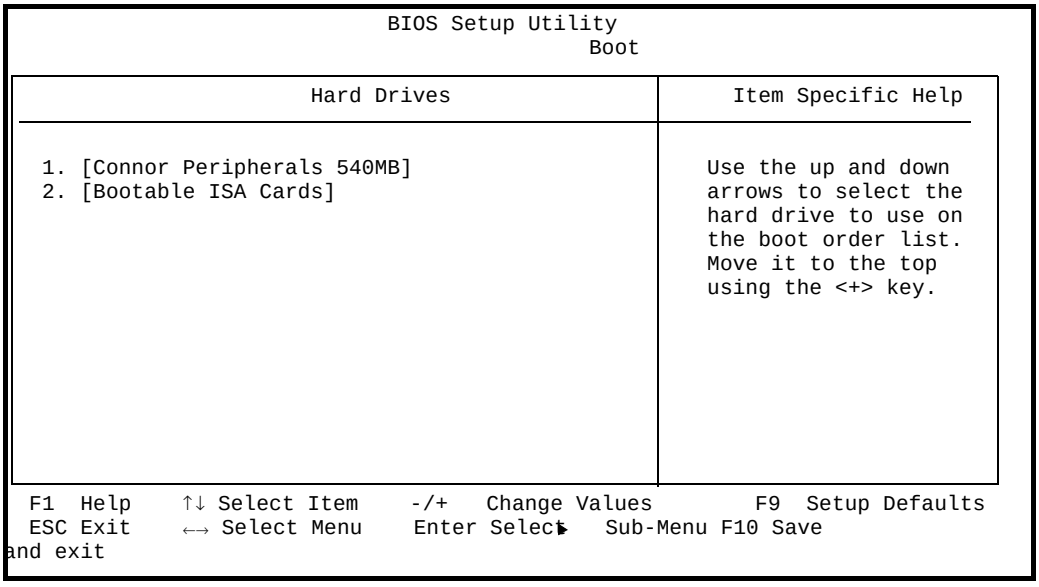


You can arrange the boot order list on this menu to specify the order of the devices from which the BIOS attempts to boot the Operating System. To move a device, first select it with the up-or-down arrows, and move it up or down using the <+> and <-> keys.

Note If you have more than one hard drive, use the Hard Disk sub menu to specify which one to use on the boot order list, as described in the following pages.

Hard Drive

If you have more than one hard drive, selecting "Hard Drive" from the Boot Menu displays a menu like this:

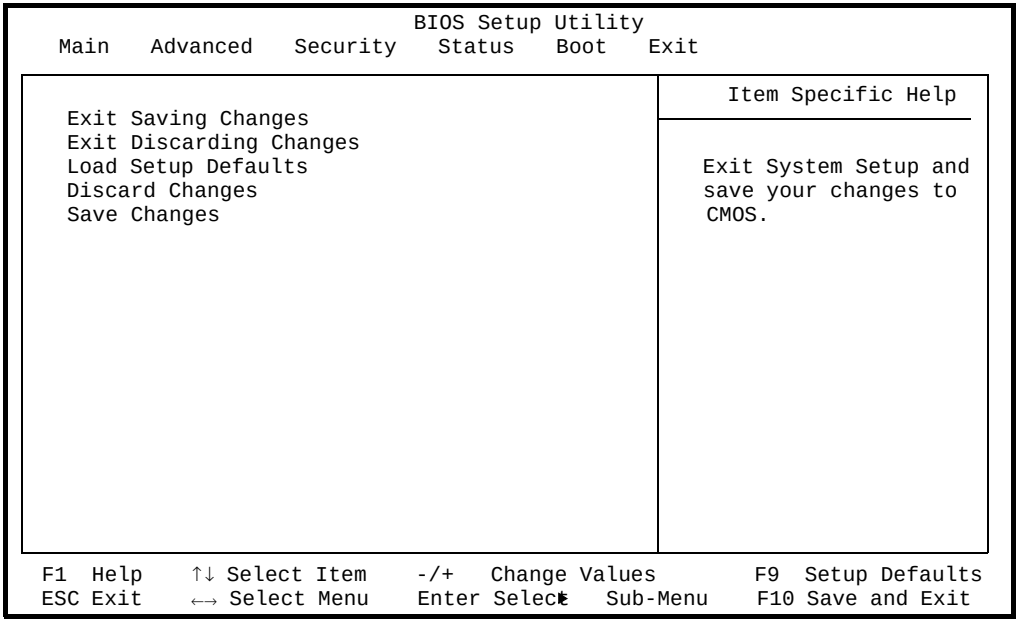


Select the hard drive to use for booting by using the up-and-down arrows. Then move it to the top of this list using the <+> key.

2

Exit Menu

Select "Exit" from the menu bar to display this menu:



The following sections describe each of the options on this menu. Note that <Esc> does not exit this menu. You must select one of the items from the menu or menu bar to exit.

Saving Values

After making your selections on the Setup menus, always select either "Saving Values" or "Save Changes." Both procedures store the selections displayed in the menus in CMOS (short for "battery-backed CMOS RAM"), a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS.

After you save your selections, the program displays this message:

```
Values have been saved to CMOS!
```

Press <space> to continue

If you attempt to exit without saving, the program asks if you want to save before exiting.

During bootup, PhoenixBIOS attempts to load the values saved in CMOS. If those values cause the system boot to fail, reboot and press <F2> to enter Setup. In Setup, you can get the Default Values (as described below) or try to change the selections that caused the boot to fail.

Exit Discarding Changes

Use this option to exit Setup without storing in CMOS any new selections you may have made. The selections previously in effect remain in effect.

Load Setup Defaults

To display the default values for all the Setup menus, select “Load Setup Defaults” from the Main Menu. The program displays this message:

```
ROM Default values have been loaded!
```

Press <space> to continue

If, during bootup, the BIOS program detects a problem in the integrity of values stored in CMOS, it displays these messages:

```
System CMOS checksum bad - run SETUP
Press <F1> to resume,  <F2> to Setup
```

The CMOS values are corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS.

Press **<F1>** to resume the boot or **<F2>** to run Setup with the ROM default values already loaded into the menus. You can make other changes before saving the values to CMOS.

Discard Changes

If, during a Setup Session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you previously saved to CMOS.

Selecting “Discard Changes” on the Exit menu updates all the selections and displays this message:

```
CMOS values have been loaded!
    Press <space> to continue
```

Save Changes

Select “Save Changes” to save all the selections without exiting Setup. You can return to the other menus if you want to review and change your selections.

PhoenixBIOS Messages

Refer to Table 3-1 for a list of messages that the BIOS can display. The table also includes explanations of the messages and remedies for reported problems. Most of them occur during POST. Some of them display information about a hardware device (for example; the amount of memory installed). Others may indicate a problem with a device, such as the way it is configured.

If your system displays one of the messages marked with an asterisk (*), write down the message and contact your dealer. If your system fails after you make changes in the Setup menus:

- reset the computer
- enter Setup
- install Setup defaults or correct the error

Table 3-1. PhoenixBIOS Messages

This message:	Means:
0200 Failure Fixed Disk	Fixed disk is not working or not configured properly. Check to see if fixed disk is attached properly. Run Setup. Find out if the fixed-disk is correctly identified.
0210 Stuck key	Stuck key on keyboard
0211 Keyboard error	Keyboard not working
*0212 Keyboard Controller Failed	Keyboard controller failed test. May require replacing keyboard controller.
0213 Keyboard locked - Unlock key switch	Unlock the system to proceed
0220 Monitor type does not match CMOS - Run SETUP	Monitor type not correctly identified in Setup
*0230 Shadow RAM Failed at offset: nnnn	Shadow RAM failed at offset nnnn of the 64k block at which the error was detected
*0231 System RAM Failed at offset: nnnn	System RAM failed at offset nnnn of the 64k block at which the error was detected.
*0232 Extended RAM Failed at offset: nnnn	Extended memory not working or not configured properly at offset nnnn
0250 System battery is dead - Replace and run SETUP	The CMOS clock battery indicator shows the battery is dead. Replace the battery and run Setup to reconfigure the system.
0251 System CMOS checksum bad - Default configuration used	System CMOS is corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS. The BIOS installed Default Setup Values. If you do not want the BIOS installed Default Setup Values, enter Setup and enter your own values. If the error persists, check the system battery or contact your dealer.
*0260 System timer error	The timer test failed. Requires repair of system board.

Table 3-1. PhoenixBIOS Messages (Continued)

This message:	Means:
*0270 Real time clock error	Real-time clock fails BIOS test. May require setting legal date (1991-2099). May require board repair.
0271 Check date and time settings	May require setting legal date (1991-2099).
0280 Previous boot incomplete - Default configuration used	Previous POST did not complete successfully. POST loads default values and offers to run Setup. If the failure was caused by incorrect values and they are not corrected, the next boot will likely fail. On systems with control of **wait states**, improper Setup settings can also terminate POST and cause this error on the next boot. Run Setup and verify that the wait-state configuration is correct. This error clears the next time the system boots.
0281 Memory Size found by POST differed from CMOS	Memory size found by POST differed from CMOS
02B0 Diskette drive A error 02B1 Diskette drive B error	Drive A: or B: is present but fails the BIOS POST diskette tests. Check to see that the drive is defined with the proper diskette type in Setup and that the diskette drive is attached correctly.
02B2 Incorrect Drive A type - run SETUP	Type of floppy drive A: not correctly identified in Setup
02B3 Incorrect Drive B type - run SETUP	Type of floppy drive B: not correctly identified in Setup
02D0 System cache error - Cache disabled	RAM cache failed and BIOS disabled the cache. On older boards, check the cache jumpers. You may have to replace the cache. See your dealer. A disabled cache slows system performance considerably.
02F0: CPU ID:	CPU socket number for Multi-Processor error.

Table 3-1. PhoenixBIOS Messages (Continued)

This message:	Means:
*02F4: EISA CMOS not writeable	ServerBIOS2 test error: Cannot write to EISA CMOS.
*02F5: DMA Test Failed	ServerBIOS2 test error: Cannot write to extended DMA (Direct Memory Access) registers
*02F6: Software NMI Failed	ServerBIOS2 test error: Cannot generate software NMI (Non-Maskable Interrupt)
*02F7: Fail-Safe Timer NMI Failed	ServerBIOS2 test error: Fail-Safe Timer takes too long
device Address Conflict	Address conflict for specified device
Allocation Error for: device	Run ISA or EISA Configuration Utility to resolve resource conflict for the specified device
CD ROM Drive	CD ROM Drive identified
Entering SETUP	Starting Setup program
*Failing Bits: nnnn	The hex number nnnn is a map of the bits at the RAM address which failed the memory test. Each 1 (one) in the map indicates a failed bit. See errors 230, 231, or 232 above for offset address of the failure in System, Extended, or Shadow memory.
Fixed Disk n	Fixed disk n (0-3) identified
Invalid System Configuration Data	Problem with NVRAM (CMOS) data
I/O device IRQ conflict	I/O device IRQ conflict error
PS/2 Mouse Boot Summary Screen:	PS/2 Mouse installed
nnnn kB Extended RAM Passed	Where nnnn is the amount of RAM in kilobytes successfully tested
nnnn Cache SRAM Passed	Where nnnn is the amount of system cache in kilobytes successfully tested

Table 3-1. PhoenixBIOS Messages (Continued)

This message:	Means:
nnnn kB Shadow RAM Passed	Where nnnn is the amount of shadow RAM in kilobytes successfully tested
nnnn kB System RAM Passed	Where nnnn is the amount of system RAM in kilobytes successfully tested
One or more I20 Block Storage Devices were excluded from the Setup Boot Menu	There was not enough room in the IPL table to display all installed I_2O block-storage devices
Operating system not found	Operating system cannot be located on either drive A: or drive C:. Enter Setup and see if fixed disk and drive A: are properly identified.
*Parity Check 1 nnnn	Parity error found in the system bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays **????**. Parity is a method for checking errors in binary data. A parity error indicates that some data is corrupted.
*Parity Check 2 nnnn	Parity error found in the I/O bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays **????**.
Press <F1> to resume, <F2> to Setup, <F3> for previous	Displayed after any recoverable error message. Press <F1> to start the boot process or <F2> to enter Setup and change the settings. Press <F3> to display the previous screen (usually an initialization error of an **Option ROM (**i.e., an add-on card). Write down and follow the information shown on the screen.
Press <F2> to enter Setup	Optional message displayed during POST. Can be turned off in Setup.
PS/2 Mouse:	PS/2 mouse identified.

Table 3-1. PhoenixBIOS Messages (Continued)

This message:	Means:
Run the I20 Configuration Utility	One or more unclaimed block storage devices has the Configuration Request bit set in the LCT. Run an I2O Configuration Utility (e.g. the SAC utility).
System BIOS shadowed	System BIOS copied to shadow RAM.
UMB upper limit segment address: nnnn	Displays the address nnnn of the upper limit of **Upper Memory Blocks** indicating released segments of the BIOS which can be reclaimed by a virtual memory manager
Video BIOS shadowed	Video BIOS successfully copied to shadow RAM

Power On Self-Tests

4

This chapter contains information to help you troubleshoot your system. It describes error reporting methods and beep codes.

The PhoenixBIOS runs a series of programs called the Power On Self-Tests (POST), which performs several tasks, including:

- a Random Access Memory (RAM) test
- inventory of the hardware devices installed in the computer
- configuration of hard and floppy disks, keyboard, monitor, and serial and parallel ports
- configuration of other devices installed in the computer such as CD-ROM drives and sound cards
- initialization of computer hardware required for computer features such as “Plug and Play” and “Power Management”
- Run Setup if requested
- Load and run the operating system such as DOS, OS/2, UNIX or Windows NT

Recoverable Power On Self-Test (POST) Errors

When a recoverable error occurs during POST, PhoenixBIOS displays an error message describing the problem.

PhoenixBIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (no card installed or faulty) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example; VGA) can also issue audible errors, usually consisting of one long tone followed by a series of short tones.

POST Terminal Errors

There are several POST routines that issue a POST Terminal Error and shut down the system if they fail. Before shutting down the system, the terminal-error handler:

1. issues a beep code signifying the test point error
2. writes the error to port 80h
3. attempts to initialize the video
4. writes the error in the upper left corner of the screen (using both mono and color adapters).

The routine derives the beep code from the test point error as follows:

1. The 8-bit error code is broken down to four 2-bit groups. Discard the most significant group if it is 00.
2. Each group is made one-based (1 through 4) by adding 1.
3. Short beeps generate for the number in each group.

Example:

Testpoint 01Ah = 00 01 10 10 = 1-2-3-3 beeps

Test Points and Beep Codes

At the beginning of each POST routine, the BIOS outputs the test point error code to I/O address 80h. Use this code during troubleshooting to establish at what point the system failed and what routine was performed.

Some motherboards have a seven-segment LED display that displays the current value of port 80h. For production boards which do not contain the LED display, you can purchase a card that performs the same function.

If the BIOS detects a terminal error condition, it:

1. issues a terminal error beep code
2. halts POST and attempts to display the error code on the upper left corner of the screen and on the port 80h LED display. It attempts

repeatedly to write the error to the screen. This may cause "hash" on some CGA displays.

If the system hangs before the BIOS can process the error, the value displayed at the port 80h is the last test performed. In this case, the screen does not display the error code.

Refer to Table 4-1 for a list of the checkpoint codes written at the start of each test and the beep codes issued for terminal errors.

Table 4-1. Checkpoint Codes and Beep Codes

Code	Beep	POST Routine Description
02h		Verify Real Mode
03h		Disable Non-Maskable Interrupt (NMI)
04h		Get CPU type
06h		Initialize system hardware
08h		Initialize chipset with initial POST values
09h		Set IN POST flag
0Ah		Initialize CPU registers
0Bh		Enable CPU cache
0Ch		Initialize caches to initial POST values
0Eh		Initialize I/O component
0Fh		Initialize the local bus IDE
10h		Initialize Power Management
11h		Load alternate registers with initial POST values
12h		Restore CPU control word during warm boot
13h		Initialize PCI Bus Mastering devices
14h		Initialize keyboard controller
16h	1-2-2-3	BIOS ROM checksum
17h		Initialize cache before memory Autosize
18h		8254 timer initialization
1Ah		8237 DMA controller initialization
1Ch		Reset Programmable Interrupt Controller
20h	1-3-1-1	Test DRAM refresh
22h	1-3-1-3	Test 8742 Keyboard Controller

Table 4-1. Checkpoint Codes and Beep Codes (Continued)

Code	Beep	POST Routine Description
24h		Set ES segment register to 4 GB
26h		Enable A20 line
28h		Autosize DRAM
29h		Initialize POST Memory Manager
2Ah		Clear 512 kB base RAM
2Ch	1-3-4-1	RAM failure on address line ***xxxx*** [1]
2Eh	1-3-4-3	RAM failure on data bits ***xxxx**** of low byte of memory bus [1]
2Fh		Enable cache before system BIOS shadow
30h	1-4-1-1	RAM failure on data bits ***xxxx**** of high byte of memory bus [1]
32h		Test CPU bus-clock frequency
33h		Initialize Phoenix Dispatch Manager
36h		Warm start shut down
38h		Shadow system BIOS ROM
3Ah		Autosize cache
3Ch		Advanced configuration of chipset registers
3Dh		Load alternate registers with CMOS values
42h		Initialize interrupt vectors
45h		POST device initialization
46h	2-1-2-3	Check ROM copyright notice
47h		Initialize I20 support
48h		Check video configuration against CMOS
49h		Initialize PCI bus and devices
4Ah		Initialize all video adapters in s
4Bh		QuietBoot start (optional)
4Ch		Shadow video BIOS ROM
4Eh		Display BIOS copyright notice
50h		Display CPU type and speed
51h		Initialize EISA board
52h		Test keyboard
54h		Set key click if enabled

Table 4-1. Checkpoint Codes and Beep Codes (Continued)

Code	Beep	POST Routine Description
58h	2-2-3-1	Test for unexpected interrupts
59h		Initialize POST display service
5Ah		Display prompt "Press F2 to enter SETUP"
5Bh		Disable CPU cache
5Ch		Test RAM between 512 and 640 kB
60h		Test extended memory
62h		Test extended memory address lines
64h		Jump to UserPatch1
66h		Configure advanced cache registers
67h		Initialize Multi Processor APIC
68h		Enable external and CPU caches
69h		Setup System Management Mode (SMM) area
6Ah		Display external L2 cache size
6Bh		Load custom defaults (optional)
6Ch		Display shadow-area message
6Eh		Display possible high address for UMB recovery
70h		Display error messages
72h		Check for configuration errors
76h		Check for keyboard errors
7Ch		Set up hardware interrupt vectors
7Eh		Initialize coprocessor if present
80h		Disable onboard Super I/O ports and IRQs
81h		Late POST device initialization
82h		Detect and install external RS232 ports
83h		Configure non-MCD IDE controllers
84h		Detect and install external parallel ports
85h		Initialize PC-compatible PnP ISA devices
86h		Re-initialize onboard I/O ports.
87h		Configure Motherboard Configurable Devices (optional)
88h		Initialize BIOS Data Area
89h		Enable Non-Maskable Interrupts (NMIs)

Table 4-1. Checkpoint Codes and Beep Codes (Continued)

Code	Beep	POST Routine Description
8Ah		Initialize Extended BIOS Data Area
8Bh		Test and initialize PS/2 mouse
8Ch		Initialize floppy controller
8Fh		Determine number of ATA drives (optional)
90h		Initialize hard-disk controllers
91h		Initialize local-bus hard-disk controllers
92h		Jump to UserPatch2
93h		Build MPTABLE for multi-processor boards
95h		Install CD ROM for boot
96h		Clear huge ES segment register
97h		Fixup Multi Processor table
98h	1-2	Search for option ROMs. One long, two short beeps on checksum failure
99h		Check for SMART Drive (optional)
9Ah		Shadow option ROMs
9Ch		Set up Power Management
9Dh		Initialize security engine (optional)
9Eh		Enable hardware interrupts
9Fh		Determine number of ATA and SCSI drives
A0h		Set time of day
A2h		Check key lock
A4h		Initialize typematic rate
A8h		Erase F2 prompt
AAh		Scan for F2 key stroke
ACh		Enter SETUP
AEh		Clear Boot flag
B0h		Check for errors
B2h		POST done - prepare to boot operating system
B4h	1	One short beep before boot
B5h		Terminate QuietBoot (optional
B6h		Check password (optional
B9		Prepare Boot

Table 4-1. Checkpoint Codes and Beep Codes (Continued)

Code	Beep	POST Routine Description
BAh		Initialize DMI parameters
BBh		Initialize PnP Option ROMs
BCh		Clear parity checkers
BDh		Display MultiBoot menu
BEh		Clear screen (optional)
BFh		Check virus and backup reminders
C0h		Try to boot with INT 19
C1h		Initialize POST Error Manager (PEM)
C2h		Initialize error logging
C3h		Initialize error display function
C4h		Initialize system error handler
C5h		PnPnd dual CMOS (optional)
C6h		Initialize note dock (optional)
C7h		Initialize note dock late
C8h		Force check (optional)
C9h		Extended checksum (optional)
D2h		Unknown interrupt
E0h		Initialize the chipset [2]
E1h		Initialize the bridge [2]
E2h		Initialize the CPU [2]
E3h		Initialize system timer [2]
E4h		Initialize system I/O [2]
E5h		Check force recovery boot [2]
E6h		Checksum BIOS ROM [2]
E7h		Go to BIOS [2]
E8h		Set Huge Segment [2]
E9h		Initialize Multi Processor [2]
EAh		Initialize OEM special code [2]
EBh		Initialize PIC and DMA [2]

Table 4-1. Checkpoint Codes and Beep Codes (Continued)

Code	Beep	POST Routine Description
ECh		Initialize Memory type [2]
EDh		Initialize Memory size [2]
EEh		Shadow Boot Block [2]
EFh		System memory test [2]
F0h		Initialize interrupt vectors [2]
F1h		Initialize Run Time Clock [2]
F2h		Initialize video [2]
F3h		Initialize System Management Manager [2]
F4h		Output one beep [2]
F5h		Boot to Mini DOS [2]
F6h		Clear Huge Segment [2]
F7h		Boot to Full DOS [2]

[1] If the BIOS detects error 2C, 2E or 30 (base 512K RAM error), it displays an additional word-bitmap (*xxxx)* indicating the address line or bits that failed. For example; "2C 0002" means address line 1 (bit one set) failed. "2E 1020 means data bits 12 and 5 (bits 12 and 5 set) failed in the lower 16 bits. Note that error 30 cannot occur on 386SX systems because they have a 16-bit bus rather than a 32-bit bus. The BIOS also sends the bitmap to the port-80 LED display. This sequence repeats continuously: check point code display, high-order byte and low-order byte.

[2] Used for boot block in Flash ROM

Functional Description 5

Introduction

This chapter gives you information about the:

- Peripheral Component Interconnect (PCI) bus
- watchdog timer
- I/O address map
- video and ultra SCSI controllers
- EIDE and floppy drive interfaces
- PLFPGA registers

Peripheral Component Interconnect (PCI) Local Bus

The PCI local bus is a high-performance, 32-bit bus with multiplexed address and data lines. It is intended for use as an interconnect mechanism between highly-integrated peripheral controller components, peripheral add-in boards and processor/memory systems.

The CPV5300 supports a 32-bit PCI interface on the physical CompactPCI connector. On-board devices connect directly to the primary bus. Off-board access is supported through the DEC 21150 PCI-PCI bridge. The PCI interface has a read or write bandwidth of at least 120Mb per second.

Watchdog Timer

The PLFPGA includes a two-level watchdog timer. The watchdog timer has four modes of operation:

1. disabled
2. set a flag in a register in ISA I/O memory map
3. item 2 + assert a selectable interrupt (ISA, NMI, SMI, SMALERT)
4. item 2 + assert NMI followed by a system Reset

The timer interfaces through the Watchdog Configuration (WDCFG) Register and Watchdog Strobe (WDSTB) port. You can program the watchdog timer via registers in the ISA I/O memory map. The watchdog timer is protected from accidental enabling. The timer supports a range of count down timeouts from 17.8 ms to 4.86 minutes.

Watchdog Timer Operation

You can enable/disable the watchdog timer and set the level 1 watchdog timeout for a delay of 17.8 ms to 291 seconds. You can also remotely monitor the system by generating a level 1 timeout. You cannot program the level 2 timer. It has a fixed period of 8.2 ms. Figure 5-1 shows a block diagram of the watchdog timer.

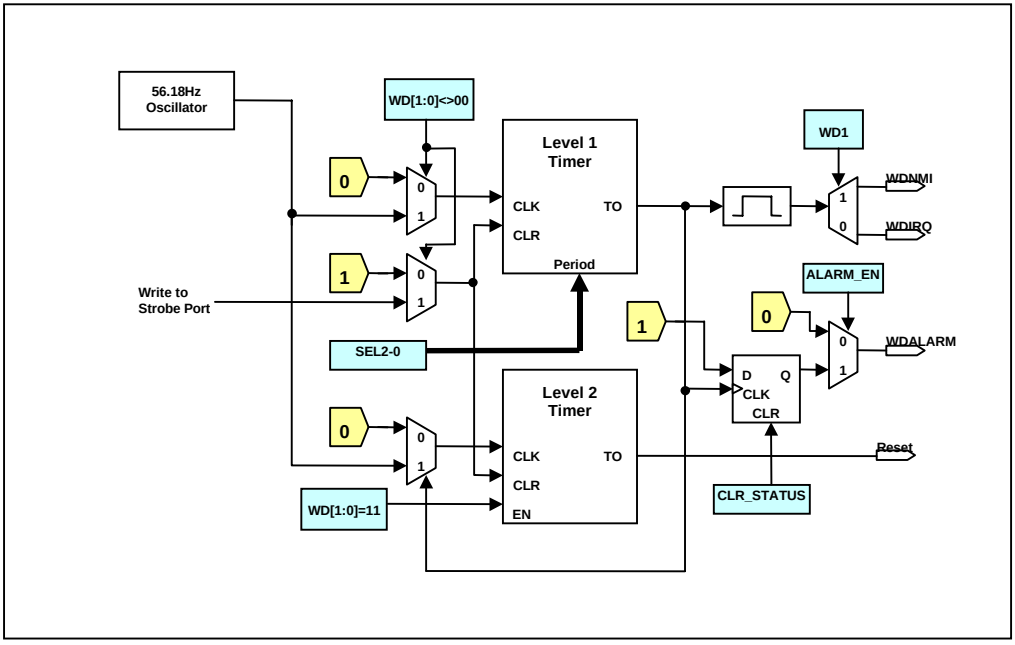


Figure 5-1. PLFPGA Watchdog Block Diagram

Enabling the timer

To enable the timer, you must initialize the WDCFG register with the timer period (SEL[2:0]) and mode (WD[1:0]). After initialization the level 1 timer begins to count down. If the level 1 timer reaches the period specified in the SEL bits in the WDCFG register, it times out and generates a system

event specified by the WD[1:0] bits. At timeout the system can generate an alarm signal (controlled by the ALARM_EN bit). It also enables the level 2 watchdog timer to begin counting down if WD[1:0] is set to 11.

If the level 2 timer enables it times out 8.4 milliseconds after the level 1 timer. At timeout of the level 2 timer a power-on type system reset generates. All FPGA registers reset to their power-on states with the exception of the watchdog timeout latch. The timeout latch can determine whether a watchdog timeout caused the system to reboot. You can view the value of the watchdog timeout latch by reading bit 2 of the watchdog strobe (WDSTB) port.

You can strobe the watchdog by writing to the WDSTB. When the watchdog strobes, both timers reset to their initial count; and the watchdog resets to its initial state of counting down the level 1 timer. Strobing affects the watchdog timeout latch and must be cleared separately.

I/O Address Map

PCI system memory and I/O are configured or enumerated dynamically each time the system boots or by an operating system (Plug and Play), but there are legacy I/O locations that remain constant.

Table 5-1 shows I/O addressing. Functions listed with (opt) are not normally occupied by on-board resources. BIOS Setup or special utilities may be used to enable or relocate these features from their default values.

Table 5-1. I/O Addresses

Address	Function
0000-000F	DMA Controller 1
0020-0021	Interrupt controller 1
0040-0043	Counter timer
0060-0064	Keyboard, NMI, speaker
0070-0071	Real time clock/NMI mask
0050-0057[1]	LM78 System monitor (opt)

Table 5-1. I/O Addresses (Continued)

Address	Function
0058-005F[1]	WatchDog timer, ENUM (opt)
0080-009F	DMA page register, POST checkpoint
00A0-00BF	Interrupt controller 2
00C0-00DF	DMA controller 2
00F0	Reset coprocessor
0170-0177[2]	Secondary IDE channel (opt)
01F0-01F7[2]	Primary IDE channel
0278-027F[3]	Parallel port 2 (opt)
02E8-02EF[3]	Serial port 4 (opt)
02F8-02FF[2]	Serial port 2 (default)
0376-0377[2]	Secondary IDE port (opt)
0378-037F[2]	Parallel port 1 (default)
03BC-03C3[3]	Parallel port 3 (opt)
03E8-03EF[3]	Serial port 3 (opt)
03F0-03F5	Floppy channel
03F6-03F7	Primary IDE and floppy
03F8-03FF[2]	Serial port 1 (default)
040A-043F	DMA scatter/gather
0480-048F	DMA high pages
04D0-04D1	Edge/level interrupts
04D6	DMA2 extended mode
0678-067A[3]	Parallel port 2 (opt)

Table 5-1. I/O Addresses (Continued)

Address	Function
0778-077A[3]	Parallel port 1 (opt)
07BC-07BE[3]	Parallel port 3 (opt)
0CF8-0Cff	PCI configuration

[1] The Watchdog timer and LM78 are normally disabled but you can relocate and enable them via PCI configuration.
[2] These ports are available if the listed function is not enabled in the BIOS.
[3] This is an alternate range that you can select in the BIOS setup.

Memory Address Mapping

PCI system memory and I/O configure or enumerate dynamically each time the system boots or by an operating system (Plug and Play), but there are legacy memory locations that remain constant.

Refer to Table 5-2 for memory address information.

Table 5-2. Memory Address

Address Range	Function
000000H-09FFFFH	640 KB conventional RAM
0A0000H-0BFFFFH	VGA DRAM (typically on the PCI backplane)
0C0000H-0C7FFFH	VGA ROM (typically on the PCI backplane)
0C8000H-0DFFFH	Expansion ROM
0E0000H-0EFFFFH	System BIOS extensions
0F0000H-0FFFFFH	Phoenix system BIOS

Video Controller

The i740 chip gives on-card video including hardware 3d rendering, hardware 3d texturing and Advanced Graphics Port (AGP) interface. AGP gives a synchronous interface at 66MHz. The AGP reaches a theoretical transfer rate of 500Mb/second and supplies a direct connection to the on-card video controller.

You can enable or disable this device through the BIOS setup utility. You can access video connections on the CPV5300 front panel and the CPV5300 Transition Module rear panel via a standard 15 pin high density D-sub video connector.

Ultra SCSI Controller

The CPV5300 uses the Adaptec 7880 chip for on-board support for Ultra SCSI. You can enable or disable this feature through the BIOS Setup screen. You can connect to the SCSI device at the front panel and the rear I/O transition module via a 68-pin, high-density connector.

The Ultra SCSI circuitry provides automatic termination when a device is plugged into the rear or front. You can connect devices to the rear, the front, or both at the same time. Ground pins on the SCSI connector are reassigned to act as cable or device detects. Two ground pins are used to distinguish between 16-bit or 8-bit devices. The active terminator used is a Dallas Semiconductor DS2105Z. This part has a power down pin (PD-) that disconnects the termination from the bus when driven low. This pin has an internal pull up resistor.

Figure 5-2 shows the termination scheme. When a CPV5300 board is installed into a system with no rear I/O, the terminators next to J4 are active. This provides termination at the end of the SCSI bus right at J4. If you plug a non-wide device into the CPV5300's 68-pin connector, pin 50 becomes grounded. This causes the terminators for the CTRL and SCD0-7 signals to turn off. The last device on the cable provides termination for these signals.

If you plug a wide device into the CPV5300's 68-pin connector, pin 1 becomes grounded, and all three terminators turn off. In this case, you must connect a wide device at the end of the cable.

If you plug in a rear I/O transition module, pin E5 is grounded. This disables the CPV5300's terminators next to J4 since the end of the SCSI bus is at the 68-pin connector on the rear I/O board. If you plug a non-wide device into the rear I/O's 68-pin connector, pin 50 becomes grounded. This causes the terminators for the CTRL and SCD0-7 signals to turn off. The last device on the cable provides termination for these signals.

If you plug a wide device into the rear I/O's 68-pin connector, pin 1 is grounded, and all three terminators turn off. In this case, you must connect a wide device at the end of the cable. If you use a 68-pin to 50-pin SCSI adapter it must have straight through connections with no pins hooked together.

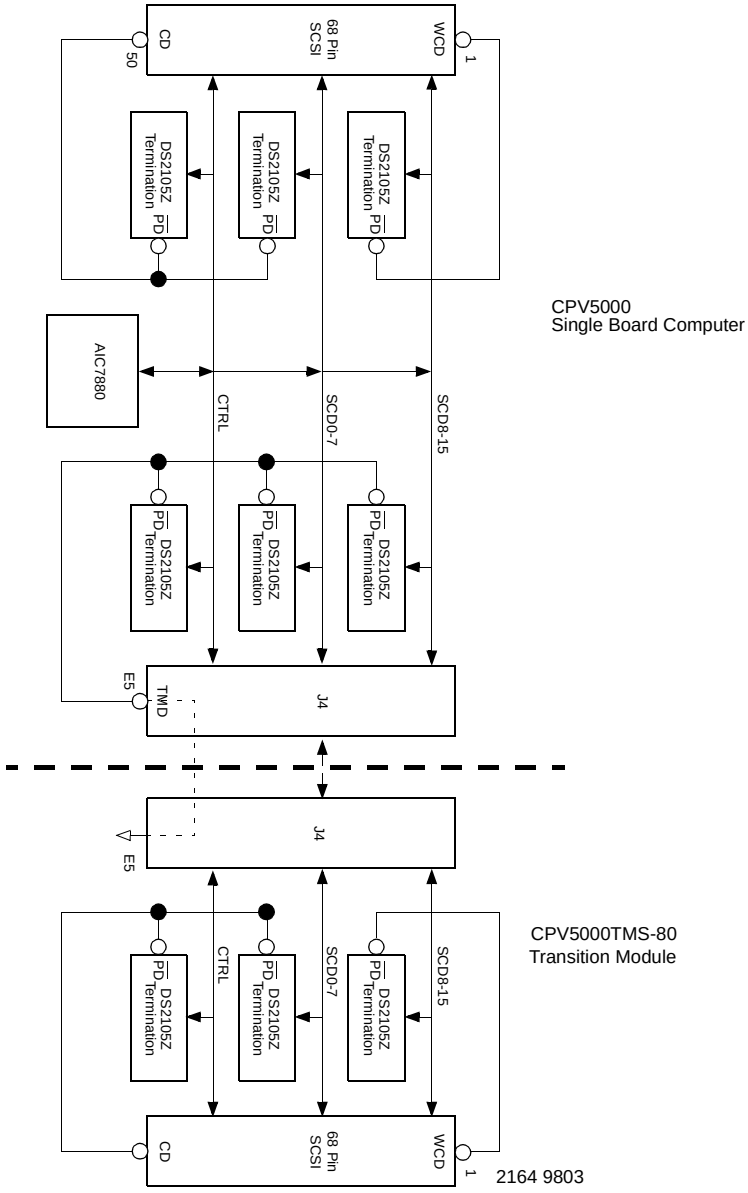


Figure 5-2. SCSI Termination

EIDE Interface

You can connect to both primary and secondary Enhanced Integrated Device Electronics (EIDE) interfaces through the rear I/O Transition Module. The primary EIDE channel is available for the connection of on-board devices through an on-board height density connector. The IDE interface supports AT Attachment Packet Interface (ATAPI) modes 0 to 4.

Each IDE interface supports two IDE devices (master and slave). The IDE interface supports disk drives up to 8.2Gbytes and CD-ROM drives.

Note If you use the on-board IDE hard drive, it connects to the primary IDE port. If this is the case, you can connect only one drive to the primary rear I/O EIDE port, and you must jumper the drive different (master or slave) than the on-board drive

Table 5-3 shows all possible on-board drive options.

Table 5-3. On-board drive options

Drive option 1	Drive option 2
Floppy	Not installed
IDE hard drive	Not installed
IDE flash drive	Not installed
Floppy	IDE hard drive
Floppy	IDE flash drive
IDE flash drive	IDE hard drive

Floppy Interface

The floppy interface supports up to two floppy drives:

- 5.25 inch - 360Kb, 1.2MB
- 3.5 inch - 720KB, 1.44MB

The floppy interface connector consists of a 34(2x17) pin shrouded header available on the rear I/O transition module, or a flex cable connector for on-board drive mounting.

Note You cannot use both the rear I/O connected floppy and the on-board floppy connection at the same time.

Parallel Port

The parallel port has Enhanced Capabilities Port (ECP) and Enhanced Parallel Port (EPP) modes of operation.

The parallel interface connector is a 25-pin D-connector header available on the rear I/O transition module, or a 25-pin micro-D connector on the front panel.

Serial Ports

The CPV5300 has two serial ports. The ports support 16550 operation. The serial interface connector is a 9-pin D style connector available on the rear I/O transition module and on the front panel. The serial ports are ESD protected to 15KV.

USB

The CPV5300 has two Universal Serial Bus (USB) ports with transfer capability from 1.2Mbits/second to 12Mbits/second.

Both ports have two USB connectors on the front panel and the rear I/O transition module. You can route USB signals to the front or rear I/O connectors and enable or disable USB in the BIOS setup.

- Jumper installed - rear connection
- Jumper removed - front connection

Keyboard/Mouse Interface

The keyboard and mouse is supported by a single PS/2 connector on the front panel and separate PS/2 style connectors on the rear I/O transition module. The front I/O keyboard/mouse connector uses a standard splitter cable to connect to a mouse and keyboard.

DMA Channels

Their are eight Direct Memory Access (DMA) channels. Refer to Table 5-4.

Table 5-4. DMA channels

Channel	Function
DMA 0	ISA memory refresh
DMA 1	Reserved
DMA 2	Floppy disk controller
DMA 3	Reserved
DMA 4	Cascade for DMA 1
DMA 5	Reserved
DMA 6	Reserved
DMA 7	Reserved

Interrupts

Their are 18 interrupt channels. Refer to Table 5-5.

Table 5-5. Interrupt channels

Channel	Function
NMI	Reports parity / System errors
SMI	System management
0	System timer
1	Keyboard
2	Cascade for IRQ 8-15
3	COM 2/serial port 2
4	COM 1/serial port 1
5	Parallel port 2
6	Floppy controller
7	Parallel port 1
8	Real time clock
9	Software redirect to IRQ2
10	Reserved
11	Reserved / special features
12	Reserved / PS/2 mouse
13	Coprocessor
14	Hard disk controller
15	Reserved

Understanding the Programmable Logic Field Programmable Gate Array Registers

The Programmable Logic Field Programmable Gate Array (PLFPGA) register set has four major functional blocks:

- a two level watchdog timer
- system monitoring
- a serial EEPROM interface
- peripheral components configuration

The PLFPGA is I/O mapped and resides on the single board computer's ISA bus. Figure 5-3 shows the PLFPGA block diagram.

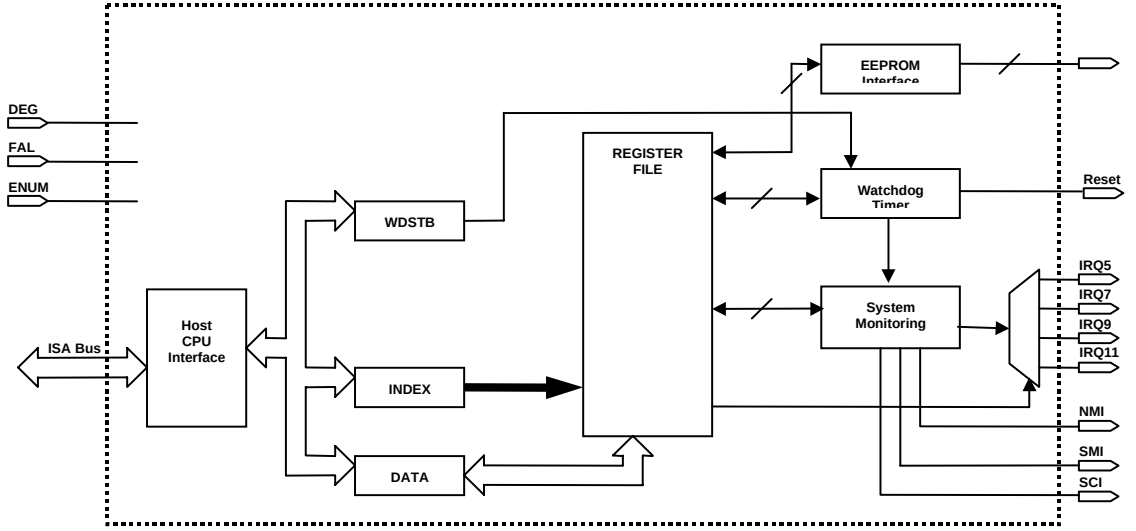


Figure 5-3. Block diagram for the PLFPGA

You can configure and control PLFPGA features by reading from and writing to the internal configuration registers. You can access the registers by:

1. writing the register number to the PLFPGA index port
2. reading or writing data to the PLFPGA data port

The index port clears to zero after writes to the data port to protect from accidental corruption of the register file. The PLFPGA also has an I/O mapped watchdog strobe port (WDSTB). Writes to this port reset the watchdog timer count. Table 5-6 shows the I/O addresses for each PLFPGA port.

Table 5-6. PLFPGA mapping for I/O ports

Address	Port/Register Name
0x005Bh	WDSTB
0x005Dh	INDEX
0x005Fh	DATA

Internally, the PLFPGA is divided into a series of register sets. The register sets logically group registers together which perform similar functions. The default register set contains registers that control most PLFPGA features. Occasionally you may need to select a different set. To switch between register sets, you must program the DEVNUM register for the register set that you want to access. Table 5-7 shows the device numbers and the descriptions for the register sets within the PLFPGA.

Table 5-8 shows the registers defined for each register set.

Table 5-7. PLFPGA register sets

Device Number	Register Set/Device Description
0x00	Legacy Features
0x10	On-Card Ethernet Controller A
0x11	On-Card Ethernet Controller B
0x12	On-Card SCSI Controller
0x13	On-Card USB Controller
0x14	Flash BIOS

Table 5-8. PLFPGA registers

Device Number	Register Number	Register Name
Any	0x0F	DEVNUM
0x00	0x00	STAT
0x00	0x02	ECTRL
0x00	0x03	WDCFG
0x00	0x04	INTNUM
0x00	0x05	SCIEN
0x00	0x06	NMIEN
0x00	0x07	IRQEN
0x00	0x08	ALEN
0x00	0x09	LTCLR
0x00	0x0A	ENMCFG
0x10	0x01	LNACTRL

Table 5-8. PLFPGA registers (Continued)

Device Number	Register Number	Register Name
0x11	0x01	LNBCTRL
0x12	0x01	SCSICTRL
0x13	0x01	USBCTRL
0x14	0x01	FLBCTRL

Register Descriptions

This section describes how to access the various PLFPGA register sets. “RES” means that bit is “reserved”. Bit description Table 5-10 on page 5-19 through Table 5-29 on page 5-35 show bits 0 through 7 on the top line and bit functions on the second line. Table 5-9 shows the location of the PLFPGA register set tables.

Table 5-9. Location of PLFPGA Register Set Tables

For this register:	Go to page:
DEVNUM	5-19
STAT	5-20
ECTRL	5-21
WDCFG	5-22
INTUM	5-24
SCIEN	5-26
NMIEN	5-27
IRQEN	5-28
ALEN	5-29
LTCLR	5-30
ENMCFG	5-31
LNACTRL	5-32
LNBCTRL	5-33
SCSICTRL	5-34
USBCTRL	5-35
FLBCTRL	5-36

DEVNUM

The Device Number/Register Set Select Register (DEVNUM) lets you select which FPGA register to access. Refer to Table 5-10.

Table 5-10. Bit descriptions for the FPGA register set

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
RES	RES	RES	DN4	DN3	DN2	DN1	DN0

Bits DN[4:0] tell you which FPGA register set you can access. Refer to Table 5-11 for allowed values. All other combinations of DN[4:0] are invalid.

Table 5-11. Bit values for selecting register access

DN4	DN3	DN2	DN1	D0	Register Set/Device Description
0	0	0	0	0	Legacy Features
1	0	0	0	0	On-Card Ethernet Controller A
1	0	0	0	1	On-Card Ethernet Controller B
1	0	0	1	0	On-Card SCSI Controller
1	0	0	1	1	On-Card USB Controller
1	0	1	0	0	Flash BIOS

STAT

The Status Register (STAT) is a read only register. Reads of the unused bits produce indeterminate values. Writes have no effect. Refer to Table 5-12.

Table 5-12. Bit descriptions for the STAT register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
RES	FAL	DEG	RES	LM78 ALARM A	LM78 ALARM B	SMB ALERT	MMC2 TEMP ALARM

MMC2 TEMP ALARM (Bit 0)

This signal connects to the MMC2's thermal sensor alarm output (ATF). The input is latched when active. You can clear this bit (0) with a write to the LATCLR register. A read of this bit returns the latched status of the input.

LM78 ALARM A (Bit 3) and LM78 ALARM B (Bit 2)

The LM78 output functions feed these signals. The input is latched when active. You can clear these bits (3 and 2) with a write to the LATCLR register. A read of this bit returns the latched status of the input.

DEG (Bit 5)

DEG comes from the CPCI bus and signals a power supply deregulation condition. A read of this bit returns the current state of the input.

FAL (Bit 6)

This signal comes from the CPCI bus and signals a power failure condition. A read of this bit returns the current state of the input.

ECTRL

The Serial EEPROM Control Register (ECTRL) lets you access the external serial configuration EEPROM. Refer to Table 5-13.

Table 5-13. Bit descriptions for the ECTRL register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
RES	RES	RES	EEPRG	EERST	EEEN	EECLK	EEDTA

EEDTA (Bit 0)

Writes to this bit are sent to the external serial EEPROM's data line. If you write a 1 to this bit, reads from the bit reflect the state of the data output from the external serial EEPROM.

EEEN (Bit 2)

Set to 1 to enable access to the serial EEPROM

EERST (Bit 3)

Set to 1 to reset the external serial configuration EEPROM

EEPRG (Bit 4)

Set to 1 to enable programming of the serial EEPROM

WDCFG

Refer to Table 5-14 for bit descriptions for the Watchdog Configuration Register (WDCFG).

Table 5-14. Bit descriptions for the WDCFG register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
CLR_STATUS	ALARM_EN	RES	WD1	WD0	SEL2	SEL1	SEL0

SEL0 (Bit 0), SEL1 (Bit 1) and SEL2 (Bit 2)

Use SEL[2:0} to select the watchdog timeout time. Writing to these bits does not clear or reset the watchdog timer. Refer to Table 5-14.

Table 5-15. Bit values for selecting watchdog timeout time

Period	SEL2	SEL1	SEL0
17.8ms	0	0	0
71.1ms	0	0	1
284ms	0	1	0
1.14s	0	1	1
4.55s	1	0	0
18.22s	1	0	1
72.8s	1	1	0
291s	1	1	1

WD0 (Bit 3) and WD1 (Bit 4)

Use these bits to define the event that occurs on a watchdog timeout and to disable the watchdog timer. Reading these bits returns the last value written. Refer to Table 5-16.

Table 5-16. Bit values defining watchdog timeout and disabling

Description	WD1	WD0
Disabled (resets watchdog)	0	0
FPGA IRQX	0	1
NMI	1	0
NMI followed by reset (8.2ms delay before single board computer reset)	1	1

ALARM_EN (Bit 6)

Use this bit to control whether a watchdog timeout event generates an FPGA Alarm.

- Write a logic 1 to cause the alarm signal to become active on a watchdog timeout event.
- Write a logic 0 to latch a watchdog timer event.

Reading this bit returns the last written value.

CLR_STATUS (Bit 7)

Use this bit to reset the watchdog timer output latch.

- Write a logic 1 to hold the watchdog timer output latch in a reset state.
- Write a logic 0 to latch a watchdog timer event.

Reading this bit returns the last written value.

INTUM

Use the Interrupt Selection Register (INTUM). Refer to Table 5-17.

Table 5-17. Bit descriptions for the INTUM register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
RES	RES	RES	RES	IRQSL3	IRQSL2	IRQSL1	IRQSL0

These bits determine which IRQ is driven when an IRQ event triggers. Refer to Table 5-18.

Table 5-18. Bit values for IRQ events

Interrupt Line	IRQSL3	IRQSL2	IRQSL1	IRQSL0
None	0	0	0	0
None	0	0	0	1
None	0	0	1	0
None	0	0	1	1
None	0	1	0	0
IRQ5	0	1	0	1
None	0	1	1	0
IRQ7	0	1	1	1
None	1	0	0	0
IRQ9	1	0	0	1
None	1	0	1	0
IRQ11	1	0	1	1

Table 5-18. Bit values for IRQ events (Continued)

Interrupt Line	IRQSL3	IRQSL2	IRQSL1	IRQSL0
None	1	1	0	0
None	1	1	0	1
None	1	1	1	0
None	1	1	1	1

SCIEN

The System Control Interrupt Enable Register (SCIEN) defines the type of events that can generate an SCI. Refer to Table 5-19.

Table 5-19. Bit descriptions for the SCIEN register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENABLE	RES	RES	RES	ALARM_A	ALARM_B	TEMP	SMB ALERT

SMB ALERT (Bit 0)

- Set to a logic 1 to allow generation of an SCI when SMB ALERT is active.
- Write a logic 0 to this bit to disable an SCI for this event.

TEMP (Bit 1)

- Set to a logic 1 to allow generation of an SCI when TEMP is active. TEMP is the ATF signal from the MMC2.
- Write a logic 0 to this bit to disable an SCI for this event.

ALARM_A (Bit 3) and ALARM_B (Bit 2)

- Set to a logic 1 to allow the generation of an SCI when the ALARM_A or ALARM_B go active.
- Write a logic 0 to this bit to disable an SCI for this event.

ENABLE

- Set to a logic 1 to allow generation of an SCI by one of the events above.
- Write a logic 0 to prevent the events from generating an SCI.

NMIEN

The NMI Enable Register (NMIEN) defines the events that can generate an NMI. Refer to Table 5-20.

Table 5-20. Bit descriptions for the NMIEN register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENABLE	RES	RES	RES	ALARM_A	ALARM_B	TEMP	SMB ALERT

SMB ALERT (Bit 0)

- Set to a logic 1 to allow the generation of an NMI when the SMB ALERT is active.
- Write a logic 0 to this bit to disable an NMI for this event.

TEMP (Bit 1)

- Set to a logic 1 to allow the generation of an NMI when TEMP is active. TEMP is the ATF signal from the MMC2).
- Write a logic 0 to this bit to disable an NMI for this event.

ALARM_A (Bit 3) and ALARM_B (Bit 2)

- Set to a logic 1 to allow the generation of an NMI when the ALARM_A or ALARM_B go active.
- Write a logic 0 to this bit to disable an NMI for this event.

ENABLE (Bit 7)

- Set to a logic 1 to allow the listed events to generate an NMI.
- Write a logic 0 to prevent the events from generating an NMI.

IRQEN

The IRQ Enable Register (IRQEN) defines the events that can generate an IRQ. The IRQ generated is set by IRQ Select Register (IRQNUM). Refer to Table 5-21.

Table 5-21. Bit descriptions for the IRQEN register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENABLE	RES	RES	RES	ALARM_A	ALARM_B	TEMP	SMB ALERT

SMB ALERT (Bit 0)

- Set to a logic 1 to allow the generation of an IRQ when the SMB ALERT is active.
- Write a logic 0 to this bit to disable an IRQ for this event.

TEMP (Bit 1)

- Set to a logic 1 to allow the generation of an IRQ when TEMP is active. TEMP is the ATF signal from the MMC2).
- Write a logic 0 to this bit to disable an IRQ for this event.

ALARM_A (Bit 3) and ALARM_B (Bit 2)

- Set to a logic 1 to allow the generation of an IRQ when the ALARM_A or ALARM_B go active.
- Write a logic 0 to this bit to disable an IRQ for this event.

ENABLE (Bit 7)

- Set to a logic 1 to allow the listed events to generate an IRQ.
- Write a logic 0 to prevent the events from generating an IRQ.

ALEN

The Alarm Enable Register (ALEN) defines the events that can generate an Alarm output. Refer to Table 5-22.

Table 5-22. Bit descriptions for the ALEN register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENABLE	RES	RES	RES	ALARM_A	ALARM_B	TEMP	SMB ALERT

SMB ALERT (Bit 0)

- Set to a logic 1 to allow the generation of an Alarm when the SMB ALERT is active.
- Write a logic 0 to this bit to disable an Alarm for this event.

TEMP (Bit 1)

- Set to a logic 1 to allow the generation of an Alarm when TEMP is active. TEMP is the ATF signal from the MMC2.
- Write a logic 0 to this bit to disable an Alarm for this event.

ALARM_A (Bit 3) and ALARM_B (Bit 2)

- Set to a logic 1 to allow the generation of an Alarm when the ALARM_A or ALARM_B go active.
- Write a logic 0 to this bit to disable an Alarm for this event.

ENABLE (Bit 7)

- Set to a logic 1 to allow the listed events to generate an Alarm.
- Write a logic 0 to prevent the events from generating an Alarm.

LTCLR

The Event Latch Clear Register (LTCLR) resets latches in the FPGA for the FAN, TEMP, ALARM_A, ALARM_B and ENUM latches. This register is write only. Reads return an indeterminate value. Write a logic 1 to clear the latch for that bit position. If you write a logic 0 it has no effect on the latch. Refer to Table 5-23.

Table 5-23. Bit descriptions for the LTCLR register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
RES	RES	RES	RES	ALARM_A	ALARM_B	TEMP	FAN

FAN (Bit 0)

This bit sets automatically when an off-card fan tachometer device signals a FAN event.

- Write a logic 1 to this bit to clear any latched FAN events.
- If you write a logic 0, it has no effect.

TEMP (Bit 1)

This bit sets automatically when an off-card thermostat device signals a TEMP event.

- Write a logic 1 to this bit to clear any latched TEMP events.
- If you write a logic 0, it has no effect.

ALARM_A (Bit 3) and ALARM_B (Bit 2)

This bit sets automatically when the on-card LM78 signals an ALARM_A or ALARM_B event.

- Write a logic 1 to this bit to clear any latched ALARM_A or ALARM_B events.
- If you write a logic 0, it has no effect.

ENMCFG

The ENUM Control/Status Register (ENMCFG) allows configuration of the event generated when the CompactPCI ENUM signal becomes active. Reading this register allows monitoring of the ENUM signal state. Refer to Table 5-24.

Table 5-24. Bit descriptions for the ENMCFG register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENUM	RES	RES	RES	RES	RES	ACT1	ACT0

ACT0 (Bit 0) and ACT1 (Bit 1)

These bits allow system software to select the action taken when the CompactPCI ENUM signal is active. Refer to Table 5-25 for the actions taken for each value of ACT1 and ACT0.

Table 5-25. Actions Taken for Each Value of ACT1 and ACT0

ACT1	ACT0	Action
0	0	None
0	1	E_IRQ [1]
1	0	E_NMI [2]
1	1	E_SCI [3]

[1] E_IRQ - An ENUM event generates an interrupt on the interrupt selected in the INTNUM register

[2] E_NMI - An ENUM event generates a non-maskable interrupt

[3] E_SCI - An ENUM event generates a System Control Interrupt

ENUM (Bit 7)

This bit reflects the state of the ENUM signal on the CompactPCI bus. When this bit is high, ENUM is active. When this bit is low, ENUM is inactive. The ENUM bit is read only. Writes have no effect.

LNACTRL

The LAN A Control Register (LNACTRL) controls the on-card LAN A controller. Bits written can also read back. Refer to Table 5-26.

Table 5-26. Bit descriptions for the LNACTRL register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENABLE	REAR	RES	RES	RES	RES	RES	RES

REAR (Bit 6)

The BIOS uses this bit to route LAN A signals to either the front or the rear connectors.

- Write a logic 0 to this bit to route LAN A signals to the front connector.
- Write a logic 1 to this bit to route LAN A signals to the rear connector.

The BIOS sets this bit according to CMOS setup.

ENABLE (Bit 7)

The BIOS uses this bit to enable LAN A.

- Write a logic 1 to this bit to enable LAN A for the operating system and application code.
- Write a logic 0 to this bit to disable it.

The BIOS sets this bit according to CMOS setup.

LNBCTRL

The LAN B Control Register (LNBCTRL) controls the on-card LAN B controller. Bits written can also read back. Refer to Table 5-27.

Table 5-27. Bit descriptions for the LNACTRL register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENABLE	REAR	RES	RES	RES	RES	RES	RES

REAR (Bit 6)

The BIOS uses this bit to route LAN B signals to either the front or the rear connectors.

- Write a logic 0 to this bit to route LAN B signals to the front connector.
- Write a logic 1 to this bit to route LAN B signals to the rear connector.

The BIOS sets this bit according to CMOS setup.

ENABLE (Bit 7)

The BIOS uses this bit to enable LAN B.

- Write a logic 1 to this bit to enable LAN B for the operating system and application code.
- Write a logic 0 to this bit to disable it.

The BIOS sets this bit according to CMOS setup.

SCSICTRL

The SCSI Control Register (SCSICTRL) controls the on-card SCSI controller. Bits written can also read back. Refer to Table 5-28.

Table 5-28. Bit descriptions for the SCSICTRL register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENABLE	RES	RES	RES	RES	RES	RES	RES

ENABLE (Bit 7)

The BIOS uses this bit to enable the on-card SCSI.

- Write a logic 1 to this bit to enable the on-card SCSI for the operating system and application code.
- Write a logic 0 to this bit to disable it.

The BIOS sets this bit according to CMOS setup.

USBCTRL

The USB Control Register (USBCTRL) controls the on-card USB routing. Bits written can also read back. Refer to Table 5-29.

Table 5-29. Bit descriptions for the USBCTRL register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
RES	REAR	RES	RES	RES	RES	RES	RES

REAR (Bit 6)

The BIOS uses this bit to route the on-card USB signals to either the front or the rear connectors.

- Write a logic 0 to this bit to route USB signals to the front connector.
- Write a logic 1 to this bit to route USB signals to the rear connector.

The BIOS sets this bit according to CMOS setup.

FLBCTRL

The Flash BIOS Control Register (FLBCTRL) controls the write protect line on the BIOS flash memory part. Bits written can also read back. Refer to Table 5-30.

Table 5-30. Bit descriptions for the FLBCTRL register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
WP-	RES	RES	RES	RES	RES	RES	RES

WP- (Bit 7)

This bit enables the Flash BIOS boot block for updating.

- Write a logic 0 to this bit to protect the BIOS boot block.
- Write a logic 1 to this bit to open it for writing.

Related Documentation A

Motorola Computer Group Documents

You can get more information about CompactPCI by looking at the publications in Table A-1. You can get paper or electronic copies of Motorola Computer Group publications by:

- Contacting your local Motorola sales office
- Visiting Motorola Computer Group's World Wide Web literature site, http://www.motorola.com/literature

We suffix each manual publication number for Motorola Computer Group with characters that represent the revision level of the document, such as /IH2 (second revision).

To get the most up-to-date product information in PDF or HTML format, visit our Web site at http://www.motorola.com/literature.

Table A-1. Motorola Computer Group Documents

Document Title	Motorola Publication Number
CPV5300 CompactPCI Single Board Computer and Transition Module Installation Guide	CPV5300A/IHx
CompactPCI CPX2000 Series System Installation and Reference Guide	CPX2108A/IHx

URLs

These URLs (uniform resource locators) may give you helpful sources for more information about this product, related services, and development tools. Please note that we verify these URLs but they can change without notice.

- Motorola Computer Group, http://www.motorola.com/computer
- Motorola Computer Group OEM Services, http://www.motorola.com/computer/support
- PCI Industrial Computer Manufacturer's Group (PICMG) Hot Swap Specification, http://www.picmg.org
- LynxOS™ from Lynx Real-Time Systems, http://www.lynx.com
- VxWorks® from Wind River Systems, http://www.wrs.com
- OSE™ from Enea OSE Systems, http://www.enea.com
- QNX® Neutrino® from QNX Software Systems Ltd., http://www.qnx.com
- Windows NT® , http://www.microsoft.com
- GoAhead Software Inc., http://www.goahead.com

Index

Symbols

1-8, 2-4

A

advanced hard disk features 2-9
advanced menu 2-12
ALEN 5-29
arrow keys 2-4

B

beep code 4-1, 4-2
beep codes 4-2
BIOS 1-1
    test points 4-2
BIOS Services 1-3
BIOS Setup 2-1
BIOS Version 2-7
block diagram 5-14
Board Serial No. 2-6
boot device priority 2-26
boot menu 2-25
boot sequence 2-7

C

Cache Ram 2-6
changes xvi
check points, POST 4-2
comments, sending xviii
configuration menu 2-15, 2-18
contents xvii
CPU Speed 2-6
CPU Type 2-6
Ctrl-Alt- 1-8, 1-8

D

device configuration 2-18
DEVNUM 5-19
discard changes 2-30
discarding changes 2-29
diskette A 2-7
diskette B 2-7
DMA channels 5-12

E

ECTRL 5-21
EIDE interface 5-10
ENMCFG 5-31
error 4-2
    port 80h codes 4-2
exit discarding changes 2-29
exit menu 2-28

F

features
    hard disk 2-9
field help window 2-4
fixed disk drives 1-5
FLBCTRL 5-36
floppy interface 5-10
FPGA registers 5-14
function keys 1-8
functional description 5-1
functions
    PhoenixBIOS 1-2
functions, ROM BIOS 1-2

G
general help window 2-5

H
hard disk features 2-9
hard drive 2-27
hardware requirements (system) 1-4
help window 2-5

I
I/O address map 5-4
I/O device configuration menu 2-18
interrupts 5-13
INTUM 5-24
IRQEN 5-28

K
keyboard/mouse 5-12

L
legend bar 2-3
LNACTRL 5-32
LNBCTRL 5-33
load setup defaults 2-29
LTCLR 5-30

M
main menu bar 2-3
main menu fields
- advanced 2-3
- boot 2-3
- exit 2-3
- main 2-3
- security 2-3
- status 2-3

main menu selections 2-6
masters 2-7
memory address mapping 5-6
menu bar 2-3
messages 3-1
models xv

N
NMIEN 5-27

O
overview 1-1
overview of contents xvii

P
parallel port 5-11
PCI 5-1
PCI configuration menu 2-15
Peripheral Component Interconnect 5-1
Phoenix setup program 2-1
PhoenixBIOS 1-1
- function keys 1-8
- functions 1-2

PhoenixBIOS messages 3-1
PLFPGA mapping 5-15
PLFPGA registers 5-14
port 80h codes 4-2
POST 1-3, 4-1
- error 4-1
- terminal error 4-2
- test points 4-2

POST Terminal Errors 4-2
power on self tests 4-1
Power-on Self Test 1-3
Programmable Logic Field Programmable Gate Array Registers 5-14

R
recoverable error 4-1
register descriptions 5-18
register sets 5-16
registers 5-14
ROM BIOS 1-1
- functions 1-2
- interfaces 1-2

INDEX

S

save changes 2-28, 2-30
Save Value 2-3
saving values 2-28
SCIEN 5-26
SCSI controller 5-7
SCSICTRL 5-34
security menu 2-21
serial port 5-11
Setup
    get CMOS values 2-30
setup
    interface 2-2
    screen 2-2
    starting 2-1
setup program 2-1
slaves 2-7
special function keys 1-8
starting setup 2-1
STAT 5-20
status menu 2-23
suggestions, submitting xviii
summary of changes xvi
System Date 2-7
System Hardware Requirements 1-4
System Memory 2-6
System Time 2-7

T

terminal error 4-2
test points 4-2
troubleshooting 4-2

U

ultra I/O devices 2-19
ultra SCSI controller 5-7
uniform resource locators A-2
URL A-2
URLs (uniform resource locators) A-2
USB 5-11
USBCTRL 5-35

V

values
    saving 2-28
VGA error 4-1
video controller 5-7

W

wait states 3-3
watchdog timer 5-2
WDCFG 5-22

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BIOS and Programmer's Reference Guide

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