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CPV8540B CompactPCI® Hot Swap PMC Carrier Card

User Manual

CPV8540B/UM1

March 2001

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The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. If the equipment is supplied with a three-conductor AC power cable, the power cable must be plugged into an approved three-contact electrical outlet, with the grounding wire (green/yellow) reliably connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards and local electrical regulatory codes.

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Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Service personnel should not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, such personnel should always disconnect power and discharge circuits before touching components.

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>
> EN50082-1:1997 “Electromagnetic Compatibility—Generic Immunity Standard, Part 1. Residential, Commercial and Light Industry”

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About This Manual

The *CPV8540B CompactPCI Hot Swap PMC Carrier Card User Manual* provides a brief description and overview of this product. (PCI stands for Peripheral Component Interconnect and PMC stands for PCI Mezzanine Card.) The Manual also provides you with tables that include all the connector pinout information needed to attach one or two PMC mezzanine modules to the carrier card. This document should be used by anyone attaching PMC modules to this card.

The information in this manual applies to model numbers listed in the following table.

Model Number	Description
CPV8540B	CompactPCI Dual PMC Carrier

Overview of Contents

Chapter 1, *Features and Specifications*, lists the features and specifications of the CPV8540B including a block diagram and a schematic diagram.

Chapter 2, *Hot Swap Operation*, details normal hot swap operation.

Chapter 3, *Connector Pinouts*, lists all connector pinouts for the CPV8540B.

Appendix A, *Related Documentation*, lists all documentation related to this product.

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In all your correspondence, please list your name, position, and company. Be sure to include the title and part number of the manual and tell how you used it. Then tell us your feelings about its strengths and weaknesses and any recommendations for improvements.

Conventions Used in This Manual

The following typographical conventions are used in this document:

bold

is used for user input that you type just as it appears; it is also used for commands, options and arguments to commands, and names of programs, directories and files.

italic

is used for names of variables to which you assign values. Italic is also used for comments in screen displays and examples, and to introduce new terms.

`courier`

is used for system output (for example, screen displays, reports), examples, and system prompts.

<**Enter**>, <**Return**> or <**CR**>

<**CR**> represents the carriage return or Enter key.

CTRL

represents the Control key. Execute control characters by pressing the Ctrl key and the letter simultaneously, for example, **Ctrl-d**.

Features and Specifications 1

Introduction

This manual provides a brief description and overview of the CPV8540B CompactPCI Hot Swap PMC Carrier Card together with the connector pinout information needed to attach one or two PMC mezzanine modules to the card as well as software controlled features. PCI stands for *Peripheral Component Interconnect* and PMC stands for *PCI Mezzanine Card*.

Product Description and Diagrams

The CPV8540B provides connectivity to a wide variety of video, ATM, analog, serial, and many other functions. The CPV8540B is a 6U CompactPCI carrier card for IEEE P1386.1 compliant PMC modules. For more information about the IEEE P1386.1 specification, see Appendix A, *Related Documentation*. The board supports one double-width or two single-width PMC mezzanine modules. The CPV8540B supports 32- and 64-bit PCI operation at the PMCs and on the CompactPCI bus.

Once connected, the modules are accessed via front panel connections. In addition, I/O lines are brought out to the carrier card's rear 2mm pin and socket connectors, allowing rear panel connections in systems such as the CPX8216 HA chassis.

Features

The CPV8540B:

- is a universal voltage CompactPCI, Full Hot Swap, 6U size board
- supports standard (IEEE P1386.1) PMC mezzanine modules
- holds one double-width or two single-width modules

- supports 5.0 volt and universal voltage PMC modules (factory option for 3.3V)
- PMC bezel I/O becomes part of the CPV8540B front panel
- optional PMC I/O on P4 is brought out to rear connectors
- 32- or 64-bit operation is automatically selected
- single CompactPCI load via DEC21154 bridge
- supports Plug and Play, but the extended capabilities is not implemented

Card ID: The CPV8540B reports itself to the system as a bridge chip with the PMC functions behind it.

Block and Schematic Diagrams

The following two figures provide overviews of the card.

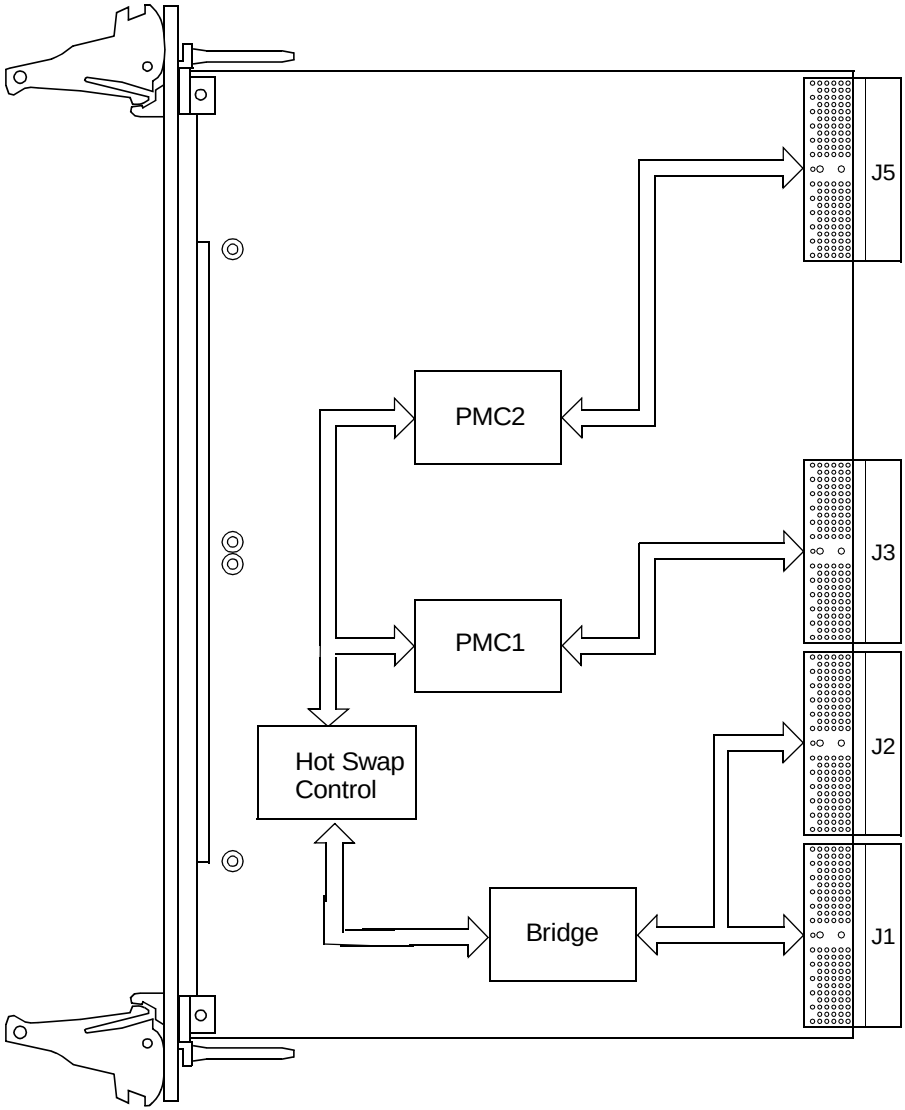


Figure 1-1. CPV8540B Block Diagram

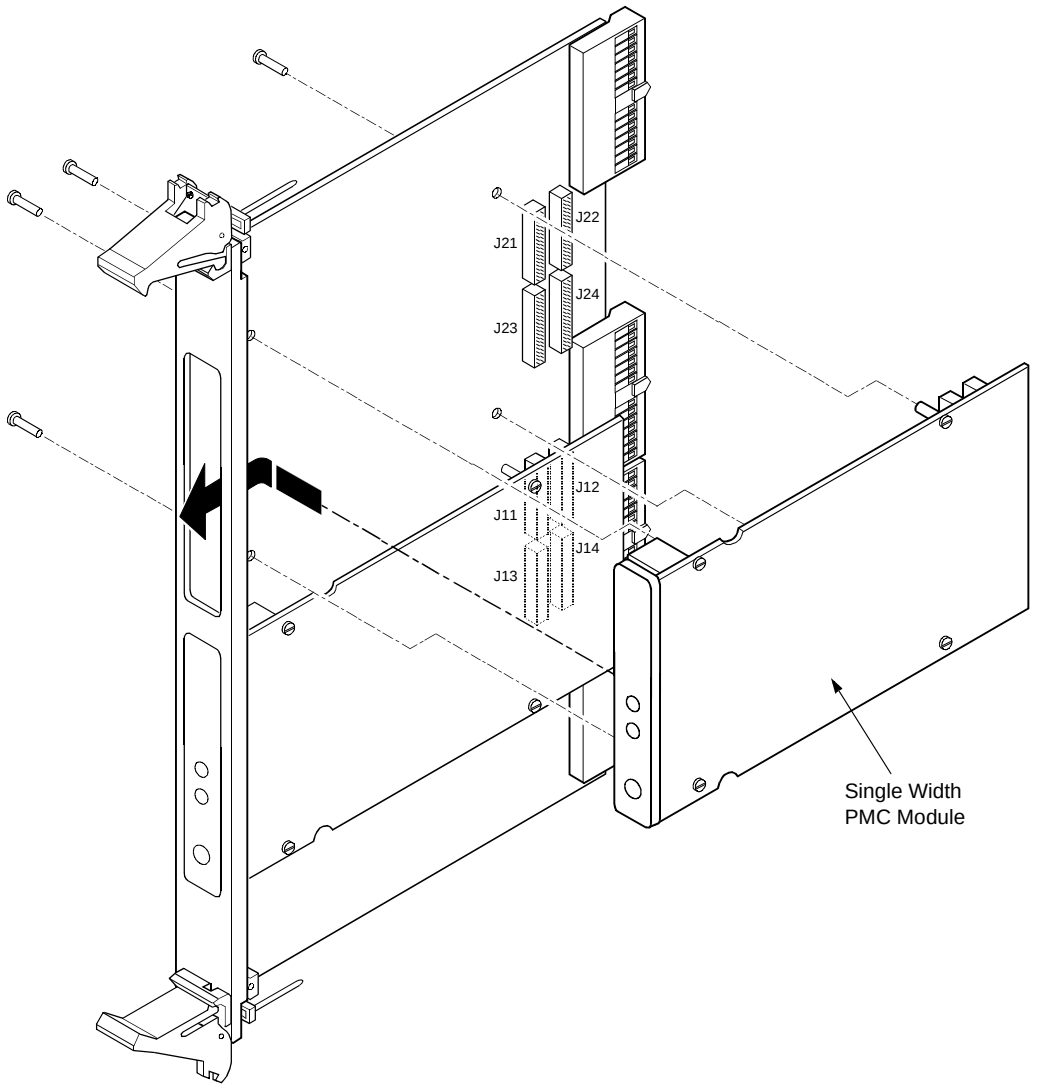


Figure 1-2. PMC Modules to CPV8540B Carrier Card with Connectors Labeled

Specifications

The following table lists the specifications for the CPV8540B.

Table 1-1. Specifications

Characteristics	Specifications
Universal CompactPCI Hot Swap Interface	Connectors J1, J2, J3, J5 used 64 address/data lines 33 MHz max. PCI Bus Clock DEC21154 PCI-to-PCI Interface Bridge Chip Signaling 5V or 3.3V compliant (Universal) Full Hot Swap Board
Supply Requirements (without PMC modules)	+5V: +5% -3%, 250 mA max. +3.3V: +5% -3%, 300 mA max. +12V: +5% -3%, 10 mA max. -12V: -5% +3%, 1 mA max.
IEEE P1386.1 PMC Interface	64 address/data lines 33 MHz max. PCI Bus Clock[1] Signaling 5V with 5V key post[2] Lower PMC J14/P14 goes to CompactPCI J3 for rear I/O Upper PMC J24/P24 goes to CompactPCI J5 for rear I/O Each PMC limited to 7.5 W max for all voltages Total power available to both PMC modules (shared): +5V: +/- 5%, 3 A max., 5 A protected +3.3V: +/- 5%, 2.3 A max., 7 A protected +3.3V current can be increased to 4.6 A at 3.0V min. +12V: +/-5%, 500 mA max., 800 mA protected -12V: +/-5%, 200 mA max., 450 mA protected Values for current protection are +-15% Over-current protection disconnects all supplies from PMCs
Indicators	Green LED Power Indicator Blue LED Hot Swap Indicator
Card Dimensions	9.2" H x 6.3" D x 0.8" W (233.4 mm x 160.0 mm x 20.3 mm)

Table 1-1. Specifications (Continued)

Characteristics	Specifications
Environmental	Operating Storage/Transit: Temperature: +5° C to +50° C; -20° C to +60° C Humidity (NC): 5% to 90% at 40° C Shock: - per ASTM 0775 Vibration: 1.0 G at 10 to 330 Hz; 1.2 G at 5 to 330 Hz Static Discharge: EN61000-3-2, 4KV contact, 8KV air
Demonstrated MTBF[3]	Minimum 50,000 hours
Safety	All printed wiring boards (PWBs) are manufactured with a flammability rating of 94V-0 by UL recognized manufacturers
Electromagnetic Compatibility (EMC)	Intended for use in systems meeting the following regulations: U.S.: FCC Part 15, Subpart B, Class A (non-residential) Canada: ICES-003, Class A (non-residential) See *CE Notice (European Community)* in the front of this manual for CE Notice information
Warranty	5-year limited warranty

Notes

1. Buffered from CompactPCI bus.
2. 3.3V may be possible as a factory option.
3. Based on sample testing in accelerated stress environment.

Hot Swap Operation 2

Overview

The CPV8540B follows requirements of the CompactPCI Hot Swap Specification, PICMG 2.1 R1.0, listed in Appendix A, *Related Documentation*, in order to allow for insertion into and extraction from CompactPCI systems while they are powered and operating. *Hot Swap friendly silicon* was not available at the time of the design of the CPV8540B, so custom circuitry was added around a standard Intel 21154 PCI-PCI bridge. Instead of a Hot Swap Control and Status Register (HS_CSR), accessible through PCI configuration space, the CPV8540B uses an *alternate register implementation*, as described in the CompactPCI Hot Swap Specification, listed in Appendix A, *Related Documentation*.

General purpose signals from the Intel 21154, in conjunction with the custom logic, provide all controls and status needed to complete the hardware and software connection process.

Control and Status

Four general purpose I/O lines, GPIO0 through GPIO3, are provided by the 21154 and are accessible through PCI configuration registers. These lines are used to support hot swap control and status bits, as described in PICMG 2.1, listed in Appendix A, *Related Documentation*. The following table shows how the lines support hot swap control and the status bits.

Table 2-1. Hot Swap Control and Status Bits

Signal	Description	GPIO
INS	Indicates board has been inserted	3
EXT	Indicates board is ready for extraction	2
LOO	Enable blue LED	1
EIM	Mask (disable) ENUM#	0

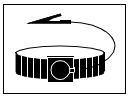
As well as indicating status as shown, INS and EXT are driven to acknowledge (and deassert) ENUM#.

Use of these signals is illustrated in the following descriptions of a normal hot insertion and extraction.

Note Use of EIM to mask ENUM#, and occurrences of atypical states, are not addressed in the following descriptions.

Full Hot Swap - Normal Insertion

Use ESD



Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to electrostatic discharge (ESD). After removing the component from its protective wrapper or from the system, place the component flat on a grounded, static-free surface (and, in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an active electrical ground. Note that a system chassis may not be grounded if it is unplugged.

Use the following procedure for full hot swap, normal board insertion.

1. PMC modules must be configured, installed, and fastened to the CPV8540B (as indicated in their manuals) prior to board insertion.
2. As the CPV8540B is started into the chassis, electrostatic charges on the board are dissipated into the chassis through limiting resistors and the ESD strip along the edge of the board.
3. When the board connects with the long CompactPCI pins in the backplane (pin staging is a requirement of PICMG 2.1, listed in Appendix A, *Related Documentation*), early power is applied to the Intel 21154 so it can initialize, reset, and hold its interfaces at higher impedance. The blue LED is lit.

4. When pressed in further, the board connects with PCI signals on the medium-length pins.
5. When the board connects with the shortest pins and BD_SEL# is asserted, power to the PMCs is turned on at a controlled rate to avoid disturbing the system. When power is stable and the local reset is deasserted, the blue LED is automatically extinguished.
6. The final step of hardware connection occurs when the ejector handle snaps into place. A micro switch in the handle causes the INS bit to set and ENUM# to be asserted to the CompactPCI bus. ENUM# can be used to signal that this hot swap event occurred.
7. Because ENUM# is an open collector, bused signal, software will need to examine the system to determine its source and cause. The Intel 21154 PCI-PCI bridge of the CPV8540B can be located using its Vendor ID, 1011h (word value at offset 00h), and its Device ID, 0026h (word value at offset 02h).
8. Once the CPV8540B's bridge has been located by bus and device number, its general purpose I/O registers should be initialized so that INS and EXT are inputs, LOO is off, and EIM is off, using the following sequence.
    a. Set byte at offset 65h to oFh.
    b. Set byte at offset 66h to 3Ch.
9. An insertion event is identified by the INS bit being set. This is indicated by a 1 at the most significant bit (bit 7) of the byte at offset 67h.
10. To clear the INS bit and deassert ENUM#, use the following sequence.
    a. Set byte at offset 66h to 80h.
    b. Set byte at offset 66h to 08h.
11. At this point, the system is free to reconfigure the PCI configurations to include the newly inserted CPV8540B.

2

Full Hot Swap - Normal Extraction

Note It is assumed that the bridge's GPIO registers are either in the last state used during the insertion process or they are initialized, as previously indicated.

Use the following procedure for full hot swap, normal board extraction.

1. When the lower ejector handle of the CPV8540B is pressed down to start extraction, the micro switch causes EXT and ENUM# to be asserted. Physical board extraction should stop until the blue LED is lit.
2. Software checks the CPV8540B to see if it caused the ENUM#, as it did during insertion. An extraction event is identified by the EXT bit being set. This is indicated by a 1 at bit 6 of the byte at offset 67h.
3. To clear the EXT bit and deassert ENUM#, use the following sequence.
   a. Set byte at offset 66h to 40h.
   b. Set byte at offset 66h to 04h.
4. The system prepares for board removal and then lights the blue LED by setting the byte at offset 65h to 20h.
5. When you see that the blue LED is lit, physical extraction can continue until the board is fully removed.

ENUM# Mask and Blue LED Control

Once GPIO registers have been initialized, as indicated in *Full Hot Swap - Normal Insertion*, the EIM and LOO are controlled by the byte at offset 65h.

To set LOO, which lights the blue LED, set the byte at offset 65h to 20h. To clear LOO, which extinguishes the blue LED, set the byte at offset 65h to 02h.

To set EIM, which inhibits ENUM#, set the byte at offset 65h to 10h. To clear EIM, which allows ENUM#, set the byte at offset 65h to 01h.

Connector Pinouts 3

Overview

The tables in this chapter provide the connector pinout information needed to attach one or two PMC mezzanine modules to the carrier card.

Table 3-1. CPCI J3 User I/O Connector Pinout

	ROW A	ROW B	ROW C	ROW D	ROW E	
14	+3.3V	+3.3V	+3.3V	+5V	+5V	14
13	PMC1IO5	PMC1IO4	PMC1IO3	PMC1IO2	PMC1IO1	13
12	PMC1IO10	PMC1IO9	PMC1IO8	PMC1IO7	PMC1IO6	12
11	PMC1IO15	PMC1IO14	PMC1IO13	PMC1IO12	PMC1IO11	11
10	PMC1IO20	PMC1IO19	PMC1IO18	PMC1IO17	PMC1IO16	10
9	PMC1IO25	PMC1IO24	PMC1IO23	PMC1IO22	PMC1IO21	9
8	PMC1IO30	PMC1IO29	PMC1IO28	PMC1IO27	PMC1IO26	8
7	PMC1IO35	PMC1IO34	PMC1IO33	PMC1IO32	PMC1IO31	7
6	PMC1IO40	PMC1IO39	PMC1IO38	PMC1IO37	PMC1IO36	6
5	PMC1IO45	PMC1IO44	PMC1IO43	PMC1IO42	PMC1IO41	5
4	PMC1IO50	PMC1IO49	PMC1IO48	PMC1IO47	PMC1IO46	4
3	PMC1IO55	PMC1IO54	PMC1IO53	PMC1IO52	PMC1IO51	3
2	PMC1IO60	PMC1IO59	PMC1IO58	PMC1IO57	PMC1IO56	2
1	V(I/O)	PMC1IO64	PMC1IO63	PMC1IO62	PMC1IO61	1

Notes

1. PMC1IO* signals are those connected to the lower PMC Slot, or Slot 1.
2. Pins in J3 columns 15 through 19 are not connected (NC).
3. Voltages in column 14 are controlled by hot swap hardware.

4. V(I/O) is normally 5V and controlled by hot swap hardware. However, 3.3V is available as a factory option.

Table 3-2. CPCI J5 User I/O Connector Pinout

	ROW A	ROW B	ROW C	ROW D	ROW E	
13	PMC2IO5	PMC2IO4	PMC2IO3	PMC2IO2	PMC2IO1	13
12	PMC2IO10	PMC2IO9	PMC2IO8	PMC2IO7	PMC2IO6	12
11	PMC2IO15	PMC2IO14	PMC2IO13	PMC2IO12	PMC2IO11	11
10	PMC2IO20	PMC2IO19	PMC2IO18	PMC2IO17	PMC2IO16	10
9	PMC2IO25	PMC2IO24	PMC2IO23	PMC2IO22	PMC2IO21	9
8	PMC2IO30	PMC2IO29	PMC2IO28	PMC2IO27	PMC2IO26	8
7	PMC2IO35	PMC2IO34	PMC2IO33	PMC2IO32	PMC2IO31	7
6	PMC2IO40	PMC2IO39	PMC2IO38	PMC2IO37	PMC2IO36	6
5	PMC2IO45	PMC2IO44	PMC2IO43	PMC2IO42	PMC2IO41	5
4	PMC2IO50	PMC2IO49	PMC2IO48	PMC2IO47	PMC2IO46	4
3	PMC2IO55	PMC2IO54	PMC2IO53	PMC2IO52	PMC2IO51	3
2	PMC2IO60	PMC2IO59	PMC2IO58	PMC2IO57	PMC2IO56	2
1	(NC)	PMC2IO64	PMC2IO63	PMC2IO62	PMC2IO61	1

Notes

1. PMC2IO* signals are those connected to the upper PMC Slot, or Slot 2.
2. Pins in J5 columns 14 through 22 are not connected (NC).
3. Pin 1A is active low on some transition modules to indicate the module is present (TMPRSNT_L).

Table 3-3. PCI Interface Connector Pinout: P11/J11, P21/J21 32-bit PCI

Pin#	Signal Name	Signal Name	Pin #
1	TCK	-12V	2
3	GND	INTA#	4
5	INTB#	INTC#	6
7	BUSMODE1#	+5V	8
9	INTD#	PCI-RSVD	10
11	GND	3.3VAUX (NC)	12
13	CLK	GND	14
15	GND	GNT#	16
17	REQ#	+5V	18
19	V(I/O)	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	GND	24
25	GND	C/BE[3]#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	V(I/O)	AD[17]	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	GND	LOCK#	40
41	PCI-RSVD*	PCI-RSVD*	42
43	PAR	GND	44
45	V(I/O)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	GND	C/BE[0]#	52
53	AD[06]	AD[05]	54

Table 3-3. PCI Interface Connector Pinout: P11/J11, P21/J21 32-bit PCI (Continued)

Pin#	Signal Name	Signal Name	Pin #
55	AD[04]	GND	56
57	V(I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	GND	REQ64#	64

Notes Pins 41 and 42 have 1 k-ohm pull-ups to PMC V(I/O), but are not used otherwise.

Table 3-4. PCI Interface Connector Pinout: P12/J12, P22/J22 32-bit PCI

Pin#	Signal Name	Signal Name	Pin #
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	PCI-RSVD	8
9	PCI-RSVD	PCI-RSVD	10
11	BUSMODE2#	+3.3V	12
13	RST#	BUSMODE3#	14
15	+3.3V	BUSMODE4#	16
17	PME# (NC)	GND	18
19	AD[30]	AD[29]	20
21	GND	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL	AD[23]	26
27	+3.3V	AD[20]	28
29	AD[18]	GND	30
31	AD[16]	C/BE[2]#	32

Table 3-4. PCI Interface Connector Pinout: P12/J12, P22/J22 32-bit PCI (Continued)

Pin#	Signal Name	Signal Name	Pin #
33	GND	PMC-RSVD	34
35	TRDY#	+3.3V	36
37	GND	STOP#	38
39	PERR#	GND	40
41	+3.3V	SERR#	42
43	C/BE[1]#	GND	44
45	AD[14]	AD[13]	46
47	M66EN*	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	PMC-RSVD	52
53	+3.3V	PMC-RSVD	54
55	PMC-RSVD	GND	56
57	PMC-RSVD	PMC-RSVD	58
59	GND	PMC-RSVD	60
61	ACK64#	+3.3V	62
63	GND	PMC-RSVD	64

Note 66 MHz operation is not supported, this pin is pulled to GND through 100 ohm.

Table 3-5. PCI Interface Connector Pinout: P14/J14, P24/J24 User-Defined I/O

Pin#	Signal Name	Signal Name	Pin #
1	I/O	I/O	2
3	I/O	I/O	4
5	I/O	I/O	6
7	I/O	I/O	8
9	I/O	I/O	10
11	I/O	I/O	12
13	I/O	I/O	14
15	I/O	I/O	16
17	I/O	I/O	18
19	I/O	I/O	20
21	I/O	I/O	22
23	I/O	I/O	24
25	I/O	I/O	26
27	I/O	I/O	28
29	I/O	I/O	30
31	I/O	I/O	32
33	I/O	I/O	34
35	I/O	I/O	36
37	I/O	I/O	38
39	I/O	I/O	40
41	I/O	I/O	42
43	I/O	I/O	44
45	I/O	I/O	46
47	I/O	I/O	48
49	I/O	I/O	50
51	I/O	I/O	52
53	I/O	I/O	54

Table 3-5. PCI Interface Connector Pinout: P14/J14, P24/J24 User-Defined I/O (Continued)

Pin#	Signal Name	Signal Name	Pin #
55	I/O	I/O	56
57	I/O	I/O	58
59	I/O	I/O	60
61	I/O	I/O	62
63	I/O	I/O	64

The final table, shown below, presents the last 32 bits needed to complete the 64-bit extension.

Table 3-6. PCI 64-bit PCI extension on PMC Connector J13, J23

Pin#	Signal Name	Signal Name	Pin #
1	PCI-RSVD	GND	2
3	GND	C/BE7#	4
5	C/BE6#	C/BE5#	6
7	C/BE4#	GND	8
9	V(I/O)	PAR64	10
11	AD63	AD62	12
13	AD61	GND	14
15	GND	AD60	16
17	AD59	AD58	18
19	AD57	GND	20
21	V(I/O)	AD56	22
23	AD55	AD54	24
25	AD53	GND	26
27	GND	AD52	28
29	AD51	AD50	30
31	AD49	GND	32
33	GND	AD48	34
35	AD47	AD46	36

Table 3-6. PCI 64-bit PCI extension on PMC Connector J13, J23 (Continued)

Pin#	Signal Name	Signal Name	Pin #
37	AD45	GND	38
39	V(I/O)	AD44	40
41	AD43	AD42	42
43	AD41	GND	44
45	GND	AD40	46
47	AD39	AD38	48
49	AD37	GND	50
51	GND	AD36	52
53	AD35	AD34	54
55	AD33	GND	56
57	V(I/O)	AD32	58
59	PCI-RSVD	PCI-RSVD	60
61	PCI-RSVD	GND	62
63	GND	PCI-RSVD	64

Related Documentation A

Motorola Computer Group Documents

The Motorola publications listed below offer you additional information about this product. You can obtain paper or electronic copies of Motorola Computer Group publications by:

- Visiting Motorola Computer Group's Product Catalog for more information on PMC products at, http://www.motorola.com/computer/literature
- Contacting your local Motorola sales office
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To obtain the most up-to-date product information in PDF or HTML format, visit http://www.motorola.com/computer/literature.

Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table A-1. Manufacturers' Documents

Document Title	Motorola Publication Number
21154 PCI-to-PCI Bridge Data Sheet; Intel Corporation http://developer.intel.com/design/bridge/datashts/278108.htm	278108.pdf

Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table A-2. Related Specifications

Document Title	Motorola Publication Number
CompactPCI Hot Swap Specification PCI Industrial Computers Manufacturers Group (PICMG) http://www.picmg.org/	PICMG 2.1 R1.0
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc. http://standards.ieee.org/catalog/	P1386.1 Draft 2.0

URLs

The following URLs (uniform resource locators) may provide helpful sources of additional information about this product, related services, and development tools. Please note that, while these URLs have been verified, they are subject to change without notice.

- Motorola Computer Group, http://www.motorola.com/computer
- Motorola Computer Group OEM Services, http://www.motorola.com/computer/support

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