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IPMC712/761 I/O Module Installation and Use

VIPMCA/IH1

February 2001 Edition

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Caution

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>
> EN50082-1:1997 “Electromagnetic Compatibility—Generic Immunity Standard, Part 1. Residential, Commercial and Light Industry”

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Preface

The *IPMC712/761 Installation and Use* manual provides the information you will need to install, use, and program your IPMC712 or IPMC761 module. The IPMC712 and IPMC761 are optional I/O modules installed on the MVME5100 Single Board Computer. Their design utilizes the PowerPlus II architecture.

The IPMC712 is a variation of the IPMC761. The primary differences between the two modules are in the physical interfaces of the Ethernet port and serial ports 3 and 4. These differences along with others are discussed in the first three chapters of this manual.

As of the printing date of this manual, the following models are available:

Model Number	Product Description and I/O Features
IPMC712-001	Multifunction Rear I/O PMC Module; Ultra-Wide SCSI, One Parallel Port, Three Asynchronous and One Synchronous/Asynchronous Serial Port
IPMC761-001	Multifunction Rear I/O PMC Module; Ultra-Wide SCSI, One Parallel Port, Two Asynchronous and Two Synchronous/Asynchronous Serial Ports

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In all your correspondence, please provide the name of your company, followed by your name and position. Please be sure to include the title and part number of the manual along with a brief explanation on how you used it. Thereafter, summarize your feelings about its strengths and weaknesses and provide us with any recommendations for improvements.

Conventions Used in This Manual

The following typographical conventions are used in this document:

bold

is used for user input that you type just as it appears; it is also used for commands, options and arguments to commands, and names of programs, directories and files.

italic

is used for names of variables to which you assign values. Italic is also used for comments in screen displays and examples, and to introduce new terms.

`courier`

is used for system output (for example, screen displays, reports), examples, and system prompts.

<Enter>, **<Return>** or **<CR>**

represents the carriage return or Enter key.

Ctrl

represents the Control key. Execute control characters by pressing the **Ctrl** key and the letter simultaneously, for example, **Ctrl-d**.

Terminology

A character precedes a data or address parameter to specify the numeric format, as follows (if not specified, the format is hexadecimal):

0x	Specifies a hexadecimal number
%	Specifies a binary number
&	Specifies a decimal number

An asterisk (#) following a signal name for signals that are *level significant* denotes that the signal is *true* or valid when the signal is low.

An asterisk (#) following a signal name for signals that are *edge significant* denotes that the#actions initiated by that signal occur on high to low transition.

In this manual, *assertion* and *negation* are used to specify forcing a signal to a particular state. In particular, *assertion* and *assert* refer to a signal that is active or true; *negation* and *negate* indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

Data and address sizes are defined as follows:

Byte	8 bits, numbered 0 through 7, with bit 0 being the least significant.
Half word	16 bits, numbered 0 through 15, with bit 0 being the least significant.
Word	32 bits, numbered 0 through 31, with bit 0 being the least significant.
Double word	64 bits, numbered 0 through 63, with bit 0 being the least significant.

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Introduction 1

Product Overview

This chapter provides information necessary to install and use the IPMC712 and IPMC761 modules on your MVME5100 Single Board Computer (SBC).

The IPMC712 and IPMC761 are optional modules that provide backward compatibility with earlier Motorola Computer Group (MCG) products using the MVME761 or MVME712M transition board. Earlier MCG products include the MVME2600 and the MVME2700 family of SBCs.

Current Models

As of the publication date of this manual, there are two models of IPMC modules available for installation and use on the MVME5100 SBC. These models are the IPMC712 and the IPMC761.

Both models are designed around a PMC form factor and both modules incorporate a PCI/ISA bridge, ultra-wide SCSI adapter, and Super I/O functionality. Both modules are single wide, standard length, standard height PMC boards. They attach to the host board PCI bus via the PMC P11, P12, P13, P14, and P15 connectors.

Both modules draw +5V and +3.3V through the PMC connectors.

General Functionality

IPMC modules provide rear I/O support for:

- One single-ended ultra-wide SCSI port
- One parallel port
- Four serial ports (2 or 3 asynchronous and 1 or 2 synchronous/asynchronous, depending on the module)

With this PMC card configuration, the memory mezzanine, one PMC slot, and the PMCspan are still available, providing support for additional product customization.

MVME5100 IPMC Mode

In IPMC mode, the MVME5100 SBC supports legacy MVME761 or MVME712M I/O modules (with limited PMC I/O) when an IPMC712 or IPMC761 module is installed in PMC Slot 1. In this configuration, PMC Slot 2 contains some signals that are reserved for extended SCSI.

Design Features

The following sections describe the basic features that are incorporated in the design of both IPMC modules.

PCI Bus Interface

Both modules contain four EIA-E700 AAAB connectors, which provide a 32-bit PCI interface to an IEEE P1386.1 PMC compliant host board such as the MVME5100.

Connectors P11-P13 on each module provide the 32-bit PCI interface while P14 provides an I/O path from the module to the MVME5100.

Signals routed to P14 include: narrow SCSI, parallel port, COM1 and COM2 synchronous serial ports, COM3 and COM4 sync serial ports, power, and P2 mux signals. The remaining SCSI data lines are routed to P15.

The on-board PCI devices on each module are as follows:

- Winbond PCI to ISA Bridge (PIB)
- LSI SCSI device (SYM53C895A)

PCI-ISA Bridge (PIB)

The PIB provides the bridging functions between PCI local bus and the ISA local resource bus. The following are a few of the features of the PIB.

- Complies with PCI Specification 2.1
- Two 82C37A DMA controllers (types A, B, and F)
- Two 82C59A interrupt controllers (all IRQ inputs may be programmed for edge or level sensitivity)

SCSI

The SCSI Controller is an LSI Logic SYM53C895A device. The SCSI clock frequency is 40 MHz. The following are a few of the features of the SYM53C895A device:

- 32-bit PCI Interface with 64-bit addressing
- 8KB internal SCRIPTS RAM
- Improved PCI Caching design (improves PCI bus efficiency)

The SCSI device maintains backward compatibility with the MVME761 and P2 adapter card. It is also ultra-wide capable and has a performance of 40MB/s synchronous transfer rate across a 16-bit bus.

Note SCSI signals leading to connector P15 go through zero ohm resistors (R92-R100) before terminating at P15. When the MVME5100 PMC slot #2 is populated with an IPMC module in Slot #1, there exists a possibility for contention on these signals, which can be avoided by not installing these zero ohm jumpers.

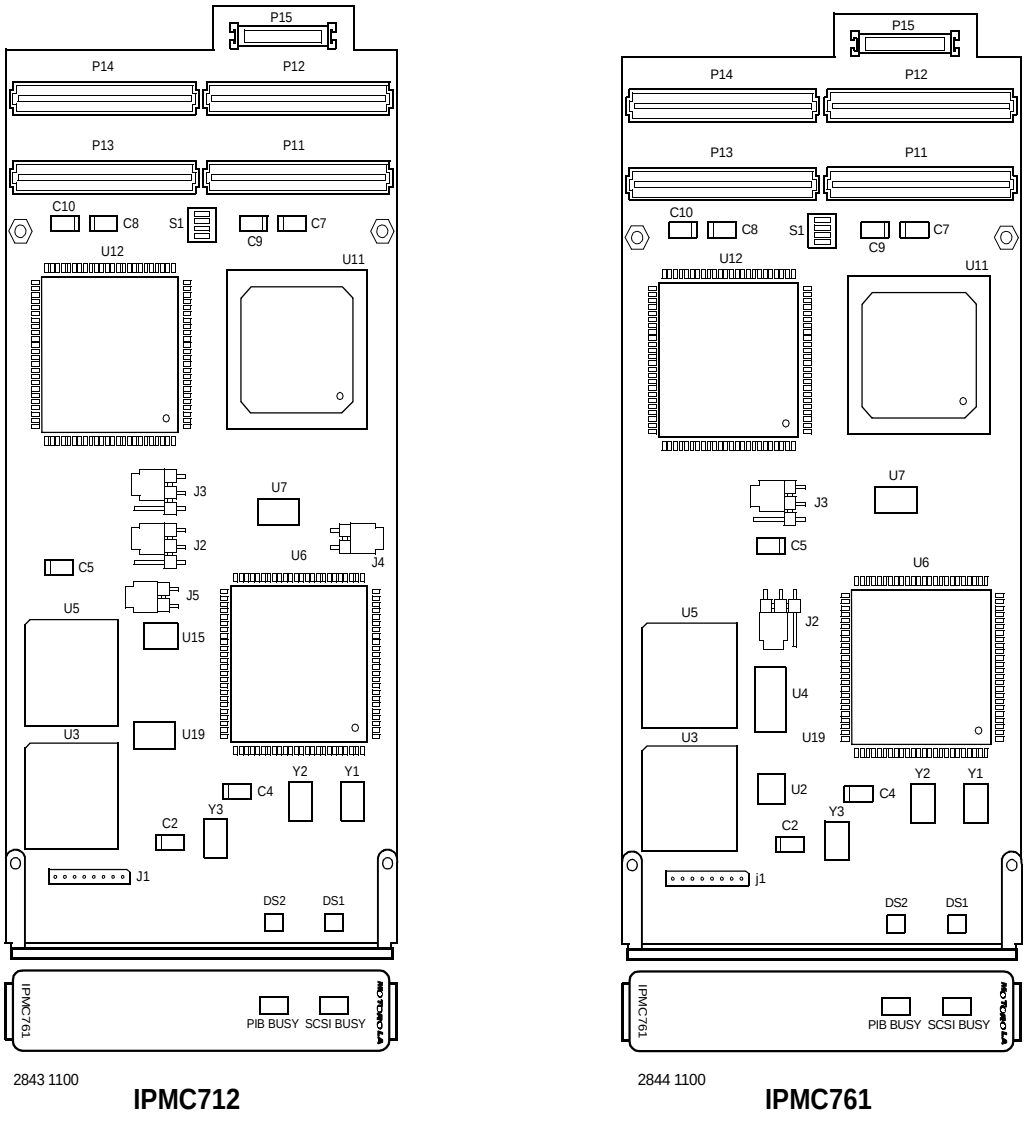


Figure 1-1. IPMC Component Layout

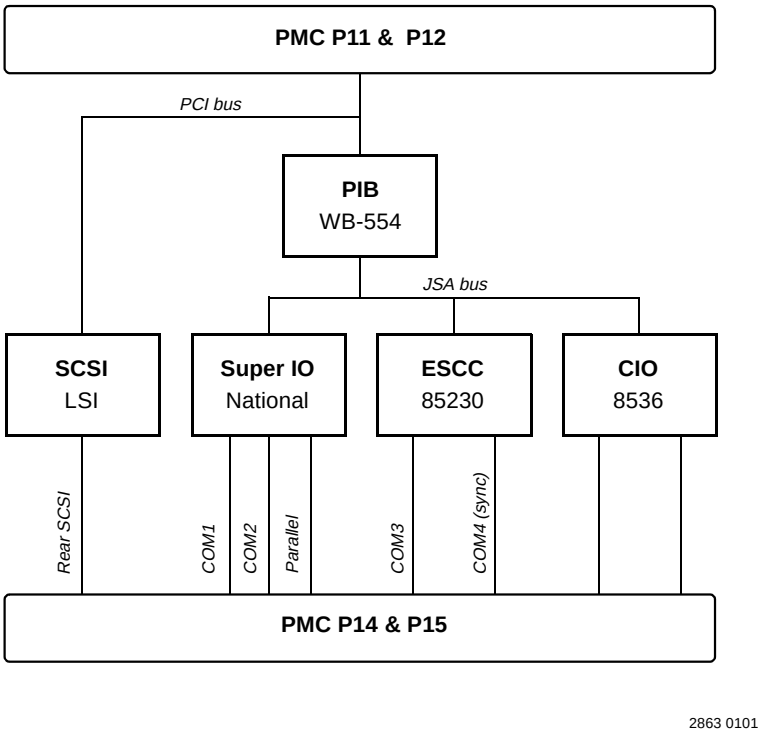


Figure 1-2. IPMC712 Functional Block Diagram

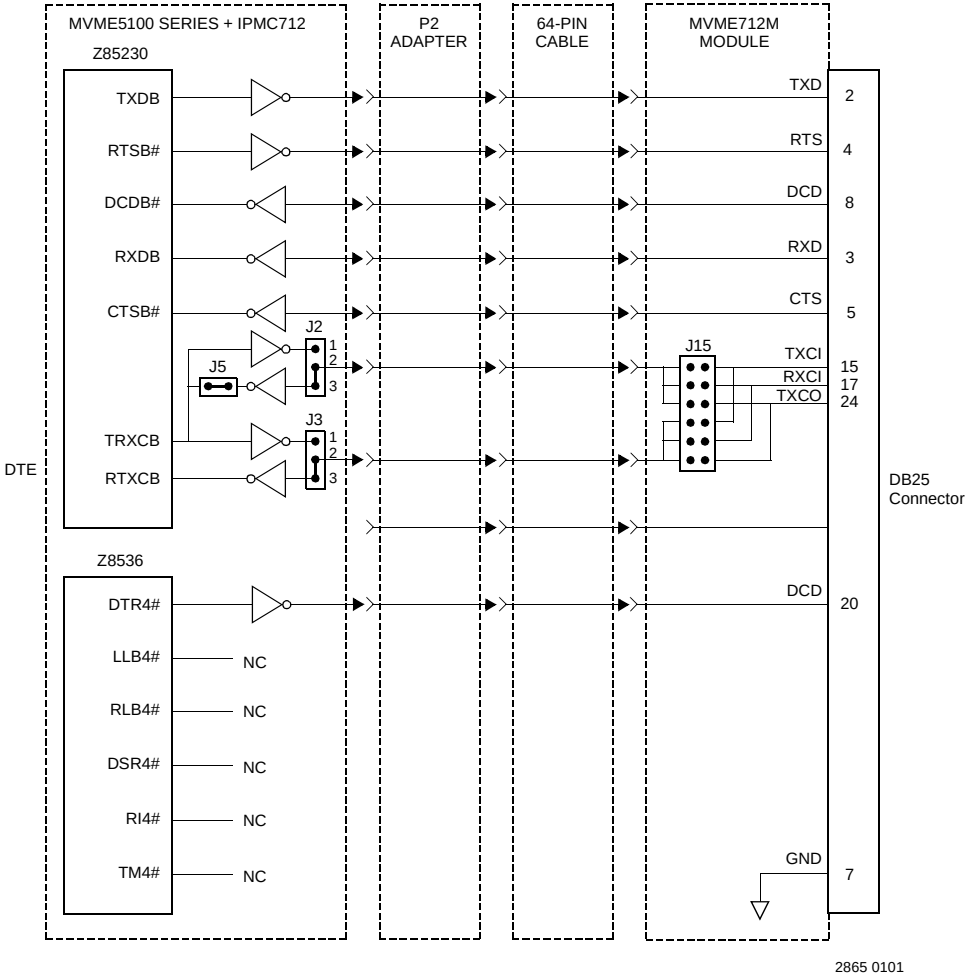


Figure 1-3. IPMC712 Serial Port 4 Clock Configuration

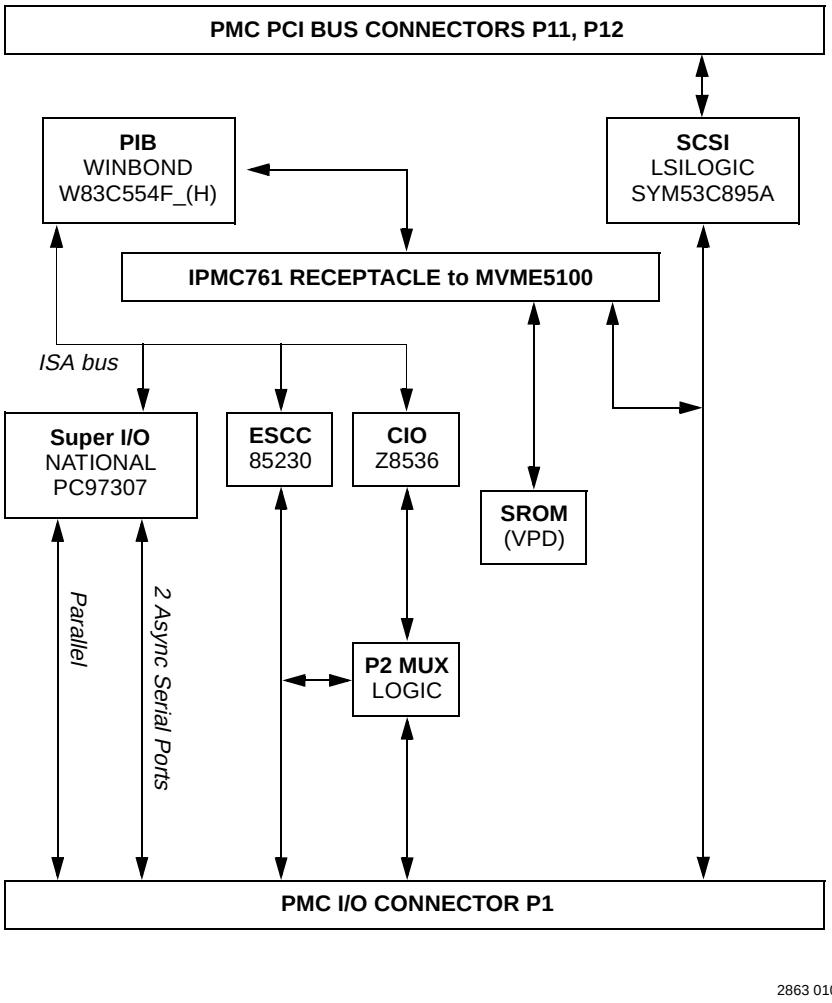


Figure 1-4. IPMC761 Functional Block Diagram

ISA Local Resource Bus

PCI-ISA Bridge (PIB)

The PIB (W83C554F) contains the ISA Bridge I/O Registers necessary for various functions. These registers are also accessible from the PCI bus.

Super I/O

The Super I/O device (PC97307) provides the following functions on the IPMC:

- Two synchronous serial ports (COM1 and COM2)
- Parallel printer port

ESCC

Two DTE synchronous/asynchronous serial ports are provided by the ESCC device (Z85230). Since the Z85230 device does not have all modem control lines, a Z8536 CIO device (described below) is used to provide the missing lines.

A PAL device is used to perform decode for the Z85230 and the Z8536 for register accesses and pseudo interrupt acknowledge cycles in the ISA I/O space. DMA supports for the Z85230 is provided by the PIB.

The clock input to the Z85230 PCLK pin is a 10 MHz clock. The Z85230 supplies an interrupt vector during a pseudo interrupt acknowledge cycle. The vector is modified based upon the interrupt source within the device.

All modem control lines from the ESCC are multiplexed/de-multiplexed through connector P2 by the P2MX function due to pin limitation of the connector.

CIO

The CIO device (Z8536) is used to provide the modem control lines not provided by the Z85230 ESCC. In addition, the device has three independent 16-bit counters/timers. The clock input to the Z8536 PCLK pin is a 5 MHz clock.

Static ROM (SROM)

Both modules contains one 3.3V, 256 x 8 serial EEPROM device (AT24C02) onboard. This device provides for Vital Product Data (VPD) storage of the module hardware configuration. The Serial EEPROM is accessed through the I^2C port in the Hawk ASIC. Its I^2C address is $A4.

Input/Output modes

Both modules are designed to be plugged into PMC Slot 1 of the MVME5100. As stated earlier, the MVME5100 has two P2 I/O modes (761 and PMC) that are user configurable with 4 jumpers on the board itself.

The jumpers route the on-board Ethernet port 2 to row C of connector P2. When used, both modules are backwards compatible with the MVME761 transition card and P2 adapter card (excluding PMC I/O routing) used on the MVME2600/2700.

LEDs

Both modules use two LEDs to provide PMC status.

- The module's green SCSI LED is lit when the SCSI device is Master.
- The module's green PIB LED is lit when the PCI bus grant to the PIB is asserted.

PCI Signaling Voltage Level

Both modules will operate with only 5V signaling levels.

RS232 Interface

On the IPMC712 module, the four serial ports are used to communicate at RS232 voltage levels (P14). The first 3 ports are fixed Asynchronous ports, while the remaining port can be configured as either a Synchronous or an Asynchronous Port.

For additional handshaking signals, Port 1 has RTS and CTS, while Ports 2, 3, and 4 have RTS, CTS, DTR, DCD. Port 4 also has configurable serial clock signals RTxC and TRxC. Jumpers J2, J3 and J5 determine the sources for these two signals (refer to Figure 1-3).

Hardware Installation 2

Introduction

This chapter discusses the installation of IPMC modules on an MVME5100 (or similar) Single Board Computer (SBC).

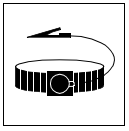
For additional information pertaining to the MVME5100 SBC, refer to the information contained in the *MVME5100 Single Board Computer Installation and Use* manual before proceeding with these instructions contained in this chapter.

Packaging

As a precautionary measure, IPMC modules are sealed in an anti-static package to protect them from static discharge. Observe standard handling practices of static sensitive equipment.

ESD Precautions

Use ESD



Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components such as disk drives, computer boards, and memory modules can be damaged by ESD. After removing the component from the system or its protective wrapper, place the component on a grounded and static-free surface (and in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available locally) that is attached to an unpainted metal part of the system chassis.

2

Installing IPMC Modules

Both the IPMC712 and the IPMC761 modules are installed on the center PMC slot of the MVME5100 SBC. As a general reminder, IPMC modules must be installed on the MVME5100 prior to installing it into the VME chassis.

To install an IPMC adapter, refer to Figure 2-1 and proceed as follows:

1. Inspect the MVME5100 and the IPMC module for evidence of any damage to the PCB itself or for evidence of any damage on the mating connectors.
2. Ensure the IPMC retention pin is installed on the MVME5100. If missing, locate the pin and install it on the MVME5100 prior to installing the IPMC module.
3. Remove the IPMC filler panel from the MVME5100 front panel.
4. Position the IPMC module over the center area of the MVME5100 as follows:
   a. Align connectors P11, P12, P13, P14, and P15 on the IPMC module with connectors J11, J12, J13, J14, and J15 on the MVME5100.
   b. Align the IPMC retention pin on the MVME5100 with the mating alignment hole on the IPMC module.
5. Install the IPMC module on the MVME5100 as follows:
   a. Sliding the IPMC module's front panel into the IPMC filler cutout slot on the MVME5100's front panel.
   b. Press the IPMC module firmly onto the MVME5100 until the mating connectors are fully seated.
6. Install four screws from the bottom of the MVME5100 into the IPMC module standoffs and securely tighten screws.

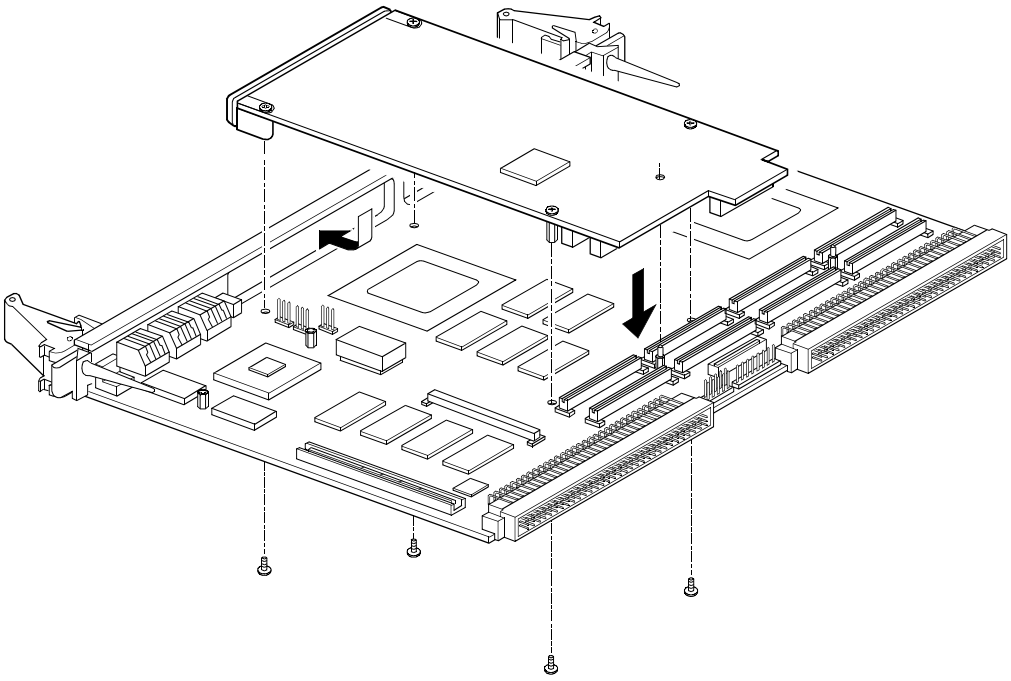


Figure 2-1. IPMC Installation

Programming 3

Introduction

Programing Details

The overall design of the IPMC712 and IPMC761 is based on the PowerPlus II architecture. The programming characteristics for both modules conforms to the PowerPlusII Programming Specification.

Note The PowerPlus II Programming Specification covers a large variety of programming configurations, many of which are not applicable to either module. This chapter describes those aspects of the specification that are unique to both modules.

PCI Local Bus

The on-board PCI devices on the IPMC712 and the IPMC761 are the PCI-ISA Bridge and the SCSI Controller.

The PCI-ISA Bridge (PIB)

The PCI-ISA Bridge (PIB) provides the bridging functions between PCI local bus and the ISA local resource bus. Other features contained in the PIB are:

- 8259 Interrupt Controller
- ISA DMA support
- Timers and counters

The SCSI Controller

The SCSI Controller's clock speed is 40 MHz. The presence of the SCSI device can be positively determined by reading the Device ID PCI Configuration Register 0*x*02 - 0*x*03. The Device ID is 0*x*0012.

The General Purpose I/O (GPIO) pin assignments for the SCSI Controller are shown in the table below. A 1x4 switch is provided to configure GPIO pins 2 and 3. The factory default setting shall be for Ultra-Speed and Ultra-Wide SCSI.

Table 3-1. GPIO Pin Assignments

GPIO Pin	Direction	Level	Usage
GPIO1_MASTER_l	output	1	SCSI LED; SCSI is not MASTER.
		0	SCSI is MASTER.
GPIO2	input	1	SCSI speed; selectable by switch S1. S1 pin 1 in off position selects Ultra-Speed.
		0	S1 pin 1 in ON position selects Ultra-FAST.
GPIO3	input	1	SCSI bus width; selectable by switch S1. S1 pin 2 in off position selects Wide-SCSI.
		0	S1 pin 2 in ON position selects Narrow-SCSI.
0, 4, 5, 6, 7, 8	-	-	Not used.

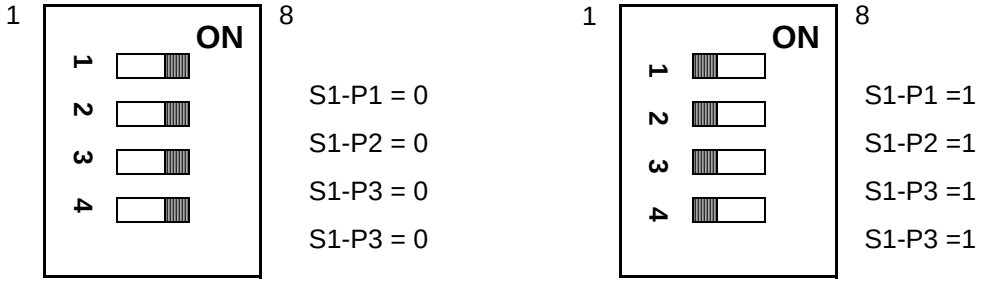


Figure 3-1. GPIO Switch Settings

IDSEL Address Assignments for PCI Local Bus

Legacy IDSEL assignment for the PCI-ISA Bridge (PIB) is maintained to ensure software compatibility between MVME2700 and MVME5100 while functioning in 761 mode. The PIB IDSEL is connected to AD11 on the IPMC761 PCI bus. The SCSI device on the modules uses the IDSEL pin J12-25 connected to AD16.

The IDSEL assignments for both modules are shown below:

Table 3-2. IDSEL Mapping for PCI Devices

Device Number Field	PCI Address Line	IDSEL Connection
0b0_1011	AD11	PCI/ISA Bridge
0b1_0000	AD16	PMC Slot 1 SCSI Device

The following table shows the Vendor ID, the Device ID, and Revision ID for each of the planar PCI devices on the IPMC712 and IPMC761:

Table 3-3. On-Board PCI Device Identification

Device	Device	Vendor ID	Device ID	Revision ID
SCSI Controller	LSI SYM53C895A	0x1000h	0x0012h	0x00h
PCI-ISA Bridge	W83C554F	0x10ADh	0x0565h	XXh

PCI Arbitration Assignments for IPMC Modules Installed on the MVME5100

PCI arbitration is performed by the Hawk ASIC on the MVME5100 which supports eight external PCI masters. This includes the Hawk itself and seven external PCI masters.

The arbitration assignments for both modules (when installed on the MVME5100) are as follows:

Table 3-4. PCI Arbitration Assignments

PCI Bus Request	PCI Master(s)
Request 1 (PARBI1)	PMC Slot 1 (SCSI device on the module in PMC Slot 1)
Request 2 (PARBI2)	PIB device on the module in PMC Slot 1

Interrupt Assignments

The interrupt architecture for the IPMC712 and IPMC761 is fully compliant with the PowerPlusII Programming Specification for a single processor board configuration.

Legacy interrupt assignment for the PCI/ISA Bridge (PIB) is maintained to ensure software compatibility between MVME2700 and IPMC761 while in 761 mode. This is accomplished by using the on-board IPMC761 connector to route the PIB's interrupt to external interrupt 0 of the Hawk's MPIC.

Likewise, the MVME5100 Ethernet port 2 is routed to the PIB's IRQ10 input. The SCSI interrupt on the IPMC761 is also routed to the PIB at IRQ14. The SCSI device is connected to the INTA# pin J11-04 of PMC Slot 1. Interrupts are routed to the Hawk from on-board resources as specified by the module's programming.

The Hawk interrupt assignments are shown below:

Table 3-5. HawPIC Interrupt Assignments

MPIC IRQ	Edge/ Level	Polarity	Interrupt Source	Notes
IRQ0	Level	High	PIB (8259) in PMC Slot 1	1
IRQ9	Level	Low	SCSI Controller interrupt shall be connected to INTA# pin J11-04	2

Notes 1. This interrupt provided for software compatibility with MVME2700.

2. MVME5100 Hawk MPIC IRQ9 interrupt sources may be one of the following: PCI-PMC1 INTA#, PMC2 INTB#, or PCIX INTA#.

ISA Local Resource Bus

The ISA devices on the IPMC712 and IPMC761 are as follows:

- PCI-ISA Bridge
- Super I/O

PCI-ISA Bridge (PIB)

The PIB contains ISA Bridge I/O Registers for various functions. These registers are accessible from the PCI bus.

Super I/O

The Super I/O device provides the following functions:

- Two serial ports (asynchronous)
- Parallel port interface

The device's hardware configuration is based on two strap-pins: BADDR0 and BADDR1. During reset, strapping options shown on BADDR0 and BADDR1 pins determine the device's operation. Clock speed is 48 MHz.

The following table shows the hardware strapping for the Super I/O device:

Table 3-6. Strap Pins Configuration

Pins	Reset Configuration
BADDR1 BADDR0	1,1 - Index Register 002Eh, Data Register 002Fh, PnP Mother board mode,Wake up in Config state

Z8536 CIO Port Pins

The following table lists Port Pins not used by the IPMC761 module.

Notes 1. The Hawk External Register Set interface now provides these functions.

2. On the IPMC712, pins PA0 through PA4, PA6, PA7, PB0 through PB4 are not used on the Z8536 CIO.

Table 3-7. Z8536 CIO Port Pins Assignment

Port Pin	Signal Name	Direction	Descriptions
PA6	BRDFAIL	Output	Not used on module
PB6	FUSE	Input	Not used on module
PB7	ABORT_	Input	Not used on module
PC1	Reserved	I/O	Not used on module
PC2	BASETYP0	Input	Not used on module
PC3	BASETYP1	Input	

ISA DMA Channels

The following table lists PIB DMA Channel Assignments not used.

Table 3-8. PIB DMA Channel Assignments

PIB Priority	PIB Label	Controller	DMA Assignment
Highest	Channel 2	DMA1	Not used on module

ISA DMA Connections/Assignments

The following table shows the DMA connections/assignments between the PC97307 and the PIB.

Table 3-9. DMA Connection/Assignments

Channel	Connection	Level	Usage
0	SCC W//REQA	high	Serial Port 3 RX
1	SCC DTR//REQA	high	Serial Port 3 TX
2	SIO DRQ2/DACK2	high	User SIO configurable, suggested use is parallel port
3	SIO DRQ3/DACK3	high	User SIO configurable, suggested use is parallel port
4	None		PIB Internal DMA cascade
5	SCC W//REQB	high	Serial Port 4 RX
6	SCC DTR//REQB	high	Serial Port 4 TX
7	None		

Interrupt Routing to PIB

Module interrupts and MVME5100 Ethernet Port 2 interrupts go through the 8259 pair and into the PIB. The output of the PIB then goes to the Hawk MPIC on the MVME5100. The table below lists the ISA interrupts routed to the PIB.

Table 3-10. PIB Interrupt Assignments

PRI	ISA IRQ	Controller	Edge/ Level	Polarity	Interrupt Source	Notes
1	IRQ0	INT1	Edge	High	Timer 1 / Counter 0	1
3-10	IRQ2		Edge	High	Cascade Interrupt from INT2	
4	IRQ9	INT2	Level	High	Z8536 CIO	2,3
					Z85230 ESCC	

Table 3-10. PIB Interrupt Assignments (Continued)

PRI	ISA IRQ	Controller	Edge/ Level	Polarity	Interrupt Source	Notes
5	IRQ10	INT2	Level	Low	PCI-Ethernet Interrupt (from MVME5100 Port 2)	2,4
9	IRQ14	INT2	Level	Low	PCI-SCSI Interrupt	2
11	IRQ3	INT1	Edge	High	COM2 (Async Serial Port 2)	
12	IRQ4		Edge	High	COM1 (Async Serial Port 1)	
15	IRQ7		Edge	High	Parallel Port Interrupt	

Notes 1. Internally generated by the PIB.

2. After a reset, all ISA IRQ interrupt lines default to edge-sensitive mode.

3. Interrupts from the Z8536 and Z85230 devices are externally wired. External logic will determine which device to acknowledge during a pseudo IACK cycle. The Z8536 CIO has higher priority than the Z85230 ESCC. This IRQ MUST be programmed for level-sensitive mode.

4. This interrupt is routed from the MVME5100 through the IPMC connector to the module's PIB to allow backward compatibility to other products.

Vital Product Data (VPD) and Serial Presence Detect (SPD) Data

These registers are accessed through the I^2C interface of the Hawk ASIC on MVME5100. The IPMC761's VPD address is $A4.

Connectors 4

Introduction

This chapter provides connector pin assignments for the IPMC712 and IPMC761 modules.

IPMC712 Connector

This connector provides the on-board interface of the IPMC712 I/O signals. The pin assignments for this connector are as follows:

Table 4-1. IPMC712 Connector

Pin	Signal Description	Signal Description	Pin
1	I^2CSCL	I^2CSDA	2
3	GND	GND	4
5	JDB8#	GND	6
7	GND	JDB9#	8
9	JDB10#	+3.3V	10
11	+3.3V	JDB11#	12
13	JDB12#	GND	14
15	GND	JDB13#	16
17	JDB14#	+3.3V	18

Table 4-1. IPMC712 Connector (Continued)

Pin	Signal Description	Signal Description	Pin
19	+3.3V	JDB15#	20
21	JDBP1#	GND	22
23	GND	LANINT2_L	24
25	PIB_INT	+3.3V	26
27	+3.3V	PIB_PMCREQ#	28
29	PIB_PMCGNT#	GND	30
31	GND	+3.3V	32
33	+5.0v	+5.0v	34
35	GND	GND	36
37	+5.0v	+5.0v	38
39	GND	GND	40

IPMC761 Connector

This connector provides the on-board interface of the IPMC761 I/O signals. The pin assignments for this connector are as follows:

Table 4-2. IPMC761 Connector

Pin	Signal Description	Signal Description	Pin
1	I^2CSCL	I^2CSDA	2
3	GND	GND	4
5	DB8#	GND	6
7	GND	DB9#	8
9	DB10#	+3.3V	10
11	+3.3V	DB11#	12
13	DB12#	GND	14
15	GND	DB13#	16
17	DB14#	+3.3V	18
19	+3.3V	DB15#	20
21	DBP1#	GND	22
23	GND	LANINT2_L	24
25	PIB_INT	+3.3V	26
27	+3.3V	PIB_PMCREQ#	28
29	PIB_PMCGNT#	GND	30
31	GND	+3.3V	32
33	+5.0v	+5.0v	34
35	GND	GND	36
37	+5.0v	+5.0v	38
39	GND	GND	40

PCI Interface and I/O Connectors

There are four 64-pin connectors on the IPMC761 (P11, P12, P13, and P14) which provide 32-bit PCI interface and P2 Input/Output (I/O) for the host board (MVME5100). The pin assignments are as follows:

Table 4-3. Connector Pin Assignments (P11)

Pin	Signal Description	Signal Description	Pin
1	TCK	-12V	2
3	GND	INTA#	4
5	INTB#	INTC#	6
7	PMCPRSNT1#	+5V	8
9	INTD#	Not Used	10
11	GND	Not Used	12
13	CLK	GND	14
15	GND	PMCGNT1#	16
17	PMCREQ1#	+5V	18
19	+5V (Vio)	AD31	20
21	AD28	AD27	22
23	AD25	GND	24
25	GND	C/BE3#	26
27	AD22	AD21	28
29	AD19	+5V	30

Table 4-3. Connector Pin Assignments (P11) (Continued)

Pin	Signal Description	Signal Description	Pin
31	+5V (Vio)	AD17	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	GND	LOCK#	40
41	SDONE#	SBO#	42
43	PAR	GND	44
45	+5V (Vio)	AD15	46
47	AD12	AD11	48
49	AD09	+5V	50
51	GND	C/BE0#	52
53	AD06	AD05	54
55	AD04	GND	56
57	+5V (Vio)	AD03	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	REQ64#	64

Table 4-4. Connector Pin Assignments (P12)

Pin	Signal Description	Signal Description	Pin
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	Not Used	8
9	Not Used	Not Used	10
11	Not Used	+3.3V	12
13	RST#	Not Used	14
15	+3.3V	Not Used	16
17	Not Used	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	+3.3V	24
25	IDSEL1	AD23	26
27	+3.3V	AD20	28
29	AD18	GND	30
31	AD16	C/BE2#	32

Table 4-4. Connector Pin Assignments (P12) (Continued)

Pin	Signal Description	Signal Description	Pin
33	GND	Not Used	34
35	TDRY#	+3.3V	36
37	GND	STOP#	38
39	PERR#	GND	40
41	+3.3V	SERR#	42
43	C/BE1#	GND	44
45	AD14	AD13	46
47	GND	AD10	48
49	AD08	+3.3V	50
51	AD07	Not Used	52
53	+3.3V	Not Used	54
55	Not Used	GND	56
57	Not Used	Not Used	58
59	GND	Not Used	60
61	ACK64#	+3.3V	62
63	GND	Not Used	64

Table 4-5. Connector Pin Assignments (P13)

Pin	Signal Description	Signal Description	Pin
1	Reserved	GND	2
3	GND	Not Used	4
5	Not Used	Not Used	6
7	Not Used	GND	8
9	+5V (Vio)	Not Used	10
11	Not Used	Not Used	12
13	Not Used	GND	14
15	GND	Not Used	16
17	Not Used	Not Used	18
19	Not Used	GND	20
21	+5V (Vio)	Not Used	22
23	Not Used	Not Used	24
25	Not Used	GND	26
27	GND	Not Used	28
29	Not Used	Not Used	30
31	Not Used	GND	32
33	GND	Not Used	34

Table 4-5. Connector Pin Assignments (P13) (Continued)

Pin	Signal Description	Signal Description	Pin
35	Not Used	Not Used	36
37	Not Used	GND	38
39	+5V (Vio)	Not Used	40
41	Not Used	Not Used	42
43	Not Used	GND	44
45	GND	Not Used	46
47	Not Used	Not Used	48
49	Not Used	GND	50
51	GND	Not Used	52
53	Not Used	Not Used	54
55	Not Used	GND	56
57	+5V (Vio)	Not Used	58
59	Reserved	Reserved	60
61	Reserved	GND	62
63	GND	Reserved	64

Table 4-6. Connector Pin Assignments (P14)

Pin	Signal Description	Signal Description	Pin
1	Not Used	DB0#	2
3	Not Used	DB1#	4
5	Not Used	DB2#	6
7	Not Used	DB3#	8
9	Not Used	DB4#	10
11	Not Used	DB5#	12
13	Not Used	DB6#	14
15	PRSTB#	DB7#	16
17	PRD0	DBP#	18
19	PRD1	ATN#	20
21	PRD2	BSY#	22
23	PRD3	ACK#	24
25	PRD4	RST#	26
27	PRD5	MSG#	28
29	PRD6	SEL#	30
31	PRD7	D/C#	32
33	PRACK#	REQ#	34

Table 4-6. Connector Pin Assignments (P14) (Continued)

Pin	Signal Description	Signal Description	Pin
35	PRBSY	O/I#	36
37	PRPE	AFD#	38
39	PRSEL	SLIN#	40
41	INIT#	TXD3	42
43	PRFLT#	RXD3	44
45	TXD1_232	RTXC3	46
47	RXD1_232	TRXC3	48
49	RTS1_232	TXD4	50
51	CTS1_232	RXD4	52
53	TXD2_232	RTXC4	54
55	RXD2_232	TRXC4	56
57	RTS2_232	Not Used	58
59	CTS2_232	Not Used	60
61	MDO	MSYNC#	62
63	MDI	MCLK	64

Specifications

A

General Specifications

The following table provides general specifications for the IPMC712 and IPMC761 module.

Table A-1. IPMC Specifications

Main Characteristic	Function	Specification
PMC INTERFACE	Address/Data	A32/D32/D64, PMC PN1, PN2, PN3, PN4 Connectors
	PCI Bus Clock	33 MHz
	Signaling	5 Volts
	Module Type	Basic, Single-Wide; P2 I/O
SCSI BUS	Controller	Symbios 53C895A
	PCI Local Bus DMA	Yes, with PCI Local Bus Burst
	Asynchronous Transfer Rate	5.0MB/s
	Ultra-SCSI Transfer Rate	20.0MB/s (8-Bit Mode), 40.0MB/s (16-Bit Mode)
	Connector	Routed to P2, 50 or 68 Pin on P2
SYNCHRONOUS SERIAL PORTS	Controller	85230/8536
	Number of Ports	2
	Configuration	TTL to P2 (Both Ports), SIM on MVME761
	Baud Rate (BPS Max)	2.5M Synchronous, 38.4K Asynchronous
	Connector	Routed to P2, HD-26 on MVME761

Table A-1. IPMC Specifications (Continued)

Main Characteristic	Function	Specification
ASYNCHRONOUS SERIAL PORTS	Controller	16C550 UART
	Number of Ports	2 (16550 Compatible)
	Configuration	EIA-574 DTE
	Asynchronous Baud Rate (BPS Max)	38.4 EIA-232, 115Kbps Raw Transfer Rate
	Connector	Routed to P2, DB-9 on MVME761
PARALLEL PORT	Controller	PC97307
	Configuration	8-Bit Bi-Directional, Full IEEE 1284 Support, Centronics Compatible
	Modes	Master Only
	Connector	Routed to P2, HD-36 on MVME761

Power Requirements

The table below lists the typical and maximum power consumption of the IPMC712 and IPMC761 modules.

Table A-2. Power Consumption

Supply Voltage	Amps (Typical)	Amps (Maximum)
+5V (±5%)	0.5 A	N/A
+12V (±10%)	0.2 A	0.5 A
-12V (±10%)	0.1 A	0.3 A

Related Documentation

B

Motorola Computer Group Documents

The Motorola publications listed below are referenced in this manual. You can obtain paper or electronic copies of Motorola Computer Group publications by:

- Contacting your local Motorola sales office
- Visiting Motorola Computer Group's World Wide Web literature site, http://www.motorola.com/computer/literature

Table B-1. Motorola Computer Group Documents

Document Title	Motorola Publication Number
MVME5100 Single Board Computer Installation and Use	V5100A/IH
MVME5100 Single Board Computer Programmer's Reference Guide	V5100A/PG
MVME2600 Series Single Board Computer Installation and Use	V2600A/IH
MVME2600 Series Single Board Computer Programmer's Reference Guide	V2600A/PG
MVME2700 Series Single Board Computer Installation and Use	V2700A/IH
MVME2700 Series Single Board Computer Programmer's Reference Guide	V2700A/PG
PPCBug Firmware Package User's Manual, Part 1 of 2	PPCBUGA1/UM
PPCBug Firmware Package User's Manual, Part 2 of 2	PPCBUGA2/UM
PPCBug Diagnostics User's Manual	PPCDIAA/UM

To obtain the most up-to-date product information in PDF or HTML format, visit http://www.motorola.com/computer/literature.

B

Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. For your convenience, a source for the listed document is also provided.

Note In many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Table B-2. Manufacturers' Documents

Document Title	Publication Number
MPC750 RISC Microprocessor Users Manual Motorola Literature Distribution Center Telephone: (800) 441-2447 or (303) 675-2140 WebSite: http://merchant.hibbertco.com/mtrlext/ E-mail: ldcformotorola@hibbertco.com	MPC750UM/AD
MPC7400 RISC Microprocessor Users Manual Motorola Literature Distribution Center Telephone: (800) 441-2447 or (303) 675-2140 WebSite: http://merchant.hibbertco.com/mtrlext/ E-mail: ldcformotorola@hibbertco.com	MPC7400UM/D
Universe II User Manual Tundra Semiconductor Corporation 603 March Road, Kanata, ON, Canada K2K 2M5 1-800-267-7231, (613) 592-0714, Fax: (613) 592-1320 http://www.tundra.com/page.cfm?tree_id=100008#Universe II (CA91C142)	8091142_MD300_01.pdf
PowerPlus II Vital Product Data Engineering Specification Motorola Literature Distribution Center Telephone: (800) 441-2447 or (303) 675-2140 WebSite: http://merchant.hibbertco.com/mtrlext/ E-mail: ldcformotorola@hibbertco.com	Revision 0.1

Related Specifications

For additional information, refer to the following table for related specifications. For your convenience, a source for the listed document is also provided.

Note In many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Table B-3. Related Specifications

Document Title and Source	Publication Number
Peripheral Component Interconnect (PCI) Local Bus Specification, PCI Special Interest Group; P.O. Box 14070 Portland, Oregon 97214-4070 Marketing/Help Line: Telephone: (503) 696-6111 Document/Specification Ordering: Telephone: 1-800-433-5177or (503) 797-4207 FAX: (503) 234-6762 http://www.pcisig.com/	PCI Specification Revision 2.0, 2.1, 2.2
IEEE - Common Mezzanine Card Specification (CMC) Institute of Electrical and Electronics Engineers, Inc. 445 Hoes Lane, P.O Box 1331 Piscataway, NJ 08855-1331 http://standards.ieee.org/catalog/	P1386 Draft 2.0
IEEE - PCI Mezzanine Card Specification (PMC) 445 Hoes Lane, P.O Box 1331 Piscataway, NJ 08855-1331 http://standards.ieee.org/catalog/	P1386.1 Draft 2.0
ANSI Small Computer System Interface-2 (SCSI-2), Draft Document Global Engineering Documents http://global.ihs.com/index.cfm	X3.131.1990

Table B-3. Related Specifications (Continued)

Document Title and Source	Publication Number
Bidirectional Parallel Port Interface Specification Institute of Electrical and Electronics Engineers, Inc. http://standards.ieee.org/catalog/	IEEE Standard 1284
VME64 Specification VITA (VMEbus International Trade Association) http://www.vita.com/	ANSI/VITA 1-1994

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