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Memory Management Board

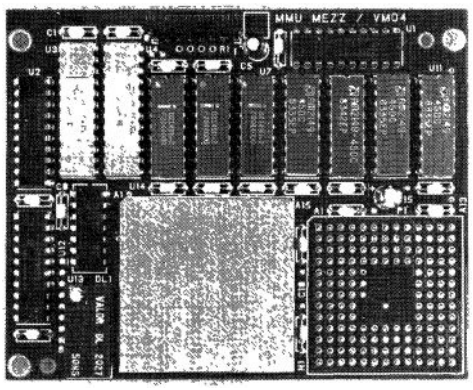
The M68KVMMB Memory Management Board (MMB) is designed to provide hardware support to MC68020/68010 users wanting to implement demand paged virtual memory systems prior to the availability of the MC68851. The MMB contains a gate array implementation of a table walking algorithm of the MC68851 and a 512 word set associative address translation cache. It is a subset of the MC68851 and is compatible to the MC68851 so that algorithms and programs developed using the MMB in a MC68020 system can be ported to the MC68851 with minor changes.

The MMB includes features that provide power and versatility for the user:

- Logical to Physical Address Translation by Chip Controlled Searching of Translation Tables in Main Memory.
- Dynamically Alterable Tree Structured Translation Tables.
- Address Translation Cache.
- 1K Byte Page Size.
- Used and Modified Bits for Pages Maintained in Translation Tables.
- Flat Address Space.
- Support of Sharing Pages Between Processes.
- Logical Address Consisting of 3-bit Function Code and 32-bit Address.
- Support for Optional 24-bit Address and for the MC68010.
- 32-bit Physical Address Output.

The MMB consists of:

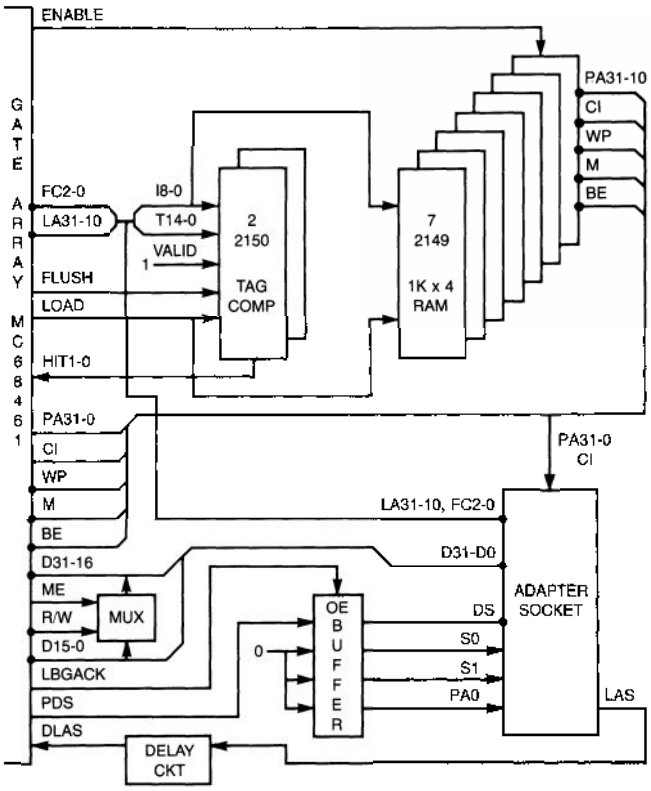
- A printed circuit board containing the Memory Management Controller MC68461 and external address translation cache. The printed circuit board is 4.5" x 3.5" and contains



a pin grid array type connector that allows it to be mounted as a mezzanine board that can be plugged into a socket reserved for the MC68851.

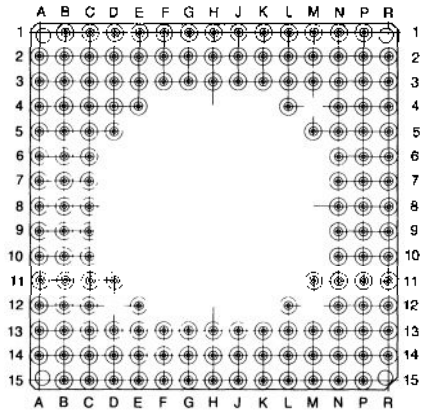
- A gate array Memory Management Controller MC68461 containing the address translation circuitry and state machine that implements the table walking algorithm of the MC68851.
- An external Address Translation Cache (ATC) consisting of a 512 entry set associative cache. The cache is a fast memory that translates logical addresses and function codes to corresponding physical addresses and protection bits. The address translation cache provides a fast mechanism for address translation by avoiding the overhead of searching translation tables on each bus access.

FIGURE 1 — MMB Block Diagram



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TABLE 1 — 149 – Terminal Pin Grid Array

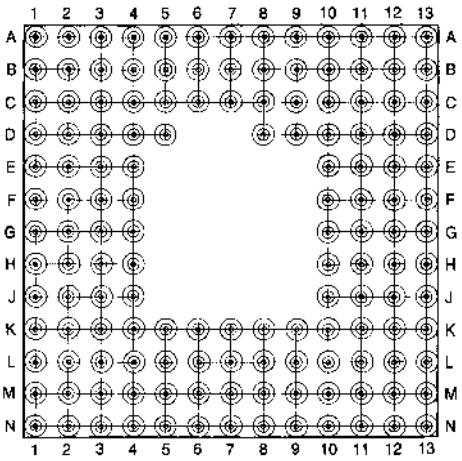


VIEWED FROM PINS

PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION
A1		C9	V_{SS}	H2	LA24	N6	V_{SS}
A2	PLDS L	C10	V_{SS}	H3	V_{CC}	N7	V_{SS}
A3	RESET L	C11	R/W	H13	V_{CC}	N8	V_{CC}
A4	DSACK1 L	C12	ENABLE L	H14	FC2	N9	V_{SS}
A5	DSACK0 L	C13	HALT L	H15	PA3	N10	V_{SS}
A6	10/20 L	C14	PA 16	J1	D19	N11	PA13
A7	BERR L	C15	PBR L	J2	D23	N12	PA15
A8	HIT0	D1	LA27	J3	V_{CC}	N13	LA14
A9	RE	D2	CLI L	J13	V_{CC}	N14	PA16
A10	WP	D3	PA27	J14	PA10	N15	PA11
A11	CLK	D4	INDEX	J15	FC0	P1	D22
A12	LAS L	D5	V_{CC}	K1	LA29	P2	PA26
A13	M	D11	V_{CC}	K2	PA29	P3	LA22
A14	LOAD L	D13	N C	K3	V_{SS}	P4	D27
A15		D14	CS L	K13	V_{SS}	P5	D21
B1	D7	D15	D3	K14	D13	P6	LA30
B2	PDSUDS L	E1	D8	K15	LA10	P7	LA21
B3	PA1	E2	D29	L1	D28	P8	D18
B4	FLUSH L	E3	D31	L2	D25	P9	D17
B5	PA17	E4	N C	L3	D26	P10	LA13
B6	HIT1	E5	V_{SS}	L4	V_{SS}	P11	LA12
B7	DS L	E12	V_{SS}	L12	V_{SS}	P12	PA12
B8	D1	E13	D2	L13	LA19	P13	D16
B9	PA2	E14	FC1	L14	D14	P14	D10
B10	LBGI L	E15	PBG L	L15	LA18	P15	LA11
B11	PBGACK L	F1	D0	M1	LA28	R2	D24
B12	TIME L	F2	PAB	M2	PA24	R3	D20
B13	PA5	F3	V_{SS}	M3	PA22	R4	LA23
B14	PA4	F13	V_{SS}	M5	V_{CC}	R5	PA21
B15	LBRO L	F14	LBGACK L	M11	V_{CC}	R6	LA26
C1	PA7	F15	PA9	M13	D9	R7	PA31
C2	PA6	G1	LA16	M14	D31	R8	D12
C3	D6	G2	LA01	M15	D15	R9	PA19
C4	PAS L	G3	V_{CC}	N1	PA28	R10	LA20
C5	ME L	G13	V_{CC}	N2	D30	R11	LA25
C6	V_{SS}	G14	D5	N3	PA23	R12	PA20
C7	V_{SS}	G15	D4	N4	PA30	R13	LA15
C8	V_{CC}	H1	LA17	N5	PA25	R14	PA14

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TABLE 2 — MMB Adapter Socket Table



VIEWED FROM COMPONENT SIDE

PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION
A1	PBR L	C11	PA04	G10	V_{SS}	L4	D23
A2	LBRI L	C12	PA05	G11	PA23	L5	D20
A3	PAS L	C13	PA06	G12	PA22	L6	D17
A4	V_{SS}	D1	LA29	G13	PA21	L7	D14
A5	LAS L	D2	LA30	H1	LA17	L8	D11
A6	ECS L	D3	LA31	H2	LA18	L9	D08
A7	R/W	D4	V_{SS}	H3	LA19	L10	D05
A8	SIZE0	D5	V_{SS}	H4	V_{CC}	L11	D02
A9	FC1	D6	N.C.	H10	V_{CC}	L12	PA11
A10	DSACK0 L	D7	N.C.	H11	PA20	L13	PA10
A11	DSACK1 L	D8	V_{CC}	H12	PA19	M1	LA09
A12	CLK	D9	V_{SS}	H13	PA18	M2	D30
A13	PA00	D10	V_{SS}	J1	LA14	M3	D27
B1	WIN	D11	PA07	J2	LA15	M4	D24
B2	PBGACK L	D12	PA31	J3	LA16	M5	D21
B3	LBRO L	D13	PA30	J4	V_{SS}	M6	D18
B4	LBGACK L	E1	LA26	J10	V_{SS}	M7	D15
B5	CLI L	E2	LA27	J11	PA17	M8	D12
B6	RESET L	E3	LA28	J12	PA16	M9	D09
B7	HALT L	E4	V_{SS}	J13	PA15	M10	D06
B8	DS L	E10	V_{SS}	K1	LA11	M11	D03
B9	FC0	E11	PA29	K2	LA12	M12	D00
B10	BERR L	E12	PA28	K3	LA13	M13	PA09
B11	PA01	E13	PA27	K4	V_{SS}	N1	LA08
B12	PA02	F1	LA23	K5	V_{SS}	N2	D31
B13	PA03	F2	LA24	K6	V_{CC}	N3	D28
C1	ASYNC L	F3	LA25	K7	V_{CC}	N4	D25
C2	10/20 L	F4	V_{CC}	K8	V_{CC}	N5	D22
C3	LBGO L	F10	V_{CC}	K9	V_{SS}	N6	D19
C4	DBDIS	F11	PA26	K10	V_{SS}	N7	D16
C5	PBG L	F12	PA25	K11	PA14	N8	D13
C6	CS L	F13	PA24	K12	PA13	N9	D10
C7	LBGI L	G1	LA20	K13	PA12	N10	D07
C8	RMC L	G2	LA21	L1	LA10	N11	D04
C9	SIZE1	G3	LA22	L2	D29	N12	D01
C10	FC2	G4	V_{SS}	L3	D26	N13	PA08

TABLE 3 — Summary of Differences Between the MC68851 and M68KVMMB

Feature	MMB	MC68851
Packaging	Gate Array Plus Support Logic	Single Pin Grid Array Device
Address Translation Cache	External, Set Associative	Internal, Fully Associative
Page Size	1K Byte	256, 512, 1K, 2K, 4K, 8K, 16K & 32K Byte
Logical Address Support	24 or 32 Bit	From 17 to 32 Bits
Supports Multiple Logical Bus Masters	No	Yes
Logical and Physical Bus Arbitration Support	Yes, But Not Identical to the MC68851	Yes
Access Level Support	Does Not Support Supervisor Root Pointer, Root Pointer Cache or DMA Root Pointer	Yes
Coprocessor Interface Support	No, Operations are Performed by Accessing Memory Mapped Locations	Yes
Translation Table Configuration	Expects One Given Table Walking Algorithm	Supports Several
Descriptor Types and Descriptor Status Bits	Some	All
Translates CPU Space Accesses	No, Acts as Peripheral Only	Yes

ORDERING INFORMATION

Part Number	Description
M68KVMMB	Memory Management Board. Includes User's Manual.
M68KVMMB/D1	Memory Management Board User's Manual.

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