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MCP750 CompactPCI Single Board Computer

Installation and Use

MCP750A/IH4

July 2000

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The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. If the equipment is supplied with a three-conductor AC power cable, the power cable must be plugged into an approved three-contact electrical outlet, with the grounding wire (green/yellow) reliably connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards and local electrical regulatory codes.

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Keep Away From Live Circuits Inside the Equipment.

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Do Not Substitute Parts or Modify Equipment.

Do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that all safety features are maintained.

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Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.



Warning

To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

Flammability

All Motorola PWBs (printed wiring boards) are manufactured with a flammability rating of 94V-0 by UL-recognized manufacturers.

EMI Caution



Caution

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used with adequate EMI protection.

Lithium Battery Caution

This product contains a lithium battery to power the clock and calendar circuitry.



Caution

Danger of explosion if battery is replaced incorrectly. Replace battery only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to the manufacturer's instructions.



Attention

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabricant.



Vorsicht

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>
> EN50082-1:1997 “Electromagnetic Compatibility—Generic Immunity Standard, Part 1. Residential, Commercial and Light Industry”

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About This Manual

This manual provides general product information; hardware preparation, installation, and operating instructions along with a functional description of the MCP750 series Single Board Computers (SBCs).

Model numbers and descriptions of the MCP750 series are included in the following table.

Model Number	Description
MCP750-1222A	MPC750-233 MHz CPU, 16MB ECC DRAM, 5MB FLASH, 1MB L2 Cache
MCP750-1232A	MPC750-233 MHz CPU, 32MB ECC DRAM, 5MB FLASH, 1MB L2 Cache
MCP750-1242A	MPC750-233 MHz CPU, 64MB ECC DRAM, 5MB FLASH, 1MB L2 Cache
MCP750-1252A	MPC750-233 MHz CPU, 128MB ECC DRAM, 5MB FLASH, 1MB L2 Cache
MCP750-1262A	MPC750-233 MHz CPU, 256MB ECC DRAM, 5MB FLASH, 1MB L2 Cache
MCP750-1432	MPC750-366 MHz CPU, 32 MB ECC DRAM, 9MB FLASH, 1MB L2 Cache
MCP750-1442	MPC750-366 MHz CPU, 64 MB ECC DRAM, 9MB FLASH, 1MB L2 Cache
MCP750-1452	MPC750-366 MHz CPU, 128 MB ECC DRAM, 9MB FLASH, 1MB L2 Cache
MCP750-1462	MPC750-366 MHz CPU, 256 MB ECC DRAM, 9MB FLASH, 1MB L2 Cache
MCP750-1431	MPC750-450MHz CPU, 32MB ECC DRAM, 9MB FLASH, 1MB L2 Cache
MCP750-1441	MPC750-450MHz CPU, 64MB ECC DRAM, 9MB FLASH, 1MB L2 Cache
MCP750-1451	MPC750-450MHz CPU, 128MB ECC DRAM, 9MB FLASH, 1MB L2 Cache
MCP750-1461	MPC750-450MHz CPU, 256MB ECC DRAM, 9MB FLASH, 1MB L2 Cache

Summary of Changes

The following changes have been made since the last release of this manual.

Date	Changes	Part Number
August 2000	Processor speed increased to 450MHz	MCP750-1431 MCP750-1441 MCP750-1451 MCP750-1461

Overview of Contents

Chapter 1, *Hardware Preparation and Installation*, includes an introduction to the MCP750, lists required equipment, gives an overview of the start-up procedure, provides unpacking instructions, and outlines base board preparation.

Chapter 2, *Operating Instructions* provides information applicable to the MCP750 family of Single Board Computers in a system configuration. This includes the power-up procedure along with descriptions of the switches and LEDs, memory maps, and software initialization.

Chapter 3, *Functional Description* describes the MCP750 single-board computer on a block diagram level. The General Description section provides an overview of the MCP750, followed by a detailed description of several blocks of circuitry.

Chapter 4, *Connector Pin Assignments* summarizes the pin assignments for the groups of interconnect signals for the MCP750 and the TMCP700.

Chapter 5, *PPCBug* provides information on the PPCBug and its architecture. Additionally, it describes the monitor (interactive command portion of the firmware), and provides instructions on using the PPCBug debugger and the associated special commands. A complete list of PPCBug commands is also included in this chapter.

Chapter 6, *CNFG and ENV Commands* contains information about the CNFG and ENV commands, system calls, and other advanced user topics.

Appendix A, *Specifications* lists the general specifications for MCP750 base boards. Subsequent sections detail cooling requirements and FCC compliance.

Appendix B, *Related Documentation* lists all documentation related to the MCP750.

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In all your correspondence, please list your name, position, and company. Be sure to include the title and part number of the manual and tell how you used it. Then tell us your feelings about its strengths and weaknesses and any recommendations for improvements.

Conventions Used in This Manual

The following typographical conventions are used in this document:

bold

is used for user input that you type just as it appears; it is also used for commands, options and arguments to commands, and names of programs, directories and files.

italic

is used for names of variables to which you assign values. Italic is also used for comments in screen displays and examples, and to introduce new terms.

`courier`

is used for system output (for example, screen displays, reports), examples, and system prompts.

<**Enter**>, <**Return**> or <**CR**>

<**CR**> represents the carriage return or Enter key.

CTRL

represents the Control key. Execute control characters by pressing the Ctrl key and the letter simultaneously, for example, **Ctrl-d**.

Hardware Preparation and Installation

1

Introduction

The MCP750 is a single-slot Compact PCI board equipped with a PowerPC™ Series microprocessor. The board can be purchased with 32MB, 64MB, 128MB, or 256MB of ECC DRAM, is provided with 1m to 9m of linear FLASH memory, IDE Compact Flash memory, and 1MB of L2 cache memory (level 2 secondary cache memory).

The complete MCP750 consists of the base (main) board plus:

- an ECC DRAM module (RAM300) for memory (shipped with the board)
- and, an Optional PCI Mezzanine Card (PMC) for additional versatility

The diagram in Figure 1-1 illustrates the architecture of the MCP750 base board.

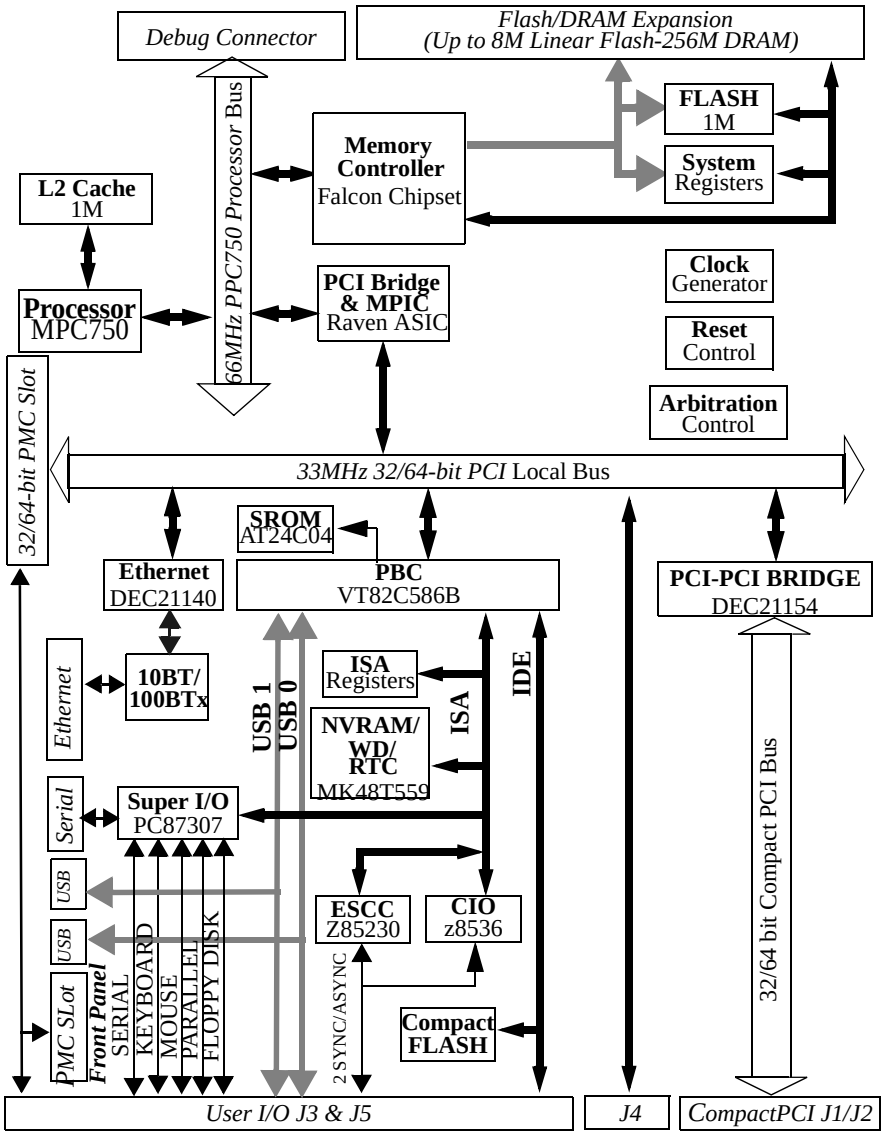


Figure 1-1. MCP750 Base Board Block Diagram

Equipment Required

The following equipment is required to complete an MCP750 system:

- CompactPCI system enclosure
- System console terminal
- Operating system (and/or application software)
- Disk drives (and/or other I/O) and controllers
- Transition module (TMCP700) and connecting cables

MCP750 modules are factory configured for I/O handling via a TMCP700 transition module. There are various MCP750 models available that correspond to different memory configurations. One transition module supports all configurations of the board.

Note Contact your local Motorola sales representative and/or your designated sales/systems engineer for the latest configuration specifications on the various MCP750 models available.

Refer also to the appropriate sections on the MCP750 and transition module installation for additional information.

Overview of Start-up Procedure

The following table lists the tasks that you will need perform before using this board. It also informs you where to find the information you need to perform each step. Be sure to read this entire chapter (including all caution and warning notes) before you begin.

Table 1-1. Startup Overview

Task	Section or Manual Reference
Unpack the hardware.	*Unpacking Instructions*
Configure the hardware by setting jumpers on the boards and transition modules.	*MCP750 Base Board Preparation* and *TMCP700 Transition Module Preparation*
Ensure CompactFLASH card is installed (if required).	*Compact FLASH Memory Card Installation*
Ensure memory mezzanines are properly installed on the board.	*RAM300 Memory Mezzanine Installation*
Install PMC Module (if required).	*PMC Module Installation*
Install the MCP750 in the chassis.	*MCP750 Module Installation*
Install transition module into chassis.	*TMCP700 Transition Module Installation*
Connect any other devices or equipment used.	Chapter 4, *Connector Pin Assignments*
	Refer also to the documentation provided with the equipment.
Power up the system.	*Applying Power*
Note that the debugger initializes the MCP750	Using the Debugger
	You may also wish to obtain the *PPCBug Firmware Package User's Manual*
Initialize the system clock.	*Using PPCBug*, *Debugger Commands*, and the SET command
Examine and/or change environmental parameters.	Chapter 6, *CNFG and ENV Commands*
Program the board as needed for your applications.	*MCP750 Series Single Board Computer Programmer's Reference Guide*, listed in *Appendix B, Related Documentation*

Unpacking Instructions

Note If the shipping carton is damaged upon receipt, request that the carrier's agent be present during the unpacking and inspection of the equipment.

Unpack the equipment from the shipping carton. Carefully check the packing list and verify that all items are present. Save the packing material for storing and reshipping of equipment.



Caution Avoid touching areas of integrated circuitry; static discharge can damage circuits.

Hardware Configuration

To produce the desired configuration and ensure proper operation of the MCP750, you may need to carry out certain hardware modifications before installing the module.

The MCP750 provides software control over most options: by setting bits in control registers after installing the module in a system, you can modify its configuration. Note that the MCP750 control registers are described in Chapter 3, *Functional Description*, and/or in the *MCP750 Series Programmer's Reference Guide* listed in Appendix B, *Related Documentation*.

Some options are not software programmable. Such options are controlled through installation or removal of jumpers or interface modules on the base board itself or the associated transition module.

MCP750 Base Board Preparation

Figure 1-2 shows the location of switches, jumpers, connectors, and LED indicators on the MCP750. Manually configured items on the base board include:

- Flash bank selection (J6)

For additional information on the configured items of the transition module, refer to the sections entitled *TMCP700 Transition Module Preparation* in this chapter or to the respective user's manuals for the transition modules (listed in Appendix B, *Related Documentation*).

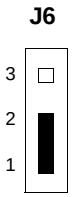
The MCP750 is factory tested and shipped with the configurations described in the following sections. The board's factory-installed debug monitor and PPCBug operates properly with these factory settings.

Flash Bank Selection (J6)

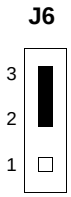
The MCP750 has provisions for 1MB of 16-bit Flash memory. The RAM300 memory mezzanine accommodates 4MB or 8MB of additional 64-bit Flash memory.

The flash memory is organized in either one or two banks, with each bank being either 16 or 64 bits wide. Bank B contains the onboard debugger and PPCBug.

To enable Flash bank A (4MB or 8MB memory on the RAM300 mezzanine), install a jumper on header J6 across pins 1 and 2. To enable Flash bank B (1MB memory on the base board), install a jumper on header J6 across pins 2 and 3.



Flash Bank A Enabled
(4MB/8MB on RAM300 mezzanine)



Flash Bank B Enabled (1MB on base board)
(Factory Configuration)

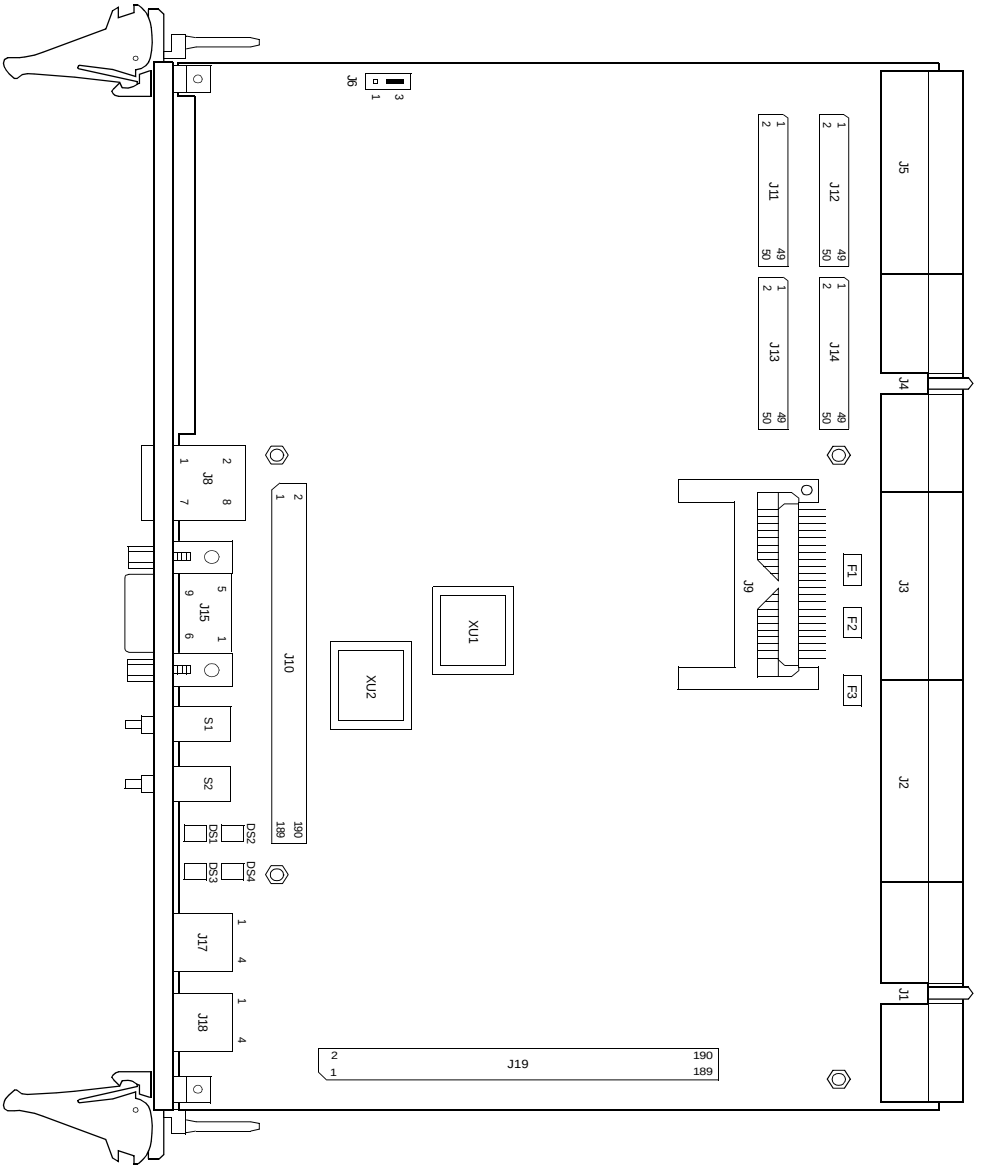


Figure 1-2. MCP750 Switches, Headers, Connectors, Fuses, LEDs

TMCP700 Transition Module Preparation

The TMCP700 transition module (refer to Figure 1-3) is used in conjunction with the MCP750 base board:

The features of the TMCP700 include:

- A parallel printer port (IEEE 1284-I compliant)
- Two EIA-232-D asynchronous serial ports (identified as COM1 and COM2 on the transition module's panel)
- Two synchronous serial ports (identified as SERIAL 3 and SERIAL 4 on the transition module's panel), configured for EIA-232-D, EIA-530, V.35, or X.21 protocols via Serial Interface Module modules
- Two Universal Serial Bus (USB) ports
- Two 60-pin Serial Interface Module (SIM) connectors, used for configuring serial ports 3 and 4
- A combination keyboard/mouse connector
- A 40-pin header for EIDE port connection
- A 34-pin header for floppy port connection
- Two 64-pin headers for PMCIO (1 ground pin provided with each signal)
- A 2-pin header for the speaker

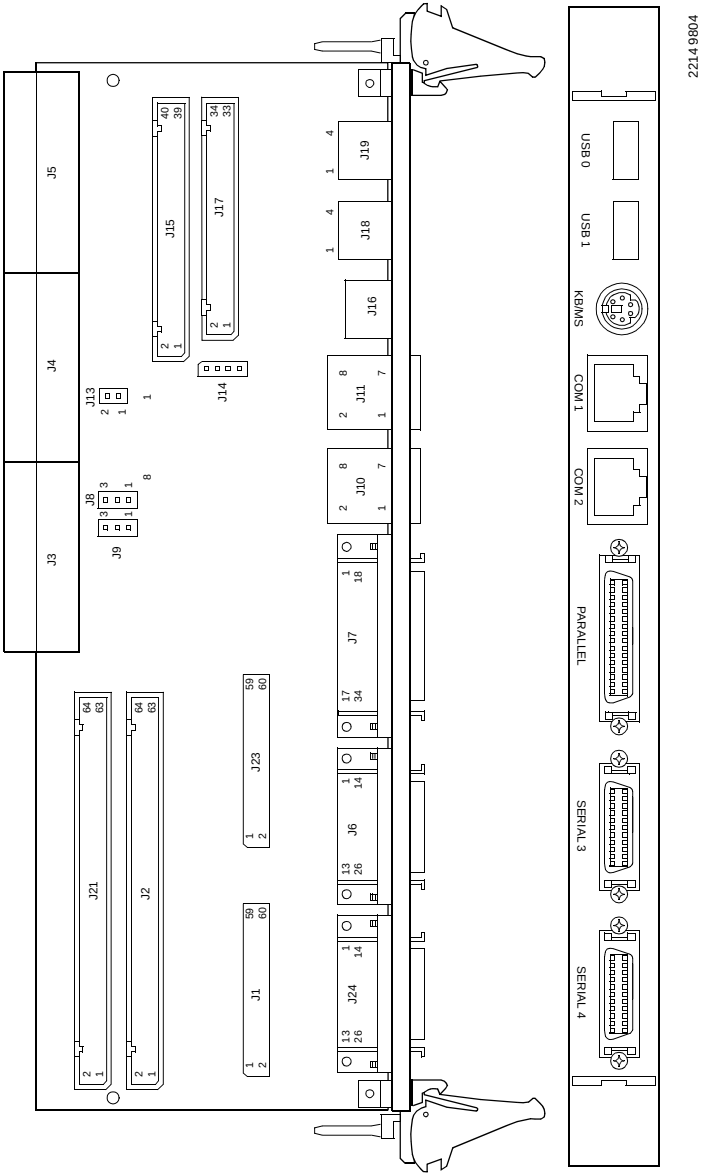


Figure 1-3. TMCP700 Connector and Header Locations

Serial Ports 1 and 2

The asynchronous serial ports (Serial Ports 1 and 2) are configured permanently as data circuit-terminating equipment (DTE). The port configuration is shown in Figure 1-4. The COM1 port is also routed to a DB9 connector on the front panel of the processor board. A terminal for COM1 may be connected to either the processor board or the transition module, but not both.

Configuration of Serial Ports 3 and 4

The synchronous serial ports (Serial Port 3 and 4) are configured through a combination of serial interface module (SIM) selection and jumper settings. The following table lists the SIM connectors and jumper headers corresponding to each of the synchronous serial ports.

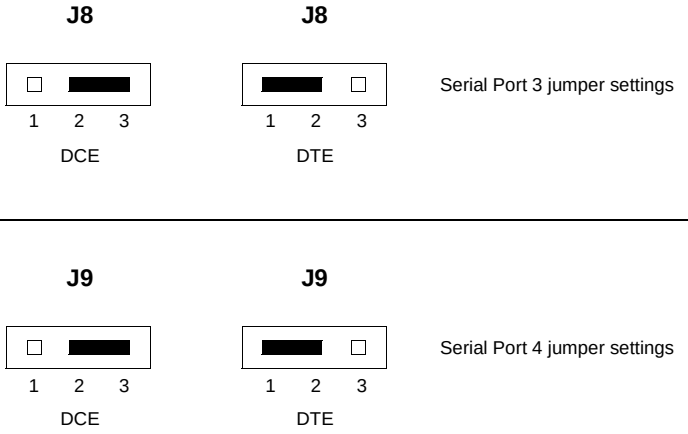
Synchronous Port	Board Connector	SIM Connector	Jumper Header
Port 3	J6	J23	J8
Port 4	J24	J1	J9

Port 3 is routed to board connector J6. Port 4 is available at board connector J24. Typical interface modules include:

- EIA-232-D (DCE and DTE)
- EIA-530 (DCE and DTE)
- V.35 (DCE and DTE)
- X.21 (DCE and DTE)

You can configure Serial Ports 3 and 4 for any of the above serial protocols by installing the appropriate serial interface module and setting the corresponding jumper. SIMs can be ordered separately as required.

Headers J8 and J9 are used to configure Serial Port 3 and 4, respectively, in tandem with SIM selection. With a jumper across pins 1-2, the port is configured as a DTE. With a jumper across pins 2-3, the port is configured as a DCE. It is important to note that the jumper setting of the port should match the configuration of the corresponding SIM module.



When installing the SIM modules, note that the headers are keyed for proper orientation.

For further information on the preparation of the transition module, refer to the user's manual for the TMCP700 (listed in Appendix B, *Related Documentation*).

The next three figures illustrate the MCP750 base board and TMCP700 transition module with the interconnections and jumper settings for DCE/DTE configuration on each serial port.

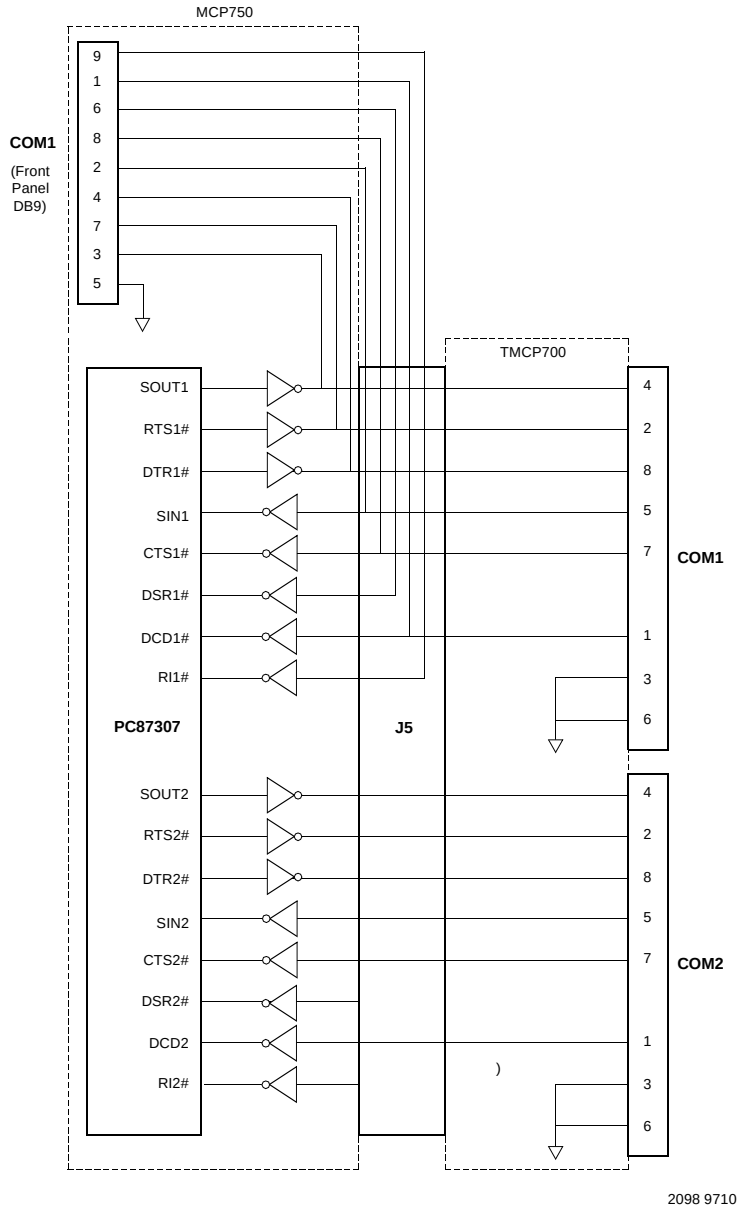


Figure 1-4. MCP750/TMCP700 Serial Ports 1 and 2 (DTE Only)

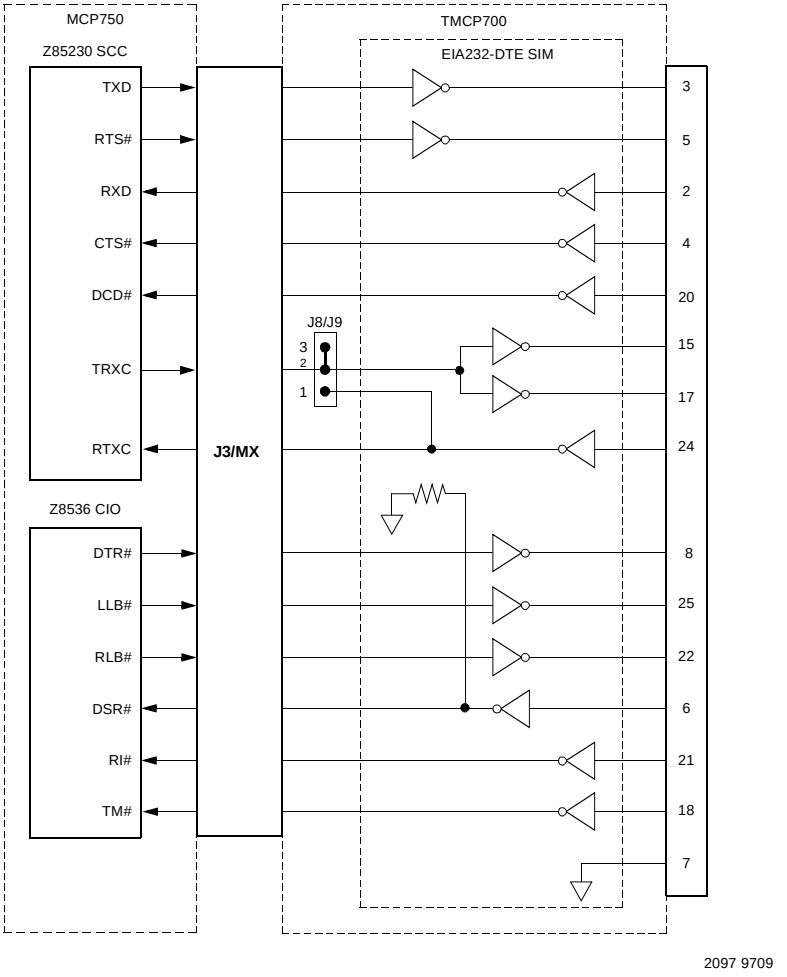


Figure 1-5. TMCP700 Serial Ports 3 and 4 DCE Configuration

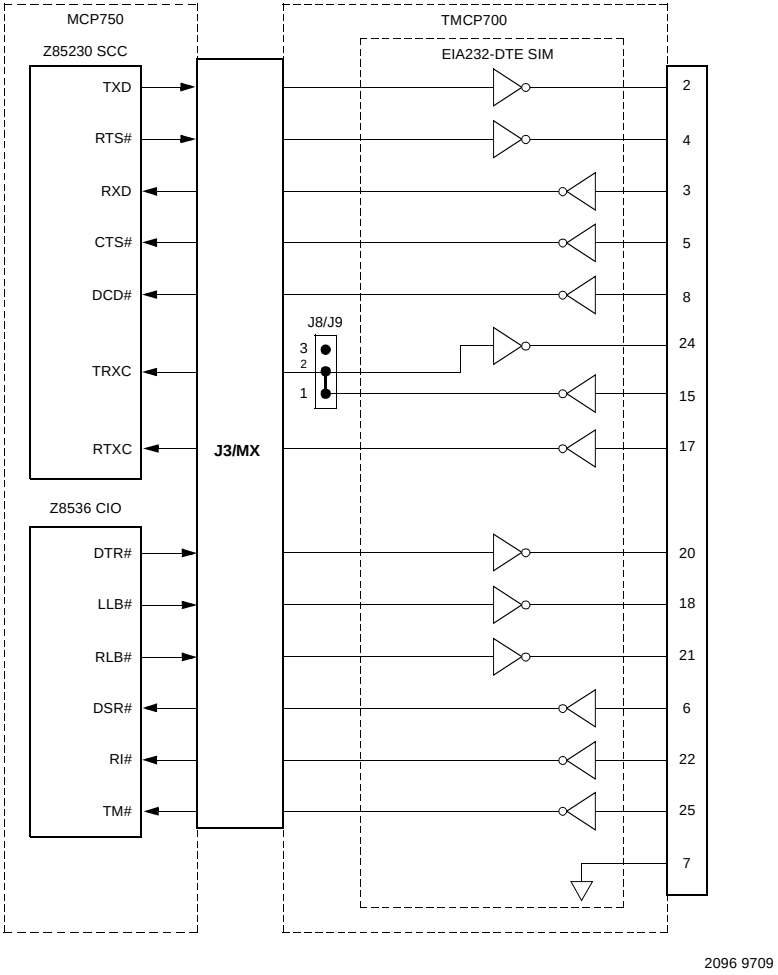


Figure 1-6. TMCP700 Serial Ports 3 and 4 DTE Configuration

Hardware Installation

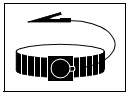
The following sections discuss the installation of mezzanine cards on the MCP750 base board, the installation of the complete MCP750 assembly into a CompactPCI chassis, and the system considerations relevant to installation. Before installing the MCP750, ensure that the serial ports and all jumpers are properly configured.

In most cases, the mezzanine card (RAM300 ECC DRAM module) is already in place on the base board. The user-configured jumpers are accessible with the mezzanines installed.

Should it be necessary to install mezzanines on the base board, refer to the following sections for a description of the installation procedure.

ESD Precautions

Use ESD



Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components such as disk drives, computer boards, and memory modules are extremely sensitive to ESD. After removing a component from the system or its protective wrapper, place the component on a grounded, static-free surface. In handling a board, place it component side up. Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available locally) attached to an unpainted metal part of the system chassis.

Compact FLASH Memory Card Installation

The Compact FLASH memory card mounts on the MCP750 base board, under the RAM300 memory mezzanine. To upgrade or install a Compact FLASH memory card, refer to Figure 1-2 and proceed as follows:

1. Attach an ESD strap to your wrist. Attach the other end of the strap to the chassis (for proper grounding). The ESD strap must be

secured to your wrist and to chassis ground throughout the procedure.

2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove the chassis or system cover(s) as necessary to access the compact PCI module.

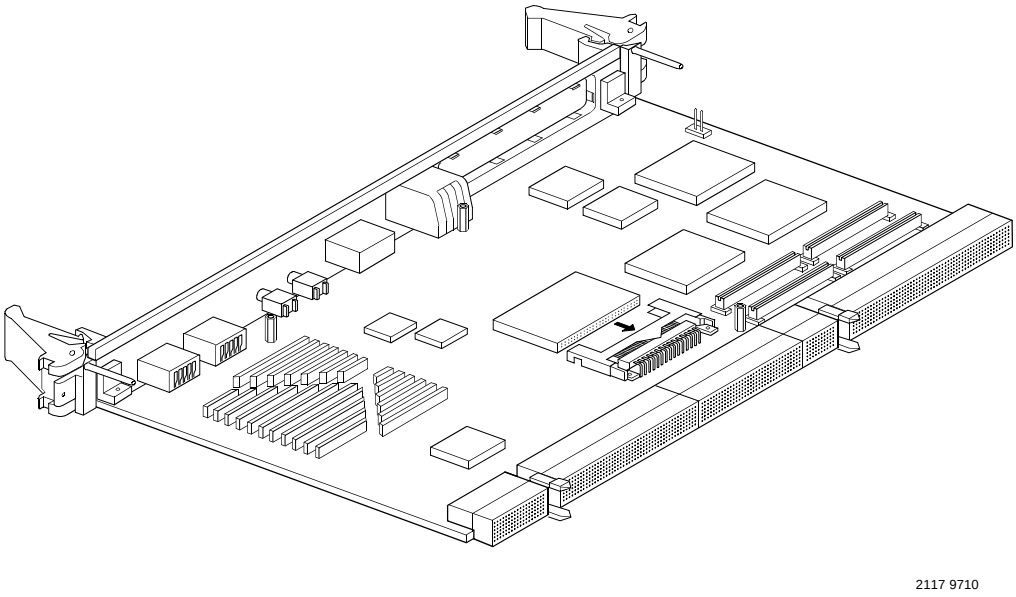


Figure 1-7. Compact FLASH Placement on MCP750

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

To prevent injury, use extreme caution when handling, testing, and adjusting this equipment. Dangerous voltages capable of causing death exist.

3. Carefully remove the MCP750 from the CompactPCI card slot and place it on a clean and adequately protected working surface with connectors J1 through J5 facing you.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

4. If necessary, remove the RAM300 mezzanine module by first removing four phillips-head screws at the corners of the mezzanine and then by gently lifting it near the connector end of the module.
5. Slide the Compact FLASH memory card into the J9 connector and ensure that pin 1 of the card aligns with pin 1 of J9.
6. Place the RAM300 mezzanine module on top of the base board. The connector on the underside of the mezzanine should connect smoothly with the corresponding connector (J10) on the MCP750.
7. Insert the four short phillips-head screws through the holes at the corners of the RAM300 mezzanine and into the standoffs on the MCP750. Tighten the screws.
8. Reinstall the MCP750 assembly in the proper card slot. Ensure that the module is properly seated in the backplane connectors. Do not damage or bend connector pins.
9. Replace the chassis or system cover(s), reconnect the system to the AC or DC power source, and turn the equipment power on.

RAM300 Memory Mezzanine Installation

The RAM300 DRAM mezzanine mounts on top of the MCP750 base board. To upgrade or install a RAM300 mezzanine, refer to Figure 1-8 and proceed as follows:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.

2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the compact PCI module.

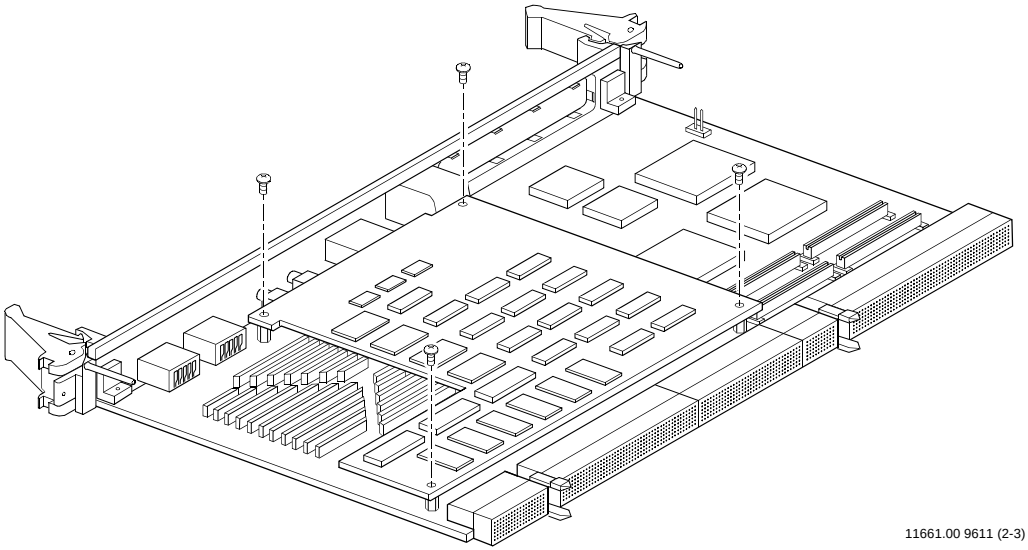


Figure 1-8. RAM300 Placement on MCP750

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

To prevent injury, use extreme caution when handling, testing, and adjusting this equipment. Dangerous voltages capable of causing death exist.

3. Carefully remove the MCP750 from the CompactPCI card slot and place it on a clean and adequately protected working surface with connectors J1 and J5 facing you.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

4. Place the RAM300 mezzanine module on top of the base board. The connector on the underside of the RAM300 should connect smoothly with the corresponding connector (J10) on the MCP750.

5. Insert the four short phillips-head screws through the holes at the corners of the RAM300 mezzanine and into the standoffs on the MCP750. Tighten the screws

6. Reinstall the MCP750 assembly in its proper card slot. Be sure the module is well seated in the backplane connectors. Do not damage or bend connector pins.

7. Replace the chassis or system cover(s), reconnect the system to the AC or DC power source, and turn the equipment power on.

PMC Module Installation

PCI mezzanine card (PMC) module mounts beside the RAM300 mezzanine on top of the MCP750 base board. To install a PMC module, refer to Figure 1-9 and proceed as follows:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.

2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the CompactPCI.

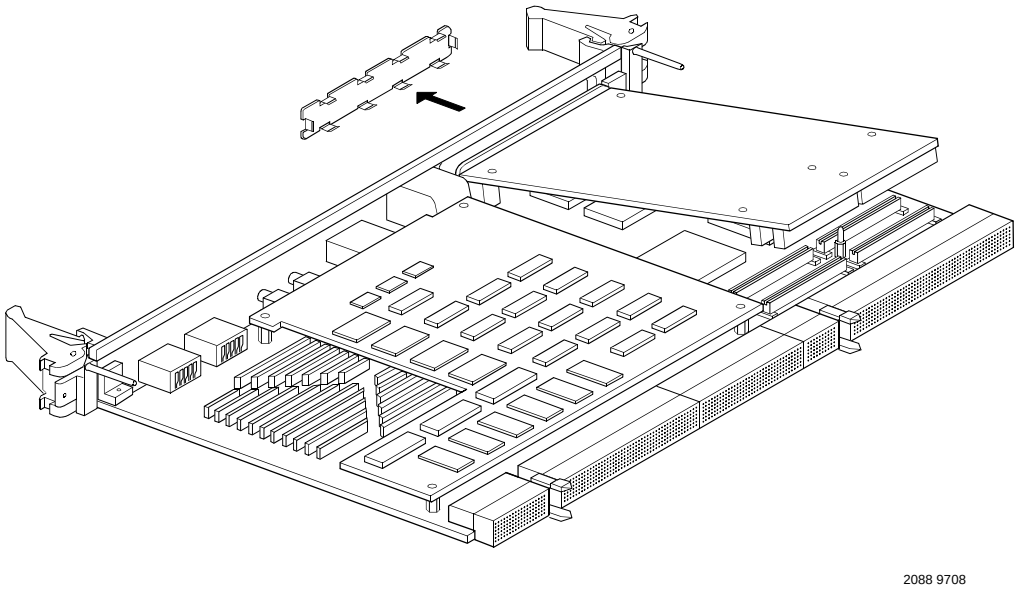


Figure 1-9. PMC Module Placement on MCP750

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

To prevent injury, use extreme caution when handling, testing, and adjusting this equipment. Dangerous voltages capable of causing death exist.

3. Carefully remove the MCP750 from the CompactPCI card slot and place it on a clean and adequately protected working surface with connectors J1 and J5 facing you.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

4. Remove the PCI filler from the front panel.
5. Slide the edge connector of the PMC module into the front panel opening from behind and place the PMC module on top of the base board. The four connectors on the underside of the PMC module should then connect smoothly with the corresponding connectors (J11/12/13/14) on the MCP750.
6. Insert the four short phillips-head screws (provided with the PMC) through the holes on the bottom side of the MCP750 and the PMC front bezel and into rear standoffs. Tighten the screws.
7. Reinstall the MCP750 assembly in its proper card slot. Be sure the module is well seated in the backplane connectors. Do not damage or bend connector pins.
8. Replace the chassis or system cover(s), reconnect the system to the AC or DC power source, and turn the equipment power on.

MCP750 Module Installation

With mezzanine board(s) installed and headers properly configured, proceed as follows to install the MCP750 in the CompactPCI chassis:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the CompactPCI modules.



Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

To prevent injury, use extreme caution when handling, testing, and adjusting this equipment. Dangerous voltages capable of causing death exist.

3. Remove the filler panel from card slot 1 (system slot).

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits

Note The MCP750 must be installed in the CompactPCI system slot in order to provide clocks and arbitration to the other slots. The system slot is identified with a triangle symbol, which is marked on the backplane. Some CompactPCI subracks may have a red guide rail to mark the system slot.

4. Set the VIO on the backplane to either 3.3V or 5V, depending upon your system's signaling requirements, and ensure the backplane does not bus J3, J4, or J5 signals.
5. Slide the MCP750 into the system slot. Grasping the top and bottom injector handles, be sure the module is well seated in the P1 through P5 connectors on the backplane. Do not damage or bend connector pins. Secure the MCP750 in the chassis with the screws provided, making good contact with the transverse mounting rails to minimize RF emissions.
6. Replace the chassis or system cover(s), making sure that no cables are pinched. Cable the peripherals to the panel connectors, reconnect the system to the AC or DC power source, and turn the equipment power on.

TMCP700 Transition Module Installation

The TMCP700 Transition Module may be required to complete the configuration of your particular MCP750 system. If so, perform the following steps to install this board. For additional information on the TMCP700 Transition Module refer, to the *TMCP700 Transition Module Installation and Use* manual (TMCP700A/IH).

1. Attach an ESD strap to your wrist. Attach the other end of the strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the chassis backplane.



Caution

Inserting or removing modules with the power applied may result in damage to the module components.



Warning

To prevent injury, use extreme caution when handling, testing, and adjusting this equipment. Dangerous voltages capable of causing death exist.

3. If Serial Ports 3 and 4 are used, be sure they are properly configured on the TMCP700 before installing the board. Refer to the section titled *TMCP700 Transition Module Preparation* for instructions on how to do this.



Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

4. With the TMCP700 in the correct vertical position that matches the pin positioning of the corresponding MCP750 board, carefully slide the transition module into the appropriate slot and seat tightly into

the backplane. Refer to Figure 1-10. TMCP700/MCP750 Mating Configuration for the correct board/connector orientation.

5. Secure in place with the screws provided, making good contact with the transverse mounting rails to minimize RF emissions.

6. Replace the chassis or system cover(s), making sure no cables are pinched. Cable the peripherals to the panel connectors, reconnect the system to the AC or DC power source, and turn the equipment power on.

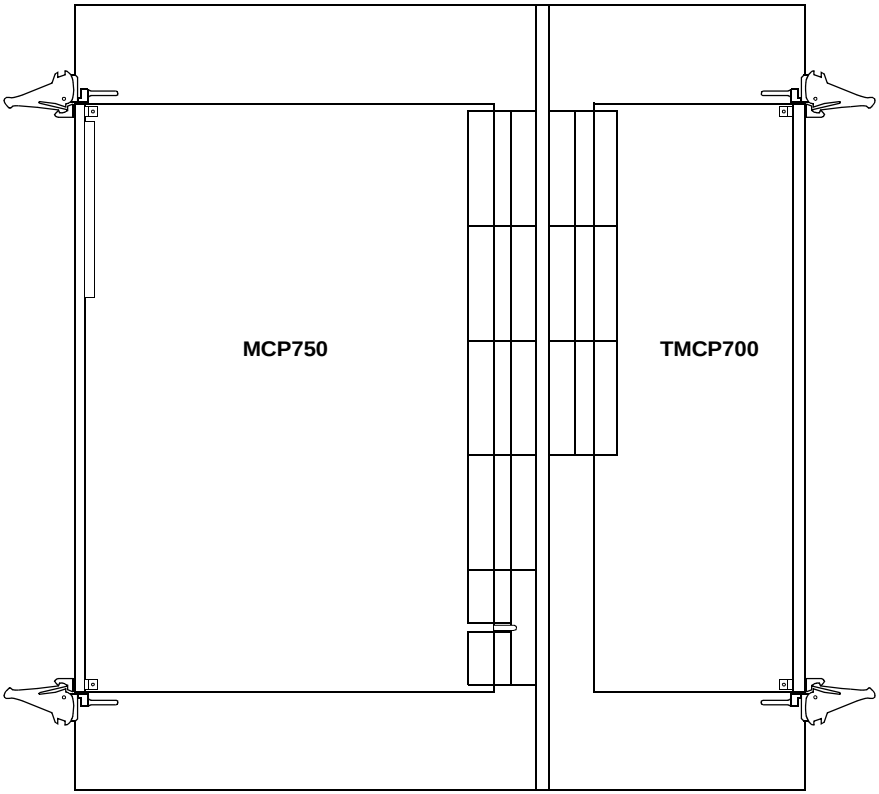


Figure 1-10. TMCP700/MCP750 Mating Configuration

System Considerations

The MCP750 is designed to operate as a CompactPCI system slot board. As a system slot board, the MCP750 provides system clocks and arbitration for the other peripheral slots in the subrack. Consequently, the MCP750 must be installed in the subrack system slot marked with the triangle symbol.

The MCP750 provides seven peripheral slot clock outputs (CLK0-CLK6) per CompactPCI specification 2.0 R2.1. These clocks are generated by the DEC21154 PCI-to-PCI bridge. Arbitration for the seven peripheral slot bus masters is provided by the MCP750 using the DEC21154 PCI-to-PCI bridge. The DEC21154 implements a programmable 2-level rotating algorithm. Refer to the DEC21154 data sheet for additional details (listed in Appendix B, *Related Documentation*).

On the MCP750 base board, the standard serial console port (COM1) serves as the PPCBug debugger console port. The firmware console should be set up as follows:

- Eight bits per character
- One stop bit per character
- Parity disabled (no parity)
- Baud rate of 9600 baud

9600 is the default baud rate for serial ports on MCP750 boards. After power-up you can reconfigure the baud rate if you wish, using the PPCBug **PF** (Port Format) command via the command line interface. Whatever the baud rate, some type of hardware handshaking — either XON/OFF or via the RTS/CTS line — is desirable if the system supports it.

MCP750 Module Power Requirements

The MCP750 module draws +5Vdc, +3.3Vdc, VIO, +12Vdc, and -12Vdc from the CompactPCI backplane connector J1. The +5Vdc and +3.3Vdc inputs are fused using 5 amp slow blow replaceable fuses (refer to Figure 1-2 for the location of the fuses and Table 3-3 on page 3-18 for

fuse assignments). The VIO, +12Vdc, and -12Vdc inputs are fused through polyswitches (resettable fuses). The +12Vdc and -12Vdc voltages are used only by the SIM modules on the TMCP700.

All fused voltages are available on either J3, J4 or J5 for use on the transition module. Separately fused +5Vdc is also provided for the keyboard/mouse. Separate +5Vdc fused power is also provided for each USB channel and the PMC slot +5V. See Table 3-3 on page 3-18 for fuse assignments.

Operating Instructions 2

Introduction

This chapter provides information applicable to the MCP750 family of Single Board Computers in a system configuration. This includes the power-up procedure along with descriptions of the switches and LEDs, memory maps, and software initialization.

Applying Power

After you have verified that all the necessary hardware preparation has been done (with all connections made correctly) and that the installation is complete, you can power up the system. The MPU, hardware, and firmware initialization process is performed by the PowerPC™ PPCBug power-up or system reset. The firmware initializes the devices on the SBC module in preparation for booting the operating system.

The firmware is shipped from the factory with an appropriate set of defaults. In most cases there is no need to modify the firmware configuration before you boot the operating system.

The following flowchart shows the basic initialization process that takes place during PowerPC system startup.

For additional information on PPCBug, refer to Chapter 5, *PPCBug*, or to the *PPCBug Firmware Package User's Manual*, listed in Appendix B, *Related Documentation* (PPCBUGA1/UM and PPCBUGA2/UM).

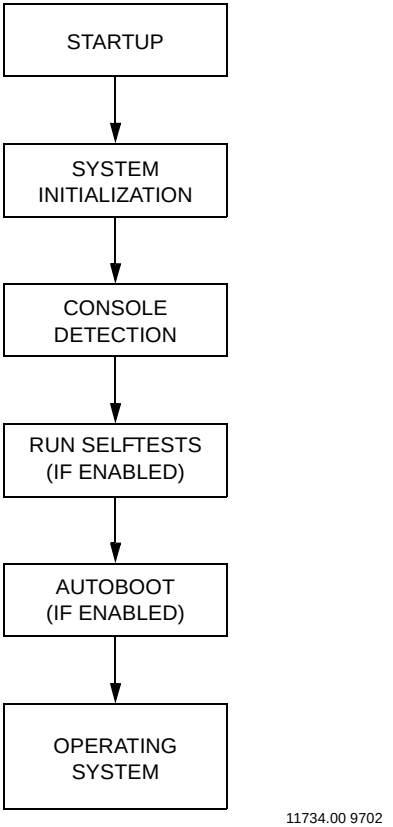


Figure 2-1. PPCBug System Startup

The MCP750 front panel has ABORT and RESET switches and four LED status indicators (BFL, CPU, PCI, CPCI). For additional information on front panel operation, refer to Chapter 3, *Functional Description*.

Memory Maps

There are three points of view for memory maps:

- The mapping of all resources as viewed by the processor (MPU bus memory map)
- The mapping of onboard resources as viewed by PCI local bus masters (PCI bus memory map)
- The mapping of onboard resources as viewed by the CompactPCI bus

The following sections provide a general description of the MCP750 memory organization from three points of view listed above. Detailed memory maps can be found in the MCP750 *Series Single Board Computer Programmer's Reference Guide* (MCP750A/PG).

Processor Memory Map

The processor memory map configuration is under the control of the Raven bridge controller ASIC and the Falcon memory controller chip set. The Raven and Falcon devices adjust system mapping to suit a given application via programmable map decoder registers. At system power-up or reset, a default processor memory map takes over.

Default Processor Memory Map

The default processor memory map that is valid at power-up or reset remains in effect until reprogrammed for specific applications. Table 2-1 defines the entire default memory map ($00000000 to $FFFFFFFF).

Table 2-1. Processor Default View of the Memory Map

Processor Address		Size	Definition	Notes
Start	End			
00000000	7FFFFFFF	2GB	Not Mapped	
80000000	8001FFFF	128KB	PCI/ISA I/O Space	1
80020000	FEF7FFFF	2GB-16MB-640KB	Not Mapped	
FEF80000	FEF8FFFF	64KB	Falcon Registers	

Table 2-1. Processor Default View of the Memory Map

Processor Address		Size	Definition	Notes
Start	End			
FEF90000	FEFEFFFF	384KB	Not Mapped	
FEFF0000	FEFFFFFF	64KB	Raven Registers	
FF000000	FFEFFFFF	15MB	Not Mapped	
FFF00000	FFFFFFFF	1MB	ROM/Flash Bank A or Bank B	2

Notes 1. Default map for PCI/ISA I/O space. Allows software to determine whether the system is MPC105-based or Falcon/Raven-based by examining either the PHB Device ID or the CPU Type register.

2. The first 1MB of ROM/Flash bank A (soldered 4MB or 8MB ROM/Flash) appears in this range after a reset if the **rom_b_rv** control bit in the Falcon's ROM B Base/Size register is cleared. If the **rom_b_rv** control bit is set, this address range maps to ROM/Flash bank B (socketed 1MB ROM/Flash).

For detailed processor memory maps, including suggested PREP-compatible memory maps, refer to the *MCP750 Series Single Board Computer Programmer's Reference Guide* (MCP750A/PG).

PCI Local Bus Memory Map

The PCI memory map is controlled by the Raven ASIC and by the 21154 PCI-to-PCI bridges. The Raven and the PCI-to-PCI bridges adjust system mapping to suit a given application via programmable map decoder registers.

A no default PCI memory map exists. Resetting the system turns the PCI map decoders off and they must be reprogrammed in software for the intended application.

For detailed PCI memory maps, including suggested PREP-compatible memory maps, refer to the *MCP750 Series Single Board Computer Programmer's Reference Guide* (part number MCP750A/PG).

CompactPCI Memory Map

The processor will access devices on the CompactPCI busses by using transaction forwarding provided by the DEC 21154 PCI-to-PCI bridge. Transaction forwarding within the 21154 is based on address ranges defined in the 21154 base and limit registers. The 21154 provides registers for I/O, memory, and prefetchable memory spaces. These registers define the address range for which PCI transactions are forwarded downstream from the primary PCI bus to the CompactPCI bus (secondary bus). All devices on the CompactPCI bus must be configured for addressing within this defined range. Conversely, these registers also define the addresses for which transactions will be forwarded upstream. Any CompactPCI bus address, generated by a CompactPCI bus master, not in the defined memory range, will be forwarded upstream, to the Primary PCI bus. There is no address translation between CompactPCI busses and the Primary PCI bus.

Recommendations for CompactPCI mapping, including suggested PREP-compatible memory maps, can be found in the *MCP750 Series Single Board Computer Programmer's Reference Guide* (MCP750A/PG).

PCI Arbitration

There are 6 potential local PCI bus masters on the MCP750 single-board computer:

- Raven ASIC (MPU/PCI bus bridge controller)
- DEC 21154 PCI-to-PCI bridge
- External PCI bus master via J4 connector
- VIA 82C586B PBC (Peripheral Bus Controller) PCI/ISA bridge
- DEC 21140 Ethernet Controller

- PMC Slot (PCI mezzanine card)

The arbitration for these six bus mastering devices is provided by custom onboard hardware. This arbiter implements a rotating priority scheme in which the last master granted becomes the lowest priority. The order of rotation is shown in the list above.

Interrupt Handling

The Raven ASIC provides an MPIC Interrupt Controller to handle various interrupt sources. It controls PHB (PCI Host Bridge) MPU/local bus interface functions on the MCP750 as well as performing interrupt handling. Sources of interrupts may be any of the following:

- The Raven ASIC itself (timer interrupts or transfer error interrupts)
- The processor (processor self-interrupts)
- The Falcon chip set (memory error interrupts)
- The PCI bus (interrupts from PCI devices)
- The CPCI bus (interrupts from CPCI devices)
- Power monitor interrupts
- Watchdog timer interrupt
- The ISA bus (interrupts from ISA devices)

For details on interrupt handling, refer to the *MCP750 Series Single Board Computer Programmer's Reference Guide* (part number MCP750A/PG).

DMA Channels

The PBC supports seven DMA channels. Channels 0 through 3 support 8-bit DMA devices. Channels 5 through 7 are dedicated to 16-bit DMA devices. The channels are allocated as follows:

Table 2-2. PBC DMA Channel Assignments

PBC Priority	PBC Label	Controller	DMA Assignment
1	Channel 0	DMA1	Serial Port 3 Receiver (Z85230 Port A Rx)
2	Channel 1		Serial Port 3 Transmitter (Z85230 Port A Tx)
3	Channel 2		Floppy Drive Controller
4	Channel 3		Parallel Port
5	Channel 4	DMA2	Not available — Cascaded from DMA1
6	Channel 5		Serial Port 4 Receiver (Z85230 Port B Rx)
7	Channel 6		Serial Port 4 Transmitter (Z85230 Port B Tx)
8	Channel 7		Not Used

Sources of Reset

The MCP750 SBC has five potential sources of reset:

1. Power-on/Undervoltage Reset.
2. Front Panel RESET switch (will generate a hard reset when depressed).
3. Watchdog timer Reset function controlled by the SGS-Thomson MK48T559 Watchdog Timer or the Raven Watchdog Timer.
4. Port 92 Register via the PBC
5. CompactPCI Bus via the 21154 Bridge Control Register.

The following table shows which devices are affected by the various types of resets. For details on using resets, refer to the *MCP750 Series Single Board Computer Programmer's Reference Guide* (MCP750A/PG).

Table 2-3. Classes of Reset and Effectiveness

Device Affected / Reset Source	Processor	Raven ASIC	Falcon Chip Set	PCI Devices	ISA Devices	Compact PCI Busses
Power-On/undervoltage	√	√	√	√	√	√
Front Panel Reset switch	√	√	√	√	√	√
Watchdog Timer reset	√	√	√	√	√	√
S/W Hard Reset (PBC Port 92 Register)	√	√	√	√	√	√
CompactPCI Reset (21154 BCR)						√

Endian Issues

The MCP750 supports both little-endian and big-endian software. The PowerPC is inherently big-endian, while the PCI bus is inherently little-endian. The following sections summarize how the MCP750 handles software and hardware differences in big- and little-endian operations. For further details on endian considerations, refer to the MCP750 *Series Single Board Computer Programmer's Reference Guide* (MCP750A/PG).

Processor/Memory Domain

The MPC750 processor can operate in both big-endian and little-endian mode. However, it always treats the external processor/memory bus as big-endian by performing *address rearrangement and reordering* when

running in little-endian mode. The PPC registers in the Raven PCI bus bridge controller ASIC and the Falcon memory controller chip set, as well as DRAM, ROM/Flash, and system registers, always appear as big-endian.

Role of the Raven ASIC

Because the PCI bus is little-endian, the Raven performs byte swapping in both directions (from PCI to memory and from the processor to PCI) to maintain address invariance while programmed to operate in big-endian mode with the processor and the memory subsystem.

In little-endian mode, the Raven *reverse-rearranges* the address for PCI-bound accesses and *rearranges* the address for memory-bound accesses (from PCI). In this case, no byte swapping is done.

PCI Domain

The PCI bus is inherently little-endian. All devices connected directly to the PCI bus operate in little-endian mode, regardless of the mode of operation in the processor's domain.

PCI and Ethernet

Ethernet is also byte-stream-oriented; the byte having the lowest address in memory is the first one to be transferred regardless of the endian mode. Since the Raven maintains address invariance in both little-endian and big-endian mode, no endian issues should arise for Ethernet data. Big-endian software must still take the byte-swapping effect into account when accessing the registers of the PCI/Ethernet device, however.

Functional Description 3

Introduction

This chapter describes the MCP750 single-board computer on a block diagram level. The *General Description* section provides an overview of the MCP750, followed by a detailed description of several blocks of circuitry. Figure 3-1 shows a block diagram of the board's architecture.

Detailed descriptions of other MCP750 blocks, including programmable registers in the ASICs and peripheral chips, can be found in the *Programmer's Reference Guide* (MCP750A/PG). You may also refer to this guide for a more detailed functional description of the MCP750.

Features

The following table summarizes the features of the MCP750 single-board computers.

Table 3-1. MCP750 Features

Feature	Description
Microprocessor	MPC750 PowerPC processor (233 MHz, 366 MHz, or 450MHz)
ECC DRAM	16MB-256MB on RAM300 module
L2 cache memory	Populated with 1MB on base board
Flash Memory	Two 32-pin PLCC sockets (1MB 16-bit Flash) on base board; two banks (4MB or 8MB 64-bit Flash) on RAM300 module
Real-time clock	8KB NVRAM with RTC and battery backup (SGS-Thomson M48T559)
Switches	RESET and ABORT
Status LEDs	four: BFL, CPU, PCI, and CPCI
Tick timers	Three programmable 16-bit timers
Watchdog timer	Provided in SGS-Thomson M48T559 or Raven 3

Table 3-1. MCP750 Features (Continued)

Feature	Description
Interrupts	Software interrupt handling via Raven (PCI-MPU bridge) and Peripheral Bus Controller
Serial I/O	1 async port (COM1) via front panel. 2 async ports, 2 sync/async ports via the transition module
Parallel I/O	IEEE 1284 bidirectional parallel port (PC87307 SIO) via the transition module
Ethernet I/O	10/100 Base-T connection via the front panel
PCI interface	One IEEE P1386.1 PCI Mezzanine Card (PMC) slot; one 110 pin CompactPCI connector (J4) for PCI expansion.
Keyboard/mouse interface	Support for keyboard and mouse input (PC87307 SIO) via the transition module
Floppy disk controller	Support for floppy disk drive (PC87307 SIO) via the transition module
CompactPCI	33MHz, 64-bit CompactPCI interface with DEC 21154 PCI-to-PCI bridge.
USB I/O	USB Host/Hub interface with two ports routed to the front panel or transition module
EIDE	Primary EIDE port routed to onboard Compact FLASH connector. Secondary EIDE port routed to the transition module

General Description

The MCP750 is a single-slot single-board computer equipped with an MPC750 PowerPC™ 750 Series microprocessor. The processor implements a backside cache controller and the board comes with 1MB of cache memory.

As shown in the *Features* section, the MCP750 offers many standard features desirable in a CompactPCI computer system—such as PCI Bridge and Interrupt Controller, an ECC Memory Controller chipset, 5MB to 9MB of linear FLASH memory, IDE Compact Flash memory, 16M to 256MB of ECC-protected DRAM, interface to a CompactPCI bus, and several I/O peripherals.

The I/O peripheral interfaces present on the onboard PCI bus include: a 10/100 Base-T Ethernet interface, a USB host controller, an ISA master/slave interface, a Fast EIDE interface and one PMC Slot. Functions provided from the ISA bus are two async and two sync/async serial ports, keyboard, mouse, a floppy disk controller, printer port, a real time clock, and NVRAM.

The MCP750 interfaces to a CompactPCI bus using a DEC 21154 PCI-to-PCI bridge device. This device provides a 64-bit primary and a 64-bit secondary interface allowing full 64-bit data access between CompactPCI bus devices and the host/PCI bridge. This bus is capable of driving seven CompactPCI slots.

Another key feature of the MCP750 family is the PCI (Peripheral Component Interconnect) bus. In addition to the on-board local bus peripherals, the PCI bus supports an industry-standard mezzanine interface, IEEE P1386.1 PMC (PCI Mezzanine Card). PMC modules offer a variety of possibilities for I/O expansion. The base board supports PMC I/O for the front panel or J3/TMCP700.

Block Diagram

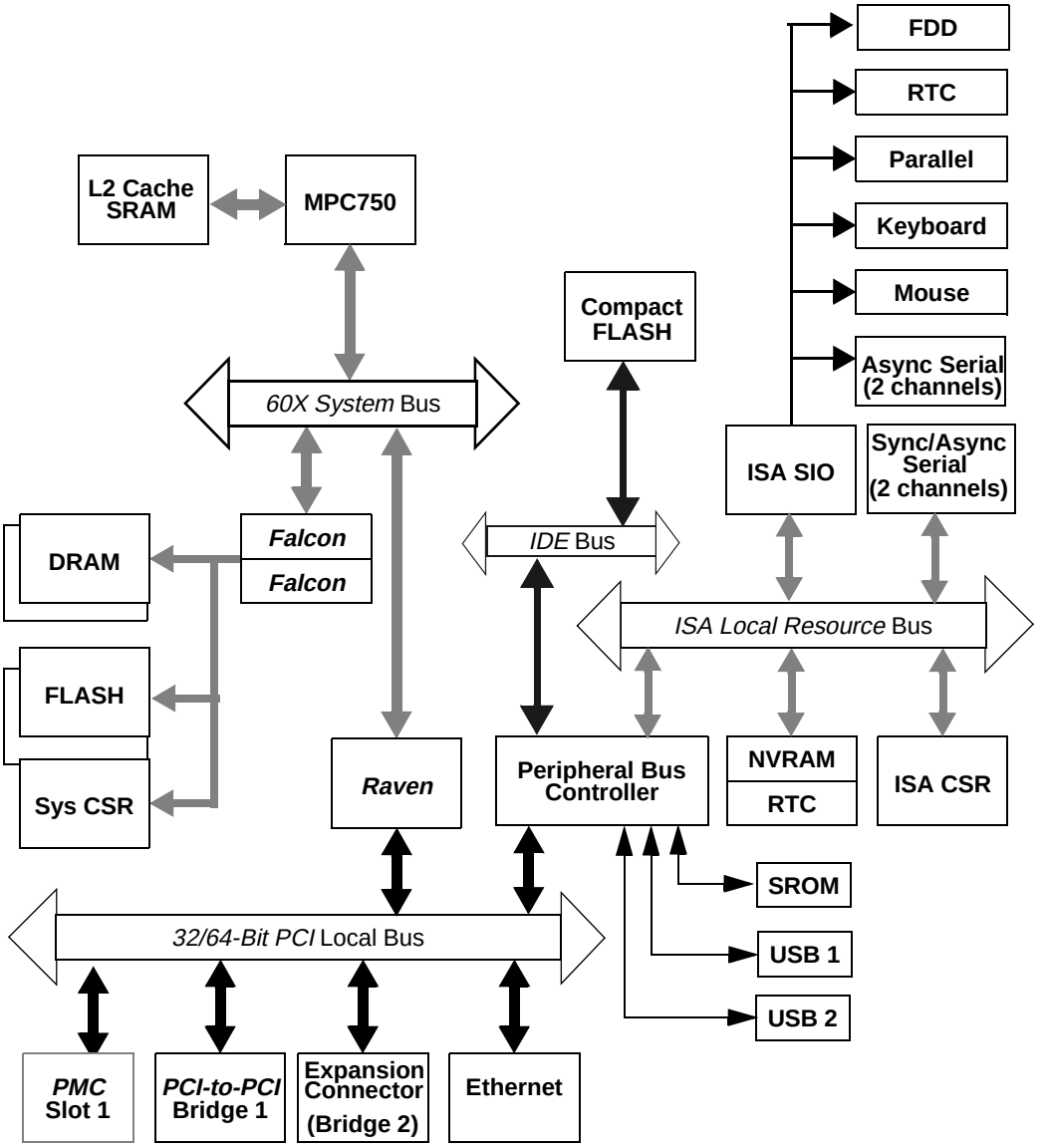


Figure 3-1. MCP750 Block Diagram

CompactPCI Interface

The CompactPCI bus interface will support up to 7 CompactPCI peripheral cards. The CompactPCI bus interface is provided using the DEC 21154 PCI-to-PCI bridge chip. This device implements a 64-bit primary data bus and 64-bit secondary data bus interface and is PCI 2.1 compliant. The 21154 provides read/write data buffering in both directions.

The device has an internal arbiter which implements a programmable 2-level rotating algorithm for all CompactPCI masters. The arbiter latency is typically one PCI clock. If the 21154 detects that an initiator has failed to assert FRAME# within 16 clock of the grant, the arbiter will negate the grant. The arbiter parks the CPCI bus at the last bus master by keeping the last grant asserted until a new bus request is asserted. After a reset, the 21154 parks the CPCI bus at itself until a new request is asserted.

The 21154 provides the 33MHz clocks for each of the CompactPCI slots. All clock source outputs are active following power-up or reset. The 21154 provides a control register to allow individual clock sources to be disabled. For additional information, refer to the DEC21154 data sheet.

The 21154 supports 3.3V or 5V signalling at the PCI busses with a separate VIO pin for the primary and secondary bus buffers. The primary bus signalling voltage is tied to +5 volts. The secondary bus signalling voltage is tied to the CPCI bus VIO, so the MCP750 is a universal board that may operate in a +3.3V or +5V chassis.

Ethernet Interface

The MCP750 module uses Digital Equipment's DECchip 21140 PCI Fast Ethernet LAN controller to implement an Ethernet interface that supports 10/100 Base-T connections. The balanced differential transceiver lines are coupled via on-board transformers.

The MCP750 routes its 10/100 Base-T lines to an RJ45 connector on the front panel.

Every MCP750 is assigned an Ethernet station address. The address is $08003E2*xxxxx*, where *xxxxx* is the unique 5-nibble number assigned to the board (that is, every board has a different value for *xxxxx*).

Each MCP750 displays its Ethernet station address on a label attached to the base board in the PMC connector "keepout" area just behind the front panel. In addition, the six bytes including the Ethernet station address are stored in an SROM off the DECchip Ethernet controller. That is, the value 08003E2*xxxxx* is stored in SROM, where *xxxxx* is a unique 5-nibble number for the board.

These bytes are stored in bytes 0x4 through 0x19 in the Ethernet SROM. The Ethernet information in the SROM is stored in DEC Version 3 format. For further information on this subject, refer to the Digital Semiconductor 21x4 Serial ROM Format, Version 3.03 document, listed in Appendix B, *Related Documentation*.

Caution Use extreme caution when viewing the contents of the Ethernet SROM via the PPCBUG SROM command. If the contents are modified incorrectly this could cause the PPCBUG Firmware Ethernet Drivers to work incorrectly.

Note: When the board is shipped from the factory, it should contain the proper SROM data for the MCP750, which has 10/100 Base-T Ethernet connections. There should not be a need to change the SROM contents.

For the pin assignments of the 10/100 Base-T connector, refer to Table 4-11. Refer to the BBRAM/TOD Clock memory map description in the *MCP750 Series Single Board Computer Programmer's Reference Guide* (MCP750A/PG) for detailed programming information.

PCI Mezzanine Interface

A key feature of the MCP750 family is the Peripheral Component Interconnect (PCI) bus. In addition to the on-board local bus devices (Ethernet, graphics, etc.), the PCI bus supports an industry-standard mezzanine interface, IEEE P1386.1 PCI Mezzanine Card (PMC).

PMC modules offer a variety of possibilities for I/O expansion through Fiber Distributed Data Interface (FDDI), Asynchronous Transfer Mode (ATM), graphics, and Ethernet ports. The base board supports PMC front panel and rear transition module I/O.

The MCP750 supports one PMC slot. Four 64-pin connectors on the base board (J11, J12, J13, and J14) interface with 32-bit or 64-bit IEEE P1386.1 PMC-compatible mezzanines to add any desirable function. The PCI Mezzanine Card slot has the following characteristics:

Mezzanine Type	PMC (PCI Mezzanine Card)
Mezzanine Size	S1B: Single width, standard depth (75mm x 150mm) with front panel
PMC Connectors	J11 through J14 (32/64-Bit PCI with front and rear I/O)
Signaling Voltage	V_{io} = 5.0Vdc

Refer to Chapter 4, *Connector Pin Assignments*, for the pin assignments of the PMC connectors. For additional programming information, refer to the PCI bus descriptions in the *MCP750 Programmer's Reference Guide* (MCP750A/PG) and to the user documentation for the PMC modules that you intend to use.

PC87307 ISA Super I/O Device (ISASIO)

The MCP750 uses the PC87307 ISASIO from National Semiconductor to provide the following:

- Two asynchronous serial ports
- Parallel port via transition module
- Floppy disk drive support via transition module

- A PS/2 keyboard and mouse interface via transition module
- A parallel printer port interface

Asynchronous Serial Ports

The Super I/O device provides two UART devices which are compatible with standard 16450 or 16550A UARTs. The default configuration assigns COM1 to IRQ4 and COM2 to IRQ3 of the PBC. The default configuration can be changed by programming the ISASIO device accordingly.

The COM1 port is wired as an RS-232 interface to a PC compatible DB9 connector on the front panel and it is also routed to the transition module via J3. COM2 is wired as an RS232 interface and is routed to the J3 I/O connector for transition module I/O.

For additional programming information, refer to the PCI and ISA bus discussions in the *MCP750 Programmer's Reference Guide* (MCP750A/PG) and to the vendor documentation for the ISASIO device.

Parallel Port/Printer Interface

The parallel port is a full IEEE1284 bidirectional parallel port/printer interface that supports standard enhanced and extended port modes. All parallel I/O interface signals are routed to the transition module that includes series damping resistors.

Hardware initializes the parallel port as PPT1 with an ISA IO base address of $3BC. This default configuration also assigns the parallel port to Peripheral Bus Controller (PBC) interrupt request line IRQ7. The default configuration can be changed by reprogramming the ISASIO device. For additional programming information, refer to the PCI and ISA bus discussions in the *MCP750 Programmer's Reference Guide* and to the vendor documentation for the ISASIO device.

Floppy Disk/Tape Drive Controller

The ISASIO device incorporates a PS/2-compatible low- and high-density disk drive controller for use with an optional external disk drive. The drive interfaces with the ISASIO controller via the transition module.

The ISASIO disk drive controller is compatible with the DP8473, 765A, and N82077 devices commonly used to implement floppy disk controllers. Software written for those devices may be used without change to operate the ISASIO controller. The ISASIO device may be used to support any of the following devices:

- 3½-inch 1.44MB floppy disk drive
- 5¼-inch 1.2MB floppy disk drive
- Standard 250kbps to 2Mbps tape drive system

Keyboard and Mouse Interface

The National Semiconductor PC87307 ISASIO chip is used to implement certain segments of the ROM-based keyboard and mouse interface control. The keyboard and mouse control signals are routed to a single 6-pin circular DIN connector on the transition module. Keyboard functions can be obtained by plugging the keyboard directly into this connector. To get both keyboard and mouse functions requires a Y adapter cable (Motorola Part Number: 30-W2309E01A). Refer to the *TMCP700 Installation and Use* manual for details.

PCI Peripheral Bus Controller (PBC)

The MCP750 uses the VIA Technologies VT82C586 Peripheral Bus Controller (PBC) to supply the interface between the PCI local bus and the ISA, IDE, and USB systems I/O bus (illustrated in Figure 1-1).

The PBC controller provides the following functions:

- ISA (Industry Standard Architecture) bus arbitration for DMA devices
- ISA interrupt mapping
- USB v1.0/HCI v1.1 compatible host/hub interface with two ports
- Enhanced IDE Controller with ultra DMA-33 support
- Interrupt controller functionality to support 14 ISA interrupts

- Edge/level control for ISA interrupts
- Seven independently programmable DMA channels
- Three interval counters/timers (82C54 functionality)
- I^{2C} interface via software programmable GPIO port

Accesses to the configuration space for the PBC are performed by way of the CONADD and Configuration Address and Data (CONDAT) registers in the Raven bridge controller ASIC. The registers are located at offsets $CF8 and $CFC, respectively, from the PCI I/O base address.

Real-Time Clock/NVRAM/Watchdog Timer Function

The MCP750 employs an SGS-Thomson surface-mount M48T559 RAM and clock chip to provide 8KB of non-volatile static RAM, a real-time clock, and a watchdog timer function. This chip supplies a clock, oscillator, crystal, power failure detection, memory write protection, 8KB of NVRAM, and a battery in a package consisting of two parts:

- A 28-pin 330mil SO device containing the real-time clock, the oscillator, power failure detection circuitry, timer logic, 8KB of static RAM, and gold-plated sockets for a battery
- A SNAPHAT battery housing a crystal along with the battery

The SNAPHAT battery package is socket mounted on top of the M48T559 device. The battery housing is keyed to prevent reverse insertion.

The clock furnishes seconds, minutes, hours, day, date, month, and year in BCD 24-hour format. Corrections for 28-, 29- (leap year), and 30-day months are made automatically. The clock generates no interrupts. Although the M48T559 is an 8-bit device, 8-, 16-, and 32-bit accesses from the ISA bus to the M48T559 are supported. Refer to the *MCP750 Programmer's Reference Guide* (MCP750/PG) and to the M48T559 data sheet for detailed programming and battery life information.

Programmable Timers

Among the resources available to the local processor are a number of programmable timers. Timers and counters on the MCP750 are provided by the Raven ASIC, the M48T559, the PBC, and the Z8536 CIO device (diagrammed in Figure 1-1). They can be programmed to generate periodic interrupts to the processor.

Raven General Purpose Timers

The Raven ASIC contains four 32-bit general purpose timers. Each timer is driven by a divide-by-eight prescaler which is synchronized to the PPC processor clock. For a 66.66MHz system, the timer frequency would be 8.25MHz. Each timer may be programmed to generate an MPIC interrupt.

Raven Watchdog Timers

The Raven ASIC contains two Watchdog timers, WDT1 and WDT2. Each timer is functionally equivalent but independent. These timers will continuously decrement until they reach a count of 0 or are reloaded by software. The timeout period is programmable from 1 microsecond up to 4 seconds. If the timer count reaches 0, a timer output signal will be asserted. The output of Watchdog Timer 1 is routed to generate an MPIC interrupt. The output of Watchdog Timer 2 is logically ORed onboard to provide a hard reset.

Following a device reset, WDT1 is enabled with a default timeout of 512 milliseconds and WDT 2 is enabled with a default timeout of 576 milliseconds. Each of these signals is typically delayed an additional 4.8 seconds (2 seconds minimum) using logic external to Raven. Each timer must be **disabled** or **reloaded** by software to prevent a timeout. Software may reload a new timer value or force the timer to reload a previously loaded value. To disable or load/reload a timer requires a two step process. The first step is to write the pattern $55 to the timer register key field which will arm the timer register to enable an update. The second step is to write the pattern $AA to the key field along with the new timer information. During the power-up configuration of the Raven ASIC, PPCBug disables the two Watchdog timers.

M48T559 Watchdog Timer

The M48T559 contains one Watchdog timer. This Watchdog timer output is logically ORed with the Raven Watchdog timer 2 output to provide a hard reset. Refer to the device data sheet and the *MCP750 Programmer's Reference Guide* (MCP750A/PG) for programming information.

Interval Timers

The PBC has three built-in counters that are equivalent to those found in an 82C54 programmable interval timer. The counters are grouped into one timer unit, Timer 1, in the PBC. Each counter output has a specific function:

- Counter 0 is associated with interrupt request line IRQ0. It can be used for system timing functions, such as a timer interrupt for a time-of-day function.
- Counter 1 generates a refresh request signal for ISA memory. This timer is not used in the MCP750.
- Counter 2 provides the tone for the speaker output function on the PBC (the SPEAKER_OUT signal which can be cabled to an external speaker via the transition module).

The interval timers use the OSC clock input as their clock source. The MCP750 drives the OSC pin with a 14.31818MHz clock source.

16-Bit Timers

Three 16-bit timers, provided by the Z8536 CIO device, are available on the MCP750. For information on programming these timers, refer to the data sheet for the Z8536 CIO device, listed in Appendix B, *Related Documentation*.

Serial Communications Interface

The MCP750 uses a Zilog Z85230 Enhanced Serial Communications Controller (ESCC) to implement the two serial communications interfaces, which are routed through the transition module. The Z85230 supports synchronous (SDLC/HDLC) and asynchronous protocols. The MCP750 hardware supports asynchronous serial baud rates of 110B/s to 38.4KB/s.

Each interface supports the CTS, DCD, RTS, and DTR control signals as well as the TxD and RxD transmit/receive data signals, and TxC/RxC synchronous clock signals. Since not all modem control lines are available in the Z85230, a Z8536 CIO is used to provide the missing modem lines.

A PAL device performs decoding of register accesses and pseudo interrupt acknowledge cycles for the Z85230 and the Z8536 in ISA I/O space. The PBC controller supplies DMA support for the Z85230.

The Z85230 receives a 10MHz clock input. The two synchronous ports will support data transfers up to 2.5Mbits/sec. The Z85230 supplies an interrupt vector during pseudo interrupt acknowledge cycles. The vector is modified within the Z85230 according to the interrupt source. Interrupt request levels are programmed via the PBC. All modem control lines from the ESCC are multiplexed/de-multiplexed through J3 by the P2MX function due to I/O pin limitations. Refer to the Z85230 data sheet and to the *MCP750 Programmer's Reference Guide* (MCP750A/PG) for additional information.

Z8536 CIO Device

The Z8536 CIO device complements the Z85230 ESCC by supplying modem control lines not provided by the Z85230 ESCC. In addition, the Z8536 CIO device has three independent 16-bit counters/ timers. The Z85230 receives a 5MHz clock input.

Base Module Feature Register

The Base Module Feature Register contains the details of the MCP750 single-board computer's configuration. It is an 8-bit read-only register located on the base board at ISA I/O address $0802.

Base Module Feature Register — Offset $0802								
BIT	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
FIELD	Not Used	SCCP*	Not Used	PMC1P*	Not Used	Not Used	LANP*	Not Used
OPER	R	R	R	R	R	R	R	R
RESET	1	N/A	1	N/A	1	1	N/A	1

SCCP* Z85230 ESCC present. If set, there is no on-board synchronous serial support (the ESCC is not present). If cleared, the Z85230 ESCC is installed and there is on-board support for synchronous serial communication.

PMC1P* PMC slot 1 present. If set, no PCI mezzanine card is installed in PMC slot 1. If cleared, PMC slot 1 contains a PCI mezzanine card.

LANP* Ethernet present. If set, no Ethernet transceiver interface is installed. If cleared, there is on-board Ethernet support.

Serial Port Signal Multiplexing

Due to pin limitations of the J3 connector, the MCP750 multiplexes and de-multiplexes some signals between the MCP750 board and the TMCP700 transition module. This hardware function is transparent to the software. The block diagram for the signal multiplexing is shown in the Figure 3-2:

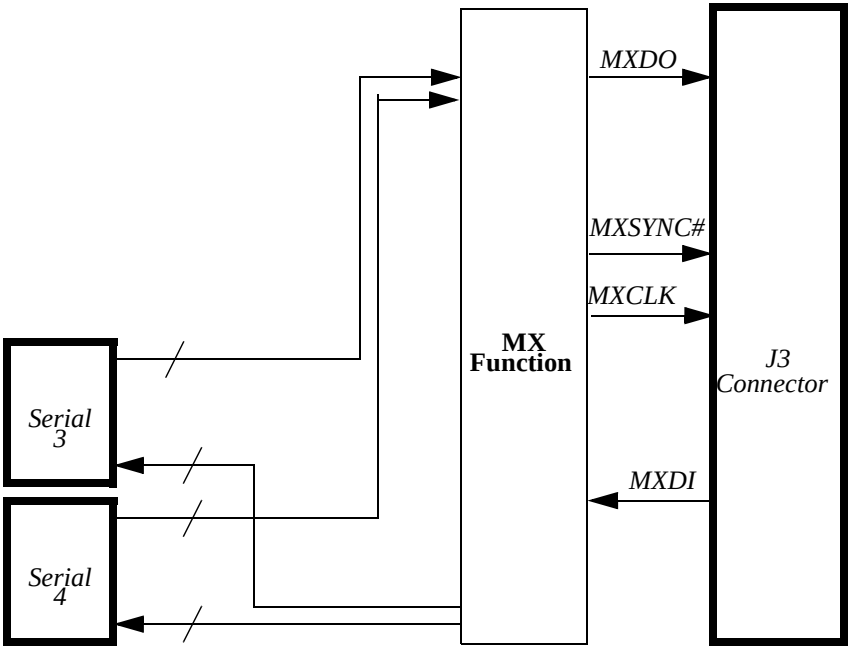


Figure 3-2. Serial Port Signal Multiplexing

Signal Multiplexing (MX)

There are four pins that are used for the MX function: MXCLK, MXSYNC#, MXDO, and MXDI. MXCLK is the 10MHz bit clock for the time-multiplexed data lines MXDO and MXDI. MXSYNC# is asserted for one bit time at Time Slot 15 by the MCP750 board. MXSYNC# is used by the transition module to synchronize with the MCP750 board. MXDO is the time-multiplexed output line from the main board and MXDI is the time-multiplexed line from the transition module. A 16-to-1 multiplexing scheme is used with 10MHz bit rate. Sixteen Time Slots are defined and allocated as follows:

Table 3-2. Multiplexing Sequence of the MX Function

MXDO (From MCP750)		MXDI (From TMCP700)	
TIME SLOT	**SIGNAL NAME**	**TIME SLOT**	**SIGNAL NAME**
0	RTS3	0	CTS3
1	DTR3	1	DSR3/MID1
2	LLB3/MODSEL	2	DCD3
3	RLB3	3	TM3/MID0
4	RTS4	4	RI3
5	DTR4	5	CTS4
6	LLB4	6	DSR4/MID3
7	RLB4	7	DCD4
8	IDREQ	8	TM4/MID2
9	Reserved	9	RI4
10	Reserved	10	Reserved
11	Reserved	11	Reserved
12	Reserved	12	Reserved
13	Reserved	13	Reserved
14	Reserved	14	Reserved
15	Reserved	15	Reserved

The MX function is used with PALs and some discrete devices. MXSYNC# is clocked out using the falling edge of MXCLK and MXDO by using the rising edge of the MXCLK. MXDI is sampled at the rising edge of MXCLK (the transition module synchronizes MXDI with MXCLK's rising edge). The timing relationships among MXCLK, MXSYNC#, MXDO, and MXDI are shown in Figure 3-3:

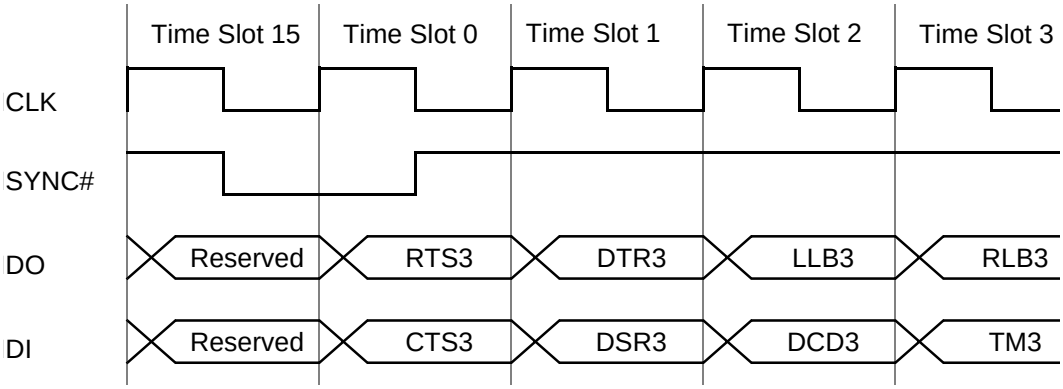


Figure 3-3. MX Signal Timings

ABORT(ABT) Switch (S2)

When activated by software, the ABORT switch can generate an interrupt signal to the processor. The interrupt is normally used to abort program execution and return control to the debugger firmware located in the MCP750 and Flash memory. The interrupt signal reaches the processor module via ISA bus interrupt line IRQ8*. The signal is also available at pin PB7 of the Z8536 CIO device, which handles various status signals, serial I/O lines, and counters.

The interrupter connected to the ABORT switch is an edge-sensitive circuit, filtered to remove switch bounce.

RESET(RST) Switch (S1)

The RESET switch resets all onboard devices and generates a CompactPCI backplane reset.

Front Panel Indicators (DS1 - DS4)

There are four LEDs on the MCP750 front panel:

- BFL (DS1, yellow). Board Failure; lights when the BRDFAIL* signal line is active.
- CPU (DS2, green). CPU activity; lights when the DBB* (Data Bus Busy) signal line on the processor bus is active.
- PCI (DS4, green). PCI activity; lights when the IRDY* (Initiator Ready) signal line on the PCI bus is active. This indicates that the local PCI bus is active.
- CPCI (DS3, green). CPCI activity; lights when the IRDY (Initiator Ready) signal line on the CPCI bus is active. This indicates that the CPCI bus is active.

Fuses and Polyswitches (Resettable Fuses)

The MCP750 provides inline slow-blow fuses for each power rail including +5Vdc, +3.3Vdc, and PMC +5Vdc. Polyswitches are provided for VIO, keyboard/mouse Vcc, and the two USB output voltages, +12Vdc and -12Vdc. The Table 3-3 lists the fuses with the voltages they protect.

Table 3-3. Fuse Assignments

Fuse#	Type	Voltage/Purpose/J Number	Fuse Rating
F1*	Slow Blow	+3.3Vdc for onboard voltage, to J12 PMC connector and to J3/J4 Transition module connectors	5A
F2*	Slow Blow	+5Vdc for onboard voltage and to J3/J4/J5 Transition module connectors	5A
F3*	Slow Blow	+5Vdc to J11/J13 PMC connectors	2.5A
R18	Poly-switch	+5Vdc to J5 Transition module connector for keyboard/mouse voltage	1.1A
R20	Poly-switch	+12Vdc to J12 PMC connector and J3 Transition module connector	2A

Table 3-3. Fuse Assignments

Fuse#	Type	Voltage/Purpose/J Number	Fuse Rating
R21	Poly-switch	VIO for onboard voltage and to J3 Transition module connector	1.1A
R23	Poly-switch	–12Vdc to J11 PMC connector and J3 Transition module connector	2A
R33	Poly-switch	+5Vdc to J17 USB Channel 1 connector	1.1A
R49	Poly-switch	+5Vdc to J18 USB Channel 0 connector	1.1A

Note *For replacement of fuses F1, F2, or F3 contact: Littelfuse, Inc. 800 E. Northwest Highway, Des Plaines, IL, 60016-3096. Order part number 452005 (5A), or 45202.5 (2.5A).

Speaker Control

The MCP750 base board supplies a SPEAKER_OUT signal to the transition module. The transition module contains a two pin jumper header (J13) which allows the SPEAKER_OUT signal to be cabled to an external speaker to obtain a beep tone.

MPC750 Processor

The MCP750 is designed to support the enhanced version of the MPC750 360-pin BGA processor chip with 16MB to 256MB of ECC DRAM, 1MB of level 2 cache (L2 cache), and up to 9MB of Flash memory. The L2 cache and 1MB of 16-bit Flash memory reside on the MCP750 base board. The ECC DRAM and 4MB or 8MB of additional (64-bit) Flash memory are located on the RAM300 memory mezzanine.

The MPC750 is a 64-bit processor with 64KB on-chip cache (32KB data cache and 32KB instruction cache). The L2 cache is implemented with an on-chip, two way set associative tag memory and with external synchronous SRAMs for data storage.

The Raven bridge controller ASIC provides the bridge between the MPC750 microprocessor bus and the PCI local bus. Electrically, the Raven chip is a 64-bit PCI connection. Four programmable map decoders in each direction provide flexible addressing between the MPC750 microprocessor bus and the PCI local bus.

Flash Memory

The MCP750 base board has provision for 1MB of 16-bit Flash memory in two 8-bit sockets. The RAM300 memory mezzanine accommodates 4MB or 8MB of additional 64-bit Flash memory.

The onboard monitor/debugger, PPCBug, resides in the **Flash chips**. PPCBug provides functionality for:

- Booting the operating system
- Initializing after a reset
- Displaying and modifying configuration variables
- Running self-tests and diagnostics
- Updating firmware ROM

Under normal operation, the Flash devices are in “read-only” mode, their contents are pre-defined, and they are protected against inadvertent writes due to loss of power conditions. However, for programming purposes, programming voltage is always supplied to the devices and the Flash contents may be modified by executing the proper program command sequence. Refer to the third-party data sheet and/or to the *PPCBug Firmware Package User’s Manual* (PPCBUGA1/UM and PPCBUGA2/UM) for further device-specific information on modifying Flash contents.

RAM300 Memory Module

The RAM300 is the ECC DRAM memory mezzanine module that (together with an optional PCI mezzanine card) plugs into the base board to make a complete MCP750 single-board computer. See Chapter 1, *Hardware Preparation and Installation*.

RAM300 modules of 16, 32, 64, 128, or 256MB are available for memory expansion. The ECC DRAM is controlled by the Falcon memory controller chip set. The Falcon ASICs perform two-way interleaving, with double-bit error detection and single-bit error correction.

In addition to the ECC DRAM, the RAM300 module supplies 4MB or 8MB of additional soldered-in 64-bit Flash memory. A jumper header (J6) tells the Falcon chip set where in memory to fetch the board reset vector. Depending on the configuration of J6, resets execute either from Flash memory bank A or from bank B.

Compact FLASH Memory Card

The MCP750 supports a single EIDE compatible Compact FLASH Memory Card off of the PBC Primary EIDE interface. Currently available Compact FLASH memory cards provide from 2 Mbytes to 24 Mbytes of formatted capacity. Once configured, this memory will appear as a standard ATA (EIDE) disk drive.

TMCP700 Transition Module

The TMCP700 transition module is used in conjunction with all models of the MCP750 base board:

The features of the TMCP700 include:

- A parallel printer port (IEEE 1284-I compliant)
- Two EIA-232-D asynchronous serial ports (identified as COM1 and COM2 on the front panel)
- Two synchronous serial ports (SERIAL 3 and SERIAL 4 on the front panel) configured for EIA-232-D, EIA-530, V.35, or X.21 protocols
- Two Universal Serial Bus (USB) ports
- Two 60-pin Serial Interface Module (SIM) connectors
- A 40-pin header for the secondary EIDE port
- Two 64-pin headers for PMC IO

- A 34-pin header for a floppy port
- A 2-pin header for speaker output

See *TMCP700 Transition Module Preparation* on page 1-9 for more information.

Serial Interface Modules

The synchronous serial ports on the TMCP700 are configured via serial interface modules (SIMs), used in conjunction with the appropriate jumper settings on the transition module. The SIMs are small, plug-in printed circuit boards which contain all the circuitry needed to convert a TTL-level port to the standard voltage levels needed by various industry-standard serial interfaces, such as EIA-232, EIA-530, etc. SIMs are available for the following configurations:

Table 3-4. SIM Type Identification

Model Number	Module Type
SIM232DCE	EIA-232 DCE
SIM232DTE	EIA-232 DTE
SIM530DCE	EIA-530 DCE
SIM530DTE	EIA-530 DTE
SIMV35DCE	V.35 DCE
SIMV35DTE	V.35 DTE
SIMX21DCE	X.21 DCE
SIMX21DTE	X.21 DTE

For additional information about the serial interface modules, refer to the TMCP700 *Transition Module Installation and Use manual*, listed in *Appendix B, Related Documentation*.

Connector Pin Assignments

4

MCP750 Connectors

This chapter summarizes the pin assignments for the following groups of interconnect signals for the MCP750 and the TMCP700:

- CompactPCI J1/J2 Connectors
- CompactPCI User I/O Connector J3
- Local Bus Expansion Connector J4
- User I/O Connector J5
- PCI Mezzanine Card (PMC) Connectors
- Front USB Connectors
- 10/100 Base-T Connector
- COM1 Connector
- Debug Connector
- Add-On Memory Mezzanine Connector
- Compact FLASH Memory Card Connector
- CompactPCI Connectors J3/J4/J5
- Serial Ports 1 and 2 (TMCP700 I/O Mode)
- Serial Ports 3 and 4 (TMCP700 I/O Mode)
- Parallel Connector (TMCP700 I/O Mode)
- Keyboard/Mouse Connector J16 (TMCP700 I/O Mode)
- USB Connectors (optional TMCP700 I/O Mode)
- 40-pin Secondary EIDE port header (TMCP700)

- 34-pin Floppy port header (TMCP700)
- Power Connector (TMCP700)
- 2-pin Speaker Output header (TMCP700)
- Two 64-pin headers for PMCIO/GND signal pairs

Common Connectors

The following tables describe connectors used with the same pin assignments by the base board.

CompactPCI Connectors (J1/J2)

The MCP750 implements a 64-bit CompactPCI interface on connectors J1 and J2. J1 is a 110 pin AMP Z-pack 2mm hard metric type A connector with keying for +3.3V or +5V. J2 is 110 pin AMP Z-pack 2mm hard metric type B connector. Each of these connectors conform to the CompactPCI specification. The pinout for connectors J1 and J2 are shown below.

Table 4-1. J1 CompactPCI Connector

	ROW A	ROW B	ROW C	ROW D	ROW E	
25	+5V	REQ64_L	ENUM_L	+3.3V	+5V	25
24	AD1	+5V	VIO	AD0	ACK64_L	24
23	+3.3V	AD4	AD3	+5V	AD2	23
22	AD7	GND	+3.3V	AD6	AD5	22
21	+3.3V	AD9	AD8	GND	CBE0_L	21
20	AD12	GND	VIO	AD11	AD10	20
19	+3.3V	AD15	AD14	GND	AD13	19
18	SERR_L	GND	+3.3V	PAR	CBE1_L	18
17	+3.3V	SDONE	SBO_L	GND	PERR_L	17
16	DEVSEL_L	GND	VIO	STOP_L	LOCK_L	16
15	+3.3v	FRAME_L	IRDY_L	GND	TRDY_L	15

Table 4-1. J1 CompactPCI Connector (Continued)

12-14	KEY AREA					12-14
11	AD18	AD17	AD16	GND	CBE2_L	11
10	AD21	GND	+3.3V	AD20	AD19	10
9	CBE3_L	No Connect (IDSEL)	AD23	GND	AD22	9
8	AD26	GND	VIO	AD25	AD24	8
7	AD30	AD29	AD28	GND	AD27	7
6	REQ_L	GND	+3.3v	CLK	AD31	6
5	No Connect (BRSVP1A5)	No Connect (BRSVP1B5)	RST_L	GND	GNT_L	5
4	No Connect (BRSVP1A4)	GND	VIO	No Connect (INTP)	No Connect (INTS)	4
3	INTA_L	INTB_L	INTC_L	+5V	INTD_L	3
2	TCK	+5V	TMS	TDO	TDI	2
1	+5V	-12V	TRST_L	+12V	+5V	1

Table 4-2. J2 CompactPCI Connector

	ROW A	ROW B	ROW C	ROW D	ROW E	
22	No Connect (RSV)	No Connect (RSV)	No Connect (RSV)	No Connect (RSV)	No Connect (RSV)	22
21	CLK6	GND	No Connect (RSV)	No Connect (RSV)	No Connect (RSV)	21
20	CLK5	GND	No Connect (RSV)	GND	No Connect (RSV)	20
19	GND	GND	No Connect (RSV)	No Connect (RSV)	No Connect (RSV)	19

Table 4-2. J2 CompactPCI Connector (Continued)

18	No Connect (BRSVP2A18)	No Connect (BRSVP2B18)	No Connect (BRSVP2C18)	GND	No Connect (BRSVP2E18)	18
17	No Connect (BRSVP2A17)	GND	PRST_L	REQ6_L	GNT6_L	17
16	No Connect (BRSVP2A16)	No Connect (BRSVP2B16)	DEG_L	GND	No Connect (BRSVP2E16)	16
15	No Connect (BRSVP2A15)	GND	FAL_L	REQ5_L	GNT5_L	15
14	AD35	AD34	AD33	GND	AD32	14
13	AD38	GND	VIO	AD37	AD36	13
12	AD42	AD41	AD40	GND	AD39	12
11	AD45	GND	VIO	AD44	AD43	11
10	AD49	AD48	AD47	GND	AD46	10
9	AD52	GND	VIO	AD51	AD50	9
8	AD56	AD55	AD54	GND	AD53	8
7	AD59	GND	VIO	AD58	AD57	7
6	AD63	AD62	AD61	GND	AD60	6
5	CBE5_L	GND	VIO	CBE4_L	PAR64	5
4	VIO	No Connect (BRSVP2B4)	CBE7_L	GND	CBE6_L	4
3	CLK4	GND	GNT3_L	REQ4_L	GNT4_L	3
2	CLK2	CLK3	SYSEN_L	GNT2_L	REQ3_L	2
1	CLK1	GND	REQ1_L	GNT1_L	REQ2_L	1

CompactPCI User I/O Connector (J3)

Connector J3 is a 95 pin (excluding row F) AMP Z-pack 2mm hard metric type B connector. This connector routes the I/O signals for the PMC I/O and serial channels. The pin assignments for J3 are as follows (outer row F is assigned and used as ground pins but is not shown in the table):

Table 4-3. J3 User I/O Connector

	ROW A	ROW B	ROW C	ROW D	ROW E	
19	Reserved	+12V	-12V	RXD3	RXD4	19
18	Reserved	GND	RXC3	GND	RXC4	18
17	Reserved	MXCLK	MXDI	MXSYNC_L	MXDO	17
16	Reserved	GND	TXC3	GND	TXC4	16
15	Reserved	Reserved	Reserved	TXD3	TXD4	15
14	+3.3V	+3.3V	+3.3V	+5V	+5V	14
13	PMCIO5	PMCIO4	PMCIO3	PMCIO2	PMCIO1	13
12	PMCIO10	PMCIO9	PMCIO8	PMCIO7	PMCIO6	12
11	PMCIO15	PMCIO14	PMCIO13	PMCIO12	PMCIO11	11
10	PMCIO20	PMCIO19	PMCIO18	PMCIO17	PMCIO16	10
9	PMCIO25	PMCIO24	PMCIO23	PMCIO22	PMCIO21	9
8	PMCIO30	PMCIO29	PMCIO28	PMCIO27	PMCIO26	8
7	PMCIO35	PMCIO34	PMCIO33	PMCIO32	PMCIO31	7
6	PMCIO40	PMCIO39	PMCIO38	PMCIO37	PMCIO36	6
5	PMCIO45	PMCIO44	PMCIO43	PMCIO42	PMCIO41	5
4	PMCIO50	PMCIO49	PMCIO48	PMCIO47	PMCIO46	4
3	PMCIO55	PMCIO54	PMCIO53	PMCIO52	PMCIO51	3
2	PMCIO60	PMCIO59	PMCIO58	PMCIO57	PMCIO56	2
1	VIO	PMCIO64	PMCIO63	PMCIO62	PMCIO61	1

Local Bus Expansion Connector (J4)

Connector J4 is a 110 pin AMP Z-pack 2mm hard metric type A connector with keying for +3.3V or +5V. This connector routes the 64-bit local PCI bus to the backplane for expansion. The pin assignments for J4 are as follows (the outer row F is assigned and used as ground pins but is not shown in the table):

Table 4-4. J4 Local PCI Expansion Connector

	ROW A	ROW B	ROW C	ROW D	ROW E	
25	AD36	AD35	AD34	AD33	AD32	25
24	AD40	AD39	AD38	GND	AD37	24
23	AD45	AD44	AD43	AD42	AD41	23
22	AD49	3.3V	AD48	AD47	AD46	22
21	AD53	AD52	AD51	GND	AD50	21
20	AD57	3.3V	AD56	AD55	AD54	20
19	AD61	AD60	AD59	GND	AD58	19
18	CBE4#	3.3V	PAR64	AD63	AD62	18
17	REQ64#	CBE7#	CBE6#	GND	CBE5#	17
16	AD2	3.3V	AD1	AD0	ACK64#	16
15	AD6	AD5	AD4	GND	AD3	15
12-14	KEY AREA					12-14
11	AD9	AD8	CBE0#	GND	AD7	11
10	AD13	5.0V	AD12	AD11	AD10	10
9	PAR	CBE1#	AD15	GND	AD14	9
8	STOP#	5.0V	LOCK#	PERR#	SERR#	8
7	FRAME#	IRDY#	TRDY#	GND	DEVSEL#	7
6	AD18	5.0V	AD17	AD16	CBE2#	6
5	AD21	CLK	AD20	GND	AD19	5
4	CBE3#	5.0V	No Connect	AD23	AD22	4
3	AD28	AD27	AD26	AD25	AD24	3
2	GNT#	REQ#	AD31	AD30	AD29	2

Table 4-4. J4 Local PCI Expansion Connector (Continued)

1	INTA#	INTB#	INTC#	INTD#	RST#	1

User I/O Connector (J5)

Connector J5 is a 110 pin (excluding row F) AMP Z-pack 2mm hard metric type B connector. This connector routes the I/O signals for the IDE (primary and secondary ports), the keyboard, the mouse, the two USB ports, and the printer ports. The pin assignments for J5 are as follows (the outer row F is assigned and used as ground pins but is not shown in the table):

Table 4-5. J5 User I/O Connector

	ROW A	ROW B	ROW C	ROW D	ROW E	
22	Reserved	GRD	Reserved	+5V	SPKROC_L	22
21	KBDDAT	KBDCLK	KBAUXVCC	AUXDAT	AUXCLK	21
20	Reserved	Reserved	Reserved	GND	Reserved	20
19	STB_L	GND	UVCC0	UDATA0+	UDATA0-	19
18	AFD_L	UDATA1+	UDATA1-	GND	UVCC1	18
17	PD2	INIT_L	PD1	ERR_L	PD0	17
16	PD6	PD5	PD4	PD3	SLIN_L	16
15	SLCT	PE	BUSY	ACK_L	PD7	15
14	RTSa	CTSa	RIa	GND	DTRa	14
13	DCDa	+5V	RXDa	DSRa	TXDa	13
12	RTSb	CTSb	RIb	+5V	DTRb	12
11	DCDb	GND	RXDb	DSRb	TXDb	11
10	TR0_L	WPROT_L	RDATA_L	HDSEL_L	DSKCHG_L	10
9	MTR1_L	DIR_L	STEP_L	WDATA_L	WGATE_L	9
8	RESERVED	INDEX_L	MTR0_L	DS1_L	DS0_L	8
7	CS1FX_L	CS3FX_L	DA1	DASP_L	RESERVED	7
6	IOCS16_L	GRD	PDIAG_L	DA0	DA2	6

Table 4-5. J5 User I/O Connector (Continued)

5	DMARQ	IORDY	DIOW_L	DMACK_L	DIOR_L	5
4	DD14	DD0	GND	DD15	INTRQ	4
3	DD3	DD12	DD2	DD13	DD1	3
2	DD9	DD5	DD10	DD4	DD11	2
1	RESET_L	DRESET_L	DD7	DD8	DD6	1

PCI Mezzanine Card Connectors (J11/J12/J13/J14)

Four 64-pin connectors (J11/J12/J13/J14 on the MCP750) supply the interface between the base board and an optional PCI mezzanine card (PMC). The pin assignments are listed in the following two tables:

Table 4-6. PCI Mezzanine Card Connector

	J11				J12		
1	TCK	–12V	2	1	+12V	TRST*	2
3	GND	PMCINTA*	4	3	TMS	TDO	4
5	PMCINTB*	PMCINTC*	6	5	TDI	GND	6
7	PMC1P*	+5V	8	7	GND	Not Used	8
9	PMCINTD*	Not Used	10	9	Not Used	Not Used	10
11	GND	Not Used	12	11	Pull-up	+3.3V	12
13	PCICLK	GND	14	13	PCIRST*	Pull-down	14
15	GND	PMC1GNT*	16	15	+3.3V	Pull-down	16
17	PMC1REQ*	+5V	18	17	Not Used	GND	18
19	+5V	AD31	20	19	AD30	AD29	20
21	AD28	AD27	22	21	GND	AD26	22
23	AD25	GND	24	23	AD24	+3.3V	24
25	GND	CBE3*	26	25	IDSEL	AD23	26
27	AD22	AD21	28	27	+3.3V	AD20	28
29	AD19	+5V	30	29	AD18	GND	30
31	+5V	AD17	32	31	AD16	C/BE2*	32
33	FRAME*	GND	34	33	GND	Not Used	34

Table 4-6. PCI Mezzanine Card Connector (Continued)

35	GND	IRDY*	36	35	TRDY*	+3.3V	36
37	DEVSEL*	+5V	38	37	GND	STOP*	38
39	GND	LOCK*	40	39	PERR*	GND	40
41	SDONE*	SBO*	42	41	+3.3V	SERR*	42
43	PAR	GND	44	43	C/BE1*	GND	44
45	+5V	AD15	46	45	AD14	AD13	46
47	AD12	AD11	48	47	GND	AD10	48
49	AD09	+5V	50	49	AD08	+3.3V	50
51	GND	C/BE0*	52	51	AD07	Not Used	52
53	AD06	AD05	54	53	+3.3V	Not Used	54
55	AD04	GND	56	55	Not Used	GND	56
57	+5V	AD03	58	57	Not Used	Not Used	58
59	AD02	AD01	60	59	GND	Not Used	60
61	AD00	+5V	62	61	ACK64*	+3.3V	62
63	GND	REQ64*	64	63	GND	Not Used	64

Table 4-7. PCI Mezzanine Card Connector

	J13				J14		
1	Not Used	GND	2	1	PMCIO1	PMCIO2	2
3	GND	C/BE7*	4	3	PMCIO3	PMCIO4	4
5	C/BE6*	C/BE5*	6	5	PMCIO5	PMCIO6	6
7	C/BE4*	GND	8	7	PMCIO7	PMCIO8	8
9	+5V (Vio)	PAR64	10	9	PMCIO9	PMCIO10	10
11	AD63	AD62	12	11	PMCIO11	PMCIO12	12
13	AD61	GND	14	13	PMCIO13	PMCIO14	14
15	GND	AD60	16	15	PMCIO15	PMCIO16	16
17	AD59	AD58	18	17	PMCIO17	PMCIO18	18
19	AD57	GND	20	19	PMCIO19	PMCIO20	20
21	+5V (Vio)	AD56	22	21	PMCIO21	PMCIO22	22

Table 4-7. PCI Mezzanine Card Connector (Continued)

23	AD55	AD54	24	23	PMCIO23	PMCIO24	24
25	AD53	GND	26	25	PMCIO25	PMCIO26	26
27	GND	AD52	28	27	PMCIO27	PMCIO28	28
29	AD51	AD50	30	29	PMCIO29	PMCIO30	30
31	AD49	GND	32	31	PMCIO31	PMCIO32	32
33	GND	AD48	34	33	PMCIO33	PMCIO34	34
35	AD47	AD46	36	35	PMCIO35	PMCIO36	36
37	AD45	GND	38	37	PMCIO37	PMCIO38	38
39	+5V (Vio)	AD44	40	39	PMCIO39	PMCIO40	40
41	AD43	AD42	42	41	PMCIO41	PMCIO42	42
43	AD41	GND	44	43	PMCIO43	PMCIO44	44
45	GND	AD40	46	45	PMCIO45	PMCIO46	46
47	AD39	AD38	48	47	PMCIO47	PMCIO48	48
49	AD37	GND	50	49	PMCIO49	PMCIO50	50
51	GND	AD36	52	51	PMCIO51	PMCIO52	52
53	AD35	AD34	54	53	PMCIO53	PMCIO54	54
55	AD33	GND	56	55	PMCIO55	PMCIO56	56
57	+5V (Vio)	AD32	58	57	PMCIO57	PMCIO58	58
59	Not Used	Not Used	60	59	PMCIO59	PMCIO60	60
61	Not Used	GND	62	61	PMCIO61	PMCIO62	62
63	GND	Not Used	64	63	PMCIO63	PMCIO64	64

Front USB Connectors (J17/J18)

Two USB Series A receptacles are located at the front panel of the MCP750 SBC. The pin assignments for these connectors are as follows:

Table 4-8. USB 0 Connector J18

1	UVCC0
2	UDATA0N
3	UDATA0P

Table 4-8. USB 0 Connector J18 (Continued)

4	GND

Table 4-9. USB 1 Connector J17

1	UVCC1
2	UDATA1N
3	UDATA1P
4	GND

10/100 Base-T Connector (J8)

The 10/100 Base-T Connector is an RJ45 connector located on the front panel of the MCP750 SBC. The pin assignments for this connector are as follows:

Table 4-10. 10/100 Base-T Connector J8

1	TD+
2	TD-
3	RD+
4	AC Terminated
5	AC Terminated
6	RD-
7	AC Terminated
8	AC Terminated

COM1 Connector (J15)

A standard DB9 receptacle is located on the front panel of the MCP750 to provide the interface to the COM1 serial port. These COM1 signals are also routed to J11 on the transition module. A terminal may be connected to J15 or J11 on the transition module but not both at the same time. The pin assignments for this connector is as follows:

Table 4-11. COM1 Connector J15

1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

Debug Connector (J19)

A 190-pin connector (J19 on the MCP750 base board) provides access to the processor bus (MPU bus) and some bridge/memory controller signals. It can be used for debugging purposes. The pin assignments are listed in the following table.

Table 4-12. Debug Connector (J19)

1	PA0		PA1	2
3	PA2		PA3	4
5	PA4		PA5	6
7	PA6		PA7	8
9	PA8		PA9	10

Table 4-12. Debug Connector (J19) (Continued)

11	PA10		PA11	12
13	PA12		PA13	14
15	PA14		PA15	16
17	PA16		PA17	18
19	PA18	GND	PA19	20
21	PA20		PA21	22
23	PA22		PA23	24
25	PA24		PA25	26
27	PA26		PA27	28
29	PA28		PA29	30
31	PA30		PA31	32
33	PA_PAR0		PA_PAR1	34
35	PA_PAR2		PA_PAR3	36
37	APE*		RSRV*	38
39	PD0		PD1	40
41	PD2		PD3	42
43	PD4		PD5	44
45	PD6		PD7	46
47	PD8		PD9	48
49	PD10		PD11	50
51	PD12		PD13	52
53	PD14		PD15	54
55	PD16		PD17	56
57	PD18	+5V	PD19	58
59	PA20		PD21	60
61	PD22		PD23	62
63	PD24		PD25	64
65	PD26		PD27	66
67	PD28		PD29	68
69	PD30		PD31	70

Table 4-12. Debug Connector (J19) (Continued)

71	PD32		PD33	72
73	PD34		PD35	74
75	PD36		PD37	76
77	PD38		PD39	78
79	PD40		PD41	80
81	PD42		PD43	82
83	PD44		PD45	84
85	PD46		PD47	86
87	PD48		PD49	88
89	PA50		PD51	90
91	PD52		PD53	92
93	PD54		PD55	94
95	PD56	GND	PD57	96
97	PD58		PD59	98
99	PD60		PD61	100
101	PD62		PD63	102
103	PDPAR0		PDPAR1	104
105	PDPAR2		PDPAR3	106
107	PDPAR4		PDPAR5	108
109	PDPAR6		PDPAR7	110
111	No Connection		No Connection	112
113	DPE*		DBDIS*	114
115	TT0		TSIZ0	116
117	TT1		TSIZ1	118
119	TT2		TSIZ2	120
121	TT3		No Connection	122
123	TT4		No Connection	124
125	CI*		No Connection	126
127	WT*		No Connection	128
129	GLOBAL*		No Connection	130

Table 4-12. Debug Connector (J19) (Continued)

131	SHARED*		DBWO*	132
133	AACK*	+3.3V	TS*	134
135	ARTY*		XATS*	136
137	DRTY*		TBST*	138
139	TA*		No Connection	140
141	TEA*		No Connection	142
143	No Connection		DBG*	144
145	No Connection		DBB*	146
147	No Connection		ABB*	148
149	TCLK_OUT		MPUBG-0*	150
151	No Connection		MPUBR0*	152

Table 4-12. Debug Connector (J19) (Continued)

153	MPUBR1*		IRQ0*	154
155	MPUBG1*		MCHK*	156
157	WDT1TO*		SMI*	158
159	WDT2TO*		CKSTPI*	160
161	L2BR*		CKSTPO*	162
163	L2BG*		HALTED (N/C)	164
165	CLAIM*		TLBISYNC*	166
167	No Connection		TBEN	168
169	No Connection*		No Connection	170
171	No Connection*	GND	No Connection	172
173	No Connection*		No Connection	174
175	No Connection		NAPRUN	176
177	SRST1*		QREQ*	178
179	SRESET*		QACK*	180
181	HRESET*		CPUTDO	182
183	GND		CPUTDI	184
185	CPUCLK1		CPUTCK	186
187	No Connection		CPUTMS	188
189	No Connection		CPUTRST*	190

DRAM Mezzanine Connector (J10)

A 190-pin connector (J10 on the MCP750 base board) supplies the interface between the memory bus and the RAM300 DRAM mezzanine. The pin assignments are listed in the following table.

Table 4-13. DRAM Mezzanine Connector (J10)

1	A_RAS*		A_CAS*	2
3	B_RAS*		B_CAS*	4
5	C_RAS*		C_CAS*	6
7	D_RAS*		D_CAS*	8
9	OEL*		OEU*	10
11	WEL*		WEU*	12
13	ROMACS*		ROMBCS*	14
15	RAMAEN		RAMBEN	16
17	RAMCEN		EN5VPWR	18
19	RAL0	GND	RAL1	20
21	RAL2		RAL3	22
23	RAL4		RAL5	24
25	RAL6		RAL7	26
27	RAL8		RAL9	28
29	RAL10		RAL11	30
31	RAL12		RAU0	32
33	RAU1		RAU2	34
35	RAU3		RAU4	36
37	RAU5		RAU6	38
39	RAU7		RAU8	40
41	RAU9		RAU10	42
43	RAU11		RAU12	44
45	RDL0		RDL1	46
47	RDL2		RDL3	48
49	RDL4		RDL5	50

Table 4-13. DRAM Mezzanine Connector (J10) (Continued)

51	RDL6		RDL7	52
53	RDL8		RDL9	54
55	RDL10		RDL11	56
57	RDL12	+5V	RDL13	58
59	RDL14		RDL15	60
61	RDL16		RDL17	62
63	RDL18		RDL19	64
65	RDL20		RDL21	66
67	RDL22		RDL23	68
69	RDL24		RDL25	70
71	RDL26		RDL27	72
73	RDL28		RDL29	74
75	RDL30		RDL31	76
77	RDL32		RDL33	78
79	RDL34		RDL35	80
81	RDL36		RDL37	82
83	RDL38		RDL39	84
85	RDL40		RDL41	86
87	RDL42		RDL43	88
89	RDL44		RDL45	90
91	RDL46		RDL47	92
93	RDL48		RDL49	94
95	RDL50	GND	RDL51	96
97	RDL52		RDL53	98
99	RDL54		RDL55	100
101	RDL56		RDL57	102
103	RDL58		RDL59	104
105	RDL60		RDL61	106
107	RDL62		RDL63	108
109	CDL0		CDL1	110

Table 4-13. DRAM Mezzanine Connector (J10) (Continued)

111	CDL2		CDL3	112
113	CDL4		CDL5	114
115	CDL6		CDL7	116
117	No Connection		No Connection	118
119	RDU0		RDU1	120
121	RDU2		RDU3	122
123	RDU4		RDU5	124
125	RDU6		RDU7	126
127	RDU8		RDU9	128
129	RDU10		RDU11	130
131	RDU12		RDU13	132
133	RDU14	+3.3V	RDU15	134
135	RDU16		RDU17	136
137	RDU18		RDU19	138
139	RDU20		RDU21	140
141	RDU22		RDU23	142
143	RDU24		RDU25	144
145	RDU26		RDU27	146
147	RDU28		RDU29	148
149	RDU30		RDU31	150
151	RDU32		RDU33	152

Table 4-13. DRAM Mezzanine Connector (J10) (Continued)

153	RDU34		RDU35	154
155	RDU36		RDU37	156
157	RDU38		RDU39	158
159	RDU40		RDU41	160
161	RDU42		RDU43	162
163	RDU44		RDU45	164
165	RDU46		RDU47	166
167	RDU48		RDU49	168
169	RDU50		RDU51	170
171	RDU52	GND	RDU53	172
173	RDU54		RDU55	174
175	RDU56		RDU57	176
177	RDU58		RDU59	178
179	RDU60		RDU61	180
181	RDU62		RDU63	182
183	CDU0		CDU1	184
185	CDU2		CDU3	186
187	CDU4		CDU5	188
189	CDU6		CDU7	190

EIDE Compact FLASH Connector (J9)

A 50-pin Compact FLASH card header connector provides the EIDE interface to the Compact FLASH Memory Card. The pin assignments for this connector are as follows:

Table 4-14. EIDE Compact FLASH Connector J9

1	GND	DATA3	2
3	DATA4	DATA5	4
5	DATA6	DATA7	6
7	DCS1A_L	GND	8

Table 4-14. EIDE Compact FLASH Connector J9 (Continued)

9	GND	GND	10
11	GND	GND	12
13	+5V	GND	14
15	GND	GND	16
17	GND	DA2	18
19	DA1	DA0	20
21	DATA0	DATA1	22
23	DATA2	NO CONNECT	24
25	CD2_L	CD1_L	26
27	DATA11	DATA12	28
29	DATA13	DATA14	30
31	DATA15	DCS3A_L	32
33	NO CONNECT	DIORA_L	34
35	DIOWA_L	NO CONNECT	36
37	INTRQA	+5V	38
39	MASTER/SLAVE	NO CONNECT	40
41	RST_L	DIORDYA	42
43	NO CONNECT	NO CONNECT	44
45	NO CONNECT	NO CONNECT	46
47	DATA8	DATA9	48
49	DATA10	GND	50

TMCP700 Transition Module

The following tables summarize the pin assignments of connectors that are specific to MCP750 modules configured for use with TMCP700 transition modules.

CompactPCI Connectors (J3/J4/J5)

Connector J3 is a 95-pin 2mm hard metric type B connector which routes I/O signals for PMC I/O and serial channels. The pinout for this connector has been described previously in Table 4-1.

Connector J4 is a 110-pin 2mm hard metric type A connector. This connector is placed on the board for alignment only. The keying tabs on the type A connector assist with alignment of pins in the backplane connector during insertion of the boards. No signals are connected to J4 except the row F ground pins.

Connector J5 is a 110-pin 2mm hard metric type B connector which routes I/O signals for IDE, keyboard, mouse, USB and printer ports. The pinout for this connector has been previously described in Table 4-3.

Serial Ports 1 and 2 (J10/J11) (TMCP700 I/O Mode)

The MCP750 provides both asynchronous (ports 1 and 2) and synchronous/asynchronous (ports 3 and 4) serial connections. The asynchronous interface is implemented with a pair of RJ45 connectors (COM1 and COM2) located on the TMCP700 transition module. The signals for COM1 are also routed to J15 on the MCP750. A terminal may be connected to J11 or J15 on the MCP750, but not both at the same time. The pin assignments are listed in the following table.

Table 4-15. Serial Connections - Ports 1 and 2 (J10 and J11) (TMCP700)

1	DCD*n*	5	RXD*n*
2	RTS*n*	6	GND
3	GND	7	CTS*n*
4	TXD*n*	8	DTR*n*

Serial Ports 3 and 4 (J6/J24) (TMCP700 I/O Mode)

The synchronous/asynchronous interface for ports 3 and 4 is implemented with a pair of HD26 connectors (J6 and J24) located on the front panel of the transition module. The pin assignments for serial ports 3 and 4 are listed in the following table.

Table 4-16. Serial Connections - Ports 3 and 4 (J6 and J24) (TMCP700)

1	No Connection
2	TXD*n*
3	RXD*n*
4	RTS*n*
5	CTS*n*
6	DSR*n*
7	GND
8	DCD*n*
9	SP*n*_P9
10	SP*n*_P10
11	SP*n*_P11
12	SP*n*_P12
13	SP*n*_P13
14	SP*n*_P14
15	TXCI*n*
16	SP*n*_P16
17	RXCI*n*
18	LLB*n*
19	SP*n*_P19
20	DTR*n*
21	RLB*n*
22	RI*n*

Table 4-16. Serial Connections - Ports 3 and 4 (J6 and J24) (TMCP700) (Continued)

23	SP*n*_P23
24	TXCO*n*
25	TM*n*
26	SPn-P26

Parallel Connector (J7) (TMCP700 I/O Mode)

The parallel interface is implemented with an IEEE P1284 36-pin connector (J7) located on the TMCP700 transition module. The pin assignments are listed in the following table.

Table 4-17. Parallel Connector J7 (TMCP700)

1	PRBSY	GND	19
2	PRSEL	GND	20
3	PRACK*	GND	21
4	PRFAULT*	GND	22
5	PRPE	GND	23
6	PRD0	GND	24
7	PRD1	GND	25
8	PRD2	GND	26
9	PRD3	GND	27
10	PRD4	GND	28
11	PRD5	GND	29
12	PRD6	GND	30
13	PRD7	GND	31
14	PRINIT*	GND	32
15	PRSTB*	GND	33
16	SELIN*	GND	34
17	AUTOFD*	GND	35
18	Pull-up	No Connection	36

For detailed descriptions of the various interconnect signals, consult the support information documentation package for the MCP750 SBC or the support information sections of the transition module documentation as necessary.

Keyboard/Mouse Connector (J16) (TMCP700 I/O Mode)

The TMCP700 has a 6-pin circular DIN connector for the keyboard and mouse functions. For keyboard only operations, the keyboard may be plugged directly into this connector. To get keyboard and mouse operations, a Y-adapter cable is required (Motorola part number 30-W2309E01A). The pin assignments are listed in the following table.

Table 4-18. Keyboard/Mouse Connector J16 (TMCP700)

1	KBDDAT
2	MSDAT
3	GND
4	+5V (Fused)
5	KBDCLK
6	MSCLK

USB Connectors (J18/J19) (Optional TMCP700 I/O Mode)

The TMCP700 has two USB series A receptacles, J18, and J19. However, the standard version of the MCP700 board does not route the USB signals to these connectors in order to prevent long stubs on the MCP750 front panel USB connections. An alternate build option of the MCP750 may route the USB signals to the TMCP700 Transition Module in place of the MCP750 front panel connectors.

EIDE Connector (J15)

The TMCP700 provides a 40-pin header (J15) to interface to the MCP750 secondary EIDE port. The pin assignments and signal mnemonics for this connector are listed in the following table:

Table 4-19. EIDE Connector (J15)

Pin	Signal	Signal	Pin
1	DRESET_L	GND	2
3	DD7	DD8	4
5	DD6	DD9	6
7	DD5	DD10	8
9	DD4	DD11	10
11	DD3	DD12	12
13	DD2	DD13	14
15	DD1	DD14	16
17	DD0	DD15	18
19	GND	No Connect	20
21	DMARQ	GND	22
23	DIOW_L	GND	24
25	DIOR_L	GND	26
27	IORDY	No Connect	28
29	DMACK_L	GND	30
31	INTRQ	No Connect	32
33	DA1	No Connect	34
35	DA0	DA2	36
37	CS1FX_L	CS3FX_L	38
39	No Connect	GND	40

Floppy Port Connector (J17)

The TMCP700 provides a 34-pin header (J17) to interface to a floppy disk drive. The pin assignments and signal mnemonics for this connector are listed in the following table:

Table 4-20. Floppy Connector (J17)

Pin	Signal	Signal	Pin
1	GND	No Connect	2
3	GND	No Connect	4
5	GND	No Connect	6
7	GND	Index_L	8
9	GND	MTRQ_L	10
11	GND	DS1_L	12
13	No Connect	DSQ_L	14
15	GND	MTR1_L	16
17	No Connect	DIR_L	18
19	GND	STEP_L	20
21	GND	WDATA_L	22
23	GND	WGATE_L	24
25	GND	TR0_L	26
27	GND	WPROT_L	28
29	GND	RDATA_L	30
31	GND	HDSEL_L	32
33	GND	DSKCHG_L	34

+5Vdc Power Connector (J14)

The TMCP700 has a 4-pin header that can be used to provide +5Vdc power to offboard devices. This power is derived from the fused +5Vdc power on the MCP750. Any external device powered from this connector must not draw more than 200mA. The pin assignments are listed in the following table.

Table 4-21. +5Vdc Power Connector (J14)

Pin	Signal
1	+5Vdc
2	GND
3	GND
4	No Connect

Speaker Output Connector (J13)

The 2-pin header (J13) provides connection to an external speaker from the MCP750 PCB Counter 2 output. The pin assignments are listed in the following table.

Table 4-22. Speaker Output Connector (J13)

Pin	Signal
1	GND
2	SPKROC_L

PMC I/O Connectors (J2/J21)

The PMC I/O connectors consist of two 64-pin header connectors J2 and J21. The pin assignments and signal mnemonics for these connectors are listed in the following two tables:

Table 4-23. PMC I/O Connector (J2)

Pin	Signal	Signal	Pin
1	GND	PMCIO1	2
3	GND	PMCIO2	4
5	GND	PMCIO3	6
7	GND	PMCIO4	8

Table 4-23. PMC I/O Connector (J2) (Continued)

Pin	Signal	Signal	Pin
9	GND	PMCIO5	10
11	GND	PMCIO6	12
13	GND	PMCIO7	14
15	GND	PMCIO8	16
17	GND	PMCIO9	18
19	GND	PMCIO10	20
21	GND	PMCIO11	22
23	GND	PMCIO12	24
25	GND	PMCIO13	26
27	GND	PMCIO14	28
29	GND	PMCIO15	30
31	GND	PMCIO16	32
33	GND	PMCIO17	34
35	GND	PMCIO18	36
37	GND	PMCIO19	38
39	GND	PMCIO20	40
41	GND	PMCIO21	42
43	GND	PMCIO22	44
45	GND	PMCIO23	46
47	GND	PMCIO24	48
49	GND	PMCIO25	50
51	GND	PMCIO26	52
53	GND	PMCIO27	54
55	GND	PMCIO28	56
57	GND	PMCIO29	58
59	GND	PMCIO30	60
61	GND	PMCIO31	62
63	GND	PMCIO32	64

Table 4-24. PMC I/O Connector (J21)

Pin	Signal	Signal	Pin
1	GND	PMCIO33	2
3	GND	PMCIO34	4
5	GND	PMCIO35	6
7	GND	PMCIO36	8
9	GND	PMCIO37	10
11	GND	PMCIO38	12
13	GND	PMCIO39	14
15	GND	PMCIO40	16
17	GND	PMCIO41	18
19	GND	PMCIO42	20
21	GND	PMCIO43	22
23	GND	PMCIO44	24
25	GND	PMCIO45	26
27	GND	PMCIO46	28
29	GND	PMCIO47	30
31	GND	PMCIO48	32
33	GND	PMCIO49	34
35	GND	PMCIO50	36
37	GND	PMCIO51	38
39	GND	PMCIO52	40
41	GND	PMCIO53	42
43	GND	PMCIO54	44
45	GND	PMCIO55	46
47	GND	PMCIO56	48
49	GND	PMCIO57	50
51	GND	PMCIO58	52
53	GND	PMCIO59	54
55	GND	PMCIO60	56

Table 4-24. PMC I/O Connector (J21) (Continued)

Pin	Signal	Signal	Pin
57	GND	PMCIO61	58
59	GND	PMCIO62	60
61	GND	PMCIO63	62
63	GND	PMCIO64	64

PPCBug Overview

The PPCBug firmware is the layer of software just above the hardware. The firmware provides the proper initialization for the devices on the MCP750 motherboard upon power-up or reset.

This chapter provides information on the PPCBug and its architecture. Additionally, it describes the monitor (interactive command portion of the firmware) and provides instructions on using the PPCBug debugger and the associated special commands. A complete list of PPCBug commands is also included in this chapter in Table 5-7.

Chapter 6, *CNFG and ENV Commands* contains information about the CNFG and ENV commands, system calls, and other advanced user topics.

For additional information about the PPCBug, refer to the *PPCBug Firmware Package User's Manual* (*PPCBUGA1/UM and PPCBUGA2/UM)* and the *PPCBug Diagnostics Manual (PPCDIAA/UM), as listed in Appendix B, Related Documentation.*

PPCBug Basics

The PowerPC debug firmware (PPCBug) is a powerful evaluation and debugging tool for systems built around the Motorola PowerPC microcomputers. Facilities are available for loading and executing user programs under complete operator control for system evaluation.

The PPCBug provides a high degree of functionality, user friendliness, portability, and ease of maintenance.

It is portable and easy to understand because it was written entirely in the C programming language, except where necessary to use assembler functions.

The PPCBug includes commands for:

- Display and modification of memory
- Breakpoint and tracing capabilities
- A powerful assembler and disassembler useful for patching programs
- A self-test at power-up feature which verifies the integrity of the system

The PPCBug consists of three parts:

- A command-driven, user-interactive *software debugger* (described in the *PPCBug Firmware Package User's Manual, PPCBUGA1/UM* and *PPCBUGA2/UM)*. It is also referred to as "the debugger" or "PPCBug".
- A command-driven *diagnostics package* for the MCP750 hardware, also referred to as the "diagnostics". The diagnostics package is described in the *PPCBug Diagnostics Manual (PPCDIAA/UM).*
- A *user interface* or *debug*/*diagnostics monitor* that accepts commands from the system console terminal.

When using the PPCBug, you operate out of either the *debugger directory* or the *diagnostic directory.*

- If you are in the debugger directory, the debugger prompt `PPC1-Bug>` is displayed and you have all of the debugger commands at your disposal.
- If you are in the diagnostic directory, the diagnostic prompt `PPC1-Diag>` is displayed and you have all of the diagnostic commands at your disposal as well as all of the debugger commands.

Use the **SD** command to switch back and forth between these directories.

Because PPCBug is command-driven, it performs its various operations in response to user commands entered at the keyboard. When you enter a command, PPCBug executes the command and the prompt reappears.

However, if you enter a command that causes execution of user target code (for example, **GO**), then control may or may not return to PPCBug, depending on the outcome of the user program.

Memory Requirements

PPCBug requires a maximum of 768KB of read/write memory (DRAM). The debugger allocates this space from the top of memory. For example, a system containing 64MB ($04000000) of read/write memory will place the PPCBug memory page at locations $03F80000 to $03FFFFFF.

PPCBug Implementation

PPCBug is written largely in the C programming language, providing benefits of portability and maintainability. Where necessary, assembly language has been used in the form of separately compiled program modules containing only assembler code. No mixed-language modules are used.

Physically, PPCBug is contained in two socketed 32-pin PLCC Flash devices that together provide 1MB of storage. The executable code is checksummed at every power-on or reset firmware entry, and the result (which includes a precalculated checksum contained in the Flash devices) is verified against the expected checksum.

MPU, Hardware, and Firmware Initialization

The debugger performs the MPU, hardware, and firmware initialization process. This process occurs each time the MCP750 is reset or powered up. The steps below represent high-level outline (not all of the detailed steps are listed):

1. Sets MPU.MSR to known value.
2. Invalidates the MPU's data/instruction caches.
3. Clears all segment registers of the MPU.

4. Clears all block address translation registers of the MPU.
5. Initializes the MPU-bus-to-PCI-bus bridge device.
6. Initializes the PCI-bus-to-ISA-bus bridge device.
7. Calculate the external bus clock speed of the MPU.
8. Delays for 750 milliseconds.
9. Determines the CPU board type.
10. Sizes the local read/write memory (that is, DRAM).
11. Initializes the read/write memory controller.
12. Sets base address of memory to $00000000.
13. Retrieves the speed of read/write memory from NVRAM.
14. Initializes the read/write memory controller with the speed of read/write memory.
15. Retrieves the speed of read only memory (that is, Flash) from NVRAM.
16. Initializes the read only memory controller with the speed of read only memory.
17. Enables the MPU's instruction cache.
18. Copies the MPU's exception vector table from $FFF00000 to $00000000.
19. Initializes the PC87307 resources' base addresses.
20. Verifies MPU type.
21. Enable the super-scalar feature of the MPU (boards with MPC750 type chips only).
22. Initialize the Keyboard Controller (PC87307).
23. Determines the debugger's console/host ports and initializes the appropriate devices (PC16550/GD54xx/Z85C230).

24. Displays the debugger's copyright message.
25. Displays any hardware initialization errors that may have occurred.
26. Checksums the debugger object, and displays a warning message if the checksum failed to verify.
27. Displays the amount of local read/write memory found.
28. Verifies the configuration data that is resident in NVRAM, and displays a warning message if the verification failed.
29. Calculates and displays the MPU clock speed, verifies that the MPU clock speed matches the configuration data, and displays a warning message if the verification fails.
30. Displays the BUS clock speed, verifies that the BUS clock speed matches the configuration data, and displays a warning message if the verification fails.
31. Displays any Keyboard Controller initialization error that occurs.
32. Probes PCI bus for supported network devices.
33. Probes PCI bus for supported mass storage devices.
34. Initializes the memory/IO addresses for the supported PCI bus devices.
35. Executes Self-Test, if so configured. (Default is no Self-Test.)
36. Extinguishes the board fail LED, if there are no self-test failures or initialization/configuration errors.
37. Executes the configured boot routine, either ROMboot, Autoboot, or Network Autoboot.
38. Executes the user interface (that is, displays the `PPC1-Bug>` or `PPC1-Diag>` prompt).

Using PPCBug

PPCBug is command-driven; it performs its various operations in response to commands that you enter at the keyboard. When the `PPC1-Bug` prompt appears on the screen, the debugger is ready to accept debugger commands. When the `PPC1-Diag>` prompt appears on the screen, the debugger is ready to accept diagnostic commands. To switch from one mode to the other, enter **SD**.

What you key in is stored in an internal buffer. Execution begins only after you press the **Return** or **Enter** key. This allows you to correct entry errors (if necessary) with the control characters described in the *PPCBug Firmware Package User's Manual* (PPCBUGA1/UM and PPCBUGA2/UM).

After the debugger executes the command, the prompt reappears. However, if the command causes execution of user target code (for example, **GO**) then control may or may not return to the debugger, depending on what the user program does. For example, if a breakpoint has been specified, then control returns to the debugger when the breakpoint is encountered during execution of the user program. Alternately, the user program could return to the debugger by means of the System Call Handler routine RETURN (described in the *PPCBug Firmware Package User's Manual*, listed in Appendix B, *Related Documentation*). For additional information about this topic, refer to the **GD**, **GO**, and **GT** command descriptions in the *PPCBug Firmware Package User's Manual*.

A debugger command is made up of the following parts:

- The command name (uppercase or lowercase) (for example, **MD** or **md**).
- Any required arguments, as specified by command.
- At least one space before the first argument. Precede all other arguments with either a space or comma.
- One or more options. Precede an option or a string of options with a semicolon (**;**). If no option is entered, the command's default option conditions are used.

Debugger Commands

Debugger commands provide an interactive means for loading and executing applications in a controlled manner so that they may be evaluated. The debugger includes commands for:

- The display and modification of memory
- Breakpoint and tracing capabilities
- Assembler and disassembler

Standard Commands

Standard debugger commands are listed in the following table. They are described in more detail in the *PPCBug Firmware Package User's Manual*, listed in Appendix B, *Related Documentation*.

Note You can list all the available debugger commands by entering the Help (**HE**) command alone. You can view the syntax (description) for a particular command by entering **HE,** followed by a space, followed by the particular command mnemonic listed below, followed by a carriage return. Keep in mind that help is now available on both the BUG and DIAG side. In addition, issuing help on a DIAG test category will give more information about the tests in that category. The later is accomplished by entering **HE**, followed by a space, followed by the test category description (for example, UART), followed by a carriage return.

Table 5-1. Debugger Commands

Command	Description
AS	One Line Assembler
BC	Block of Memory Compare
BF	Block of Memory Fill
BI	Block of Memory Initialize
BM	Block of Memory Move
BR	Breakpoint Insert

Table 5-1. Debugger Commands (Continued)

Command	Description
NOBR	Breakpoint Delete
BS	Block of Memory Search
BV	Block of Memory Verify
CM	Concurrent Mode
NOCM	No Concurrent Mode
CNFG	Configure Board Information Block
CS	Checksum
CSAR	PCI Configuration Space READ Access
CSAW	PCI Configuration Space WRITE Access
DC	Data Conversion
DMA	Block of Memory Move
DS	One Line Disassembler
DU	Dump S-Records
ECHO	Echo String
ENV	Set Environment
FORK	Fork Idle MPU at Address
FORKWR	Fork Idle MPU with Registers
GD	Go Direct (Ignore Breakpoints)
GEVBOOT	Global Environment Variable Boot
GEVDEL	Global Environment Variable Delete
GEVDUMP	Global Environment Variable(s) Dump
GEVEDIT	Global Environment Variable Edit
GEVINIT	Global Environment Variable Initialization
GEVSHOW	Global Environment Variable(s) Display
GN	Go to Next Instruction
GO	Go Execute User Program
GT	Go to Temporary Breakpoint
HE	Help
IDLE	Idle Master MPU

Table 5-1. Debugger Commands (Continued)

Command	Description
IOC	I/O Control for Disk
IOI	I/O Inquiry
IOP	I/O Physical (Direct Disk Access)
IOT	I/O Teach for Configuring Disk Controller
IRD	Idle MPU Register Display
IRM	Idle MPU Register Modify
IRS	Idle MPU Register Set
LO	Load S-Records from Host
MA	Macro Define/Display
NOMA	Macro Delete
MAE	Macro Edit
MAL	Enable Macro Listing
NOMAL	Disable Macro Listing
MAR	Load Macros
MAW	Save Macros
MD, MDS	Memory Display
MENU	System Menu
MM	Memory Modify
MMD	Memory Map Diagnostic
MS	Memory Set
MW	Memory Write
NAB	Automatic Network Boot
NAP	Nap MPU
NBH	Network Boot Operating System, Halt
NBO	Network Boot Operating System
NIOC	Network I/O Control
NIOP	Network I/O Physical
NIOT	Network I/O Teach (Configuration)
NPING	Network Ping

Table 5-1. Debugger Commands (Continued)

Command	Description
OF	Offset Registers Display/Modify
PA	Printer Attach
NOPA	Printer Detach
PBOOT	Bootstrap Operating System
PF	Port Format
NOPF	Port Detach
PFLASH	Program FLASH Memory
PS	Put RTC into Power Save Mode
RB	ROMboot Enable
NORB	ROMboot Disable
RD	Register Display
REMOTE	Remote
RESET	Cold/Warm Reset
RL	Read Loop
RM	Register Modify
RS	Register Set
RUN	MPU Execution/Status
SD	Switch Directories
SET	Set Time and Date
SROM	SROM Examine/Modify
SYM	Symbol Table Attach
NOSYM	Symbol Table Detach
SYMS	Symbol Table Display/Search
T	Trace
TA	Terminal Attach
TIME	Display Time and Date
TM	Transparent Mode

Table 5-1. Debugger Commands (Continued)

Command	Description
TT	Trace to Temporary Breakpoint
VE	Verify S-Records Against Memory
VER	Revision/Version Display
WL	Write Loop

Caution

Although a command to allow the erasing and reprogramming of Flash memory is available to you, keep in mind that reprogramming any portion of the MCP750's Flash memory (bank B) will erase everything currently contained in the Flash memory, including the PPCBug debugger.

High Availability Supported Commands

The following table lists PPCBug debugger commands that have been added to support High Availability (HA) features.

Table 5-2. High Availability Specific Debugger Commands

Name	Description
PEEPROM	Program/Verify the HSC EEPROM
PCIDOM	Initialize/Control PCI Bus Domain
PWROFF	Power Off an HA PCI Bus Module
PWRON	Power On a HA PCI Bus Module
PCIIOI	PCI Domain I/O Inquiry

You can list the syntax for one of these commands using the **HE** command with the command name. For example,

HE PWROFF <Return>

shows the syntax for using the **PWROFF** command to power an I/O module.

Unsupported Commands

The following table lists standard PPCBug debugger commands that are not supported on the MCP750.

Table 5-3. Unsupported Debugger Commands

Name	Description
DMA	DMA Block of Memory Move
FORK	Fork Idle MPU at Address
FORKWR	Fork Idle MPU with Registers
IDLE	Idle Master MPU
IRD	Idle MPU Register Display
IRM	Idle MPU Register Modify
IRS	Idle MPU Register Set
NAP	Nap MPU
RUN	MPU Execution/Status

Debugger System Call Interfaces

Supported System Call Interfaces

The following table lists debugger system call interfaces that have been added to support High Availability (HA) functionality.

Table 5-4. High Availability Specific Debugger System Calls

Name	Description
.PCIDOM	Initialize/Control PCI Bus Domain
.PWROFF	Power Off an HA PCI Bus Module
.PWRON	Power On a HA PCI Bus Module

PCIDOM allows a CPU module to claim control of one or both of the PCI domains. In an active/standby arrangement, for example, the CPU in domain A uses **PCIDOM** to take control of both the local PCI domain, domain A, and of the remote domain, domain B.

PWROFF and **PWRON** allow the user to power off or to power on a module in order to hot swap it.

Unsupported System Call Interfaces

The following table lists standard PPCBug debugger system call interfaces that are not supported on the MPC750.

Table 5-5. Unsupported Debugger System Calls

Name	Description
.FORKMPU	Fork MPU
.FORKMPUR	Fork MPU with Registers
.IDLEMPU	Idle MPU

Bug Diagnostics

PPCBug hardware diagnostics package allows for testing and troubleshooting the MPC750 hardware, including the High Availability (HA) features of the CPU module. It includes tests for:

- Memory Read/Write
- L2 Cache
- Real Time Clock
- Ethernet Controller
- ISA Bridge
- Serial Communications Controller
- UART
- Keyboard/Mouse Controller
- Parallel Interface
- PCI/PMC Interface
- EIDE

- Counter/Timer

Diagnostic Tests

In order to use the diagnostics, you must switch to the diagnostic directory. You may switch between directories by using the **SD** (Switch Directories) command. You may view a list of the commands in the directory that you are currently in by using the **HE** (Help) command.

If you are in the debugger directory, the debugger prompt `PPC1-Bug>` displays, and all of the debugger commands are available. Diagnostics commands cannot be entered at the `PPC1-Bug>` prompt.

If you are in the diagnostic directory, the diagnostic prompt `PPC1-Diag>` displays, and all of the debugger and diagnostic commands are available.

Note that not all tests are valid for the MCP750. Using the **HE** command, you can list the diagnostic routines available in each test group. Refer to the *PPCBug Diagnostics Manual*, listed in *Appendix B, Related Documentation*, for complete descriptions of the diagnostic routines and instructions on how to invoke them.

Table 5-6. Specific Diagnostic Test Groups

Test Set	Description
CL1283	Parallel Interface (CL1283)
DEC	DECchip 21x40 EIDE Tests
ISABRDGE	PCI/ISA Bridge Tests
KBD8730x	PC8730x Keyboard/Mouse Tests
L2CACHE	Level 2 Cache Tests
NCR	NCR 53C8xx SCSI-2 I/O Processor Tests*
PAR8730x	PC8730x Parallel Port Test
PCIBUS	Generic PCI/PMC Slot Test
RAM	Random Access Memory Tests
RTC	MK48Txx Real-Time Clock Tests

Table 5-6. Specific Diagnostic Test Groups (Continued)

Test Set	Description
SCC	Serial Communications Controller Tests
UART	Serial Input/Output UART Tests
VGA543x	Video Graphics Tests*
Z8536	Zilog Z8536 Counter/Timer Tests

Notes 1. You may enter command names in either uppercase or lowercase.

2. Some diagnostics depend on restart defaults that are set up only in a particular restart mode. Refer to the documentation on a particular diagnostic for the correct mode.

3. Test Sets marked with an asterisk (*) are not available on the MCP750, unless SCSI or Video PMCs are installed.

High Availability Specific PPCBug Diagnostic Commands

The following table lists PPCBug diagnostic commands that have been added to support High Availability features. PPCBug Diagnostic Commands Specific for HA systems.

Table 5-7. PPCBug Diagnostic Commands For High Availability Systems

Name	Description
AST	Abbreviated Self-Tests
HSC	Hot Swap Controller/Bridge Tests

Unsupported PPCBug Diagnostic Commands

The following table lists PPCBug diagnostic commands that are part of the standard PPCBug package, but are not supported on the MPC750 system.

Table 5-8. Unsupported PPCBug Diagnostic Commands

Name	Description
CL1283	Parallel Interface (Cirrus CL-CD1283) Tests
CS4231	CS4231 Audio Codec Tests
NCR	NCR 53C8XX SCSI I/O Processor Tests
VGA543X	VGA Controller (GD543X) Tests

CNFG and ENV Commands 6

Overview

You can use the factory-installed debug monitor, PPCBug, to modify certain parameters contained in the PowerPC board's Non-Volatile RAM (NVRAM), also known as Battery Backed-up RAM (BBRAM).

- The Board Information Block in NVRAM contains various elements concerning operating parameters of the hardware. Use the PPCBug command **CNFG** to change those parameters.
- Use the PPCBug command **ENV** to change configured PPCBug parameters in NVRAM.

The **CNFG** and **ENV** commands are both described in the *PPCBug Firmware Package User's Manual* (PPCBUGA1/UM and PPCBUGA2/UM). Refer to that manual for general information about their use and capabilities.

The following paragraphs present additional information about **CNFG** and **ENV** that is specific to the PPCBug debugger, along with the parameters that can be configured with the **ENV** command.

CNFG - Configure Board Information Block

This command is used to display and configure the Board Information Block, which is stored in the NVRAM. The Board Information Block lists details of your specific board, such as the Board Serial Number, the Board Identifier, the Bus Clock Speed, and other operational or ID characteristics. The example below displays a typical Board Information Block:

```
Board (PWA) Serial Number   = "2717994             "
Board Identifier            = "MCP750-60X-0XX       "
Artwork (PWA) Identifier    = "01-w3378F01B         "
```

```
MPU Clock Speed             = “233                  ”
Bus Clock Speed             = “067                  ”
Ethernet Address            = “08003E25D0C5         ”
Local SCSI Identifier*      = “07                   ”
System Serial Number        = “1234567              ”
System Identifier           = “Motorola MCP750603-001a”
License Identifier          = “12345678             ”
```

The value or identifier to the left of the equal sign is displayed as left-justified character (ASCII) strings padded with space characters and quotes (“) are displayed to indicate the size of the string. Values that are not in quotes are considered data strings and data strings are right-justified. The data strings are padded with zeroes if the length is not met. It is important to note that the MCP750 has no local SCSI bus controller, hence, the Local SCSI Identifier parameter is ignored by the PPCBug.

The Board Information Block is factory-configured before shipment. There is no need to modify block parameters unless the NVRAM is corrupted.

Refer to the *Programmer’s Reference Guide* (MCP750A/PG) for the actual location and other information about the Board Information Block.

Refer also to the *PPCBug Firmware Package User's Manual* (PPCBUGA1/UM and PPCBUGA2/UM) for a description of **CNFG** and examples.

ENV - Set Environment

Use the **ENV** command to view and/or configure interactively all PPCBug operational parameters that are kept in Non-Volatile RAM (NVRAM).

Refer to the *PPCBug Firmware Package User's Manual* (PPCBUGA1/UM and PPCBUGA1/UM, listed in Appendix B, *Related Documentation*) for a description of the use of **ENV**.

Listed and described in the section below, *Configuring the PPCBug Parameters*, are the parameters that you can configure using **ENV**. The default values shown were those in effect when this publication went to print.

Configuring the PPCBug Parameters

The parameters that can be configured using **ENV** are:

```
Bug or System environment [B/S] = B?
```

B Bug is the mode where no system type of support is displayed. However, system-related items are still available (Default).

S System is the standard mode of operation, and is the default mode if NVRAM should fail. System mode is defined in the *PPCBug Firmware Package User's Manual*.

```
Field Service Menu Enable [Y/N] = N?
```

Y Display the field service menu.

N Do not display the field service menu (Default).

```
Probe System for Supported I/O Controllers [Y/N] = Y?
```

Y Accesses will be made to the appropriate system buses (for example, VMEbus, local MPU bus) to determine the presence of supported controllers (Default).

N Accesses will not be made to the VMEbus to determine the presence of supported controllers.

```
Auto-Initialize of NVRAM Header Enable [Y/N] = Y?
```

Y NVRAM (PReP partition) header space will be initialized automatically during board initialization, but only if the PReP partition fails a sanity check (Default).

N NVRAM header space will not be initialized automatically during board initialization.

```
Network PReP-Boot Mode Enable [Y/N] = N?
```

Y Enable PReP-style network booting (same boot image from a network interface as from a mass storage device).

N Do not enable PReP-style network booting (Default).

```
SCSI Bus Reset on Debugger Startup [Y/N] = N?
```

Y SCSI bus is reset on debugger setup.

N SCSI bus is not reset on debugger setup (Default).

```
Primary SCSI Bus Negotiations Type [A/S/N] = A?
```

A Asynchronous SCSI bus negotiation (Default).

S Synchronous SCSI bus negotiation.

N None.

```
Primary SCSI Data Bus Width [W/N] = N?
```

W Wide SCSI (16-bit bus).

N Narrow SCSI (8-bit bus) (Default).

```
Secondary SCSI Identifier = “07”?
```

If the board has a secondary SCSI controller, this number is the secondary SCSI ID or address. For the MCP750, all PCI add-on SCSI controllers/adaptors supported by PPCBug are set to the SCSI ID value entered here.

```
NVRAM Bootlist (GEV.fw-boot-path) Boot Enable [Y/N] = N?
```

Y Give boot priority to devices defined in the *fw-boot-path* global environment variable (GEV).

N Do not give boot priority to devices listed in the *fw-boot-path* GEV (Default).

Note When enabled, the GEV (Global Environment Variable) boot takes priority over all other boots, including Autoboot and Network Boot.


```
NVRAM Bootlist (GEV.fw-boot-path) Boot at power-up only [Y/N] = N?
```

Y Give boot priority to devices defined in the *fw-boot-path* GEV at power-up reset only.

N Give power-up boot priority to devices listed in the *fw-boot-path* GEV at any reset (Default).

```
NVRAM Bootlist (GEV.fw-boot-path) Boot Abort Delay = 5?
```

The time in seconds that a boot from the NVRAM boot list will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 5 seconds)

```
Auto Boot Enable [Y/N]   = N?
```

Y The Autoboot function is enabled.

N The Autoboot function is disabled (Default).

```
Auto Boot at power-up only [Y/N] = N?
```

Y Autoboot is attempted at power-up reset only.

N Autoboot is attempted at any reset (Default).

```
Auto Boot Scan Enable [Y/N]   = Y?
```

Y If Autoboot is enabled, the Autoboot process attempts to boot from devices specified in the scan list (for example, FDISK/CDROM/TAPE/HDISK) (Default).

N If Autoboot is enabled, the Autoboot process uses the Controller LUN and Device LUN to boot.

```
Auto Boot Scan Device Type List = FDISK/CDROM/TAPE/HDISK?
```

This is the listing of boot devices displayed if the Autoboot Scan option is enabled. If you modify the list, follow the format shown above (uppercase letters, using forward slash as separator).


```
Auto Boot Controller LUN   = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* (listed in Appendix B, *Related Documentation*) for a listing of disk/tape controller modules currently supported by PPCBug. (Default = $00)

```
Auto Boot Device LUN    = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of disk/tape devices currently supported by PPCBug. (Default = $00)

```
Auto Boot Partition Number = 00?
```

Which disk "partition" is to be booted, as specified in the PowerPC Reference Platform (PRP) specification. If set to zero, the firmware will search the partitions in order (1, 2, 3, 4) until it finds the first "bootable" partition. That is then the partition that will be booted. Other acceptable values are 1, 2, 3, or 4. In these four cases, the partition specified will be booted without searching.

```
Auto Boot Abort Delay = 7?
```

The time in seconds that the Autoboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds (Default = 7 seconds).

```
Auto Boot Default String [NULL for an empty string] =?
```

You may specify a string (filename) which is passed on to the code being booted. The maximum length of this string is 16 characters (Default = null string).

```
ROM Boot Enable [Y/N] = N?
```

Y The ROMboot function is enabled.

N The ROMboot function is disabled. (Default)

```
ROM Boot at power-up only [Y/N] = Y?
```

Y ROMboot is attempted at power-up only (Default).

N ROMboot is attempted at any reset.


```
ROM Boot Abort Delay = 5?
```

The time in seconds that the ROMboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds (Default = 5 seconds).

```
ROM Boot Direct Starting Address = FFF00000?
```

The first location tested when PPCBug searches for a ROMboot module (Default = $FFF00000).

```
ROM Boot Direct Ending Address = FFFFFFFC?
```

The last location tested when PPCBug searches for a ROMboot module (Default = $FFFFFFFC).

```
Network Auto Boot Enable [Y/N] = N?
```

Y The Network Auto Boot (NETboot) function is enabled.

N The NETboot function is disabled (Default).

```
Network Auto Boot at power-up only [Y/N] = N?
```

Y NETboot is attempted at power-up reset only.

N NETboot is attempted at any reset (Default).

```
Network Auto Boot Controller LUN = 00?
```

Refer to the *PPCBug Firmware Package User's Manual*, listed in Appendix B, *Related Documentation*, for a listing of network controller modules currently supported by PPCBug (Default = $00).

```
Network Auto Boot Device LUN = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of network controller modules currently supported by PPCBug (Default = $00).

```
Network Auto Boot Abort Delay = 5?
```

The time in seconds that the NETboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds (Default = 5 seconds).

```
Network Auto Boot Configuration Parameters Offset (NVRAM) =
00001000?
```

The address where the network interface configuration parameters are to be saved/retained in NVRAM; these parameters are the necessary parameters to perform an unattended network boot. A typical offset might be $1000, but this value is application-specific (Default = $00001000).



Caution

If you use the **NIOT** debugger command, these parameters need to be saved somewhere in the offset range $00001000 through $000016F7. The **NIOT** parameters do not exceed 128 bytes in size. The setting of this ENV pointer determines their location. If you have used the same space for your own program information or commands, they will be overwritten and lost.

You can relocate the network interface configuration parameters in this space by using the **ENV** command to change the Network Auto Boot Configuration Parameters Offset from its default of $00001000 to the value you need to be clear of your data within NVRAM.

```
Memory Size Enable [Y/N] = Y?
```

Y Memory will be sized for Self Test diagnostics (Default).

N Memory will not be sized for Self Test diagnostics.

```
Memory Size Starting Address = 00000000?
```

The default Starting Address is $00000000.

```
Memory Size Ending Address = 02000000?
```

The default Ending Address is the calculated size of local memory. If the memory start is changed from $00000000, this value will also need to be adjusted.

```
DRAM Speed in NANO Seconds = 60?
```

The default setting for this parameter will vary depending on the speed of the DRAM memory parts installed on the board. The default is set to the slowest speed found on the available banks of DRAM memory.

```
ROM First Access Length (0 - 31) = 10?
```

This is the value programmed into the MPC105 “ROMFAL” field (Memory Control Configuration Register 8: bits 23-27) to indicate the number of clock cycles used in accessing the ROM. The lowest allowable ROMFAL setting is $00; the highest allowable is $1F. The value to enter depends on processor speed; refer to your *Processor/Memory Mezzanine Module User’s Manual* for appropriate values. The default value varies according to the system’s bus clock speed.

Note ROM First Access Length is not applicable to the MCP750. The configured value is ignored by PPCBug.

```
ROM Next Access Length (0 - 15) = 0?
```

The value programmed into the MPC105 “ROMNAL” field (Memory Control Configuration Register 8: bits 28-31) to represent wait states in access time for nibble (or burst) mode ROM accesses. The lowest allowable ROMNAL setting is $0; the highest allowable is $F. The value to enter depends on processor speed; refer to your *Processor/Memory Mezzanine Module User’s Manual* for appropriate values. The default value varies according to the system’s bus clock speed.

Note ROM Next Access Length is not applicable to the MCP750. The configured value is ignored by PPCBug.

```
DRAM Parity Enable [On-Detection/Always/Never - O/A/N] = 0?
```

O	DRAM parity is enabled upon detection. (Default)
A	DRAM parity is always enabled.
N	DRAM parity is never enabled

Note This parameter (above) also applies to enabling ECC for DRAM.

```
L2 Cache Parity Enable [On-Detection/Always/Never - O/A/N] = O?
```

O	L2 Cache parity is enabled upon detection. (Default)
A	L2 Cache parity is always enabled.
N	L2 Cache parity is never enabled

```
PCI Interrupts Route Control Registers (PIRQ0/1/2/3) = 0A0B0E0F?
```

Initializes the PIRQx (PCI Interrupts) route control registers in the IBC (PCI/ISA bus bridge controller). The **ENV** parameter is a 32-bit value that is divided by 4 to yield the values for route control registers PIRQ0/1/2/3. The default is determined by system type. For details on PCI/ISA interrupt assignments and for suggested values to enter for

this parameter, refer to the *8259 Interrupts* section in Chapter 4 of the *MCP750 Programmer's Reference Guide*, listed in *Appendix B, Related Documentation*.

`Serial Startup Code Master Enable [Y/N]=N?`

The Serial Startup Codes can be displayed at key points in the initialization of the hardware devices. Should the debugger fail to come up to a prompt, the last code displayed will indicate how far the initialization sequence had progressed before stalling. The codes are enabled by an **ENV** parameter.

`Serial Startup Code LF Enable [Y/N]=N?`

A line feed can be inserted after each code is displayed to prevent it from being overwritten by the next code. This is also enabled by an **ENV** parameter.

A list of LED/serial codes is included in the section on MPU, Hardware, and Firmware Initialization in Chapter 1 of the *PPCBug Firmware Package User's Manual, Part 1*, listed in *Appendix B, Related Documentation*.

Specifications

Table A-1 lists the general specifications for MCP750 base boards. Subsequent sections detail cooling requirements and FCC compliance.

A complete functional description of the MCP750 base boards appears in Chapter 3, *Functional Description*. Specifications for the optional PCI mezzanines can be found in the documentation for those modules.

Table A-1. MCP750 Specifications

Characteristics	Specifications
Power requirements (Excluding transition module, PMC, keyboard, mouse)	+5Vdc (±5%), 3.8A typical, 4.4A max. +3.3Vdc (±5%), 1.9A typical, 2.5A max.
Operating temperature	-5°C to +55°C entry air with forced-air cooling (refer to *Cooling Requirements* section)
Storage temperature	–40°C to +85° C
Relative humidity	5% to 85% (non-condensing)
Physical dimensions Base board only Height Depth Base board with front panel and connectors Height Depth Front panel width	6U Eurocard 9.2 in. (233 mm) 6.3 in. (160 mm) 10.3 in. (262 mm) 7.4 in. (188 mm) 0.8 in. (20mm)

Cooling Requirements

The Motorola MCP750 family of Single Board Computers is specified, designed, and tested to operate reliably with an incoming air temperature range from -5° to +55° C (32° to 131° F) with forced air cooling of the entire assembly (base board and modules) at a velocity typically achievable by using a 100 CFM axial fan.

Temperature qualification is performed in a standard Motorola CompactPCI chassis. Twenty-five-watt load boards are inserted in two card slots, one on each side, adjacent to the board under test, to simulate a high power density system configuration. An assembly of three axial fans, rated at 100 CFM per fan, is placed directly under the CompactPCI card cage. The incoming air temperature is measured between the fan assembly and the card cage, where the incoming airstream first encounters the module under test. Test software is executed as the module is subjected to ambient temperature variations. Case temperatures of critical, high power density integrated circuits are monitored to ensure component vendors' specifications are not exceeded.

While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 10 CFM and 490 LFM flowing over the module. Less airflow is required to cool the module in environments having lower maximum ambients. Under more favorable thermal conditions, it may be possible to operate the module reliably at higher than 55° C with increased airflow.

It is important to note that there are several factors, in addition to the rated CFM of the air mover, which determine the actual volume and speed of air flowing over a module.

EMC Compliance

The MCP750 Single Board Computer was tested in an EMC-compliant chassis and meets the requirements for EN55022 Class B equipment. Compliance was achieved under the following conditions:

- Shielded cables on all external I/O ports.

- Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel.
- Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.
- Front panel screws properly tightened.

For minimum RF emissions, it is essential that the conditions above be implemented. Failure to do so could compromise the EMC compliance of the equipment containing the module.

Related Documentation B

Motorola Computer Group Documents

The Motorola publications listed below are referenced in this manual. You can obtain paper or electronic copies of Motorola Computer Group publications by:

- Contacting your local Motorola sales office
- Visiting Motorola Computer Group's World Wide Web literature site, http://www.motorola.com/computer/literature

Table B-1. Motorola Computer Group Documents

Document Title	Publication Number
MCP750 CompactPCI Single Board Computer Installation and Use	MCP750A/IH
MCP750 CompactPCI Single Board Computer Programmer's Reference Guide	MCP750A/PG
TMCP700 Transition Module Installation and Use	TMCP700A/IH
PPCBug Firmware Package User's Manual (Parts 1 and 2)	PPCBUGA1/UM PPCBUGA2/UM
PPCBug Diagnostics Manual	PPCDIAA/UM

To obtain the most up-to-date product information in PDF or HTML format, visit http://www.motorola.com/computer/literature.

B

Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table B-2. Manufacturers' Documents

Document Title and Source	Publication Number
MPC750™ RISC Microprocessor Technical Summary Motorola Literature Distribution Center Telephone: (800) 441-2447 or (303) 675-2140 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com	MPC750/D
MPC750™ RISC Microprocessor User's Manual Literature Distribution Center for Motorola Semiconductor Products Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com OR	MPC750UM/AD
IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPR604UMU-01

Table B-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
PowerPC™ Microprocessor Family: The Programming Environments Literature Distribution Center for Motorola Semiconductor Products Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPCFPE/AD MPRPPCFPE-01
DECchip 21140 PCI Fast Ethernet LAN Controller Hardware Reference Manual Digital Equipment Corporation Maynard, Massachusetts DECchip Information Line Telephone (United States and Canada): 1-800-332-2717 TTY (United States only): 1-800-332-2515 Telephone (outside North America): +1-508-568-6868	EC-QC0CA-TE
DECchip 21154 PCI-to-PCI Bridge Data Sheet Digital Equipment Corporation Maynard, Massachusetts DECchip Information Line Telephone (United States and Canada): 1-800-332-2717 TTY (United States only): 1-800-332-2515 Telephone (outside North America): +1-508-568-6868	EC-R24JA-TE

Table B-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
Digital Semiconductor 21x4 Serial ROM Format, Version 3.03 Specification, May 28, 1996. Digital Equipment Corporation Maynard, Massachusetts DECchip Information Line Telephone (United States and Canada): 1-800-332-2717 TTY (United States only): 1-800-332-2515 Telephone (outside North America): +1-508-568-6868	
PC87307VUL (Super I/O™ Enhanced Sidewinder Lite) Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, IEEE 1284 Parallel Port, and IDE Interface National Semiconductor Corporation Customer Support Center (or nearest Sales Office) 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, California 95052-8090 Telephone: 1-800-272-9959	PC87307VUL
MK48T559 CMOS 8K x 8 TIMEKEEPER™ SRAM Data Sheet SGS-Thomson Microelectronics Group Marketing Headquarters (or nearest Sales Office) 1000 East Bell Road Phoenix, Arizona 85022 Telephone: (602) 867-6100	M48T559
SCC (Serial Communications Controller) User's Manual (for Z85230 and other Zilog parts) Zilog, Inc. 210 East Hacienda Ave., mail stop C1-0 Campbell, California 95008-6600 Telephone: (408) 370-8016 FAX: (408) 370-8056	DC-8293-02

Table B-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
Z8536 CIO Counter/Timer and Parallel I/O Unit Product Specification and User's Manual (in Z8000® Family of Products Data Book) Zilog, Inc. 210 East Hacienda Ave., mail stop C1-0 Campbell, California 95008-6600 Telephone: (408) 370-8016 FAX: (408) 370-8056	DC-8319-00
VT82C586B PIPC PCI Integrated Peripheral Controller VIA Technologies, Inc. 5020 Brandin Court Fremont, CA 94538 Telephone: (510) 683-3300 FAX: (510) 683-3301	VT82C586B
ATMEL Nonvolitile Memory Data Book Atmel Corporation 2325 Orchord Parkway San Jose, CA 95131 Telephone: (408) 441-0311 FAX: (408) 436-4300 Website: http://www.atmel.com	AT24C04

B

Related Specifications

For additional information, refer to the following table for related specifications. As an additional aid, a source for the listed document is also provided. Please note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Table B-3. Related Specifications

Document Title and Source	Publication Number
IEEE - Common Mezzanine Card Specification (CMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386.1
Bidirectional Parallel Port Interface Specification Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	IEEE Standard 1284
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.1 PCI Special Interest Group 2575 NE Kathryn St. #17 Hillsboro, OR 97124 Telephone: (800) 433-5177 (inside the U.S.) or (503) 693-6232 (outside the U.S.) FAX: (503) 693-8344	PCI Local Bus Specification

Table B-3. Related Specifications (Continued)

Document Title and Source	Publication Number
PowerPC™ Microprocessor Common Hardware Reference Platform: A System Architecture (CHRP), Version 1.0 Literature Distribution Center for Motorola Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com OR APDA, Apple Computer, Inc. P.O. Box 319 Buffalo, NY 14207 Telephone: (800) 282-2732 FAX: (716) 871-6511 OR IBM 1580 Route 52, Bldg. 504 Hopewell Junction, NY 12533-6531 Telephone: (800) PowerPC OR Morgan Kaufmann Publishers, Inc. 340 Pine Street, Sixth Floor San Francisco, CA 94104-3205, USA Telephone: (415) 392-2665 FAX: (415) 982-2665	TB338/D MPRPPCHRP-01 ISBN 1-55860-394-8
PowerPC Reference Platform (PRP) Specification, Third Edition, Version 1.0, Volumes I and II International Business Machines Corporation Power Personal Systems Architecture 11400 Burnet Rd. Austin, TX 78758-3493 Document/Specification Ordering Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 Telephone: 708-296-9332	MPR-PPC-RPU-02

Table B-3. Related Specifications (Continued)

Document Title and Source	Publication Number
IEEE Standard for Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	IEEE 802.3

Table B-3. Related Specifications (Continued)

Document Title and Source	Publication Number
Information Technology - Local and Metropolitan Networks - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Global Engineering Documents 15 Inverness Way East Englewood, CO 80112-5704 Telephone: 1-800-854-7179 Telephone: (303) 792-2181 *(This document can also be obtained through the national standards body of member countries.)*	ISO/IEC 8802-3
Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange (EIA-232-D) Electronic Industries Association Engineering Department 2001 Eye Street, N.W. Washington, D.C. 20006	ANSI/EIA-232-D Standard
Compact PCI Specification PCI Industrial Manufacturers Group (PICMG) 401 Edgewater Pl, Suite 500 Wakefield, MA 01880 Telephone: 781-246-9318 Fax: 781-224-1239	CPCI Rev. 2.1 Dated 9/2/97
PCI-to-PCI Bridge Specification PCI-ISA Specification PCI Industrial Manufacturers Group (PICMG) 401 Edgewater Pl, Suite 500 Wakefield, MA 01880 Telephone: 781-246-9318 Fax: 781-224-1239	Rev. 1.02 Rev. 2.0

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