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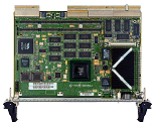
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Datasheets: MCPN765

MCPN765

CompactPCI Peripheral Processor

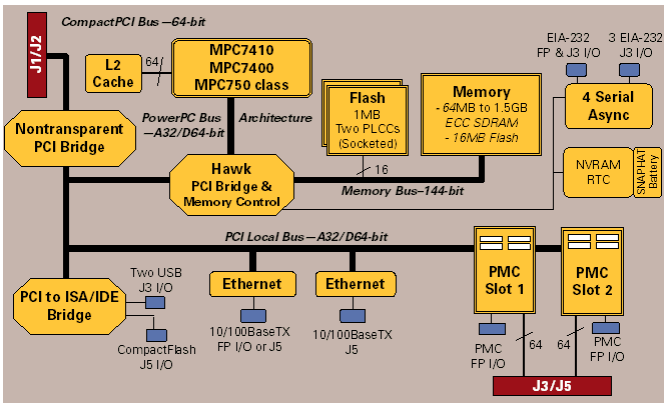


- MPC7400, MPC7410 or MPC750 class processor
- 1MB or 2MB of L2 cache
- Up to 1.5GB ECC SDRAM, with optional RAM500 memory expansion modules
- Dual 10/100BaseTX Ethernet interface
- Two 32/64-bit PMC expansion slots with front panel or backplane I/O
- 16MB on-board Flash memory for user-specified requirements
- Two 32-pin PLCC/CLCC sockets for Flash memory, up to 1MB capacity for on-board firmware or user-specified requirements
- Optional CompactFlash™ memory card socket on accompanying transition module
- On-board debug monitor with self-test diagnostics
- Two USB ports, four async serial ports
- 32KB NVRAM and time-of-day clock with replaceable battery backup
- Four 32-bit timers, one watchdog timer

Maximum performance and flexibility ideal for high availability applications

The MCPN765 series of CompactPCI® boards provides competitive processors, Motorola's PowerPlus II Architecture, dual 10/100BaseTX Ethernet, two PCI mezzanine card (PMC) slots and up to 1.5GB of ECC SDRAM. All this is available in a single CompactPCI slot.

Using the low-power, high-performance MPC7400, MPC7410 or MPC750 class processors, 64-bit local peripheral component interconnect (PCI) bus for the on-board peripherals and processor/memory bus to PCI bus bridge, the MCPN765 offers maximum performance and flexibility. It is also fully compliant to the PICMG® 2.1 Hot Swap Specification, making it the ideal choice for high availability applications.



MCPN765 Details

IEEE P1386.1 Compliant PMC Slots

The MCPN765 features dual PMC ports with support for both front-panel and backplane I/O. In addition to providing high-performance expansion I/O, the IEEE P1386.1 compliant PMC ports form a common architecture for future generations of products. Changing I/O requirements can be satisfied by simply replacing PMCs while reusing the same base platform and software, reducing the long-term cost of ownership.

PowerPlus II Architecture

A second-generation architecture, PowerPlus II Architecture is a processor and bus architecture fully optimized to get the maximum performance from the PowerPC architecture-compatible microprocessor family, the PCI bus and the CompactPCI bus. Features added to the original PowerPlus architecture include support for 100 MHz local bus operation and utilization of synchronous DRAM (SDRAM) technology. The outstanding performance of the PowerPlus II Architecture is not due to a single factor. A number of elements in the design of the PowerPlus II Architecture contribute to its outstanding performance including the processor/memory subsystem, high-speed local bus, optimally decoupled architecture, decoupling the processor from PCI and the advanced CompactPCI interface that reduces PCI delays.

TM-PIMC-0101

The TM-PIMC-0101 transition module provides industry-standard connector access to two RJ-45 Ethernet connectors, two RJ-45 async serial port connectors (configured as EIA DTE), two headers for async serial ports and two PIM slots for PMC interface modules. One socket for optional CompactFlash memory is also provided.

Firmware Monitor

Firmware must fulfill the traditional functions of test and initialization, in addition to operating system boot support. The MCPN765 firmware monitor exceeds these requirements, plus expands features like power-up tests with extensive diagnostics, as well as a powerful evaluation and debug tool for simple checkout or when high-level development debuggers require additional support. All this is included with the MCPN765 firmware, plus it supports booting both operating systems and kernels.

Operating Systems and Kernels

MCPN765 supports booting a complete range of real-time operating systems and kernels which may be purchased from the following companies:

Lynx Real-Time Systems, Inc.: LynxOS™

Wind River Systems, Inc.: VxWorks®

Specifications

Processor

Microprocessor:	450 or 500 MHz MPC750 class 400 MHz MPC7400 500 MHz MPC7410
On-chip Cache (I/D):	32K/32K

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We buy equipment

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