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VME147A/IH1A1
December 1997

Supplement to

MVME147

MPU VMEmodule

Installation and Use

(VME147A/IH1)

The original manual was written for the MVME147 MPU VMEmodule. The attached supplement pages are corrections for the Ethernet interface.

Please place this page behind the title page of the manual as a record of this change. Replace pages according to the following table:

Replace Old	With New	Add New
5-3/5-4	5-3/5-4	
5-17/5-18	5-17/5-18	

- ❑ A vertical bar (▌) in the margin of a revised page indicates a text change or addition.
- ❑ The supplement number appears at the bottom of each revised page.

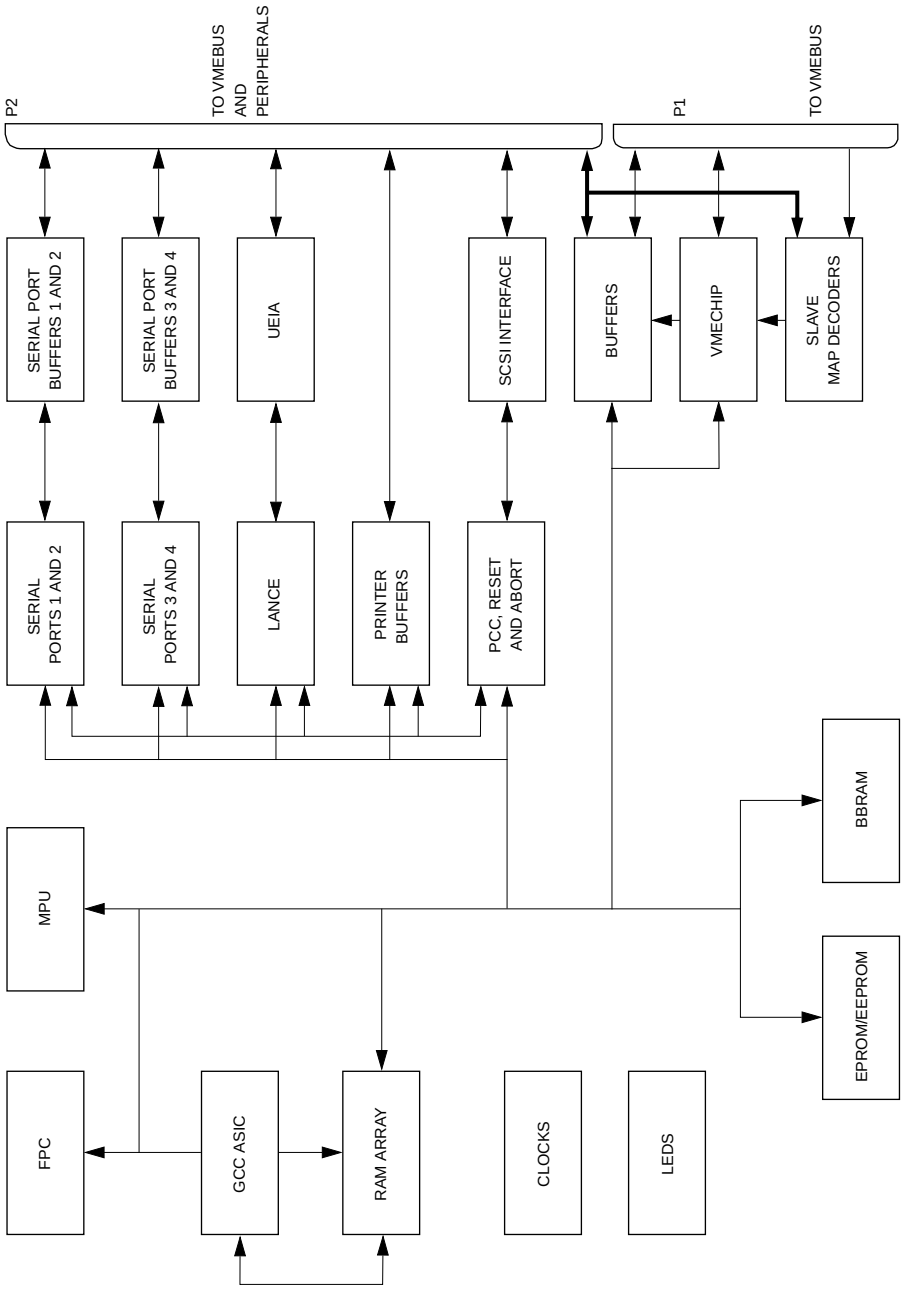


Figure 5-1. MVME147 Block Diagram

VMEbus System Controller

One of the many functions provided by the VMEchip is the VMEbus system controller function. The system controller includes the following:

- VMEbus global time-out timer
- System Clock (SYSCLK*) driver
- Arbiter
- Interrupt Acknowledge (IACK*) daisy-chain driver.

The system reset utility is also described here because it is enabled when the MVME147 is system controller. The system controller function is enabled/disabled by header J3. When the MVME147 is system controller, the System Controller (SCON) LED is turned on.

VMEbus Time-Out

The VMEbus timer is started when either Data Strobe (DS0* or DS1*) goes active and is disabled when they both go inactive. If the timer times out before the data strobes go inactive, the Bus Error (BERR*) signal is activated. The time-out period is controlled by the timer interval register and may be 102 µs, 205 µs, 410 µs, or infinite.

System Clock Utility

The 16 MHz system clock is driven onto the VMEbus SYSCLK* signal line by the VMEchip system clock driver.

Arbiter

The VMEchip implements two different arbitration modes. They are prioritized and round-robin. The mode is software selectable.

In the prioritized mode, the arbiter prioritizes the bus request signals and responds with grant to the highest priority requester. The arbiter also informs the current bus master by activating the Bus Clear (BCLR*) signal when a request from a higher priority master has been received.

Ethernet Interface

The Ethernet interface is not used on the MVME147-010.

The MVME147 uses the AM79C90 Local Area Network Controller for Ethernet (LANCE) and the LXT901 Universal Ethernet Interface Adapter (UEIA) to implement the Ethernet transceiver interface. The balanced differential transceiver signal lines from the LXT901 are coupled via an onboard transformer to signal lines that go to the P2 connector and eventually to the MVME712 transition board, where they are connected to an industry standard DB-15 connector.

Note The balanced differential transceiver signal lines are also coupled through an onboard transformer to the front panel 10BaseT connector, an option available for special orders only.

The AM79C90 performs DMA operations to perform its normal functions. The MVME147 restricts AM79C90 DMA to local DRAM only. The AM79C90 cannot access the VMEbus. If the DRAM size is less than 16MB then it repeats itself in the AM79C90 16MB memory map. If it is more than 16MB, then the AM79C90 accesses the section of DRAM defined by the LANA24 and LANA25 bits in the PCC Slave Base Address Register (bits 6 and 7 of $FFFE102B).

Every MVME147 is assigned an Ethernet station address. The address is $08003E2*xxxxx* where *xxxxx* is the unique number assigned to the module (i.e., every MVME147 has a different value for *xxxxx*).

Each Ethernet station address is displayed on a label attached to the MVME147's backplane connector P2. In addition, the *xxxxx* portion of the Ethernet station address is stored in BBRAM, location $FFFE0778 as $2*xxxxx*.

If Motorola networking software is running on an MVME147, it uses the 2*xxxxx* value from BBRAM to complete the Ethernet station address ($08003E2*xxxxx*). The user must assure that the value of 2*xxxxx* is maintained in BBRAM. If the value of 2*xxxxx* is lost in BBRAM, the user should use the number on the label on the

P2 connector to restore it. Note that MVME147bug includes the "LSAD" command for examining and updating the BBRAM *xxxxx* value.

If non-Motorola networking software is running on an MVME147, it must set up the AM79C90 so that the Ethernet station address is that shown on the label to ensure that the module has a globally unique Ethernet station address.

SCSI Interface

The MVME147 has a SCSI mass storage bus interface. The SCSI bus is provided to allow mass storage subsystems to be connected to the MVME147. These subsystems may include hard and floppy disk drives, streaming tape drives, and other mass storage devices.

The SCSI interface is implemented using the WD33C93 controller. DMA to/from the WD33C93 is implemented through the PCC.

Data Bus Structure

The data bus structure on the MVME147 is arranged to accommodate the 8-bit, 16-bit, 32-bit, and 16/32-bit ports that reside on the board. The 8-bit ports are connected to D24-D32 of the local bus, 16-bit ports are connected to D16- D32 of the local bus and 32-bit ports are connected to D00-D32 of the local bus.

Battery Backed Up RAM and Clock

The SGS-Thompson M48T18 RAM and clock chip is used on the MVME147. This chip provides a time-of-day clock, oscillator, power fail detection, memory write protection, and 8184 bytes of RAM. However, only 4088 bytes of RAM are accessible on the MVME147. The battery and crystal plug into the M48T18.

The clock provides seconds, minutes, hours, day, date, month, and year in BCD 24-hour format. Corrections for 28, 29 (leap year), and 30 day months are automatically made. No interrupts are generated by the clock.

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