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V162FXA / LT2
November 1995

Dear Valued Customer:

Thank you for your purchase of a Motorola MVME162-4*xx* or MVME162-5*xx* series Embedded Controller. These new versions provide existing MVME162-0*xx* series customers a means to migrate to higher performance IndustryPack bus functionality, a faster local bus (MC68040 bus), and additional memory options.

Although every attempt has been made to retain compatibility with earlier versions of the MVME162-0*xx*, there are some differences that should be noted.

The following section details the major differences between the original MVME162 family (MVME162-0*xx*) and the MVME162-5*xx* and MVME162-*4xx* families of Embedded Controller Modules.

MVME162-0xx and MVME162-4xx/5xx Differences

Differences that Affect the Programming Model

MC2 chip

1. The Revision Register has been changed. The MCchip revision level was previously 00; the MC2 chip revision level is now 01.
2. Three control bits were added to the General Control Register. The PPC bit should not be set. The SCCIT<1:0> bits are set depending on the board level implementation of the serial device interrupt daisy chain. For the MVME162-5*xx* , the SCCIT field should remain at its power-up / reset value.
3. An initialization bit (i.e., read-only) was added to the DRAM / SRAM Options Register. The initialization bit was defined to be bit 7 of that register; it indicates whether the base board is populated with 1MB or 4MB of DRAM. The setting of this bit is a function of a resistor population option on the module parts list.

4. The FLASH write enable was moved from BBRAM space to a bit in the FLASH Access Time Control Register.

IP2 chip

1. Reset control functionality to the IP bus was changed. The IPchip ASIC previously generated an IP_reset when the local bus was reset, or when the reset control bit in the IPchip ASIC was set. The reset control bit was self-clearing.

   The IP2 chip ASIC no longer generates an IP_reset when the local bus is reset, and the power-up reset is not connected to the IP2 chip ASIC. Therefore, all IP_reset activity is a function of code execution.

   The IP2 chip ASIC no longer clears the reset bit in the control register. Therefore, it is necessary for software to time out the 200 ms reset delay and clear the IP_reset.

   Note that the IP_reset control bit should be accessed as a *byte*, since greater functionality has been added to the word or longword register.

   Note also that the 162Bug debugger **ENV** command has a software switch that will enable / disable the firmware to assert IP reset when the debugger is restarted with system or local bus reset. The default for this **ENV** software switch is to reset the IP bus.
2. The IP2 chip ASIC CSR has additional functionality for DMA. The programming model for this functionality appears at the end of the CSR set that was defined for the IPchip ASIC. The programming model of the IP2 chip, while similar to that of the IPchip ASIC, has several changes:
   - A vector base register was added at $FFFBC003.
   - Bus turnaround delay bits were added to the General Control registers. These bits should be left cleared. DMA arbitration control is located at $FFFBC01E and clock synchronization control is at $FFFBC01D.

DRAM Mezzanines

The MVME162-4*xx* / 5*xx* implements 4MB on the host board. These versions can be field upgraded to 8MB or 16MB. The following table shows the allowable combinations.

Marketing Number	Description	Comments
MEM162-502	4MB DRAM Mezzanine	Used to create 8MB versions
MEM162-503	12MB DRAM Mezzanine	Used to create 16MB versions

Jumpers

1. The System Controller jumper has two active positions on the MVME162-4*xx* / 5*xx* series: the system controller function is either enabled or disabled. **Please note that the auto-syscon feature is not implemented at this time.**
2. The new IP Clock Selection jumper (J24) has two positions. Selections are 8MHz or 32MHz. Note that the IP32 CSR bit (IP2 chip, register at offset $1D, bit 0) must be set to correspond to the jumper setting. This bit must be cleared if the 8MHz jumper setting is selected.
3. On boards identified with assembly numbers 01-W3960B*xxx*, the IP Clock Selection jumper is factory hardwired in the 8MHz position (pins 1 and 2 connected). If the 32MHz option is desired, remove the staple between pins 1 and 2 and install a jumper between pins 2 and 3. The person performing this work must ensure that the MVME162 is ESD (electrostatic discharge) protected.
4. Note that the MVME162-5*xx* series supports either the 8MHz or the 32MHz IndustryPack bus speed option. The MVME162-4*xx* series supports only the 8MHz IndustryPack bus speed option.

Errata

MC2 chip

1. The data registers of the Zilog Z85230 device which is interfaced by the MC2 chip ASIC cannot be accessed directly. The Zilog Z85230 has an indirect access mode which must be used with the data registers.

   A bug in MVME162-4*xx* / 5*xx* units equipped with MC2 chip revision $01 does not allow the data registers to be accessed directly. You must access them indirectly via the SCC chip. The software must send a command to the control register telling it that the next thing read or written to the control register will go to the data register. The following two macros are examples.

   dev_addr is a pointer to the base address of the SCC. SCCR0 is the offset to SCC control register #0.

```
#define READ_SCC(VAR_NAME)\
         dev_addr[SCCR0] = 0x08;\
         (VAR_NAME) = dev_addr[SCCR0]

#define WRITE_SCC(VAR_NAME)\
         dev_addr[SCCR0] = 0x08;\
         dev_addr[SCCR0] = (VAR_NAME)
```

IP2 chip

1. The revision register reads zero. It should be a 1. The workaround for this is to test the MC2 chip revision register.
2. The Vector Base Register is write only.

Once again, thank you for purchasing Motorola products. If you have any questions or comments, please contact your local Motorola Computer Group sales representative.

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