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PPMCBASE Board

Installation and Use

PPMCBSA/IH1

July 2000

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The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. If the equipment is supplied with a three-conductor AC power cable, the power cable must be plugged into an approved three-contact electrical outlet, with the grounding wire (green/yellow) reliably connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards and local electrical regulatory codes.

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Do not operate the equipment in any explosive atmosphere such as in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment could result in an explosion and cause injury or damage.

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Warning

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Caution

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> EN55022 “Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment”; this product tested to Equipment Class A
>
> EN50082-1:1997 “Electromagnetic Compatibility—Generic Immunity Standard, Part 1. Residential, Commercial and Light Industry”

System products also fulfill EN60950 (product safety) which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

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About This Manual

The PPMCBASE Board Installation and Use describes the installation, components, and configurations of the Base board. The document should be used by anyone who wants general as well as technical information about the PPMCBASE product. This product was designed as a development platform to work in conjunction with one or more mezzanine boards, such as the PPMC750. Therefore, all programming and configuration operations cannot be completed without the installation of one or more PMCs.

The following table lists the current model numbers for the PPMCBASE product:

Model Number	Description
PPMCBASE-001	CompactPCI Carrier, Standard Model
PPMCBASE-002	CompactPCI Carrier, Rear I/O Model
PPMCBASE-003	CompactPCI Carrier, Stand-Alone Model

Summary of Changes

The following changes have been made since the last release of this manual.

Date	Changes	Replaces
July 2000	New front matter regulatory descriptions	Previous front matter
July 2000	Added information about the Intel 21554 bus clock on page 3-9	Previous information

Overview of Contents

The following is a summary of the contents of each chapter in this manual for easy reference.

Chapter 1, *Hardware Preparation and Installation*, provides general information, hardware preparation and installation instructions, operating instructions, and a functional description of the PPMC (Processor PCI Mezzanine Card) Base board.

Chapter 2, *Operating Instructions*, supplies information for use of the PPMCBASE in a system configuration.

Chapter 3, *Functional Description*, describes the PPMCBASE board on a block diagram level.

Chapter 4, *Connector Pin Assignments*, summarizes the pin assignments for the connectors on the PPMCBASE.

Chapter 5, *PPCBug*, briefly describes PPCBug and gives references to where you can find more information.

Appendix A, *Specifications*, lists the general specifications for the PPMCBASE board.

Appendix B, *PPMCBASE VPD Reference Information*, gives VPD definitions, configuration options, flash configuration data, L2 cache configuration data, VPD revision data, and other information related to the PPMCBASE VPD.

Appendix C, *Related Documentation*, lists all documentation related to the PPMCBASE board.

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In all your correspondence, please list your name, position, and company. Be sure to include the title and part number of the manual and tell how you used it. Then tell us your feelings about its strengths and weaknesses and any recommendations for improvements.

Conventions Used in This Manual

The following typographical conventions are used in this document:

bold

is used for user input that you type just as it appears; it is also used for commands, options and arguments to commands, and names of programs, directories and files.

italic

is used for names of variables to which you assign values. Italic is also used for comments in screen displays and examples, and to introduce new terms.

`courier`

is used for system output (for example, screen displays, reports), examples, and system prompts.

<**Enter**>, <**Return**> or <**CR**>

<**CR**> represents the carriage return or Enter key.

CTRL

represents the Control key. Execute control characters by pressing the Ctrl key and the letter simultaneously, for example, **Ctrl-d**.

Hardware Preparation and Installation

1

Introduction

This manual provides general information, hardware preparation and installation instructions, operating instructions, and a functional description of the PPMC (Processor PCI Mezzanine Card) Base board.

The PPMCBASE is a CompactPCI, non-system slot Processor PCI Mezzanine Card carrier board that is ideal for PPMC development. It consists of a DEC 21554 non-transparent PCI-to-PCI bridge interface between the local PCI bus and the CompactPCI bus, one onboard 10/100 Base-T Ethernet, two PPMC/PMC slots, and 1MB of onboard socketed Flash accessible only from PMC Slot 2. This board does not require or provide hot swap functionality.

Three versions of the PPMCBASE are available.

- One standard version provides the functions described above plus access to two serial interfaces and two RISCwatch headers, one of each per PMC slot. This version includes debug access for PMC Slot 1. In this configuraton, connectors J3 and J4 are not installed and the power connector is not installed.
- The second standard version provides the functions described in the previous paragraph plus access to one serial interface and one RISCwatch header for PMC Slot 2 and rear 32/64-bit rear PMC I/O for PMC Slot 1. In this configuration, connectors J3 (rear PMC I/O) and J4 (alignment only) are installed, and the power connector is not installed.
- A third “stand-alone” version resembles the first version except for additional components required for stand-alone operation, which includes an on-board power connector, CompactPCI termination resistors, and an alternate CompactPCI clock supply. This stand-alone version includes debug access for PMC Slot 1 and connectors J3 and J4 are not installed.

A complete PPMCBASE configuration consists of the base board plus:

- A PPMC mezzanine module in PMC Slot 2
- One optional PCI mezzanine card (PMC) for additional versatility, or a second PPMC module in PMC Slot 1

Note The block diagram in Figure 1-1 does not reflect a particular model, but illustrates a combined architecture of the PPMCBASE board with all components shown. Block diagrams for specific models are not shown in this manual; however, two top-level component views of the board are shown in Figure 1-2 and Figure 1-3 to distinguish between the standard and stand-alone models.

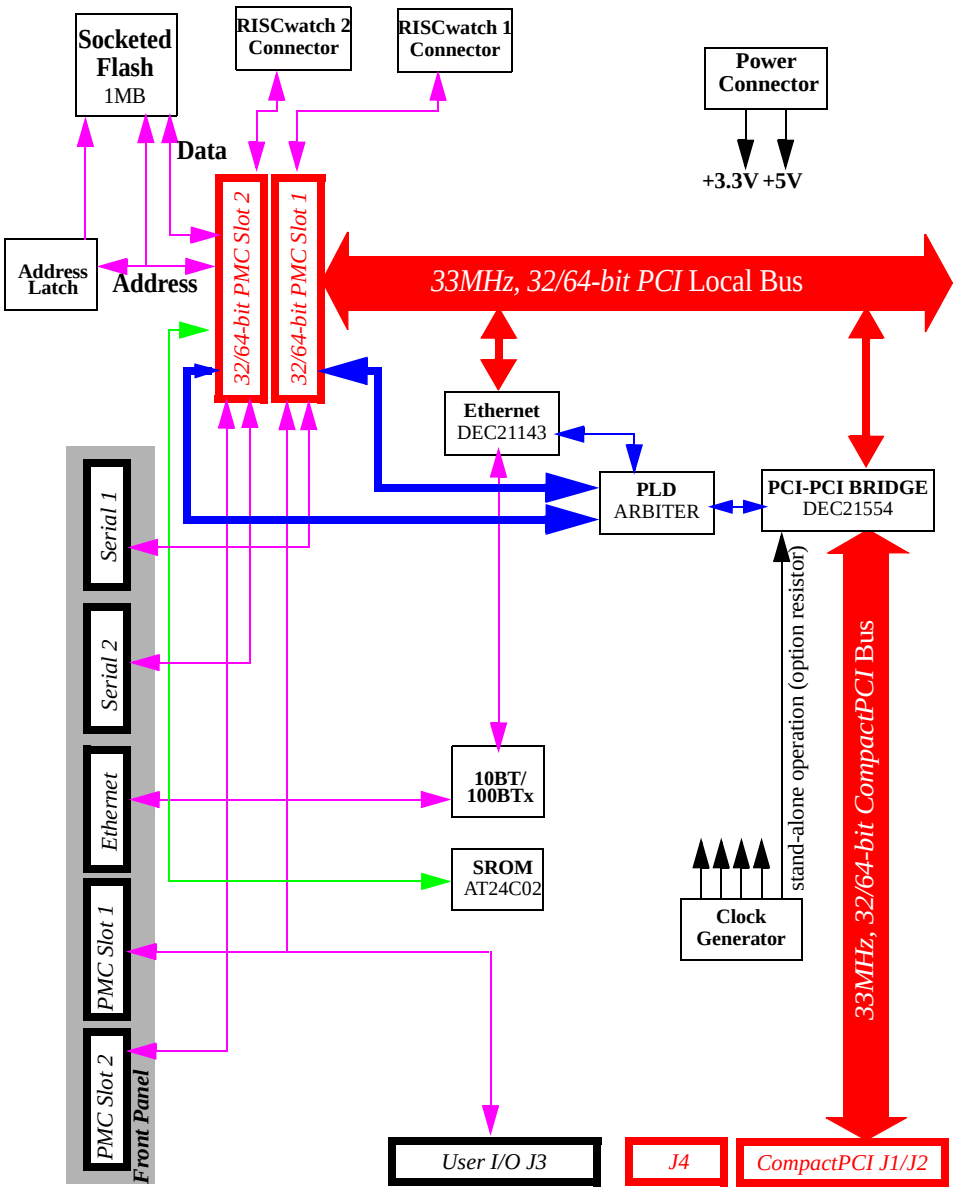


Figure 1-1. PPMCBASE Board Block Diagram

Equipment Required

The following equipment is required to complete a PPMCBASE system:

- CompactPCI system enclosure or ATX power supply (PPMCBASE-003)
- System console terminal
- Operating system (and/or application software)
- Disk drives (and/or other I/O) and controllers
- At least one PPMC and connecting cables

PPMCBASE boards are factory-configured for I/O handling via front and rear I/O ports (depending on the model). *Three versions of the PPMCBASE are available.* See that section for a description of the three basic PPMCBASE versions.

Overview of Start-up Procedure

The following table lists the things you will need to do before you can use this board and tells where to find the information you need to perform each step. Be sure to read this entire chapter, including all Caution and Warning notes, before you begin.

Table 1-1. Startup Overview

Task	Section or Manual Reference
Unpack the hardware.	*Unpacking Instructions*
Configure the hardware by setting jumpers on the board.	*PPMCBASE Board Preparation*
Install the PMC Module	*PMC/PPMC Module Installation*
Install the PPMCBASE in the chassis.	*PPMCBASE Installation*
Connect any other equipment you will be using.	Chapter 4, *Connector Pin Assignments*
	For more information on optional devices and equipment, refer to the documentation provided with the equipment.

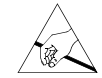
Table 1-1. Startup Overview (Continued)

Task	Section or Manual Reference
Power up the system.	*Applying Power*
Note that the debugger initializes the PPMCBASE	*Using the Debugger* from the PPMC750A/IH
	You may also wish to obtain the PPCBug Firmware Package User's Manual, listed in Appendix C, *Related Documentation*.
Program the board as needed for your applications.	*PPMC Series Programmer's Reference Guide*, listed in Appendix C, *Related Documentation*.

Unpacking Instructions

Note If the shipping carton is damaged upon receipt, request that the carrier's agent be present during the unpacking and inspection of the equipment.

Unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping of equipment.



Caution Avoid touching areas of integrated circuitry; static discharge can damage circuits.

Hardware Configuration

To produce the desired configuration and ensure proper operation of the PPMCBASE, you may need to carry out certain hardware modifications before installing the module in a chassis.

The PPMCBASE receives most software control from the mezzanine boards installed on the Base's PMC slots. By setting bits in control registers of those mezzanine cards after installing the combined

Base/Mezzanine module in a system, you can modify its configuration. These control registers are described in the programmer's guide of the particular PPMC you are installing on the Base board. For example, refer to the *PPMC750 Processor PMC Module Programmer's Reference Guide* (PPMC750A/PG), for control register information if you are installing that particular mezzanine board on the PPMCBASE board. Also, refer to the programming information in this document for the *PPMCBASE board.*

Some options, however, are not software-programmable. Such options are controlled through manual installation or removal of header jumpers or interface modules on the base board or the associated mezzanine. For jumper settings on the mezzanine, refer to that particular installation guide. For jumper settings on the PPMCBASE, refer to the following sections of this manual.

PPMCBASE Board Preparation

Figure 1-2 illustrates the placement of the switches, jumper headers, connectors, and LED indicators on the standard model PPMCBASE. Figure 1-3 illustrates the placement of the switches, jumper headers, connectors and LED indicators on the stand-alone version of the PPMCBASE. Manually configured items on the PPMCBASE board include:

- Flash bank selection (J29)

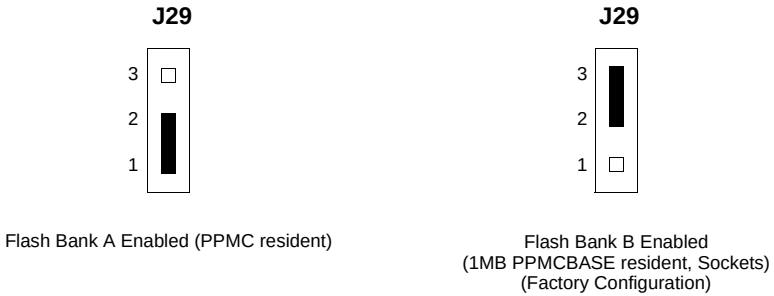
The PPMCBASE is factory tested and shipped with the configurations described in the following sections. The PPMCBASE's required and factory-installed debug monitor, PPC6Bug, operates with those factory settings.

Flash Bank Selection (J29)

The PPMCBASE board has provision for one bank of 1MB of 8-bit Flash memory.

Bank B contains the onboard debugger, PPC6Bug.

To enable Flash Bank A, which is provided for on the PPMC module in PMC Slot 2, place a jumper across header J29 pins 1 and 2. To enable Flash bank B (1MB of firmware located in sockets on the base board), place a jumper across header J29 pins 2 and 3.



Flash Bank A Enabled (PPMC resident)

Flash Bank B Enabled
(1MB PPMCBASE resident, Sockets)
(Factory Configuration)

Note If a PPMC module, such as a PPMC750-2xxx, is installed in PMC Slot 2 (Monarch slot) which also has Bank B sockets on board, ensure that only one set of sockets is populated for proper operation. The following table depicts Flash bank setting options when using a PPMCBASE in conjunction with another Flash jumpered board (PPMC750-2xxx), and then with another board without a Flash jumper (PPMC750):

Table 1-2. J29 Flash Bank A/B Selection with other PPMCs

PPMCBASE	PPMC750	PPMC750-2xxx Bank A Set	PPMC750-2xxx Bank B Set	PPMC750-2xxx Jumper Not Populated
Bank B selected	Use BASE Bank B	Use BASE Bank B	Use BASE Bank B	Use BASE Bank B
Bank B not selected	Use Bank A	Use -2xxx Bank A	Use -2xxx Bank B	Use -2xxx Bank A
Not populated	Use Bank A	Use Bank A	Use -2xxx Bank B	Use -2xxx Bank A

Header J30

Header J30 is an ISP header that is used for programming PLDs and is left on the PPMCBASE board for factory use only.

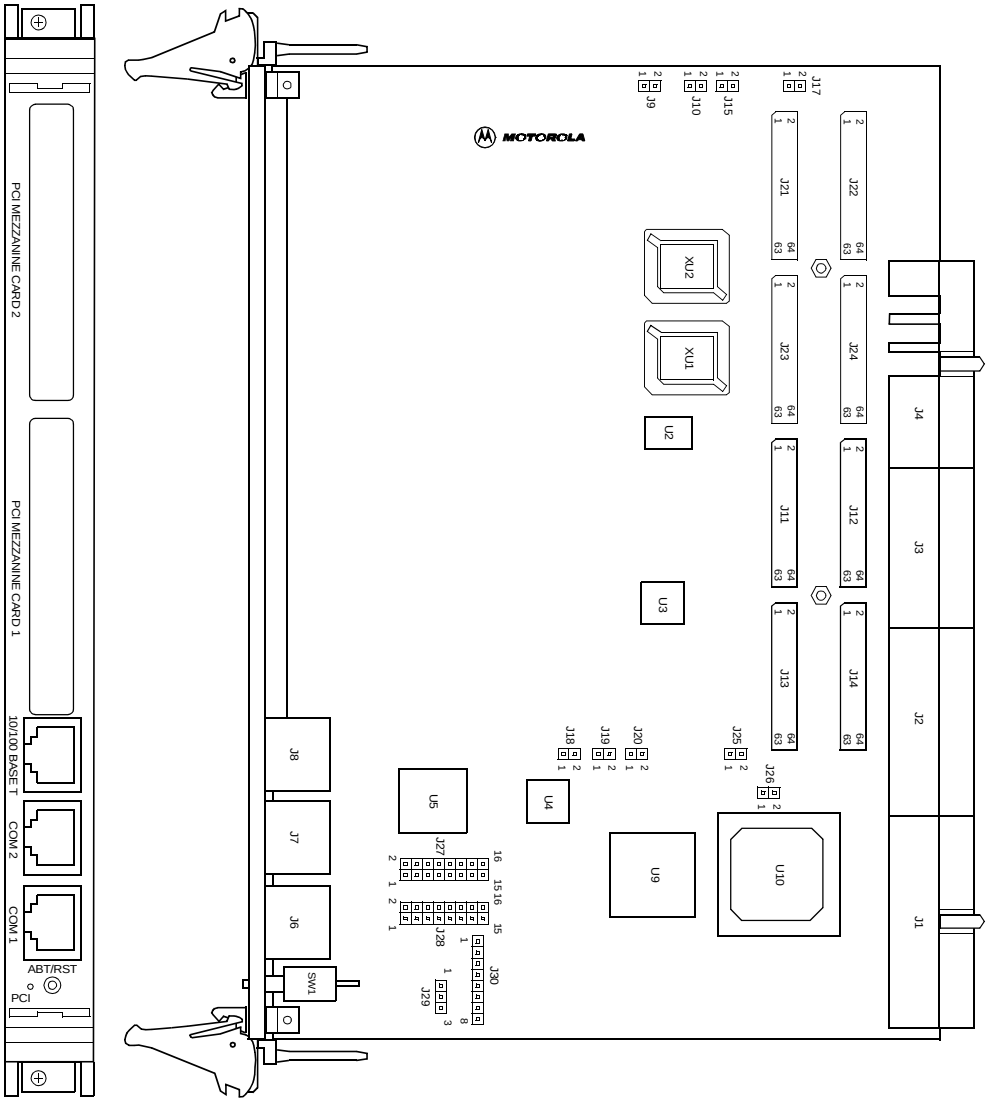


Figure 1-2. PPMCBASE-002 Switches, Headers, Connectors, Fuses, LEDs

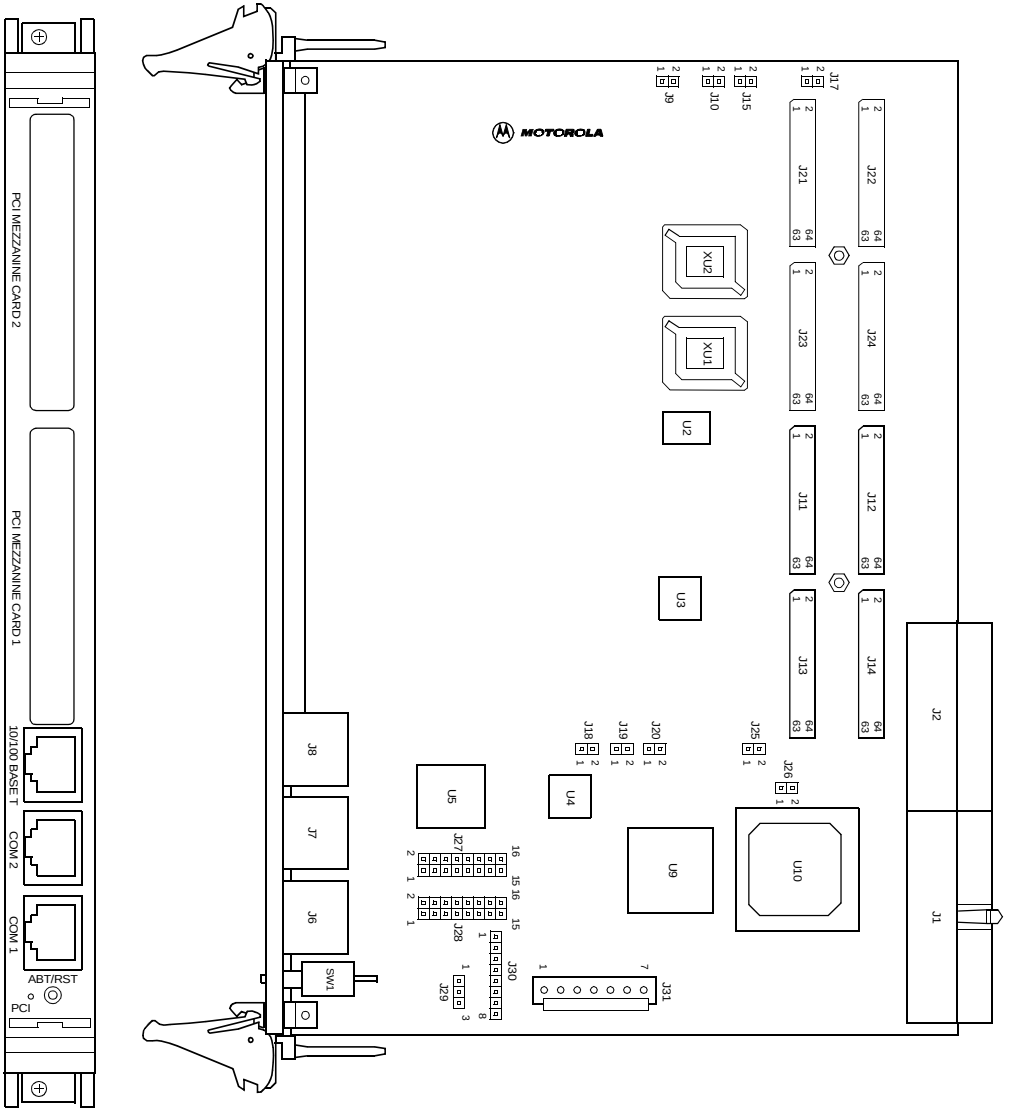


Figure 1-3. PPMCBASE-001/002 Switches, Headers, Connectors, Fuses, LEDs

Hardware Installation

The following sections provide directions for the placement of a PMC (PCI Mezzanine Card), or PPMC (Processor PCI Mezzanine Card) on the PPMCBASE board, the installation of the complete PPMCBASE assembly into a CompactPCI chassis, and the system considerations relevant to the installation. Before installing the PPMCBASE, ensure that all header jumpers are configured as desired.

The user-configured jumpers are accessible with the mezzanines installed.

ESD Precautions

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to (Electro Static Discharge) ESD. After removing the component from the system or its protective wrapper, place the component flat on a grounded, static-free surface (and in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an unpainted metal part of the system chassis.



Caution Inserting or removing modules with power applied may result in damage to module components.



Warning Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.



Caution Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

PMC/PPMC Module Installation

One dual wide, one single wide, or two single wide PCI mezzanine card (PMC) modules can be mounted on top of the PPMCBASE board. The Monarch (master/host) PPMC is installed as PMC2 (J21 through J24). The non-monarch (slave/target) PPMC or standard PMC is installed as PMC1 (J17 through J14). A standard PMC could also be installed as PMC2. Refer to the VITA32 standard on PPMCs (www.vita.com) for details on the use of a Monarch PPMC. The PPMCBASE is designed with a 5V I/O; therefore, it will only accept 5V, or Universal PMC/PPMCs modules. It can supply up to 25W of power per PMC connector. Refer to Table 1-3, *PPMCBASE Current Limits*, for corresponding current limits. This allocation can be with any single PMC voltage (+3.3V, +5V or +12V) or any combination thereof, as long as the total does not exceed 25W per PMC or PPMC. To install a PMC/PPMC module, refer to Figure 1-4 PMC or PPMC module placement on PPMCBASE, and proceed as follows:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.

2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the CompactPCI.

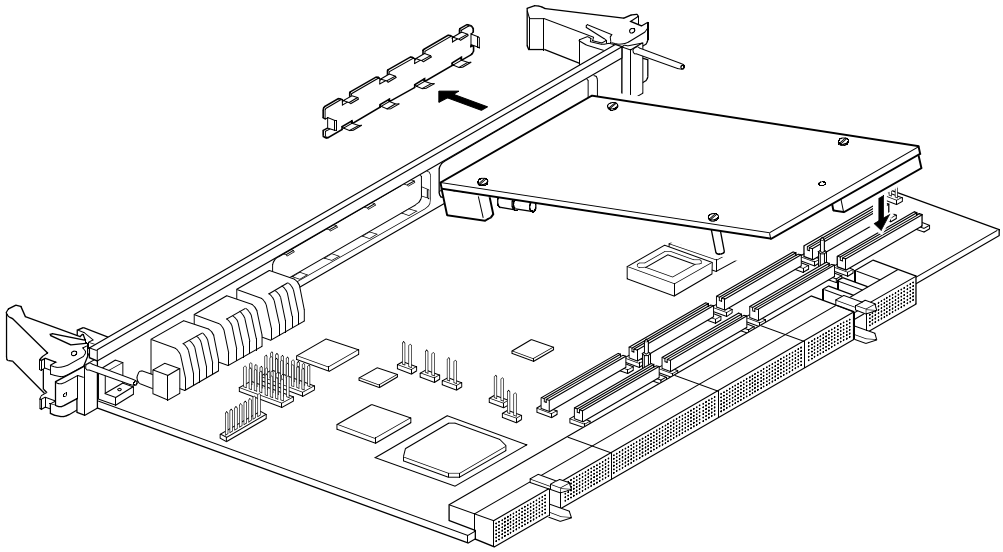


Figure 1-4. PMC or PPMC Module Placement on PPMCBASE

Caution

The PPMCBASE is not hot swappable. Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. Carefully remove the PPMCBASE from its CompactPCI card slot and lay it flat, with connectors J1 through J5 facing you.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

4. Remove the PMC filler from the front panel.

5. Slide the edge connector of the PMC/PPMC module into the front panel opening from behind and place it on top of the base board. The four connectors on the underside of the PMC/PPMC module should then connect smoothly with the corresponding connectors (J11/12/13/14 on PMC1 or J21/22/23/24 on PMC2) on the PPMCBASE.
6. Insert the four short Phillips screws, provided with the PMC, through the holes on the bottom side of the PPMCBASE into the PMC/PPMC front bezel and rear standoffs. Tighten the screws.

Note If the PMC/PPMC provides rear I/O, refer to Chapter 4, *Connector Pin Assignments* for the pin assignments.

PPMCBASE Installation

With mezzanine board(s) installed and headers properly configured, proceed as follows to install the PPMCBASE in the CompactPCI chassis:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the CompactPCI modules.



Caution The PPMCBASE is not a hot swappable board and may not be inserted in a hot swap chassis such as a CPX2000, or a CPX8000 series chassis with power applied. Inserting or removing the PPMCBASE with power applied may result in damage to board components.



Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. Remove the filler panel from the appropriate non-system card slot.
4. Set the VIO on the backplane to either 3.3V or 5V, depending upon your CompactPCI system signaling requirements and ensure the backplane does not bus J3, or J5 signals. Note: the PPMCBASE board is a Universal CompactPCI board; therefore, it will accept either a 3.3V or 5V setting.
5. Slide the PPMCBASE into the appropriate non-system slot. Grasping the top and bottom injector handles, be sure the module is well seated in the P1 through P5 connectors on the backplane. Do not damage or bend connector pins.



Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits

6. Secure the PPMCBASE in the chassis with the screws provided, making good contact with the transverse mounting rails to minimize RF emissions.
7. Replace the chassis or system cover(s), making sure no cables are pinched. Cable the peripherals to the panel connectors, reconnect the system to the AC or DC power source, and turn the equipment power on.

System Considerations

The PPMCBASE is designed to operate as a CompactPCI non-system slot board. Consequently, the PPMCBASE must be installed in a subrack slot marked with the circle symbol.

In order for the PPMCBASE to operate properly, the PPMCBASE must be installed in a system with a system slot controller board. The system slot board is required to provide clock and arbitration signals to the PPMCBASE.

On the PPMCBASE board, the standard serial console port (COM1) serves as the PPCBug debugger console port. The firmware console should be set up as follows:

- Eight bits per character
- One stop bit per character
- Parity disabled (no parity)
- Baud rate of 9600 baud

9600 baud is the power-up default for serial ports on PPMCBASE boards. After power-up you can reconfigure the baud rate if you wish, using the PPCBug **PF** (Port Format) command via the command line interface. Whatever the baud rate, some type of hardware handshaking — either **XON/OFF** or via the RTS/CTS line — is desirable if the system supports it.

PPMCBASE Power Requirements

The PPMCBASE board draws +5V, +3.3V, and VIO power from the J1 connector. The +12V and -12V voltage are not used by the PPMCBASE but is provided for the PMCs. The PPMCBASE also contains a poly fuse that limits the total +12V and -12V current drawn by the PPMCBASE. Refer to Table 1-3 for the current limits and Appendix A, *Specifications*, for other specifications.

Table 1-3. PPMCBASE Current Limits

Voltage	Total Current Available to PMCs (Sum of PMC1 & PMC2)
+5.0V	3.0 Amps
+3.3V	4.5 Amps
+12.0V	0.5 Amp
-12.0V	0.5 Amp
VIO	0.75 Amps

Operating Instructions 2

Introduction

This chapter supplies information for use of the PPMCBASE in a system configuration. Here you will find the power-up procedure and descriptions of the switches and LEDs, memory maps, and software initialization.

Applying Power

After you have verified that all necessary hardware preparation has been done, that all connections have been made correctly, and that the installation is complete, you can power up the system. The MPU, hardware, and firmware initialization process is performed by the PowerPC™ PPCBug power-up or system reset. The firmware initializes the devices on the Base board in preparation for booting the operating system on one of the PPMCs, which is required for full operation.

The firmware is shipped from the factory with an appropriate set of defaults. In most cases there is no need to modify the firmware configuration before you boot the operating system.

The following flowchart shows the basic initialization process that takes place during PowerPC system startup (the PowerPC in this case is on the PMC).

For further information on PPCBug, refer to the PPCBug chapters in the install guide that corresponds to the PMC or PPMC that is being installed on the PPMCBASE board, or to the *PPCBug Firmware Package User's Manual* (PPCBUGA1/UM and PPCBUGA2/UM).

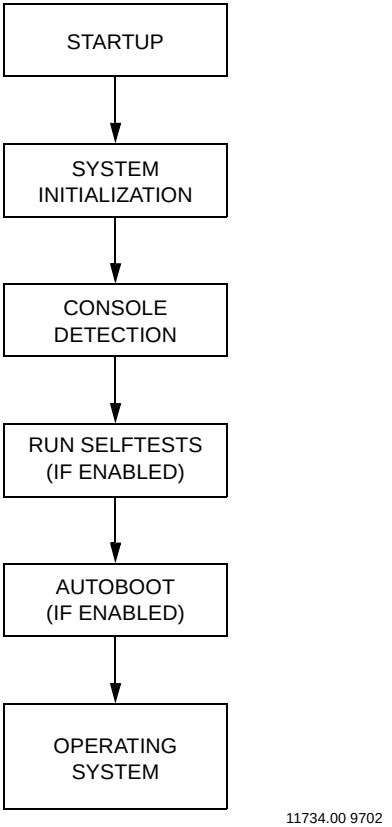


Figure 2-1. PPCBug System Startup

The PPMCBASE front panel has one ABORT/RESET switch and one LED (light-emitting diode) status indicator for PCI activity. For more information on front panel operation refer to Chapter 3, *Functional Description*.

Memory Maps

For detailed processor memory map information, including suggested PREP-compatible memory maps, refer to the appropriate *PPMC Programmer's Reference Guide*, such as the *PPMC750 Processor PMC Module Programmer's Reference Guide (PPMC750A/PG).*

PCI Local Bus Memory Map

The local PCI memory map is the PCI memory map as viewed by the host PMC, which is installed on the PPMCBASE board. This is also the secondary bus side of the 21554 on the PPMCBASE. This map is controlled by the Monarch PPMC's bridge and the 21554 PCI-to-PCI bridge. The Monarch PPMC's bridge and the 21554 PCI-to-PCI bridge have flexible programmable map decoder registers to customize the system for a wide range of applications.

After a reset, software must program the appropriate map decoders for a specific environment. The 21554 bridge map decoders default state is determined by the SROM values loaded.

For detailed PCI memory maps, including suggested PREP-compatible memory maps, refer to the *PPMC module Programmer's Reference Guide*, listed in Appendix C, *Related Documentation*.

CompactPCI Memory Map

The PPMCBASE uses the DEC21554 non-transparent PCI-to-PCI bridge to interface between the local PCI bus and the CompactPCI bus. The 21554 is different from traditional PCI-to-PCI bridges in that it uses address translation instead of a flat address map between primary and secondary PCI buses. In the PPMCBASE configuration, the primary bus is the CompactPCI bus and the secondary bus is the PPMCBASE local bus. Downstream transactions are those that are initiated on the primary bus and are forwarded to the secondary bus. Upstream transactions are those initiated on the secondary bus and forwarded to the primary bus.

Address Decoding with the 21554

The 21554 implements multiple base address registers on both the primary and secondary interfaces that denote separate address ranges for both downstream and upstream transactions. It also has base registers for access to its Control and Status Register (CSR) space. Consequently, on the primary interface (CompactPCI bus) the 21554 responds only to those

transactions which are in the address range defined by one of the base address ranges. All other addresses are ignored. The same is true for transactions on the secondary interface (local PCI bus).

The address ranges defined by the primary base address registers reside in the primary or system address map. The address ranges defined by the secondary base address registers reside in the secondary or local address map. Each of these address maps is independent of each other. The 21554 provide address translation between these two address maps when forwarding transactions upstream or downstream.

Recommendations for CompactPCI mapping, including suggested PREP-compatible memory maps, can be found in the PPMC Programmer's Guide, listed in Appendix C, *Related Documentation*.

System Clock Generator

The PPMCBASE system clocks for the onboard PCI devices and the PMC slots (33.33 MHz) are generated by a 66 MHz oscillator and distributed by the MPC 949 clock buffer. Separate oscillators are provided as follows: 20 MHz for the ethernet MAC interface and 25 MHz for the ethernet PHY device. For stand-alone operation, an alternate clocking scheme is available for the DEC21554 primary side in place of the CompactPCI clock via a population resistor on a clock signal from the clock generator.

PCI Arbitration

The PPMCBASE arbitration control for the onboard PCI devices is provided by a non-programmable onboard PLD. The arbiter implements a round robin (rotating) algorithm whereby the priorities are reevaluated at the start of each new transaction on the PCI bus. From this point until the time that the next transaction starts, the arbiter will assert grant corresponding to the highest priority request asserted. If a grant is asserted and a higher priority request subsequently asserts, the arbiter will deassert the asserted grant and assert the higher priority grant on the next PCI clock cycle. When priorities are reevaluated, the highest priority is assigned to the next highest priority master relative to the master that initiated the previous transaction. The master that initiated the last transaction now has

the lowest priority. This arbiter supports up to 6 request/grant pairs. If the bus is idle and there are no requests, the bus is parked on PMC 2 by asserting its grant. The request/grant assignments for the Base using the PLD arbiter are shown in the following table.

Table 2-1. PLD Request/Grant Assignments

PPMC REQ/GNT	Local PCI Bus Device
0	PMC 2
1	PMC 1
2	DEC21143 (LAN)
3	PMC 2 Alternate Device
4	PMC 1 Alternate Device
5	DEC21554

Sources of Reset

The PPMCBASE board provides reset control from various sources:

Power-On Reset

The PPMCBASE generates a hard reset at power-on. During power up, reset is maintained for 140 to 560 milliseconds after the voltages have reached the minimum threshold.

Undervoltage Reset

The PPMCBASE generates a hard reset when the voltage monitor detects a supply voltage of +5V or +3.3V that falls below minimum thresholds of 4.75V and 3.135V respectively. The reset is maintained for 140 to 560 milliseconds after the voltages have returned to the minimum threshold. For undervoltage, the Vcc threshold to reset delay is typically 10 microseconds.

Front Panel Push Button Reset

The front panel switch generates a hard reset when depressed for more than 3 seconds (**Note**: it is a dual function switch, and if depressed for less than 3 seconds it produces an interrupt to each PPMC process). The reset is maintained as long as the switch is depressed.

CompactPCI Reset (RST#)

The CompactPCI reset signal RST# is monitored by the 21554 PCI-to-PCI bridge chip as the primary bus reset input. The bridge will generate a secondary bus reset that is used to generate a board hard reset.

Software Resets

A board hard reset may be generated by writing to the DEC21554 Bridge Control Register from the PCI address space. This allows the System Slot Processor to perform a software controlled reset of the PPMCBASE board. Refer to the DEC21554 data sheet for details.

RSTOUT# from PPMC Module

The PRST# signal to the DEC21554 is asserted if a RSTOUT# is detected by the PPMCBASE to be asserted from a PPMC module installed in either PMC Slot 1 or PMC Slot 2. The DEC21554 generates SRST# when it detects the PRST# which in turn generates a PCIRST# as an output to each PMC slot.

Stand-Alone Board Operation

In addition to the alternate clocking method mentioned earlier, the PPMCBASE provides an optional power connector for stand-alone operation. Voltages of +3.3V and +5V are derived from this connector rather than from the CompactPCI backplane connectors. A voltage of +12V is not used and -12V is not available from this connector and thus PMCs that use +/-12V are not supported in stand-alone operation.

Note Since the stand-alone configuration of the PPMCBASE is meant to be used for system development purposes only, the EMC compliance standards mentioned in Appendix A may not be met. It is however important to be aware of applicable regulatory requirements that may apply.

Functional Description 3

Introduction

This chapter describes the PPMCBASE board on a block diagram level. The *General Description* provides an overview of the PPMCBASE, followed by a description of several components and functional features. Figure 3-1 shows a block diagram of the overall board architecture.

Some descriptions of PPMCBASE features include a brief explanation of programmable features if it applies, but the majority of programming information is included in the Programmer's Guide that comes with the particular PMC or PPMC that resides on the PPMCBASE board.

Features

The following table summarizes the features of the PPMCBASE single-board computers.

Table 3-1. PPMCBASE Features

Feature	Description
Flash Memory	Sockets for 1MB (8-bit) FLASH, accessible only from PMC Slot 2
Local PCI Interface	32/64-bit Data Up to 33MHz operation 5V signaling interface P11, P12, P13, and P14 PMC connectors for Slot 1 P21, P22, P23, and P24 PMC connectors for Slot 2
CompactPCI	Intel 21554 non-transparent PCI-to-PCI bridge 64-bit primary bus/64-bit secondary bus interface asynchronous clocks on primary and secondary bus interfaces up to 33MHz operation
Form Factor	6U Eurocard

Table 3-1. PPMCBASE Features (Continued)

Feature	Description
Peripheral Support	One 10Base-T/100Base-Tx Ethernet interface routed to the front panel Two 16550-compatible async serial interfaces routed to the front panel (only PMC Slot 2 has access to a serial port if PMC I/O is required for PMC Slot 1)
Dual PMC Slots	Two 32/64-bit PMC slots with front PMC I/O support 32/64-bit rear PMC I/O for PMC Slot 1 (only for the version where PMC Slot 1 does not provide serial port and RISCwatch header access)
Front Panel Connectors	One RJ45 for 10Base-T/100Base-Tx ethernet port Two RJ45 for 16550-compatible async serial port, one per PMC slot (only PMC Slot 2 has access to a serial port if PMC I/O is required for PMC Slot 1)
Switches	ABORT/RESET switch on front panel
Status LED	One PCI activity LED
Miscellaneous	Two RISCwatch headers, one per PMC slot (only PMC Slot 2 has access to a RISCwatch header if PMC I/O is required for PMC Slot 1) Optional power connector for stand-alone operation

General Description

The PPMCBASE is a CompactPCI, non-system slot board that occupies a single slot in the CompactPCI backplane. It consists of a CompactPCI bus interface, one onboard 10/100 Base-T Ethernet, access to up to two serial interfaces, two PMC slots, up to two RISCwatch headers, one power connector, and 1MB of onboard socket Flash accessible only from PMC Slot 2. The PPMCBASE does not provide or require hot swap functionality.

The local PCI bus interfaces to the CompactPCI bus using a Intel 21554 non-transparent PCI-to-PCI bridge, which provides a 64-bit primary and a 64-bit secondary interface allowing full 64-bit data access between the CompactPCI bus and the local PCI bus. The non-transparent characteristics of this bridge allow the local PPMC module to configure and control the local resources independently from the system host processor.

The PPMCBASE supports two single-wide or one double-wide PMC Card Slots. Both PMC Slots are 32/64-bit capable and support front I/O, but only PMC slot 1 supports 32/64-bit rear PMC I/O routed to the J3 connector. Front panel connectors include three RJ45 connectors in which one functions as a 10 Base-T/100 Base-Tx ethernet port and the remaining two function as serial port access for each PPMC module installed in the PMC slots. The PPMCBASE provides one RISCwatch header for each PPMC module installed in a PMC slot.

The PPMCBASE supports three versions which include the following configurations:

- **PPMCBASE-001 -** PMC Slot 1 with Serial Port 1 and RISCwatch header 1 routed from PMC Slot 1. PMC Slot 2 with Serial Port 2 and RISCwatch header 2 routed from PMC Slot 2
- **PPMCBASE-002 -** PMC Slot 1 with 32/64-bit PMC I/O routed from PMC Slot 1 to J3 connector. PMC Slot 2 with Serial Port 2 and RISCwatch header 2 routed from PMC Slot 2
- **PPMCBASE-003 -** PMC Slot 1 with Serial Port 1 and RISCwatch header 1 routed from PMC Slot 1. PMC Slot 2 with Serial Port 2 and RISCwatch header 2 routed from PMC Slot 2, and stand-alone options populated.

For stand-alone operation, power is supplied through an onboard power connector.

Block Diagram

Figure 3-1 is a block diagram of the PPMCBASE's overall architecture.

Note This block diagram encompasses all three versions of the PPMCBASE. Consequently, specific components may not be included on your particular model (for example, the power connector is not included on versions -001 or -002).

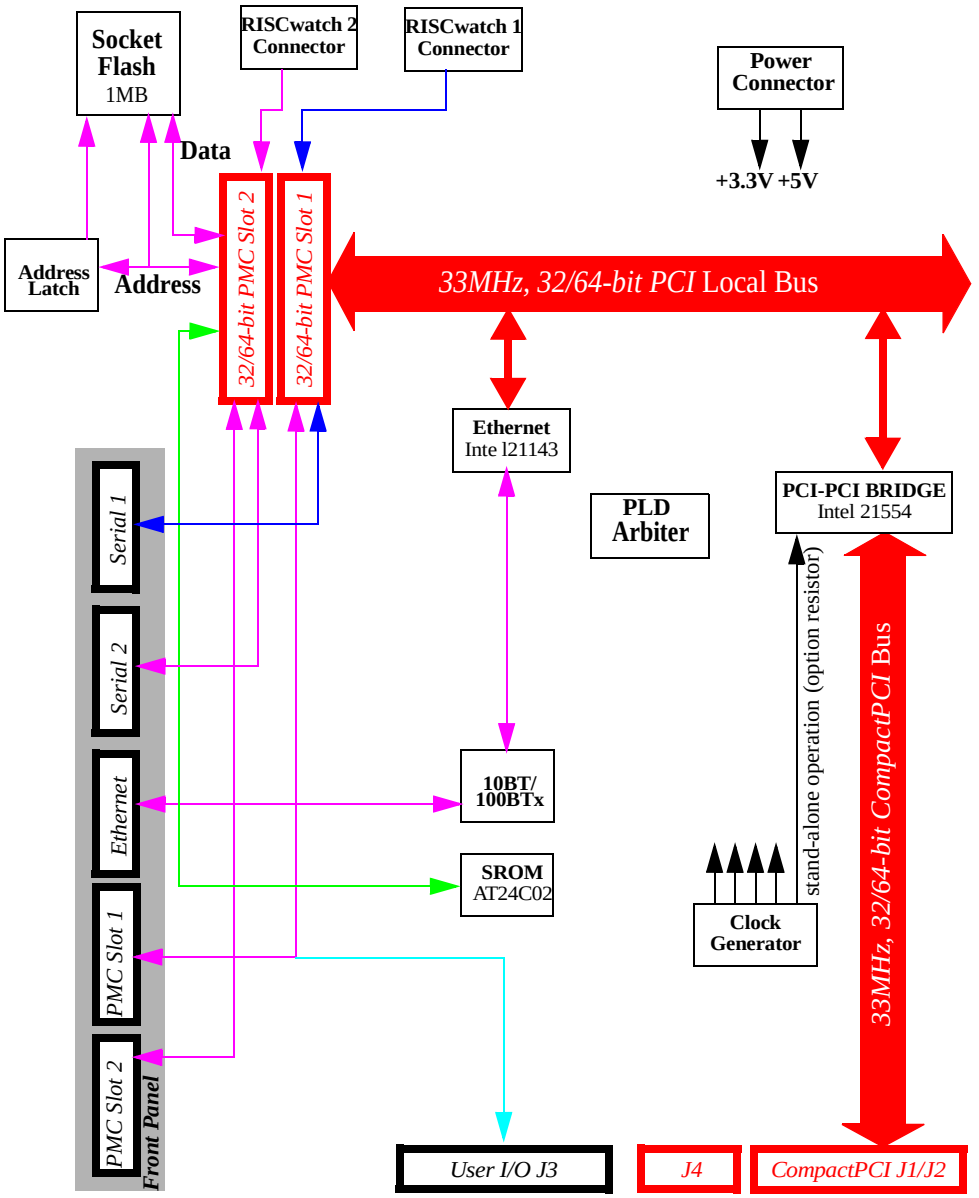


Figure 3-1. PPMCBASE Block Diagram

PCI Interface

The PPMCBASE contains two sets of four PMC connectors that provide a 32/64-bit PCI interface to an IEEE P1386.1 PMC compliant PPMC/PMC module. Connectors J11/J21, J12/J22, and J13/J23 provide the 32/64-bit PCI interface while J14/J24 provide an I/O path from the PPMCBASE board to the PPMC/PMC module. Signals routed to J14 include a RISCwatch and an asynchronous serial port or rear 64-bit PMC I/O. Signals routed to J24 include the I2C bus, an asynchronous serial port, a RISCWatch, and the Bank B FLASH.

PCI IDSEL Definition

The PPMC module PCI device configuration registers are accessed by using the IDSEL signal of each PCI agent to an A/D signal as defined in version 2.1 of the PCI specification. IDSEL definitions for the PPMCBASE are shown in the following table:

Table 3-2. IDSEL Mapping for PCI Devices

PCI Address Line	Local PCI Device IDSEL Connection
AD31	PMC 2 (Monarch Slot)
AD20	Intel 21554 (PCI-to-PCI Bridge)
AD18	PMC 1 Alternate Device
AD17	PMC 2 Alternate Device
AD16	PMC 1
AD14	Intel 21143 (LAN)

PCI Interrupt Routing

External interrupts that are controlled by the installed PPMC module are routed to the onboard PCI devices/slots as follows:

Table 3-3. PCI Interrupt Routing

Base PCI Interrupt Assignment	PMC 2 (System Controller) PCI Interrupt Line	PMC 1 (Non-System Controller) PCI Interrupt Line
PMCINTA# / Intel 21554 SINT#	PMC2INTA# (J21 pin 4)	PMC1INTD# (J11 pin 9)
PMCINTB#	PMC2INTB# PMC2 PCI Agent (J21 pin 5)	PMC1INTA# (J11 pin 4)
PMCINTC#	PMC2INTC# (J21 pin 6)	PMC1INTB# PMC1 PCI Agent (J11 pin 5)
PMCINTD# Intel 21143 INT#	PMC2INTD# (J21 pin 9)	PMC1INTC# (J11 pin 6)

FLASH Sockets

The PPMCBASE provides FLASH sockets for one bank, Bank B, of writable Boot FLASH memory. This FLASH is only accessible from PMC slot 2 and these signals are routed from the PMC connector J24 to the PLCC sockets. Bank B consists of two 32-pin PLCC sockets which can be populated with 1MB of FLASH memory. Only 8-bit writes are supported for this bank. A header is provided onboard for Bank A or Bank B selection and configuration by the PPMC module.

Note If the PPMC module also provides sockets for Bank B FLASH memory, ensure that only one set of these sockets are populated.

Ethernet Interface

PPMCBASE provides an Ethernet interface via the Intel 21143 device. This device, along with an external Level One LXT970 PHY device, implement a 10 Base-T/100Base-Tx autoselect ethernet interface. The Ethernet interface is routed to an RJ45 connector located at the front panel of the Base board.

Each PPMCBASE is assigned an Ethernet Station Address. The address is $08003E2XXXXX where XXXXX is the unique number assigned to a particular PPMCBASE. Each board's Ethernet Station Address is displayed on a label attached to the board. In addition, the Ethernet address is stored in a 256 byte serial EEPROM (NM93C46L) for storage of configuration information that will include the Ethernet address. For additional details, refer to the Intel 21143 Hardware Reference manual.



Caution Use extreme caution when viewing the contents of the Ethernet EEPROM via the PPCBUG SROM command. If the contents are modified incorrectly this could cause the PPCBUG Firmware Ethernet Drivers to work incorrectly.

Note: When the board is shipped from the factory, it should contain the proper EEPROM data for the PPMCBASE, which has 10Base-T/100Base-Tx Ethernet connections. There should not be a need to change the EEPROM contents.

For the pin assignments of the 10 Base-T/100 Base-Tx connector, refer to Chapter 4, *Connector Pin Assignments*.

PCI Mezzanine Interface

A key feature of the PPMCBASE family is the PCI (Peripheral Component Interconnect) bus. In addition to the on-board local bus devices (Ethernet, etc.), the PCI bus supports an industry-standard mezzanine interface, IEEE P1386.1 PMC (PCI Mezzanine Card). This support consists of two single-

wide or one double-wide PMC slots. Each slot provides four EIA-E700 AAAB connectors located on the PPMCBASE board to interface to a 32/64-bit PMC to add any desirable function.

PMC modules offer a variety of possibilities for I/O expansion through FDDI (Fiber Distributed Data Interface), ATM (Asynchronous Transfer Mode), graphics, and Ethernet ports. The Base board supports PMC front panel I/O.

Two sets of four 64-pin connectors on the base board (J11 - J14 and J21 - J24) interface with 32-bit or 64-bit IEEE P1386.1 PMC-compatible mezzanines to add any desirable function. The PCI Mezzanine Card slots have the following characteristics:

Mezzanine Type	PMC (PCI Mezzanine Card)
Mezzanine Size	S1B: Single width, standard depth (74mm x 149mm) with front panel S2B: Double width, standard depth (149mm x 149mm)
PMC Connectors	J11-J14 and J21-J24 (32/64-Bit PCI with front PMC I/O)
Signaling Voltage	V_{io} = 5.0Vdc

Refer to Chapter 4, *Connector Pin Assignments*, for the pin assignments of the PMC connectors. For detailed programming information, refer to Chapter 2, *Operating Instructions*, and to the user documentation for the PMC or PPMC modules you intend to use, listed in Appendix C, *Related Documentation*.

Asynchronous Serial Ports

The PPMCBASE provides access for two asynchronous serial ports, one located on each PPMC module. One serial interface is routed from PMC Slot 2 connector J24 to the RJ45 front panel connector identified as Serial 2, and the second serial interface is routed from PMC Slot 1 connector J14 to the RJ45 front panel connector identified as Serial 1.

CompactPCI Bus Interface

The CompactPCI bus interface is provided by using the Intel 21554 non-transparent PCI-to-PCI bridge chip. This device implements a 64-bit primary data bus and 64-bit secondary data bus interface and is PCI 2.1 compliant. The 21554 provides read/write data buffering in both directions.

Unlike a transparent PCI-to-PCI bridge, such as the 21154, the 21554 is designed to bridge two processor domains. The system CompactPCI bus is connected to the primary bus side of the bridge, which is also referred to as the host domain or the host processor side. The secondary bus interfaces to the PPMCBASE local PCI bus, referred to as the local domain or local processor side. The 21554 supports independent primary and secondary address spaces and address translation between the two processor domains. The 21554 accepts a Type 0 configuration header and the configuration space is accessible from both primary and secondary busses. Refer to the Intel 21554 Hardware Reference Manual for additional information and programming details.

The 21554 also provides for independent primary and secondary PCI clocks which means that the PPMCBASE has it's own local processor/PCI bus clock source independent of the system backplane clocks. Nevertheless, both the primary and secondary PCI clocks must be provided for the PPMC Carrier to function.

The 21554 supports 3.3V or 5V signalling at the PCI busses with a separate VIO pin for the primary and secondary bus I/O's. The secondary bus signalling voltage is selectable via resistor options and thus may be tied to either +5 volts for compatibility with +5V PMCs or +3.3 volts for compatibility with +3.3V PMCs. However, currently the PPMCBASE is only configured to support +5V VIO on the secondary bus. The primary bus signalling voltage is tied to the CPCI bus VIO, so the PPMCBASE is a universal board that may operate in a +3.3V or +5V chassis.

The Intel 21554 is attached to a 3.3V, 256 byte serial EEPROM device (93LC66A) in which configuration information for the Intel 21554 is stored. This information is used for serial pre-load in configuring the Intel 21554 if the serial pre-load is enabled. Refer to the Intel 21554 Hardware Reference Manual for additional information and programming details.

Serial EEPROM

The PPMCBASE board contains a 3.3V, 256 x 8 Serial EEPROM device (AT24C02) onboard. The Serial EEPROM provides for vital product data storage of the Base's hardware configuration information. The Serial EEPROM is accessed through the I^2C port from PMC Slot 2 as routed from the J24 PMC User I/O connector. The connection to the PMC connector provides a means for a PPMC module, operating as the Monarch, to access the SROM on the PPMCBASE to determine configuration information. Refer to the sections on Programming the PPMCBASE for SROM device address assignments.

Front Panel Indicators

The PPMCBASE provides one front panel LED for PCI activity.

- The green PCI Activity LED is lit when the IRDY# signal of the local PCI bus is active.

ABORT/RESET Switch

The PPMCBASE provides a single front panel accessible push button switch which provides both ABORT and RESET functions. When the switch is depressed for less than 3 seconds, an interrupt is generated to each PPMC processor. If the switch is held for more than 3 seconds, a board hard reset is generated and the reset is maintained as long as the switch is depressed.

Connector Pin Assignments

4

PPMCBASE Connectors

This chapter summarizes the pin assignments for the connectors on the PPMCBASE. The following connectors are described:

- CompactPCI J1/J2 Connectors
- CompactPCI User I/O Connector J3 (optional)
- CompactPCI Connector J4 (for alignment only, no signals)
- CompactPCI User I/O Connector J5 (not installed on PPMCBASE)
- PCI Mezzanine Card (PMC) Connectors (J21, J11, J22, J12, J13/23, J24, J14)
- PPMCBASE 10 Base-T/100 Base-Tx Connector, J8
- Asynchronous Serial Port Connector, J6 and J7
- RISCwatch Headers, J27 and J28
- FLASH Bank Select Header, J29
- Power Connector, J31 (optional - for stand-alone version)

CompactPCI J1/J2 Connectors

The PPMCBASE implements a 64-bit CompactPCI interface on connectors J1 and J2. J1 is a 110 pin AMP Z-pack 2mm hard metric type A connector with keying for +3.3V or +5V. J2 is 110 pin AMP Z-pack 2mm hard metric type B connector. Each of these connectors conform to the CompactPCI specification, Ver. 2.1. The pinout for connectors J1 and J2 are shown in Table 4-1 and Table 4-2.

Table 4-1. J1 CompactPCI Connector

	ROW A	ROW B	ROW C	ROW D	ROW E	
25	+5V	REQ64_L	ENUM_L	+3.3V	+5V	25
24	AD1	+5V	VIO	AD0	ACK64_L	24
23	+3.3V	AD4	AD3	+5V	AD2	23
22	AD7	GND	+3.3V	AD6	AD5	22
21	+3.3V	AD9	AD8	M66EN	CBE0_L	21
20	AD12	GND	VIO	AD11	AD10	20
19	+3.3V	AD15	AD14	GND	AD13	19
18	SERR_L	GND	+3.3V	PAR	CBE1_L	18
17	+3.3V	No Connect (SDONE)	No Connect (SBO_L)	GND	PERR_L	17
16	DEVSEL_L	GND	VIO	STOP_L	No Connect (LOCK_L)	16
15	+3.3v	FRAME_L	IRDY_L	BD_SEL_L	TRDY_L	15
12-14	KEY AREA					12-14
11	AD18	AD17	AD16	GND	CBE2_L	11
10	AD21	GND	+3.3V	AD20	AD19	10
9	CBE3_L	IDSEL	AD23	GND	AD22	9
8	AD26	GND	VIO	AD25	AD24	8
7	AD30	AD29	AD28	GND	AD27	7
6	REQ_L	GND	+3.3v	CLK	AD31	6
5	No Connect (BRSVP1A5)	No Connect (BRSVP1B5)	RST_L	GND	GNT_L	5
4	No Connect (BRSVP1A4)	HEALTHY_L	VIO	No Connect (INTP)	No Connect (INTS)	4
3	INTA_L	INTB_L	INTC_L	+5V	INTD_L	3
2	TCK	+5V	TMS	TDO	TDI	2
1	+5V	-12V	TRST_L	+12V	+5V	1

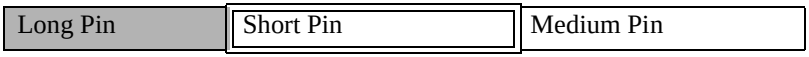


Table 4-2. J2 CompactPCI Connector

	ROW A	ROW B	ROW C	ROW D	ROW E	
22	GA4	GA3	GA2	GA1	GA0	22
21	No Connect (CLK6)	GND	No Connect (RSV)	No Connect (RSV)	No Connect (RSV)	21
20	No Connect CLK5	GND	No Connect (RSV)	GND	No Connect (RSV)	20
19	GND	GND	No Connect (RSV)	No Connect (RSV)	No Connect (RSV)	19
18	No Connect BRSVP2A18	No Connect BRSVP2B18	No Connect BRSVP2C18	GND	No Connect BRSVP2E18	18
17	No Connect BRSVP2A17	GND	No Connect (PRST_L)	No Connect (REQ6_L)	No Connect (GNT6_L)	17
16	No Connect BRSVP2A16	No Connect BRSVP2B16	No Connect (DEG_L)	GND	No Connect (BRSVP2E16)	16
15	No Connect BRSVP2A15	GND	No Connect (FAL_L)	No Connect (REQ5_L)	No Connect (GNT5_L)	15
14	AD35	AD34	AD33	GND	AD32	14
13	AD38	GND	VIO	AD37	AD36	13
12	AD42	AD41	AD40	GND	AD39	12
11	AD45	GND	VIO	AD44	AD43	11
10	AD49	AD48	AD47	GND	AD46	10
9	AD52	GND	VIO	AD51	AD50	9
8	AD56	AD55	AD54	GND	AD53	8
7	AD59	GND	VIO	AD58	AD57	7
6	AD63	AD62	AD61	GND	AD60	6
5	CBE5_L	64EN-L	VIO	CBE4_L	PAR64	5

Table 4-2. J2 CompactPCI Connector (Continued)

4	VIO	No Connect BRSVP2B4	CBE7_L	GND	CBE6_L	4
3	No Connect (CLK4)	GND	No Connect (GNT3_L)	No Connect (REQ4_L)	No Connect (GNT4_L)	3
2	No Connect (CLK2)	No Connect (CLK3)	No Connect (SYSEN_L)	No Connect (GNT2_L)	No Connect (REQ3_L)	2
1	No Connect (CLK1)	GND	No Connect (REQ1_L)	No Connect (GNT1_L)	No Connect REQ2_L	1

CompactPCI User I/O Connector J3

Connector J3 is a 110 pin AMP Z-pack 2mm hard metric type B connector. This connector routes the PMC 1 I/O and is only populated for the version that supports rear PMC I/O. The pin assignments for J3 on the PPMCBASE board are as follows (outer row F is assigned and used as ground pins but is not shown in the table):

Table 4-3. J3 CompactPCI User I/O Connector

	ROW A	ROW B	ROW C	ROW D	ROW E	
19	Not Used	+12V	-12V	Not Used	Not Used	19
18	Not Used	Not Used	Not Used	Not Used	Not Used	18
17	Not Used	Not Used	Not Used	Not Used	Not Used	17
16	Not Used	Not Used	Not Used	Not Used	Not Used	16
15	Not Used	Not Used	Not Used	Not Used	Not Used	15
14	+3.3V	+3.3V	+3.3V	+5V	+5V	14
13	PMC1IO5	PMC1IO4	PMC1IO3	PMC1IO2	PMC1IO1	13
12	PMC1IO10	PMC1IO9	PMC1IO8	PMC1IO7	PMC1IO6	12
11	PMC1IO15	PMC1IO14	PMC1IO13	PMC1IO12	PMC1IO11	11
10	PMC1IO20	PMC1IO19	PMC1IO18	PMC1IO17	PMC1IO16	10
9	PMC1IO25	PMC1IO24	PMC1IO23	PMC1IO22	PMC1IO21	9
8	PMC1IO30	PMC1IO29	PMC1IO28	PMC1IO27	PMC1IO26	8

Table 4-3. J3 CompactPCI User I/O Connector (Continued)

7	PMC1IO35	PMC1IO34	PMC1IO33	PMC1IO32	PMC1IO31	7
6	PMC1IO40	PMC1IO39	PMC1IO38	PMC1IO37	PMC1IO36	6
5	PMC1IO45	PMC1IO44	PMC1IO43	PMC1IO42	PMC1IO41	5
4	PMC1IO50	PMC1IO49	PMC1IO48	PMC1IO47	PMC1IO46	4
3	PMC1IO55	PMC1IO54	PMC1IO53	PMC1IO52	PMC1IO51	3
2	PMC1IO60	PMC1IO59	PMC1IO58	PMC1IO57	PMC1IO56	2
1	VIO (+5V)	PMC1IO64	PMC1IO63	PMC1IO62	PMC1IO61	1

Signal Descriptions

PMCIO:

PMC1IO(1:64) - PMC1 I/O signals 1 through 64

Connector J4

Connector J4 is not used to carry signals, but it is installed on the PPMCBASE for alignment purposes. The keying tabs in the Type A connector assist with alignment of pins in the backplane connector during insertion of the boards. No signals are connected to the J4 pins except the ground pins in Row F (F1, F3, F5, F7, F9, and F11) of the outer shield, which are connected to the board logic ground. The connector is only populated for the version that supports rear PMC I/O.

User I/O Connector J5

Connector J5 is not installed on the PPMCBASE, since no signals are connected to the J5 pins.

PCI Mezzanine Card Connectors

There are two sets of four 64-pin SMT connectors on the PPMCBASE to provide a 32/64-bit PCI interface for two optional add-on PMC/PPMC modules (J21, J11, J22, J12, J13/23, J24, J14). The pin assignments are listed in the tables on the next several pages.

Table 4-4. PMC Connector J21 Pin Assignments

1	TCK	-12V	2
3	GND	PMCINTA_L	4
5	PMCINTB_L	PMCINTC_L	6
7	PMC2PRSNT_L	+5V	8
9	PMCINTD_L	Not Used (PCI RSVD - B14)	10
11	GND	Not Used (PCI RSVD - 3.3V aux)	12
13	PCICLK	GND	14
15	GND	PMC2GNT_L	16
17	PMC2REQ_L	+5V	18
19	VIO	AD31	20
21	AD28	AD27	22
23	AD25	GND	24
25	GND	C/BE3_L	26
27	AD22	AD21	28
29	AD19	+5V	30
31	VIO	AD17	32
33	FRAME_L	GND	34
35	GND	IRDY_L	36
37	DEVSEL_L	+5V	38
39	GND	LOCK_L	40
41	SDONE_L	SBO_L	42
43	PAR	GND	44
45	VIO	AD15	46

Table 4-4. PMC Connector J21 Pin Assignments (Continued)

47	AD12	AD11	48
49	AD09	+5V	50
51	GND	C/BE0_L	52
53	AD06	AD05	54
55	AD04	GND	56
57	VIO	AD03	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	REQ64_L	64

Table 4-5. PMC Connector J11 Pin Assignments

1	TCK	-12V	2
3	GND	PMCINTB_L	4
5	PMCINTC_L	PMCINTD_L	6
7	PMC1PRSNT_L	+5V	8
9	PMCINTA_L	Not Used (PCI RSVD - B14)	10
11	GND	Not Used (PCI RSVD - 3.3V aux)	12
13	PCICLK	GND	14
15	GND	PMC1GNT_L	16
17	PMC1REQ_L	+5V	18
19	VIO	AD31	20
21	AD28	AD27	22
23	AD25	GND	24
25	GND	C/BE3_L	26
27	AD22	AD21	28
29	AD19	+5V	30
31	VIO	AD17	32
33	FRAME_L	GND	34

Table 4-5. PMC Connector J11 Pin Assignments (Continued)

35	GND	IRDY_L	36
37	DEVSEL_L	+5V	38
39	GND	LOCK_L	40
41	SDONE_L	SBO_L	42
43	PAR	GND	44
45	VIO	AD15	46
47	AD12	AD11	48
49	AD09	+5V	50
51	GND	C/BE0_L	52
53	AD06	AD05	54
55	AD04	GND	56
57	VIO	AD03	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	REQ64_L	64

Table 4-6. PMC Connector J22 Pin Assignments

1	+12V	TRST_L	2
3	TMS	Not Used (TDO)	4
5	pullup (TDI)	GND	6
7	GND	Not Used (PCI RSVD - A9)	8
9	Not Used (PCI RSVD - B10)	Not Used (PCI RSVD - A11)	10
11	Not Used (PMC RSVD)	+3.3V	12
13	PCIRST_L	Not Used (PMC RSVD)	14
15	+3.3V	Not Used (PMC RSVD)	16
17	Not Used (PCI RSVD - PME_L)	GND	18
19	AD30	AD29	20
21	GND	AD26	22

Table 4-6. PMC Connector J22 Pin Assignments (Continued)

23	AD24	+3.3V	24
25	PMC2IDSEL	AD23	26
27	+3.3V	AD20	28
29	AD18	GND	30
31	AD16	C/BE2_L	32
33	GND	PMC2IDSELB	34
35	TRDY_L	+3.3V	36
37	GND	STOP_L	38
39	PERR_L	GND	40
41	+3.3V	SERR_L	42
43	C/BE1_L	GND	44
45	AD14	AD13	46
47	GND (M66EN)	AD10	48
49	AD08	+3.3V	50
51	AD07	PMC2REQB_L	52
53	+3.3V	PMC2GNTB_L	54
55	Not Used (PMC RSVD)	GND	56
57	Not Used (PMC RSVD)	EREADY	58
59	GND	RSTOUT_L	60
61	ACK64_L	+3.3V	62
63	GND	MONARCH_L	64

Table 4-7. PMC Connector J12 Pin Assignments

1	+12V	TRST_L	2
3	TMS	Not Used (TDO)	4
5	pullup (TDI)	GND	6
7	GND	Not Used (PCI RSVD - A9)	8
9	Not Used (PCI RSVD - B10)	Not Used (PCI RSVD - A11)	10

Table 4-7. PMC Connector J12 Pin Assignments (Continued)

11	pullup (PMC RSVD - BUSMODE[2])	+3.3V	12
13	PCIRST_L	pulldown (PMC RSVD - BUSMODE[3])	14
15	+3.3V	pulldown (PMC RSVD - BUSMODE[4])	16
17	Not Used (PCI RSVD - PME_L)	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	+3.3V	24
25	PMC1IDSEL	AD23	26
27	+3.3V	AD20	28
29	AD18	GND	30
31	AD16	C/BE2_L	32
33	GND	PMC1IDSELB	34
35	TRDY_L	+3.3V	36
37	GND	STOP_L	38
39	PERR_L	GND	40
41	+3.3V	SERR_L	42
43	C/BE1_L	GND	44
45	AD14	AD13	46
47	GND (M66EN)	AD10	48
49	AD08	+3.3V	50
51	AD07	PMC1REQB_L	52
53	+3.3V	PMC1GNTB_L	54
55	Not Used (PMC RSVD)	GND	56
57	Not Used (PMC RSVD)	EREADY	58
59	GND	RSTOUT_L	60
61	ACK64_L	+3.3V	62

Table 4-7. PMC Connector J12 Pin Assignments (Continued)

63	GND	Not Used (MONARCH_L)	64

Table 4-8. PCI Mezzanine Card Connector

	J13/23		
1	Reserved	GND	2
3	GND	C/BE7_L	4
5	C/BE6_L	C/BE5_L	6
7	C/BE4_L	GND	8
9	VIO	PAR64	10
11	AD63	AD62	12
13	AD61	GND	14
15	GND	AD60	16
17	AD59	AD58	18
19	AD57	GND	20
21	VIO	AD56	22
23	AD55	AD54	24
25	AD53	GND	26
27	GND	AD52	28
29	AD51	AD50	30
31	AD49	GND	32
33	GND	AD48	34
35	AD47	AD46	36
37	AD45	GND	38
39	VIO	AD44	40
41	AD43	AD42	42
43	AD41	GND	44
45	GND	AD40	46
47	AD39	AD38	48
49	AD37	GND	50
51	GND	AD36	52

Table 4-8. PCI Mezzanine Card Connector (Continued)

53	AD35	AD34	54
55	AD33	GND	56
57	VIO	AD32	58
59	Reserved	Reserved	60
61	Reserved	GND	62
63	GND	Reserved	64

Table 4-9. PMC Connector J24 Pin Assignments

1	I2CSDA	I2CSCL	2
3	TXD2	RXD2	4
5	CPUTDI	CPUTDO	6
7	CPUTRST_L	GND	8
9	GND	BANKB_SEL	10
11	CPUTCK	CPUTMS	12
13	SRST_L	CPURST_L	14
15	CHKSTPO_L	FLASHOE_L	16
17	FLASHUWE_L	FLASHCS_L	18
19	FLASHLWE_L	FLASHALE_L	20
21	FLASHBA0	FLASHDBOE_L	22
23	FLASHBA1	GND	24
25	GND	FLASHRA0	26
27	FLASHRA1	FLASHRA2	28
29	FLASHRA3	FLASHRA4	30
31	FLASHRA5	FLASHRA6	32
33	FLASHRA7	FLASHRA8	34
35	FLASHRA9	FLASHRA10	36
37	FLASHRA11	FLASHRA12	38
39	Not Used	GND	40

Table 4-9. PMC Connector J24 Pin Assignments (Continued)

41	GND	ABORT_L	42
43	Not Used	Not Used	44
45	Not Used	Not Used	46
47	FLASHRD0	FLASHRD1	48
49	FLASHRD2	FLASHRD3	50
51	FLASHRD4	FLASHRD5	52
53	FLASHRD6	FLASHRD7	54
55	FLASHRD8	GND	56
57	GND	FLASHRD9	58
59	FLASHRD10	FLASHRD11	60
61	FLASHRD12	FLASH1RD13	62
63	FLASHRD14	FLASHRD15	64

Table 4-10. PMC Connector J14 Pin Assignments

1	Not Used	Not Used	2
3	TXD1	RXD1	4
5	CPUTDI	CPUTDO	6
7	CPUTRST_L	GND	8
9	GND	Not Used	10
11	CPUTCK	CPUTMS	12
13	SRST_L	CPURST_L	14
15	CHKSTPO_L	Not Used	16
17	Not Used	Not Used	18
19	Not Used	Not Used	20
21	Not Used	Not Used	22
23	Not Used	GND	24
25	GND	Not Used	26
27	Not Used	Not Used	28

Table 4-10. PMC Connector J14 Pin Assignments (Continued)

29	Not Used	Not Used	30
31	Not Used	Not Used	32
33	Not Used	Not Used	34
35	Not Used	Not Used	36
37	Not Used	Not Used	38
39	Not Used	GND	40
41	GND	ABORT_L	42
43	Not Used	Not Used	44
45	Not Used	Not Used	46
47	Not Used	Not Used	48
49	Not Used	Not Used	50
51	Not Used	Not Used	52
53	Not Used	Not Used	54
55	Not Used	GND	56
57	GND	Not Used	58
59	Not Used	Not Used	60
61	Not Used	Not Used	62
63	Not Used	Not Used	64

Signal Descriptions for J14/J24

I2CSDA I2C bus serial data
I2CSCL I2C bus clock
TXD RS232 serial port transmit data
RXD RS232 serial port receive data
CPUTDI Processor RISCwatch TDI
CPUTDO Processor RISCwatch TDO
CPUTTRST_L Processor RISCwatch Test Reset
CPUTCK Processor RISCwatch Test Clock
CPUTMS Processor RISCwatch Test Mode Select
SRESET_L Processor RISCwatch Soft Reset
CPURST_L Processor RISCwatch CPU Reset

CHKSTPO_L Processor RISCwatch CPU Checkstop Out
BANKB_SEL FLASH Bank B select
FLASHOE_L FLASH Output Enable
FLASHUWE_L FLASH Upper Byte Write Enable
FLASHLWE_L FLASH Lower Byte Write Enable
FLASHCS_L FLASH Chip Select
FLASHALE_L FLASH Address Latch Enable
FLASHDBOE_L FLASH (optional) Data Buffer Output Enable
FLASHBA(0:1) FLASH address lines
FLASHRA(0:12) FLASH address lines
FLASHRD(0:15) FLASH data lines
ABORT_L ABORT Interrupt

Table 4-11. Alternate PMC I/O Supported PMC Connector J14 Pin Assignments

	J14		
1	PMC IO1	PMC IO2	2
3	PMC IO3	PMC IO4	4
5	PMC IO5	PMC IO6	6
7	PMC IO7	PMC IO8	8
9	PMC IO9	PMC IO10	10
11	PMC IO11	PMC IO12	12
13	PMC IO13	PMC IO14	14
15	PMC IO15	PMC IO16	16
17	PMC IO17	PMC IO18	18
19	PMC IO19	PMC IO20	20
21	PMC IO21	PMC IO22	22
23	PMC IO23	PMC IO24	24
25	PMC IO25	PMC IO26	26
27	PMC IO27	PMC IO28	28
29	PMC IO29	PMC IO30	30
31	PMC IO31	PMC IO32	32
33	PMC IO33	PMC IO34	34

Table 4-11. Alternate PMC I/O Supported PMC Connector J14 Pin Assignments (Continued)

35	PMC IO35	PMC IO36	36
37	PMC IO37	PMC IO38	38
39	PMC IO39	PMC IO40	40
41	PMC IO41	PMC IO42	42
43	PMC IO43	PMC IO44	44
45	PMC IO45	PMC IO46	46
47	PMC IO47	PMC IO48	48
49	PMC IO49	PMC IO50	50
51	PMC IO51	PMC IO52	52
53	PMC IO53	PMC IO54	54
55	PMC IO55	PMC IO56	56
57	PMC IO57	PMC IO58	58
59	PMC IO59	PMC IO60	60
61	PMC IO61	PMC IO62	62
63	PMC IO63	PMC IO64	64

PPMCBASE 10 Base-T/100 Base-Tx Connector (J8)

The 10 Base-T/100 Base-Tx Connector is an RJ45 connector located on the front panel of the PPMCBASE. The pin assignments for this connector are as follows:

Table 4-12. 10 Base-T/100 Base-Tx Connector J8

1	TD+
2	TD-
3	RD+
4	AC Terminated
5	AC Terminated
6	RD-

Table 4-12. 10 Base-T/100 Base-Tx Connector J8 (Continued)

7	AC Terminated
8	AC Terminated

Asynchronous Serial Port Connector (J6 and J7)

There are two industry standard RJ45 connectors located on the front panel of the PPMCBASE that provide access to asynchronous serial ports. One is identified as Serial 1 for the PPMC module installed in PMC Slot 1 and the second is identified as Serial 2 for the PPMC module installed in PMC Slot 2. Serial 1 is disabled if rear 32/64-bit PMC I/O is required for PMC Slot 1. The pin assignments are listed in Table 4-13.

Table 4-13. Asynchronous Serial Port Pin Assignments

1	Not Used
2	Not Used
3	GND
4	TXD
5	RXD
6	GND
7	Not Used
8	Not Used

Processor RISCwatch Headers (J27 and J28)

There are two standard 16-pin headers located on the PPMCBASE that provide an interface for the RISCwatch function. One RISCwatch header is provided for each PPMC module installed in a PMC slot. RISCwatch 1 corresponds to PMC Slot 1 and RISCwatch 2 corresponds to PMC Slot 2. RISCwatch 1 is disabled if rear 32/64-bit PMC I/O is required for PMC Slot 1. The pin assignments for the RISCwatch header is as follows:

Table 4-14. RISCwatch Header Pin Assignments

1	CPUTDO	No Connect	2
3	CPUTDI	CPUTRST_L	4
5	No Connect	Pullup	6
7	CPUTCK	No Connect	8
9	CPUTMS	No Connect	10
11	SRESET_L	No Connect	12
13	CPURST_L	VOID (Key)	14
15	CKSTPO_L	GND	16

Flash Bank Select Header (J29)

The PPMCBASE provides a 3-pin header for selecting the flash bank from which to boot during power up. Placing the jumper across pins 1 and 2 will select Flash Bank A, while placing the jumper across pins 2 and 3 (default) will select Flash Bank B. If Bank B is selected and there are conflicting sockets on the PPMC module, verify that only one set of sockets is populated. The pin assignments for the Flash Bank Select header are as follows:

Table 4-15. Flash Bank Select Header Pin Assignments

1	GND
2	BANKB_SEL
3	+3.3V

Power Connector (J31) (Optional)

The PPMCBASE provides a power connector for stand-alone operation. The pin assignments for the power connector are as follows:

Table 4-16. Power Connector Pin Assignments

1	+5V
2	GND
3	GND

Table 4-16. Power Connector Pin Assignments (Continued)

4	Not Used
5	+3.3V
6	GND
7	+5V

Power Measurement Headers

There are nine 2-pin headers provided for power measurements at each PMC slot. Each header is located across a 0.012 ohm, 1% tolerance, 1W sense resistor as shown below:

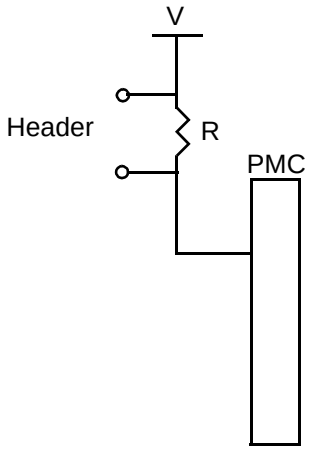


Figure 4-1. Power Measurement Header

The following table shows the location of each header and corresponding PMC Slot and voltage.

Table 4-17. Power Measurement Headers

PMC Slot #	Voltage	Ref Des
1	+3.3v	J25
2	+3.3v	J17

Table 4-17. Power Measurement Headers (Continued)

PMC Slot #	Voltage	Ref Des
	VIO	J26
1	+5v	J20
2	+5v	J15
1	+12v	J19
2	+12v	J10
1	-12v	J18
2	-12v	J9

PPCBug Overview

The PPCBug firmware is the layer of software just above the hardware. The firmware provides the proper initialization for the devices on the PPMCBASE and the PPMC module, such as the PPMC750-2xxx upon power-up or reset.

The PPCBug firmware is programmed in the FLASH ROMs that are installed in the PPMCBASE on-board sockets. For information about PPCBug, the monitor (interactive command portion of the firmware), and the special commands, refer to the specific Motorola PMC or PPMC Installation and Use Guide that corresponds to the PMC or PPMC module you are using in conjunction with the PPMCBASE.

For full user information about PPCbug, refer to the *PPCBug Firmware Package User's Manual (PPCBUGA1/UM and PPCBUGA2/UM)* and the *PPCBug Diagnostics Manual (PPCDIAA/UM),* listed in Appendix C, *Related Documentation*.

Specifications A

Specifications

Table A-1 lists the general specifications for the PPMCBASE board. Subsequent sections detail cooling requirements and EMC compliance.

A complete functional description of the PPMCBASE board appears in Chapter 3, *Functional Description*. Specifications for the optional PCI mezzanines can be found in the documentation for those modules.

Table A-1. PPMCBASE Specifications

Characteristics	Specifications
Power requirements (not PPMC or PMC)	+5Vdc (±5%), 0.41A typical +3.3Vdc (±5%), 0.33A typical
PMC I/O Signal Impedance	44 to 65 ohms (nominal impedance)
Operating temperature	-5°C to +55°C entry air with forced-air cooling (refer to the *Cooling Requirements* section)
Storage temperature	–40°C to +85° C
Relative humidity	5% to 85% (non-condensing)
Physical dimensions Base board only Height Depth Front panel width	6U Eurocard 9.2 in. (233.35 mm) 6.3 in. (160 mm) 0.8 in. (20mm)

Cooling Requirements

The Motorola PPMCBASE board is specified, designed, and tested to operate reliably with an incoming air temperature range from -5° to +55° C (32° to 131° F) with forced air cooling of the entire assembly (base board and modules) at a velocity typically achievable by using a 150 LFM axial fan. Temperature qualification is performed in a standard Motorola CompactPCI chassis. Twenty-five-watt load boards are inserted in two

card slots, one on each side, adjacent to the board under test, to simulate a high power density system configuration. An assembly of three axial fans, rated at 100 CFM per fan, is placed directly under the CompactPCI card cage. The incoming air temperature is measured between the fan assembly and the card cage, where the incoming airstream first encounters the module under test. Test software is executed as the module is subjected to ambient temperature variations. Case temperatures of critical, high power density integrated circuits are monitored to ensure component vendors' specifications are not exceeded.

While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 10 CFM and 490 LFM flowing over the module. Less airflow is required to cool the module in environments having lower maximum ambients. Under more favorable thermal conditions, it may be possible to operate the module reliably at higher than 55° C with increased airflow. It is important to note that there are several factors, in addition to the rated CFM of the air mover, which determine the actual volume and speed of air flowing over a module.

PPMCBASE VPD Reference Information B

Vital Product Data (VPD) Introduction

The Vital Product Data (VPD) portion of on-board memory contains static board build information, which is typically used for board initialization, configuration, and verification. The PPMCBASE VPD is stored in the board's SROM and contains local hardware configuration information. The data in the VPD portion of the SROM consists of a header section, followed by contiguous formatted data packets. The header section consists of eye-catcher and size fields, and the data packets consist of identifier, data length and data content fields.

The header section begins with an eye-catcher field that can be used to verify the existence of an initialized VPD SROM (an EEPROM CRC packet is also used to verify the integrity of the VPD content). The size field contains the total number of bytes assigned to the VPD portion of the SROM.

Each packet begins with a unique identifier field that defines the content and data structures of the packet's data section. The data length field contains the size of the data section in bytes which is also added to the data section base address to locate the starting address of the following VPD packet. Different data section lengths are sometimes used to denote different revision levels or array sizes for packets of a particular identifier. Packets must be contiguous, but may be placed in any order. The termination packet identifier marks the end of the VPD and must immediately follow the last valid packet. Common VPD packets include assigned ethernet address, board serial number, processor internal/external clock frequency, processor identifier, connector population, and other packets.

Users may add additional data packets which are assigned to the user range of packet identifiers and adhere to the data structure described in this appendix. Although the addition of user packets is discouraged, one potential user packet application is the specification of field installed hardware modules.

B

The data listed in the following tables are for general reference information. The VPD identifies board information that may be useful during board initialization, configuration and verification.

VPD Definitions - Packet Types

Table B-1 describes and lists the currently assigned packet identifiers.

Note: Additional packet identifiers may be added to this list as future versions of the VPD are released**.**

Table B-1. VPD Packet Types

ID#	Size	Description	Data Type	Notes
00	N/A	Guaranteed Illegal	N/A	
01	Variable	Product Identifier (for example, “PPMC750”, “MCP750”, “MVME2400”, “PPMC750-2xx”, “PPMCBASE,” etc.)	ASCII	1
02	Variable	Factory Assembly Number (e.g., “01-W3510F01x”, etc.)	ASCII	1
03	Variable	Serial Number (e.g., “3383185”, etc.)	ASCII	1
04	10	Product Configuration Options Data The data in this packet further describes the board configuration (for example, header population, I/O routing, etc.). Its exact contents is dependent upon the product configuration/type. A following table describes this packet.	Binary	
05	04	MPU Internal Clock Frequency in Hertz (for example, 350,000,000 decimal, etc.)	Integer (4-byte)	2
06	04	MPU External Clock Frequency in Hertz (for example, 100,000,000 decimal, etc.). This is also called the local processor bus frequency.	Integer (4-byte)	2
07	04	Reference Clock Frequency in Hertz (for example, 32,768 decimal, etc.). This value is the frequency of the crystal driving the OSCM.	Integer (4-byte)	2
08	06	Ethernet Address (for example, 08003E26A475, etc.)	Binary	3, 4

Table B-1. VPD Packet Types (Continued)

ID#	Size	Description	Data Type	Notes
09	Variable	MPU Type (for example, 601, 602, 603, 604, 750, 801, 821, 823, 860, 860DC, 860DE, 860DH, 860EN, 860MH, etc.)	ASCII	1
0A	04	EEPROM CRC This packet is optional. This packet would be utilized in environments where CRC protection is required. When computing the CRC this field (that is., 4 bytes) is set to zero. This CRC only covers the range as specified the size field.	Integer (4-byte)	2
0B	0C	FLASH Memory Configuration A table found later in this document further describes this packet.	Binary	
0C	TBD	VLSI Device Revisions/Versions	Binary	
0D	04	Host PCI-Bus Clock Frequency in Hertz (for example, 33,333,333 decimal, etc.)	Integer (4-byte)	2
0E	0F	L2 Cache Configuration A table found later in this document further describes this packet.	Binary	
0F	04	VPD Revision. A table found later in this section further describes this packet.	Binary	
10-BF		Reserved		
C0-FE		User Defined An example of a user defined packet could be the type of LCD panel connected in an MPC821 based application.		
FF	N/A	Termination Packet (follows the last initialized data packet)	N/A	

Notes:

1. Data size varies, depending on the product configuration/type.
2. Integer values are formatted/stored in big-endian byte ordering.

3. This packet may be omitted if the ethernet interface is non-existent, or the ethernet interface has an associative SROM (e.g., DEC21x4x).

4. This packet may contain an additional byte following the address data. This additional byte indicates the ethernet interface number and is specified in applications where the host product supports multiple ethernet interfaces. For each ethernet interface present, the instance number is incremented by one starting with zero.

VPD Definitions - Product Configuration Options Data

The product configuration options data packet consists of a binary bit field. The first bit of the first byte is bit 0 (that is, PowerPC bit numbering). An option is present when the assigned bit is a one. Table B-2 further describes the product configuration options of the VPD data packet:

Table B-2. MCG Product Configuration Options Data

Bit Number	Bit Mnemonic	Bit Description
0	PCO_PCI0_CONN1	PCI/PMC bus 0 connector 1 present
1	PCO_PCI0_CONN2	PCI/PMC bus 0 connector 2 present
2	PCO_PCI0_CONN3	PCI/PMC bus 0 connector 3 present
3	PCO_PCI0_CONN4	PCI/PMC bus 0 connector 4 present
4	PCO_PCI1_CONN1	PCI/PMC bus 1 connector 1 present
5	PCO_PCI1_CONN2	PCI/PMC bus 1 connector 2 present
6	PCO_PCI1_CONN3	PCI/PMC bus 1 connector 3 present
7	PCO_PCI1_CONN4	PCI/PMC bus 1 connector 4 present
8	PCO_ISA_CONN1	ISA bus connector 1 present
9	PCO_ISA_CONN2	ISA bus connector 2 present
10	PCO_ISA_CONN3	ISA bus connector 3 present
11	PCO_ISA_CONN4	ISA bus connector 4 present
12	PCO_EIDE1_CONN1	IDE/EIDE device 1 connector 1 present
13	PCO_EIDE1_CONN2	IDE/EIDE device 1 connector 2 present
14	PCO_EIDE2_CONN1	IDE/EIDE device 2 connector 1 present
15	PCO_EIDE2_CONN2	IDE/EIDE device 2 connector 2 present

Table B-2. MCG Product Configuration Options Data (Continued)

Bit Number	Bit Mnemonic	Bit Description
16	PCO_ENET1_CONN	Ethernet device 1 connector present
17	PCO_ENET2_CONN	Ethernet device 2 connector present
18	PCO_ENET3_CONN	Ethernet device 3 connector present
19	PCO_ENET4_CONN	Ethernet device 4 connector present
20	PCO_SCSI1_CONN	SCSI device 1 connector present
21	PCO_SCSI2_CONN	SCSI device 2 connector present
22	PCO_SCSI3_CONN	SCSI device 3 connector present
23	PCO_SCSI4_CONN	SCSI device 4 connector present
24	PCO_SERIAL1_CONN	Serial device 1 connector present
25	PCO_SERIAL2_CONN	Serial device 2 connector present
26	PCO_SERIAL3_CONN	Serial device 3 connector present
27	PCO_SERIAL4_CONN	Serial device 4 connector present
28	PCO_FLOPPY_CONN1	Floppy device connector 1 present
29	PCO_FLOPPY_CONN2	Floppy device connector 2 present
30	PCO_PARALLEL1_CONN	Parallel device 1 connector present
31	PCO_PARALLEL2_CONN	Parallel device 2 connector present
32	PCO_PMC1_IO_CONN	PMC slot 1 I/O connector present
33	PCO_PMC2_IO_CONN	PMC slot 2 I/O connector present
34	PCO_USB0_CONN	USB channel 0 connector present
35	PCO_USB1_CONN	USB channel 1 connector present
36	PCO_KEYBOARD_CONN	Keyboard connector present
37	PCO_MOUSE_CONN	Mouse connector present
38	PCO_VGA1_CONN	VGA device 1 connector present
39	PCO_SPEAKER_CONN	Speaker connector present
40	PCO_VME_CONN	VME backplane connector present
41	PCO_CPCI_CONN	Compact PCI backplane connector present
42	PCO_ABORT_SWITCH	Abort switch present
43	PCO_BDFAIL_LIGHT	Board fail light present
44	PCO_SWREAD_HEADER	Software readable header present
45	PCO_MEMMEZ_CONN	Memory mezzanine connector present
46	PCO_PCI0_EXP_CONN	PCI bus 0 expansion connector present

Table B-2. MCG Product Configuration Options Data (Continued)

Bit Number	Bit Mnemonic	Bit Description
47		Reserved for future configuration options
48	PCO_DIMM1_CONN	DIMM slot 1 connector present
49	PCO_DIMM2_CONN	DIMM slot 2 connector present
50	PCO_DIMM3_CONN	DIMM slot 3 connector present
51	PCO_DIMM4_CONN	DIMM slot 4 connector present
52-127		Reserved for future configuration options

VPD Definitions - FLASH Memory Configuration Data

The FLASH memory configuration data packet consists of byte fields which indicate the size/organization/type of the FLASH memory array. Table B-3 further describes the FLASH memory configuration VPD data packet.

Table B-3. FLASH Memory Configuration Data

Byte Offset	Field Size (Bytes)	Field Mnemonic	Field Description
00	2	FMC_MID	Manufacturer's Identifier (FFFF = Undefined/Not-Applicable)
02	2	FMC_DID	Manufacturer's Device Identifier (FFFF = Undefined/Not-Applicable)
04	1	FMC_DDW	Device Data Width (e.g., 8-bits, 16-bits)
05	1	FMC_NOD	Number of Devices/Sockets Present
06	1	FMC_NOC	Number of Columns (Interleaves)
07	1	FMC_CW	Column Width in Bits This will always be a multiple of the device's data width.

Table B-3. FLASH Memory Configuration Data (Continued)

Byte Offset	Field Size (Bytes)	Field Mnemonic	Field Description
08	1	FMC_WEDW	Write/Erase Data Width The FLASH memory devices must be programmed in parallel when the write/erase data width exceeds the device's data width.
09	1	FMC_BANK	Bank Number of FLASH Memory Array: 0 = A, 1 = B
0A	1	FMC_SPEED	ROM Access Speed in Nanoseconds
0B	1	FMC_SIZE	Total Bank Size (Should agree with the physical organization above): 00=256K, 01=512K, 02=1M, 03=2M, 04=4M, 05=8M

A product may contain multiple FLASH memory configuration packets.

VPD Definitions - L2 Cache Configuration Data

The L2 cache configuration data packet consists of byte fields that show the size, organization, and type of the L2 cache memory array. **Note: The PPMCBASE does not contain L2 Cache** . Table B-4 further describes the L2 cache memory configuration VPD data packet.

Table B-4. L2 Cache Configuration Data

Byte Offset	Field Size (Bytes)	Field Mnemonic	Field Description
00	2	L2C_MID	Manufacturer's Identifier (FFFF = Undefined/Not-Applicable)
02	2	L2C_DID	Manufacturer's Device Identifier (FFFF = Undefined/Not-Applicable)
04	1	L2C_DDW	Device Data Width (for example, 8-bits, 16-bits, 32-bits, 64-bits, 128-bits)
05	1	L2C_NOD	Number of Devices Present
06	1	L2C_NOC	Number of Columns (Interleaves)

Table B-4. L2 Cache Configuration Data (Continued)

Byte Offset	Field Size (Bytes)	Field Mnemonic	Field Description
07	1	L2C_CW	Column Width in Bits This will always be a multiple of the device's data width.
08	1	L2C_TYPE	L2 Cache Type: 00 - Arthur Backside 01 - External 02 - In-Line
09	1	L2C_ASSOCIATE	Associative Microprocessor Number (If Applicable)
0A	1	L2C_OPERATIONMODE	Operation Mode: 00 - Either Write-Through or Write-Back (S/W Configurable) 01 - Either Write-Through or Write-Back (H/W Configurable) 02 - Write-Through Only 03 - Write-Back Only
0B	1	L2C_ERROR_DETECT	Error Detection Type: 00 - None 01 - Parity 02 - ECC
0C	1	L2C_SIZE	L2 Cache Size (Should agree with the physical organization above): 00 - 256K 01 - 512K 02 - 1M 03 - 2M 04 - 4M

Table B-4. L2 Cache Configuration Data (Continued)

Byte Offset	Field Size (Bytes)	Field Mnemonic	Field Description
0D	1	L2C_TYPE_BACKSIDE	L2 Cache Type (Backside Configurations): 00 - Late Write Sync, 1nS Hold, Differential Clock, Parity 01 - Pipelined Sync Burst, 0.5nS Hold, No Differentia Clock, Parity 02 - Late Write Sync, 1nS Hold, Differential Clock, No Parity 03 - Pipelined Sync Burst, 0.5nS Hold, No Differential Clock, No Parity
0E	1	L2C_RATIO_BACKSIDE	L2 Cache Core to Cache Ration (Backside Configurations): 00 - Disabled 01 - 1:1 (1) 02 - 3:2 (1.5) 03 - 2:1 (2) 04 - 5:2 (2.5) 05 - 3:1 (3)

A product may contain multiple L2 cache configuration packets. This product, the PPMCBASE, does not contain a L2 Cache device.

VPD Definitions - VPD Revision Data

The VPD revision data packet consists of byte fields that indicate the type, version, and revision of the vital product data. Table B-5 further describes the VPD revision data packet.

Table B-5. VPD Revision Data

Byte Offset	Field Size (Bytes)	Field Mnemonic	Field Description
00	1	VR_TYPE	Vital Product Data Type: 00 - Processor board VPD 01 - Baseboard (non-processor) VPD 02 - Transition module VPD
01	1	VR_ARCH	Vital Product Data Architecture Revision (currently at 2)
02	1	VR_BUILD	Vital Product Data Board Build Revision (starts at 0)
03	1	VR_REASON	Vital Product Data Revision Flags: 00 - Initial release

A product must have exactly one VPD revision packet.

SROM_CRC.C

```
/*
 * srom_crc - generate CRC data for the passed buffer
 * description:
 * This function's purpose is to generate the CRC for the
 * passed buffer.
 * call:
 *    argument #1 = buffer pointer
 *    argument #2 = number of elements
 * return:
 *    CRC data
 */
unsigned int
srom_crc(elements_p, elements_n)
register unsigned char *elements_p; /* buffer pointer */
register unsigned int elements_n;   /* number of elements */
{
   register unsigned int crc;
   register unsigned int crc_flipped;
   register unsigned char cbyte;
   register unsigned int index, dbit, msb;

   crc = 0xffffffff;
```

```
   for (index = 0; index < elements_n; index++) {
      cbyte = *elements_p++;
      for (dbit = 0; dbit < 8; dbit++) {
         msb = (crc >> 31) & 1;
         crc <<= 1;
         if (msb ^ (cbyte & 1)) {
            crc ^= 0x04c11db6;
            crc |= 1;
         }
         cbyte >>= 1;
      }
   }
crc_flipped = 0;
   for (index = 0; index < 32; index++) {
      crc_flipped <<= 1;
      dbit = crc & 1;
      crc >>= 1;
      crc_flipped += dbit;
   }
   crc = crc_flipped ^ 0xffffffff;
   return (crc);
}
```

Ethernet SROM Contents for PPMCBASE Boards

Table B-6 describes and lists the contents of the Ethernet SROM which is programmed onto the raw PPMCBASE part number 51NW9637H66. Note: not part of VPD SROM.

Table B-6. Ethernet SROM Configuration Contents for 01-W3510Fxxr*

Offset	Value	Description
00 (0x00)	57	SubSystem Vendor ID lower byte - Optional and manufacturer defined Eye-Catcher (“MOTOROLA”) **Note: Lowest CRC byte for the calculation of CRC**.
01 (0x01)	10	SubSystem Vendor ID upper byte - Optional and manufacturer defined.
02 (0x02)	56	SubSystem ID lower byte - Optional and manufacturer defined.
03 (0x03)	34	SubSystem ID upper byte - Optional and manufacturer defined.

Table B-6. Ethernet SROM Configuration Contents for 01-W3510Fxxr* (Continued)

Offset	Value	Description
04 (0x04)	00	Pointer to Card Bus (if supported - must be zero if not supported)
05 (0x05)	00	Pointer byte 2
06 (0x06)	00	Pointer byte 3
07 (0x07)	00	Pointer byte 4
08 (0x08)	00	ID_Reserved1 (8 bytes).
09 (0x09)	00	ID_Reserved1 byte 2
10 (0x0a)	00	ID_Reserved1 byte 3
11 (0x0b)	04	ID_Reserved1 byte 4
12 (0x0c)	00	ID_Reserved1 byte 5
13 (0x0d)	02	ID_Reserved1 byte 6
14 (0x0e)	00	ID_Reserved1 byte 7
15 (0x0f)	00	ID_Reserved1 byte 8
16 (0x10)	13	ID_BLOCK_CRC - CRC of bytes in offsets 00-15
17 (0x11)	00	ID_Reserved2
18 (0x12)	03	SROM format Version “Version 3”.
19 (0x13)	01	Number of controllers sharing this SROM
20 (0x14)	08	MAC address byte 1
21 (0x15)	00	MAC address byte 2
22 (0x16)	3e	MAC address byte 3
23 (0x17)	xx	MAC address byte 4 - defined at ATE
24 (0x18)	xx	MAC address byte 5 - defined at ATE
25 (0x19)	xx	MAC address byte 6 - defined at ATE
26 (0x1a)	0e	Controller Device number (this should be PCE DEVSEL for chip). This is the device ID for PCI configuration cycles to this device.
27 (0x1b)	1e	Offset to controller leaf information (0x1e = byte 30d)
28 (0x1c)	00	Offset to controller lead information MSB
29 (0x1d)	00	Controller offset list NULL terminator (Must be zero)
30 (0x1e)	00	**Controller 1 Info lead start**: LSB of driver last connection type (AutoSense 0x0800)
31 (0x1f)	08	MSB of connection type (AutoSense 0x0800)

Table B-6. Ethernet SROM Configuration Contents for 01-W3510Fxxr* (Continued)

Offset	Value	Description
32 (0x20)	01	Media Count - 1 media supported by this device (TP).
33 (0x21)	93	Format/Length (Extended Format 13 bytes long)
34 (0x22)	03	Block Type (0x03 = MII PHY chips only)
35 (0x23)	00	PHY number (index of the PHY controlled by this block)
36 (0x24)	00	GPR Sequence Length
37 (0x25)	03	Reset Sequence Length
38 (0x26)	01	Reset Sequence (0801, 0000, 0001)
39 (0x27)	08	
40 (0x28)	00	
41 (0x29)	00	
42 (0x2a)	01	
43 (0x2b)	00	
44 (0x2c)	00	Media Capabilities (0x7800) - 100Tx-FD/HD 10T-FD/HD
45 (0x2d)	78	Media Capabilities MSB
46 (0x2e)	e0	Nway advertisement 100Tx-FD/HD, 10T-FD/HD
47 (0x2f)	01	Nway advertisement MSB
48 (0x30)	00	Full duplex map - in order to support Full Duplex these bits
49 (0x31)	50	in Media capabilities mask are to be written. 100/10FD bits.
50 (0x32)	00	Transmit Threshold Bit Map - these bits describe which media
51 (0x33)	18	capabilities mask are to be written. (100 base medium only)
52 (0x34)	00	MII Connector Interrupt
53 (0x35)	00	
:	:	
125 (0x7d)	00	
126 (0x7e)	yy	Lower CRC byte - CRC for entire SROM (Refer to
127 (0x7f)	yy	Upper CRC byte

Note *This data will change to reflect the specific configuration of the corresponding board assembly number to which it applies.

B

VPD SROM Contents for PPMCBASE (01-W3510Fxx) Boards

The following tables describe the variable and static contents of the VPD that is programmed onto the PPMCBASE's raw part number 51NW9637L49. Table B-7 contains the variable data and Table B-8 contains the static data.

Table B-7. Variable VPD Contents Specifications for 01-W3510Fxx

Offset	01-W3510F01	01-W3510F02	01-W3510F03
Field Description: Product Identifier (Packet ASCII)			
21 (0x15)	30	30	30
22 (0x16)	30	30	30
23 (0x17)	31	32	33
Field Description: Assembly Number (Packet ASCII)			
35 (0x23)	30	30	30
36 (0x24)	31	32	33
37 (0x25)	xx	xx	xx
Field Description: Product Configuration Options Data (Packet Binary)			
54 (0x36)	60	60	20

Table B-8. Static VPD SROM Configuration Specifications for 01-W3510Fxx

Offset	Value	Field Type	Description
00 (0x00)	4D	ASCII	Eye-Catcher ("MOTOROLA") Note: Starting byte for the calculation of CRC
01 (0x01)	4F		
02 (0x02)	54		
03 (0x03)	4F		
04 (0x04)	52		
05 (0x05)	4F		
06 (0x06)	4C		

Table B-8. Static VPD SROM Configuration Specifications for 01-W3510Fxx (Continued)

Offset	Value	Field Type	Description
07 (0x07)	41		
08 (0x08)	01	BINARY	Size of VPD area in bytes. The size is viewed as logical, it is not the size of the EEPROM.
09 (0x09)	00		
10 (0x0a)	01	PACKET ASCII	Product Identifier [PPMCBASE-xxx]. Refer to Table B-7 for ‘xx’ values.
11 (0x0b)	0C		
12 (0x0c)	50		
13 (0x0d)	50		
14 (0x0e)	4D		
15 (0x0f)	43		
16 (0x10)	42		
17 (0x11)	41		
18 (0x12)	53		
19 (0x13)	45		
20 (0x14)	2D		
21 (0x15)	xx		
22 (0x16)	xx		
23 (0x17)	xx		
24 (0x18)	02	PACKET ASCII	Factory Assembly Number [01-W3510F01-W3510Fxx]. Refer to Table B-7 for ‘xx’ values.
25 (0x19)	0C		
26 (0x1a)	30		
27 (0x1b)	31		
28 (0x1c)	2d		
29 (0x1d)	57		
30 (0x1e)	33		
31 (0x1f)	35		
32 (0x20)	31		

Table B-8. Static VPD SROM Configuration Specifications for 01-W3510Fxx (Continued)

Offset	Value	Field Type	Description
33 (0x21)	30		
34 (0x22)	46		
35 (0x23)	xx		To be filled in at ATE. Refer to Table B-7 for 'xx' values. Refer also to Notes 1 & 2.
36 (0x24)	xx		
37 (0x25)	xx		
38 (0x26)	03		Serial Number
39 (0x27)	07		
40 (0x28)	xx		Serial number to be filled in at ATE. Refer to Note 1 and 2.
41 (0x29)	xx		
42 (0x2a)	xx		
43 (0x2b)	xx		
44 (0x2c)	xx		
45 (0x2d)	xx		
46 (0x2e)	xx		
47 (0x2f)	04	PACKET BINARY	Product Configuration Options Data. Refer to Note 1.
48 (0x30)	10		
49 (0x31)	C0		
50 (0x32)	00		
51 (0x33)	40		
52 (0x34)	80		
53 (0x35)	C0		
54 (0x36)	xx		
55 (0x37)	00		
56 (0x38)	00		
57 (0x39)	00		
58 (0x3A)	00		
59 (0x3B)	00		
60 (0x3C)	00		

Table B-8. Static VPD SROM Configuration Specifications for 01-W3510Fxx (Continued)

Offset	Value	Field Type	Description
61 (0x3D)	00		
62 (0x3E)	00		
63 (0x3F)	00		
64 (0x40)	00		
65 (0x41)	0A	PACKET INTEGER	EEPROM CRC (4 Bytes). Refer to Note 1. EPROM CRC When computing the CRC, this field (i.e., 4 bytes) is set to zero. This CRC only covers the range as Integer (4-byte). Refer to Sample CRC Generation Code figure for more details.
66 (0x42)	04		
67 (0x43)	xx		
68 (0x44)	xx		
69 (0x45)	xx		
70 (0x46)	xx		
71 (0x47)	0B	PACKET BINARY	FLASH Memory Configuration (Bank B)
72 (0x48)	0C		
73 (0x49)	FF		
74 (0x4A)	FF		
75 (0x4B)	FF		
76 (0x4C)	FF		
77 (0x4D)	08		
78 (0x4E)	02		
79 (0x4F)	02		
80 (0x50)	08		
81 (0x51)	08		
82 (0x52)	01		
83 (0x53)	78		
84 (0x54)	02		

Table B-8. Static VPD SROM Configuration Specifications for 01-W3510Fxx (Continued)

Offset	Value	Field Type	Description
85 (0x55)	0D	PACKET BINARY	Host PCI-Bus Clock Frequency in Hertz. [33,333,333Decimal]
86 (0x56)	04		
87 (0x57)	01		
88 (0x58)	FC		
89 (0x59)	A0		
90 (0x5A)	55		
91 (0x5B)	0F	BINARY	VPD Revision [2.0]
92 (0x5C)	04		
93 (0x5D)	01		
94 (0x5E)	02		
95 (0x5F)	00		
96 (0x60)	00		
97 (0x61)	FF	BINARY	Reserved for future expansion
:	:	:	:
255	FF		Reserved for future expansion Note: End byte for the calculation of CRC

PCI-to-PCI Bridge SROM Contents for 01-W3510Fxx Boards

The following tables describe and list the contents of the PCI-to-PCI Bridge SROM that is programmed onto the raw PPMCBASE part number 51NW9637M27. Table B-9 contains only variable contents of the PCI-to-PCI Bridge for 01-W3510Fxx boards. Table B-10 contains static contents of the PCI-to-PCI Bridge for 01-W3510Fxx boards.

Table B-9. PCI-to-PCI Bridge Contents Specification for 01-W3510Fxx

Offset	01-W3510F01	01-W3510F02	01-W3510F03
Field Description: Chip Control 0 Register			
49 (0x31)	00	00	00

Table B-10. PCI-to-PCI Bridge SROM Configuration Specification for 01-W3510Fxx

Offset	Value	Description
00 (0x00)	80	ROM present and reserved bytes
01 (0x01)	00	
02 (0x02)	00	
03 (0x03)	00	
04 (0x04)	00	Primary programming interface
05 (0x05)	20	Primary Sub-class code
06 (0x06)	0B	Primary Base class code
07 (0x07)	57	Subsystem vendor ID
08 (0x08)	10	
09 (0x09)	0E	Subsystem Device ID
10 (0x0a)	48	
11 (0x0b)	00	Primary minimum grant
12 (0x0c)	00	Primary maximum latency
13 (0x0d)	00	Secondary programming interface
14 (0x0e)	80	Secondary Sub-class code
15 (0x0f)	06	Secondary Base class code
16 (0x10)	00	Secondary minimum grant
17 (0x11)	00	Secondary maximum latency
18 (0x12)	00	Downstream memory 0 setup register
19 (0x13)	00	
20 (0x14)	00	
21 (0x15)	00	
22 (0x16)	00	Downstream memory 1 setup register
23 (0x17)	00	
24 (0x18)	00	
25 (0x19)	FF	
26 (0x1a)	00	Downstream memory 2 setup register
27 (0x1b)	00	
28 (0x1c)	00	

Table B-10. PCI-to-PCI Bridge SROM Configuration Specification for 01-W3510Fxx (Continued)

Offset	Value	Description
29 (0x1d)	FF	
30 (0x1e)	00	Downstream memory 3 setup register
31 (0x1f)	00	
32 (0x20)	00	
33 (0x21)	00	
34 (0x22)	00	Downstream memory 3 upper setup register
35 (0x23)	00	
36 (0x24)	00	
37 (0x25)	00	
38 (0x26)	00	Primary expansion ROM setup register
39 (0x27)	00	
40 (0x28)	00	Upstream memory 0 setup register
41 (0x29)	00	
42 (0x2a)	00	
43 (0x2b)	FE	
44 (0x2c)	00	Upstream memory 1 setup register
45 (0x2d)	00	
46 (0x2e)	00	
47 (0x2f)	FE	
48 (0x30)	00	Chip control 0 register
49 (0x31)	xx	Refer to Table B-9 for ‘xx’ values
50 (0x32)	00	Chip control 1 register
51 (0x33)	00	
52 (0x34)	00	Arbiter control register
53 (0x35)	02	
54 (0x36)	00	Primary SERR Disables
55 (0x37)	00	Secondary SERR Disables
56 (0x38)	00	PCI Power Management Data Register Values
57 (0x39)	01	
58 (0x3A)	02	

Table B-10. PCI-to-PCI Bridge SROM Configuration Specification for 01-W3510Fxx (Continued)

Offset	Value	Description
59 (0x3B)	03	
60 (0x3C)	04	
61 (0x3D)	05	
62 (0x3E)	06	
63 (0x3F)	07	
64 (0x40)	00	CompactPCI Hot-Swap ECP ID
65 (0x41)	48	PCI Power Management and BIST
66 (0x42)	00	
67 (0x43)	00	Unused and reserved
:	:	:
127 (0x7F)	00	Unused and reserved

Related Documentation C

Motorola Computer Group Documents

The Motorola publications listed below are referenced in this manual. You can obtain paper or electronic copies of Motorola Computer Group publications by:

- Contacting your local Motorola sales office
- Visiting Motorola Computer Group's World Wide Web literature site, http://www.motorola.com/computer/literature

Table C-1. Motorola Computer Group Documents

Document Title	Publication Number
PPMC750 Processor PMC Module Installation and Use	PPMC750A/IH
PPMC750 Processor PMC Module Programmer's Reference Guide	PPMC750A/PG
PPMC750 Extended Processor PMC Module Installation and Use	PPMC750XTA/IH
PPMC750 Extended Processor PMC Module Programmer's Reference Guide	PPMC750XTA/PG
PPCBug Firmware Package User's Manual (Parts 1 and 2)	PPCBUGA1/UM PPCBUGA2/UM
PPCBug Diagnostics Manual	PPCDIAA/UM

To obtain the most up-to-date product information in PDF or HTML format, visit http://www.motorola.com/computer/literature.

Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table C-2. Manufacturers' Documents

Document Title and Source	Publication Number
DECchip 21554 PCI-to-PCI Bridge for Embedded Applications Data Sheet Digital Equipment Corporation Maynard, Massachusetts DECchip Information Line Telephone (United States and Canada): 1-800-332-2717 TTY (United States only): 1-800-332-2515 Telephone (outside North America): +1-508-568-6868	EC-R7BMA-TE
Digital Semiconductor 21x4 Serial ROM Format, Version 3.03 Specification, May 28, 1996. Digital Equipment Corporation Maynard, Massachusetts DECchip Information Line Telephone (United States and Canada): 1-800-332-2717 TTY (United States only): 1-800-332-2515 Telephone (outside North America): +1-508-568-6868	
Digital Semiconductor 2155X PCI-to-PCI Bridge for Embedded Applications. Hardware Reference Manual Digital Equipment Corporation Maynard, Massachusetts DECchip Information Line Telephone (United States and Canada): 1-800-332-2717 TTY (United States only): 1-800-332-2515 Telephone (outside North America): +1-508-568-6868	EC-R8WGA-TE

Table C-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
Texas Instruments TI16C550C Asynchronous Communications Element - March 1994. Revised March 1997 Texas Instruments P.O. Box 655303 Dallas, TX 75265	SLLS177C

Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table C-3. Related Specifications

Document Title and Source	Publication Number
IEEE - Common Mezzanine Card Specification (CMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386.1

C

Table C-3. Related Specifications (Continued)

Document Title and Source	Publication Number
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.1 PCI Special Interest Group 2575 NE Kathryn St. #17 Hillsboro, OR 97124 Telephone: (800) 433-5177 (inside the U.S.) or (503) 693-6232 (outside the U.S.) FAX: (503) 693-8344	PCI Local Bus Specification
Processor PMC Standard (for Processor PCI Mezzanine Cards) VITA Standards Organization 7825 E. Gelding Drive, Suite 104 Scottsdale, AZ 85260 Telephone: 1-602-951-8866 FAX: 1-602-951-0720 URL: www.vita.com	VITA32 - 199x Draft 0.21 27 May 1999

Table C-3. Related Specifications (Continued)

Document Title and Source	Publication Number
PowerPC™ Microprocessor Common Hardware Reference Platform: A System Architecture (CHRP), Version 1.0 Literature Distribution Center for Motorola Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com OR APDA, Apple Computer, Inc. P.O. Box 319 Buffalo, NY 14207 Telephone: (800) 282-2732 FAX: (716) 871-6511 OR IBM 1580 Route 52, Bldg. 504 Hopewell Junction, NY 12533-6531 Telephone: (800) PowerPC OR Morgan Kaufmann Publishers, Inc. 340 Pine Street, Sixth Floor San Francisco, CA 94104-3205, USA Telephone: (415) 392-2665 FAX: (415) 982-2665	TB338/D MPRPPCHRP-01 ISBN 1-55860-394-8
PowerPC Reference Platform (PRP) Specification, Third Edition, Version 1.0, Volumes I and II International Business Machines Corporation Power Personal Systems Architecture 11400 Burnet Rd. Austin, TX 78758-3493 Document/Specification Ordering Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 Telephone: 708-296-9332	MPR-PPC-RPU-02

C

Table C-3. Related Specifications (Continued)

Document Title and Source	Publication Number
IEEE Standard for Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	IEEE 802.3
Information Technology - Local and Metropolitan Networks - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Global Engineering Documents 15 Inverness Way East Englewood, CO 80112-5704 Telephone: 1-800-854-7179 Telephone: (303) 792-2181 *(This document can also be obtained through the national standards body of member countries.)*	ISO/IEC 8802-3
Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange (EIA-232-D) Electronic Industries Association Engineering Department 2001 Eye Street, N.W. Washington, D.C. 20006	ANSI/EIA-232-D Standard
Compact PCI Specification PCI-to-PCI Bridge Specification PCI-ISA Specification PCI Industrial Manufacturers Group (PICMG) 401 Edgewater Pl, Suite 500 Wakefield, MA 01880 Telephone: 781-246-9318 Fax: 781-224-1239	CPCI Rev. 2.1 Dated 9/2/97 Rev. 1.02 Rev. 2.0

URLs

The following URLs (uniform resource locators) may provide helpful sources of additional information about this product, related services, and development tools. Please note that, while these URLs have been verified, they are subject to change without notice.

- Motorola Computer Group, http://www.motorola.com/computer
- Motorola Computer Group OEM Services, http://www.motorola.com/computer/support

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