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TMCPN710
Transition Module
Installation and Use

TMCPN710A/IH1

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Preface

The *TMCPN710 Installation and Use* describes the installation, components, and configurations of the main board. The document should be used by anyone who wants general as well as technical information about the TMCPN710 products.

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Safety Summary
Safety Depends On You

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola, Inc. assumes no liability for the customer's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must be plugged into an approved three-contact electrical outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

Keep Away From Live Circuits.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone.

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Use Caution When Exposing or Handling the CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.



Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

All Motorola PWBs (printed wiring boards) are manufactured by UL-recognized manufacturers, with a flammability rating of 94V-0.

Warning

This equipment generates, uses, and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used in a cabinet with adequate EMI protection.

If any modifications are made to the product, the modifier assumes responsibility for radio frequency interference issues. Changes or modifications not expressly approved by Motorola Computer Group could void the user's authority to operate the equipment.

CE European Notice: Board products with the CE marking comply with the EMC Directive (89/336/EEC). Compliance with this directive implies conformity to the following European Norms:

EN55022 Radio Frequency Interference, Class B

EN50082-1 Electromagnetic Immunity

This board product was tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a CE-marked system will maintain the required EMC/safety performance.

For minimum RF emissions, it is essential that you implement the following conditions:

1. Install shielded cables on all external I/O ports.

2. Connect conductive chassis rails to earth ground to provide a path for connecting shields to earth ground.

3. Tighten all front panel screws.

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General Information 1

Introduction

This manual provides general information, hardware preparation, installation instructions, and a functional description for the TMCPN710 Transition Modules.

Product Overview

The TMCPN710 Transition Modules (TMCPN710-001 or TMCPN710-002) provide the interface between the MCPN750-1xxx (hereafter referred to as MCPN750) CompactPCI Single Board Computer and various peripheral devices. This module provides industry standard connector access to two RJ-45 connectors and two onboard headers providing access to the asynchronous serial ports configured as EIA DTE, an RJ-45 connector for optional routing of 10BaseT/100Base-TX Ethernet interface, two CHAMP connectors for access to PMC I/O (TMCPN710-002 only), two USB Series A receptacles for access to USB interface, and two connectors for IDE CompactFLASH card access.

Features

The features of the TMCPN710 Transition Module include:

- Industry-standard connectors for these interfaces:
  - Two asynchronous serial ports (DTE)
  - 10Base-T/100Base-TX Ethernet port (requires MCPN750 build option)
  - Two 64-bit PMC I/O ports (TMCPN710-002)
  - Two USB ports
  - Two IDE Compact FLASH card interfaces

- Single-width board
- Electro-Magnetic Interference (EMI) and Electro-Static Discharge (ESD) protection

General Description

The TMCPN710 Transition Module provides connectors for optional ethernet, two USB ports, two serial ports and two 64-signal PMC I/O interfaces on the rear panel, as well as connection to the MCPN750 CompactPCI Single Board Computer module through the J3 and J5 connectors.

Because of space limitations, only two of the four serial ports have connectors on the rear panel. The interface to the other two serial ports is provided by two 26-pin headers. The Transition Module contains two 50-pin connectors which support two removable IDE Compact FLASH memory cards on the Primary EIDE channel. Refer to Chapter 4 for a listing of the pinouts of these connectors. The Compact FLASH connectors are not accessible through the rear panel. The Transition Module must be removed in order to install a Compact FLASH memory card.

All MCPN750 models use the same transition module.

Figure 1-1 shows the TMCPN710 transition module component layout and the front panel. See Table 1-1 for a list of the front panel port connectors.

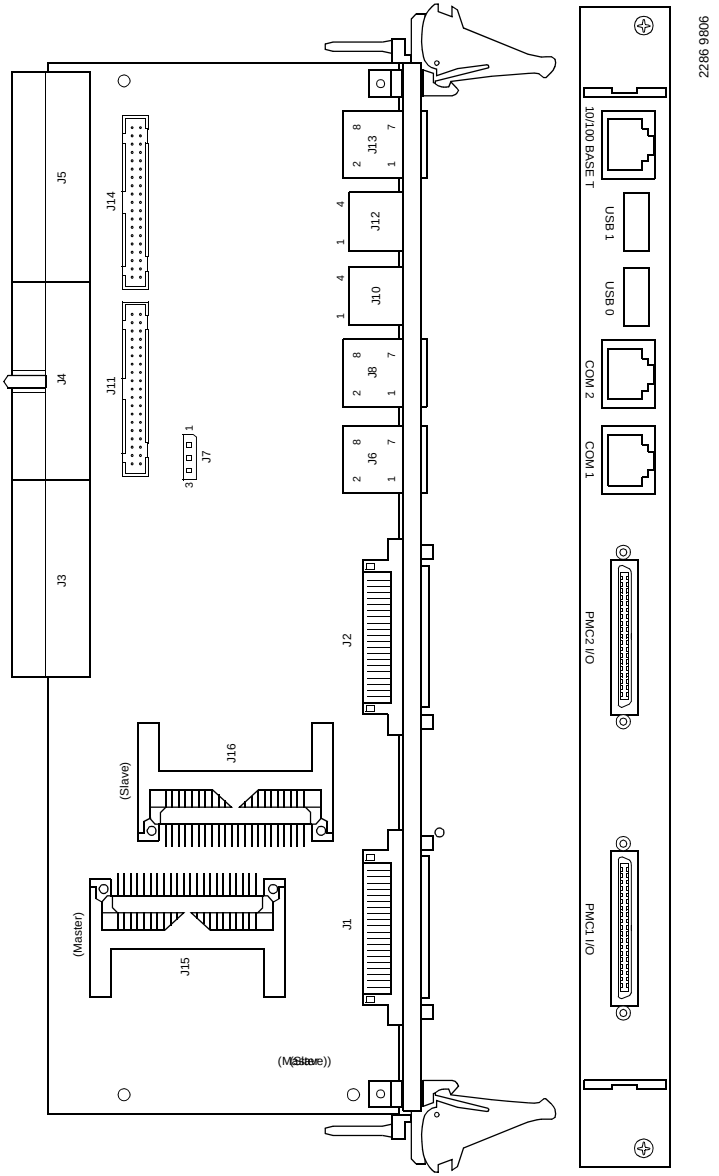


Figure 1-1. TMCPN710-002 Transition Module Front Panel and Component Side

Connectors and Cables

The connectors on the TMCPN710 transition module are listed in Table 1-1. The port connectors are located on the front panel and the top side of the transition module, which is shown in Figure 1-1. Refer to Table 1-2 for a list of the cables and Chapter 4 for the connector pin assignments.

Table 1-1. TMCPN710 Transition Module Connectors

Type	J Number	Description
COM1 and COM2	J6 and J8	8-pin female RJ-45 DIN asynchronous serial port connector
CompactPCI	J3	95-pin female connector for MCP750 I/O
CompactPCI	J4	110-pin female connector for MCP750 (alignment only)
CompactPCI	J5	110-pin female connector for MCP750 I/O
USB0 & USB1	J10, J12	4-pin USB Series A receptacles
EIDE	J15, J16	50-pin male connector for IDECompactFlash memory cards
PMC I/O	J1, J2	Two 68-pin 0.8mm CHAMP connectors for PMC I/O
Ethernet	J13	8-pin female RJ-45 DIN 10Base-T/100Base-TX connector (optional routing from MCPN750)

Table 1-2. TMCPN710 Transition Module Cables

Part Number	Description
User-supplied	8-conductor EIA-232-D DTE or DCE cable
User-supplied	68-line conductor cable

Specifications

The TMCPN710 transition module specifications are shown in Table 1-3.

Table 1-3. TMCPN710 Specifications

Characteristics	Specifications
Power Requirements	+5Vdc, 100mA typical, 150mA maximum
Operating temperature	5^{o} to 55^{o} C at chassis point of entry of forced air (approximately 5 CFM)
Storage temperature	-40^{o} to $+85^{o}$ C
Relative Humidity	5% to 85% (non-condensing)
Board Size (excluding front panel)	Height: 9.187 inches(233.35 mm) Height: 3.200 inches(80.00 mm) Thickness: 0.063 inches (1.60 mm)

Cooling Requirements

The TMCPN710 is tested to operate under forced air cooling with an incoming air temperature range of 5 degrees C to 55 degrees C. Adequate cooling can be achieved with air flowing over the module at 5 cubic feet per minute. The exact amount of air flow required for cooling depends on the ambient air temperature and the type, number, and location of modules and other heat sources.

EMC Compliance

The TMCPN710 was tested in an EMC-compliant chassis, and meets the requirements for EN55022 Class B equipment. For minimum RF emissions, it is essential that you implement the following conditions:

- Install shielded cables on all external I/O ports
- Connect conductive chassis rails to earth ground to provide a path for connecting shields to earth ground

- Tighten all front panel screws

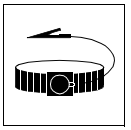
Hardware Preparation and Installation 2

Introduction

This chapter provides unpacking instructions, hardware preparation, and installation instructions for the TMCPN710 transition module, and the Compact FLASH memory cards.

Unpacking the Hardware

Use ESD



Wrist Strap

The TMCPN710 is packed in an anti-static wrapper to protect it from static discharge. Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when handling the equipment. Electronic components can be extremely sensitive to electro-static discharge (ESD). After removing the board from the protective wrapper, place it component side up on a grounded, static-free surface. Do not slide the board over any surface.

Unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping of the equipment.

2

Installing the Compact FLASH Modules

The Compact FLASH memory cards (CFLASH-xxx) plug into connectors J15 and J16 on the TMCPN710 transition module. Connector J15 is configured for a master IDE device and J16 is configured for a slave IDE device.

Install the Compact FLASH on the TMCPN710 transition module per the following procedure:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the compact PCI module.



Caution

Inserting or removing modules in a non-hot swap chassis with power applied may result in damage to module components. The TMCPN710 is not a hot swap board, but it may be installed in a hot swap chassis with power applied, if the corresponding MCPN750 is removed before the TMCPN710 is installed.



Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. Carefully remove the TMCPN710 from its CompactPCI card slot and lay it flat, with connectors J3, J4 and J5 facing you.
4. Slide the Compact FLASH memory card into the J15 or J16 connector making sure that pin 1 on the card aligns with pin 1 of J15 or J16. If you are installing two Compact FLASH devices, install the other one at this time.

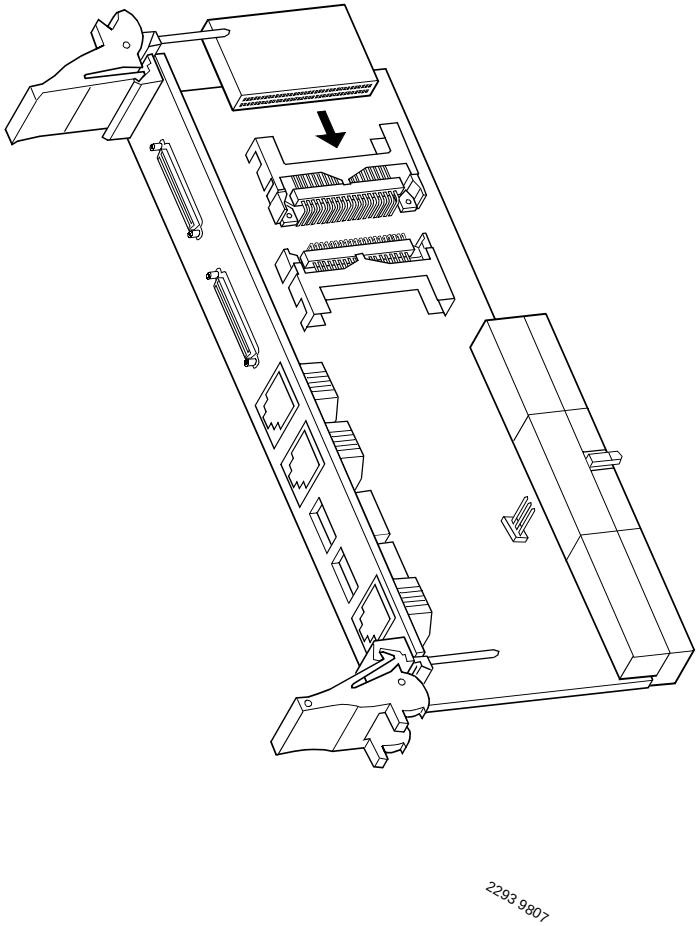


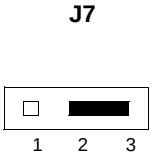
Figure 2-1. Installing Compact FLASH onto the TMCPN710 Transition Module

Note Do not force the Compact FLASH module onto the transition module. Compact FLASH modules must be installed prior to inserting the Transition Module into the system chassis.

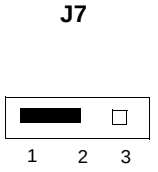
5. Reinstall the TMCPN710 assembly in its proper card slot. Be sure the module is well seated in the backplane connectors. Do not damage or bend connector pins.
6. Replace the chassis or system cover(s), reconnect the system to the AC or DC power source, and turn the equipment power on.

COM1 Port Jumper Installation

Jumper J7 on the TMCPN710 Transition Module must be configured to enable COM1 on either the transition module or the processor board. To enable the COM1 port on the transition module, connect pins 2-3 of J7. To enable COM1 on the processor board, connect pins 1-2 of J7.



Enable COM1 on TMCPN710



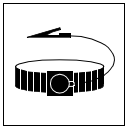
Enable COM1 on MCPN750

Note If the TMCPN710 board does not have a J7 jumper then COM1 is automatically enabled on the MCPN750.

Installing the Transition Module

Installation of the TMCPN710 transition module is accomplished from the rear of the system chassis. Any rear panel must be removed in order to see the backplane and install the transition module.

Use ESD



Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing boards in a system chassis. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to ESD. Place the board flat on a grounded, static-free surface, component-side up. Do not slide the board over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by attaching the ESD wrist strap to an unpainted metal part of the system chassis.

Install the TMCPN710 in the system chassis per the following procedure.

1. Attach an ESD strap to your wrist. Attach the other end of the strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the chassis backplane.



Caution

Inserting or removing modules with the power applied may result in damage to the module components. The TMCPN710 is not a hot swap board, but it may be installed in a hot swap chassis with power applied, if the corresponding MCPN750 is removed before the TMCPN710 board is installed.

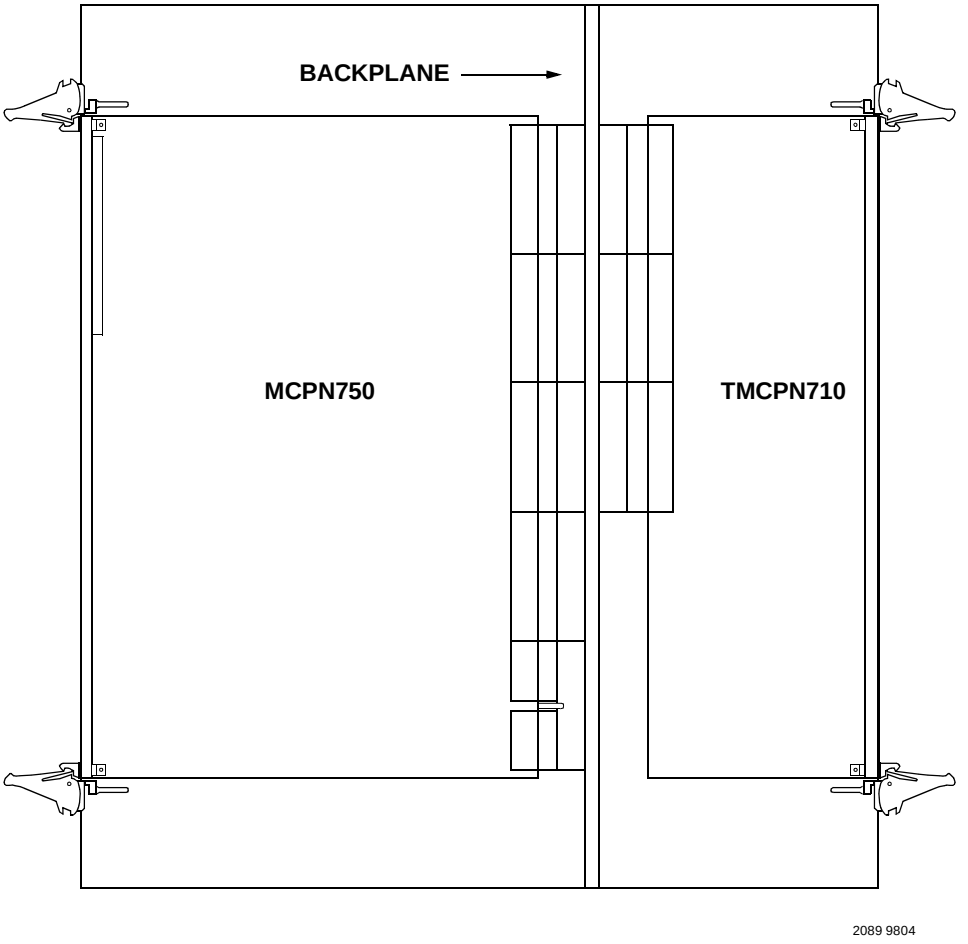


Figure 2-2. TMCPN710 Backplane Connections

Warning

Dangerous voltages, capable of causing death, are present in this equipment. use extreme caution when handling, testing, and adjusting.

Caution Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

3. With the TMCPN710 in the correct vertical position that matches the pin positioning of the corresponding MCPN750 board carefully slide the transition module into the appropriate slot and seat tightly into the backplane. Refer to Figure 1-7. TMCPN710/MCPN750 Mating Configuration for the correct board/connector orientation.
4. Secure in place with the screws provided, making good contact with the transverse mounting rails to minimize RF emissions.
5. Replace the chassis or system cover(s), making sure no cables are pinched. Cable the peripherals to the panel connectors, reconnect the system to the AC or DC power source, and turn the equipment power on.

Note Make sure there is good contact with the transverse mounting rails in order to minimize RF emissions.

Functional Description 3

Introduction

This chapter provides information on TMCPN710 transition module.

Circuitry

The TMCPN710 transition module contains a small amount of “house keeping” circuitry. Bulk capacitors are on the +5Vdc power source.

The block diagram for the TMCPN710 transition module is shown in Figure 3-1.

USB Port Fuses

Each USB port has a resettable polyswitch providing +5Vdc to the USB peripherals. Each polyswitch is rated at 1.1 Amps. However, the USB specification limits the current draw to 500 milliamps per port.

SROM

The TMCPN710 contains an I^2C SROM device that stores vital product data for the transition module. This information is accessible from the Falcon I^2C interface on the MCPN750. Refer to the *MCPN750 Programmers Reference Guide* for details.

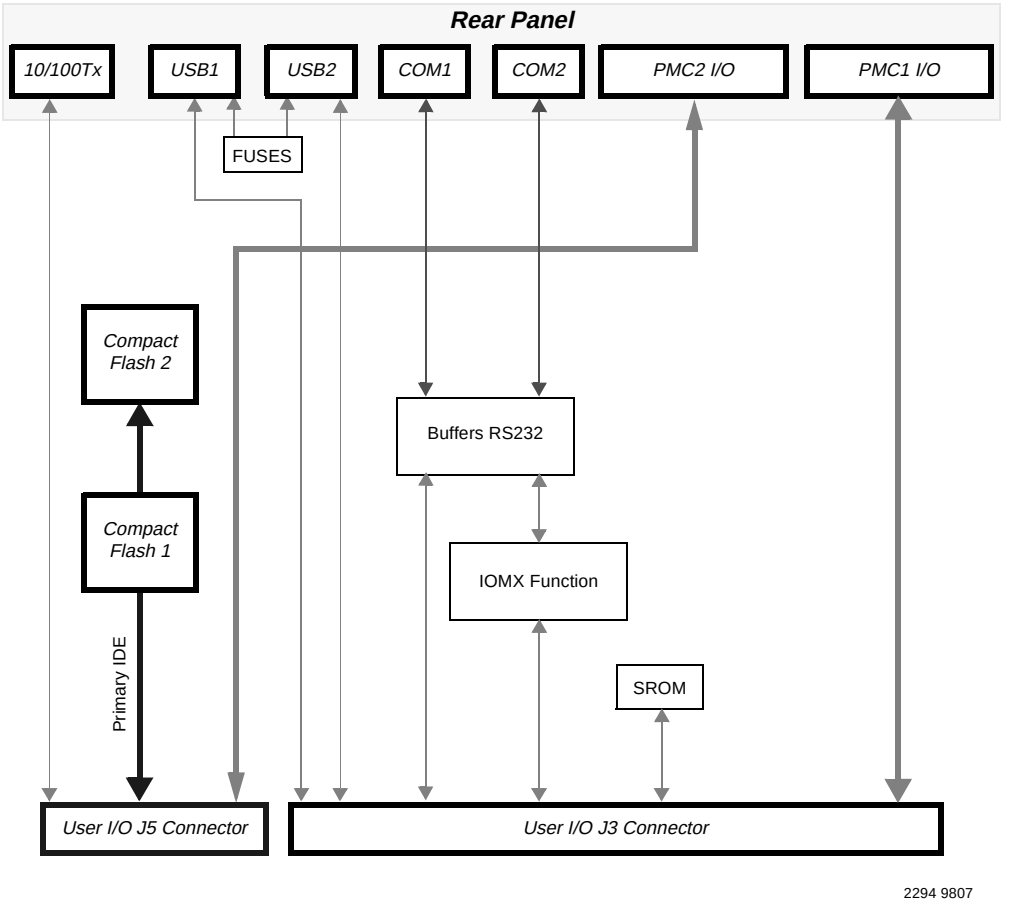


Figure 3-1. TMCPN710 Transition Module Block Diagram

Note On TMCPN710-001 models that mate with MCPN750-1xxx models, a J4 connector is present for mechanical alignment purposes only. There are no pin assignments or functionality on this connector.

Signal Multiplexing (MX)

Because of a limited number of pins on the J3 connector, both the MCPN750 processor board and the transition module multiplex and de-multiplex some of the Serial I/O signals. This function, called IOMX is transparent to the software and the user.

Four pins are used for the signal multiplexing:

- MXCLK
- MXSYNC#
- MXDO
- MXDI

Sixteen Time Slots are defined and allocated. The signal multiplexing sequences are listed in Table 3-1.

Table 3-1. Signal Multiplexing Sequence

MXDO (from the MCPN750)		**MXDI (from the TMCPN710)**	
Time Slot	**Signal Name**	**Time Slot**	**Signal Name**
0	RTS3	0	CTS3
1	DTR3	1	DSR3
2	RTS1	2	DCD3
3	RTS2	3	CTS1
4	RTS4	4	RI3
5	DTR4	5	CTS4
6	Reserved	6	DSR4
7	Reserved	7	DCD4
8	Reserved	8	CTS2
9	DTR1	9	RI4
10	DTR2	10	RI1
11	Reserved	11	DSR1

Table 3-1. Signal Multiplexing Sequence (Continued)

MXDO (from the MCPN750)		**MXDI (from the TMCPN710)**	
12	Reserved	12	DCD1
13	Reserved	13	RI1
14	Reserved	14	DSR2
15	Reserved	15	DCD2

MXCLK is the 10MHz bit clock for the time-multiplexed data lines, MXDO and MXDI.

MXSYNC# is asserted for one bit time at Time Slot 15 by the MCPN750. MXSYNC# is used by the transition module to synchronize with the MCPN750.

MXDO is the time-multiplexed output line from the main board and MXDI is the time-multiplexed line from the TMCPN710 transition module. A 16-to-1 multiplexing scheme is used with a 10MHz bit rate.

MXSYNC# is clocked out using the falling edge of MXCLK and MXDO is clocked out with the rising edge of the MXCLK. MXDI is sampled at the rising edge of MXCLK (the transition module synchronizes MXDI with MXCLK's rising edge).

The timing relationships among MXCLK, MXSYNC#, MXDO, and MXDI are illustrated in Figure 3-2.

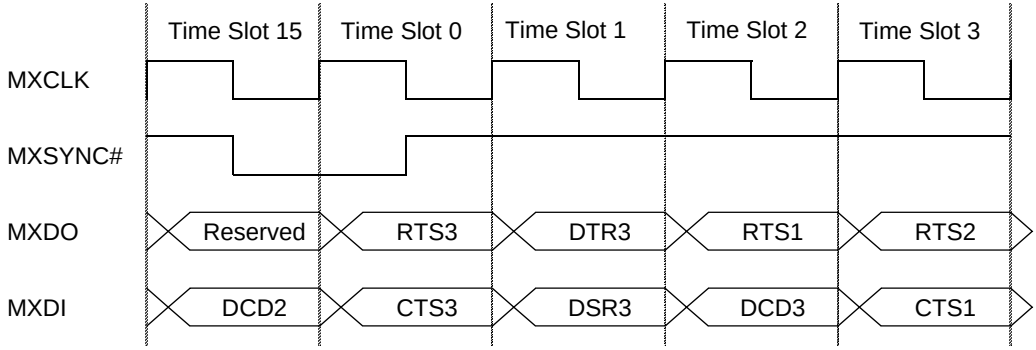


Figure 3-2. Multiplex Signal Timing Chart

Port Configuration Diagrams

COM1 and COM2 Asynchronous Serial Ports

The asynchronous serial port (COM1 and COM2) configuration is shown in Figure 3-3.

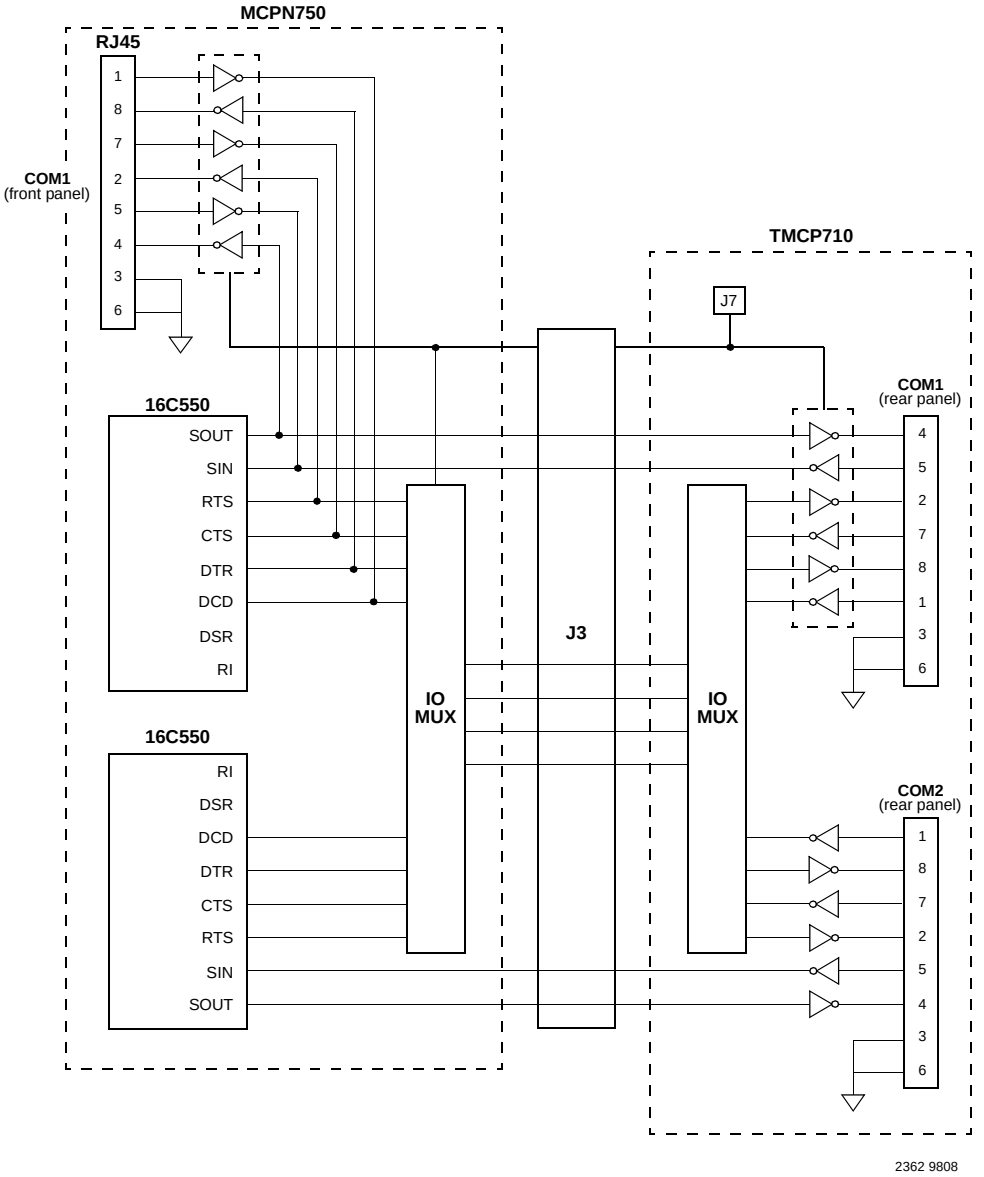


Figure 3-3. DTE Port Configuration (COM1 and COM2)

COM3 and COM4 Asynchronous Serial Ports

The asynchronous serial port (Port 3 and Port 4) interface configuration diagram is shown below. The signals for COM3 and COM4 serial ports are routed to onboard headers J11 and J14. These headers are intended for debug purposes only.

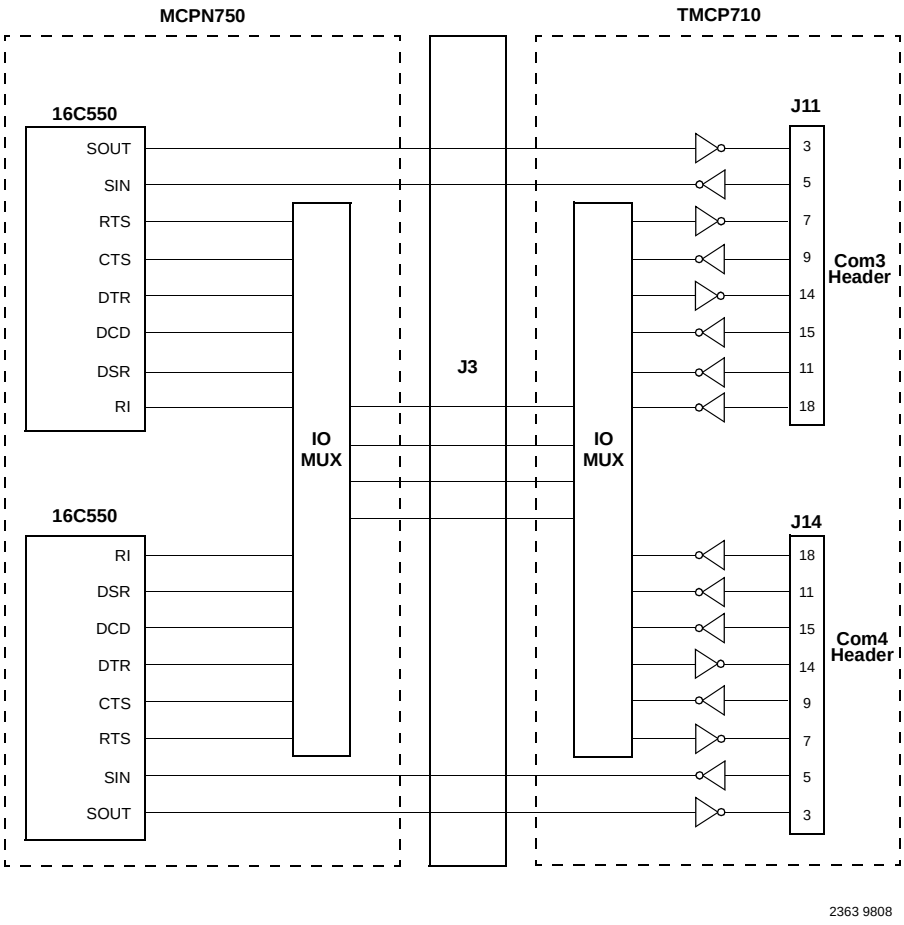


Figure 3-4. TMCPN710 Serial Ports 3 and 4

Connector Pin Assignments

4

Introduction

This chapter provides the pin assignments for the J3/J5 connectors and front panel port connectors on the TMCPN710 transition module, as well as for the IDE CompactFLASH memory interface, and PMC I/O connectors.

TMCPN710 Transition Module Connectors

J3/J4/J5 Connectors

I/O signals and power are provided to the TMCPN710 from the MCPN750 through CompactPCI connectors J3 and J5. The J4 connector is for physical alignment purposes only and has no functional pin connections or assignments.

The pin assignments and signal mnemonics for connector J3 of the TMCPN710 transition module is listed in Table 4-1. The pin assignments for connector J5 is listed in Table 4-2. No pin assignments are listed for J4.

CompactPCI User I/O Connector J3

Connector J3 is a 95 pin AMP Z-pack 2mm hard metric type B connector. This connector routes the I/O signals for the PMC1 I/O, serial ports, and USB ports. The pin assignments for J3 are as follows (outer row F is assigned and used as ground pins but is not shown in the table):

Table 4-1: J3 User I/O Connector

	ROW A	ROW B	ROW C	ROW D	ROW E	
19	COM3TD	+12V	-12V	COM4RD	UDATA1P	19
18	COM3RD	GND	USBV1_OK	COM4TD	UDATA1N	18
17	TMCOM1_L	MXCLK	MXDI	MXSYNC_L	MXDO	17
16	COM1TD	GND	I2CSCL	I2CSDA	UDATA0P	16
15	COM1RD	COM2RD	COM2TD	USBV0_OK	UDATA0N	15
14	+3.3V	+3.3V	+3.3V	+5V	+5V	14
13	PMC1IO5	PMC1IO4	PMC1IO3	PMC1IO2	PMC1IO1	13
12	PMC1IO10	PMC1IO9	PMC1IO8	PMC1IO7	PMC1IO6	12
11	PMC1IO15	PMC1IO14	PMC1IO13	PMC1IO12	PMC1IO11	11
10	PMC1IO20	PMC1IO19	PMC1IO18	PMC1IO17	PMC1IO16	10
9	PMC1IO25	PMC1IO24	PMC1IO23	PMC1IO22	PMC1IO21	9
8	PMC1IO30	PMC1IO29	PMC1IO28	PMC1IO27	PMC1IO26	8
7	PMC1IO35	PMC1IO34	PMC1IO33	PMC1IO32	PMC1IO31	7
6	PMC1IO40	PMC1IO39	PMC1IO38	PMC1IO37	PMC1IO36	6
5	PMC1IO45	PMC1IO44	PMC1IO43	PMC1IO42	PMC1IO41	5
4	PMC1IO50	PMC1IO49	PMC1IO48	PMC1IO47	PMC1IO46	4
3	PMC1IO55	PMC1IO54	PMC1IO53	PMC1IO52	PMC1IO51	3
2	PMC1IO60	PMC1IO59	PMC1IO58	PMC1IO57	PMC1IO56	2
1	VIO (+5V)	PMC1IO64	PMC1IO63	PMC1IO62	PMC1IO61	1

Signal Descriptions

PMCIO:

PMC1IO(1:64) - PMC1 I/O signals 1 through 64

Universal Serial Bus (USB 0 & 1). USB levels:

UDATAn + - high signal of differential data for USB channel
UDATAn - - low signal of differential data for USB channel

Serial COM Ports 1-4:

COMnTD - COM Port n Transmit Data Output
COMnRD - COM Port n Receive Data Input

Miscellaneous:

TMCOM1_L - Used to select COM1 active on processor board or on Transition Module

MXCLK - multiplexed I/O signal clock, 10 MHz

MXSYNC_L - multiplexed I/O sync signal

MXDI - multiplexed I/O data in signal from transition module

MXDO - multiplexed I/O data out signal to transition module

I2CSCL - I^2C Serial Clock for Transition Module SROM

I2CSDA - I^2C Serial Data for Transition Module SROM

USBV0_OK - USB Port 0 Voltage Monitor

USBV1_OK - USB Port 1 Voltage Monitor

Connector J4

Connector J4 is a 110 pin AMP Z-pack 2mm hard metric type A connector installed on both the processor board and the Transition Module for mechanical alignment purposes only. The keying tabs in the Type A connector assist with alignment of pins in the backplane connector during insertion of the boards. No signals are connected to the J4 pins except the ground pins in Row F of the outer shield, which are connected to the board logic ground.

User I/O Connector J5

Connector J5 is a 110 pin AMP Z-pack 2mm hard metric type B connector. This connector routes the I/O signals for the PMC2 I/O signals, the IDE interface, and the optional ethernet port. The pin assignments for J5 on the processor board and the Transition Module are as follows (note the outer row F is assigned and used as ground pins but is not shown in the table):

Table 4-2: J5 User I/O Connector

	ROW A	ROW B	ROW C	ROW D	ROW E	
22	DRESET_L	TXP	RXP	No Connect	No Connect	22
21	INTRQA	TXN	RXN	No Connect	No Connect	21
20	CS1FXA_L	CS3FXA_L	DA2	No Connect	No Connect	20
19	DMACKA_L	DIORDYA	DA1	No Connect	No Connect	19
18	DIOWA_L	DA0	GND	No Connect	No Connect	18
17	GND	DD14	DD15	DIORA_L	DMARQA	17
16	DD9	DD10	DD11	DD12	DD13	16
15	DD5	DD6	GND	DD7	DD8	15
14	DD0	DD1	DD2	DD3	DD4	14
13	PMC2IO5	PMC2IO4	PMC2IO3	PMC2IO2	PMC2IO1	13
12	PMC2IO10	PMC2IO9	PMC2IO8	PMC2IO7	PMC2IO6	12
11	PMC2IO15	PMC2IO14	PMC2IO13	PMC2IO12	PMC2IO11	11
10	PMC2IO20	PMC2IO19	PMC2IO18	PMC2IO17	PMC2IO16	10
9	PMC2IO25	PMC2IO24	PMC2IO23	PMC2IO22	PMC2IO21	9
8	PMC2IO30	PMC2IO29	PMC2IO28	PMC2IO27	PMC2IO26	8
7	PMC2IO35	PMC2IO34	PMC2IO33	PMC2IO32	PMC2IO31	7
6	PMC2IO40	PMC2IO39	PMC2IO38	PMC2IO37	PMC2IO36	6
5	PMC2IO45	PMC2IO44	PMC2IO43	PMC2IO42	PMC2IO41	5
4	PMC2IO50	PMC2IO49	PMC2IO48	PMC2IO47	PMC2IO46	4
3	PMC2IO55	PMC2IO54	PMC2IO53	PMC2IO52	PMC2IO51	3
2	PMC2IO60	PMC2IO59	PMC2IO58	PMC2IO57	PMC2IO56	2
1	TMPRSNT_L	PMC2IO64	PMC2IO63	PMC2IO62	PMC2IO61	1

Signal Descriptions

PMCIO:

PMC2IO (1:64) - PMC 2 I/O signals 1 through 64

EIDE Primary Port (ATA-2):

DMARQA - DMA request

DMACKA_L - DMA acknowledge

DIORA_L - I/O read

DIOWA_L - I/O write

DIORDYA - indicates drive ready for I/O

DD (15:0) - IDE data lines

CS1FXA_L - chip select drive 0 or command register block select

CS3FXA_L - chip select drive 1 or command register block select

DA (2:0) - drive register and data port address lines

DRESET_L - drive reset

Ethernet:

TDP - high side of differential transmit data

TDN - low side of differential transmit data

RDP - high side of differential receive data

RDN - low side of differential receive data

Miscellaneous:

TMPRSNT_L - indicates that the Transition Module is installed

Transition Board COM1 Connector

An RJ45 connector is located on the rear panel of the TMCPN710 Transition Module to provide the interface to the COM1 serial port. The TMCOM1 signal jumper on the Transition Module must be installed to enable COM1 on the Transition Module. The pin assignments for this connector is as follows:.

Table 4-3: COM1 Connector

Pin	Signal
1	DCD1
2	RTS1
3	GND
4	TXD1
5	RXD1
6	GND
7	CTS1
8	DTR1

Transition Board COM2 Connector

An RJ45 connector is located on the rear panel of the TMCPN710 Transition Module to provide the interface to the COM2 serial port. The pin assignments for this connector is as follows:

Table 4-4: COM2 Connector

Pin	Signal
1	DCD2
2	RTS2
3	GND
4	TXD2
5	RXD2
6	GND
7	CTS2
8	DTR2

Transition Board COM3 Header (J11)

The signals for the COM3 port are routed to a 26 pin header. The pin assignments for this header are as follows:

Table 4-5: COM3/COM4 Headers

1	NC	NC	2
3	TXD	NC	4
5	RXD	NC	6
7	RTS	NC	8
9	CTS	NC	10
11	DSR	NC	12
13	GND	DTR	14

Table 4-5: COM3/COM4 Headers

15	NC	DCD	16
17	NC	RI	18
19	NC	NC	20
21	NC	NC	22
23	NC	NC	24
25	NC	NC	26

Transition Board COM4 Header (J14)

Same as above.

Ethernet Connector

An RJ45 connector is located on the rear panel of the TMCPN710 Transition Module to provide optional routing to the 10Base-T/100Base-TX ethernet port (J13) using an alternate build option of the MCPN750. Contact your local Motorola Sales office for details.

IDE Compact FLASH Interface

The TMCPN710 provides 50-pin connectors (J15 and J16) for access to the Compact FLASH memory cards via the primary EIDE channel. The pin assignments and signal mnemonics for this connector are listed in the following table. Connector J15 is configured as the master EIDE interface, while J16 is configured as the slave EIDE interface.

Table 4-6: IDE Compact FLASH Connectors (J15 and J16)

Pin	Signal	Signal	Pin
1	GND	DD3	2
3	DD4	DD5	4
5	DD6	DD7	6
7	CS1FXA_L	GND	8

Table 4-6: IDE Compact FLASH Connectors (J15 and J16)

Pin	Signal	Signal	Pin
9	GND	GND	10
11	GND	GND	12
13	+5V	GND	14
15	GND	GND	16
17	GND	DA2	18
19	DA1	DA0	20
21	DD0	DD1	22
23	DD2	No Connect	24
25	CD2_L	CD1_L	26
27	DD11	DD12	28
29	DD13	DD14	30
31	DD15	CS3FXA_L	32
33	No Connect	DIORA_L	34
35	DIOWA_L	No Connect	36
37	INTRQA	+5V	38
39	Master/Slave	No Connect	40
41	DRESET_L	DIORDYA	42
43	No Connect	No Connect	44
45	DASP	PDIAG	46
47	DD8	DD9	48
49	DD10	GND	50

PMC I/O Connectors

Two 68-pin.08mm CHAMP connectors located on the TMCPN710 Transition Module rear panel provide I/O for each of the PMCs on the processor board. The pin assignments and signal mnemonics for these connectors are listed below.

Table 4-7: TM P 1 and 2 I/O Connector (J1 & J2)

Pin	Signal	Signal	Pin
1	PMCIO1	PMCIO32	35
2	PMCIO2	PMCIO33	36
3	PMCIO3	PMCIO34	37
4	PMCIO4	PMCIO35	38
5	PMCIO5	PMCIO36	39
6	GND	PMCIO37	40
7	PMCIO6	PMCIO38	41
8	PMCIO7	PMCIO39	42
9	PMCIO8	PMCIO40	43
10	PMCIO9	PMCIO41	44
11	PMCIO10	PMCIO42	45
12	PMCIO11	PMCIO43	46
13	PMCIO12	PMCIO44	47
14	PMCIO13	PMCIO45	48
15	PMCIO14	PMCIO46	49
16	PMCIO15	GND	50
17	PMCIO16	PMCIO47	51
18	PMCIO17	PMCIO48	52
19	PMCIO18	PMCIO49	53
20	PMCIO19	PMCIO50	54

Table 4-7: TM P 1 and 2 I/O Connector (J1 & J2) (Continued)

Pin	Signal	Signal	Pin
21	GND	PMCIO51	55
22	PMCIO20	PMCIO52	56
23	PMCIO21	PMCIO53	57
24	PMCIO22	PMCIO54	58
25	PMCIO23	PMCIO55	59
26	PMCIO24	PMCIO56	60
27	PMCIO25	PMCIO57	61
28	PMCIO26	PMCIO58	62
29	PMCIO27	PMCIO59	63
30	GND	PMCIO60	64
31	PMCIO28	PMCIO61	65
32	PMCIO29	PMCIO62	66
33	PMCIO30	PMCIO63	67
34	PMCIO31	PMCIO64	68

Related Documentation A

Motorola Computer Group Documents

This product ships with an installation and user manual, which includes installation instructions, cable connections, jumper configuration settings, and any other information needed to install and operate this transition module in conjunction with the MCPN750 SBC product family.

To obtain additional information about programming or installation instructions of the MCPN750, as well as the operational relationship between the MCPN750 and the TMCPN710 Transition Module, select one of the following ordering options and refer to the document list in Table A-1:

- Contact your local Motorola sales office,
- Access the World Wide Web site listed on the back cover of this and other MCG manuals and select “Product Literature” (PDF files on most manuals are available from the web site), or
- (USA and Canada only) —Contact the Literature Center via phone or fax at the numbers listed under *Product Literature* at MCG’s World Wide Web site

Any supplements issued for a specific revision of a manual or guide are furnished with that document. The “type” and “revision level” of a specific manual are indicated by the last three characters of the document number, such as “/IH2” (the second revision of an installation manual); a supplement bears the same number as a manual but has two additional characters that indicate the revision level of the supplement, for example “/IH2A1” (the first supplement to the second edition of the installation manual).

Table A-1. Motorola Computer Group Documents

Document Title	Publication Number
MCPN750 CompactPCI Single Board Computer Installation and Use	MCPN750A/IH
MCPN750 CompactPCI Single Board Computer Programmer's Reference Guide	MCPN750A/PG
PPCBug Firmware Package User's Manual (Parts 1 and 2)	PPCBUGA1/UM PPCBUGA2/UM
PPC1Bug Diagnostics Manual	PPCDIAA/UM

Manufacturers' Documents

Additional component or software information is available directly from the manufacturer. Please note that the revision levels of the documents are subject to change without notice. These documents are listed in Table A-2, along with the appropriate ordering information.

Table A-2. Manufacturers' Documents

Document Title and Source	Publication Number
ATMEL Nonvolatile Memory Data Book Atmel Corporation 2325 Orchord Parkway San Jose, CA 95131 Telephone: (408) 441-0311 FAX: (408) 436-4300 Website: http://www.atmel.com	AT24C04

Related Specifications

Refer to the following table, for product specifications on this and related products. The document name, number and ordering source is provided. Please note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Table A-3. Related Specifications

Document Title and Source	Publication Number
IEEE - Common Mezzanine Card Specification (CMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386.1
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.1 PCI Special Interest Group 2575 NE Kathryn St. #17 Hillsboro, OR 97124 Telephone: (800) 433-5177 (inside the U.S.) or (503) 693-6232 (outside the U.S.) FAX: (503) 693-8344	PCI Local Bus Specification

Table A-3. Related Specifications (Continued)

Document Title and Source	Publication Number
PowerPC™ Microprocessor Common Hardware Reference Platform: A System Architecture (CHRP), Version 1.0 Literature Distribution Center for Motorola Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com OR APDA, Apple Computer, Inc. P.O. Box 319 Buffalo, NY 14207 Telephone: (800) 282-2732 FAX: (716) 871-6511 OR IBM 1580 Route 52, Bldg. 504 Hopewell Junction, NY 12533-6531 Telephone: (800) PowerPC OR Morgan Kaufmann Publishers, Inc. 340 Pine Street, Sixth Floor San Francisco, CA 94104-3205, USA Telephone: (415) 392-2665 FAX: (415) 982-2665	TB338/D MPRPPCHRP-01 ISBN 1-55860-394-8
PowerPC Reference Platform (PRP) Specification, Third Edition, Version 1.0, Volumes I and II International Business Machines Corporation Power Personal Systems Architecture 11400 Burnet Rd. Austin, TX 78758-3493 Document/Specification Ordering Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 Telephone: 708-296-9332	MPR-PPC-RPU-02

Table A-3. Related Specifications (Continued)

Document Title and Source	Publication Number
IEEE Standard for Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	IEEE 802.3
Information Technology - Local and Metropolitan Networks - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Global Engineering Documents 15 Inverness Way East Englewood, CO 80112-5704 Telephone: 1-800-854-7179 Telephone: (303) 792-2181 *(This document can also be obtained through the national standards body of member countries.)*	ISO/IEC 8802-3
Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange (EIA-232-D) Electronic Industries Association Engineering Department 2001 Eye Street, N.W. Washington, D.C. 20006	ANSI/EIA-232-D Standard
Compact PCI Specification PCI Industrial Manufacturers Group (PICMG) 401 Edgewater Pl, Suite 500 Wakefield, MA 01880 Telephone: 781-246-9318 Fax: 781-224-1239	CPCI Rev. 2.1 Dated 9/2/97
PCI-to-PCI Bridge Specification PCI-ISA Specification PCI Industrial Manufacturers Group (PICMG) 401 Edgewater Pl, Suite 500 Wakefield, MA 01880 Telephone: 781-246-9318 Fax: 781-224-1239	Rev. 1.02 Rev. 2.0

Glossary

Abbreviations, Acronyms, and Terms to Know

This glossary defines some of the abbreviations, acronyms, and key terms used in this document.

10Base-5 An Ethernet implementation in which the physical medium is a doubly shielded, 50-ohm coaxial cable capable of carrying data at 10 Mbps for a length of 500 meters (also referred to as thicknet). Also known as thick Ethernet.

10Base-2 An Ethernet implementation in which the physical medium is a single-shielded, 50-ohm RG58A/U coaxial cable capable of carrying data at 10 Mbps for a length of 185 meters (also referred to as AUI or thinnet). Also known as thin Ethernet.

10Base-T An Ethernet implementation in which the physical medium is an unshielded twisted pair (UTP) of wires capable of carrying data at 10 Mbps for a maximum distance of 185 meters. Also known as twisted-pair Ethernet.

100Base-TX An Ethernet implementation in which the physical medium is an unshielded twisted pair (UTP) of wires capable of carrying data at 100 Mbps for a maximum distance of 100 meters. Also known as fast Ethernet.

ACIA **A**synchronous **C**ommunications **I**nterface **A**dapter

AIX **A**dvanced **I**nteractive e**X**ecutive (IBM version of UNIX)

architecture The main overall design in which each individual hardware component of the computer system is interrelated. The most common uses of this term are 8-bit, 16-bit, or 32-bit architectural design systems.

ASCII **A**merican **S**tandard **C**ode for **I**nformation **I**nterchange. This is a 7-bit code used to encode alphanumeric information. In the IBM-compatible world, this is expanded to 8-bits to encode a total of 256 alphanumeric and control characters.

ASIC	**A**pplication-**S**pecific **I**ntegrated **C**ircuit
AUI	**A**ttachment **U**nit **I**nterface
BBRAM	Battery Backed-up Random Access Memory
bi-endian	Having big-endian and little-endian byte ordering capability.
big-endian	A byte-ordering method in memory where the address *n* of a word corresponds to the most significant byte. In an addressed memory word, the bytes are ordered (left to right) 0, 1, 2, 3, with 0 being the most significant byte.
BIOS	**B**asic **I**nput/**O**utput **S**ystem. This is the built-in program that controls the basic functions of communications between the processor and the I/O (peripherals) devices. Also referred to as ROM BIOS.
BLT	**BL**ock **T**ransfer
board	The term more commonly used to refer to a PCB (printed circuit board). Basically, a flat board made of nonconducting material, such as plastic or fiberglass, on which chips and other electronic components are mounted. Also referred to as a circuit board or card.
bpi	**b**its **p**er **i**nch
bps	**b**its **p**er **s**econd
bus	The pathway used to communicate between the CPU, memory, and various input/output devices, including floppy and hard disk drives. Available in various widths (8-, 16-, and 32-bit), with accompanying increases in speed.
cache	A high-speed memory that resides logically between a central processing unit (CPU) and the main memory. This temporary memory holds the data and/or instructions that the CPU is most likely to use over and over again and avoids accessing the slower hard or floppy disk drive.
CAS	**C**olumn **A**ddress **S**trobe. The clock signal used in dynamic RAMs to control the input of column addresses.
CD	**C**ompact **D**isc. A hard, round, flat portable storage unit that stores information digitally.
CD-ROM	**C**ompact **D**isk **R**ead-**O**nly **M**emory

CFM	**C**ubic **F**eet per **M**inute
CHRP	See Common Hardware Reference Platform (CHRP).
CHRP-compliant	See Common Hardware Reference Platform (CHRP).
CHRP Spec	See Common Hardware Reference Platform (CHRP).
CIO	Counter/Timer and Parallel I/O unit (Zilog Z8536).
CISC	**C**omplex-**I**nstruction-**S**et **C**omputer. A computer whose processor is designed to sequentially run variable-length instructions, many of which require several clock cycles, that perform complex tasks and thereby simplify programming.
CODEC	**CO**der/**DEC**oder
Common Hardware Reference Platform (CHRP)	A specification published by the Apple, IBM, and Motorola which defines the devices, interfaces, and data formats that make up a CHRP-compliant system using a PowerPC processor.
CPU	**C**entral **P**rocessing **U**nit. The master computer unit in a system.
DCE	**D**ata **C**ircuit-terminating **E**quipment.
DLL	**D**ynamic **L**ink **L**ibrary. A set of functions that are linked to the referencing program at the time it is loaded into memory.
DMA	**D**irect **M**emory **A**ccess. A method by which a device may read or write to memory directly without processor intervention. DMA is typically used by block I/O devices.
DOS	**D**isk **O**perating **S**ystem
dpi	**d**ots **p**er **i**nch
DRAM	**D**ynamic **R**andom **A**ccess **M**emory. A memory technology that is characterized by extreme high density, low power, and low cost. It must be more or less continuously refreshed to avoid loss of data.
DTE	**D**ata **T**erminal **E**quipment.
ECC	**E**rror **C**orrection **C**ode
ECP	**E**xtended **C**apability **P**ort

EEPROM — **E**lectrically **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory. A memory storage device that can be written repeatedly with no special erasure fixture. EEPROMs do not lose their contents when they are powered down.

EIDE — Enhanced Intelligent Device Expansion

EISA (bus) — **E**xtended **I**ndustry **S**tandard **A**rchitecture (bus) (IBM). An architectural system using a 32-bit bus that allows data to be transferred between peripherals in 32-bit chunks instead of 16-bit or 8-bit that most systems use. With the transfer of larger bits of information, the machine is able to perform much faster than the standard ISA bus system.

EPP — **E**nhanced **P**arallel **P**ort

EPROM — **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory. A memory storage device that can be written once (per erasure cycle) and read many times.

ESCC — **E**nhanced **S**erial **C**ommunication **C**ontroller

ESD — **E**lectro-**S**tatic **D**ischarge/Damage

Ethernet — A local area network standard that uses radio frequency signals carried by coaxial cables.

Falcon — A DRAM controller chip developed by Motorola for a series of PowerPC board level products. It is intended to be used in sets of two to provide the necessary interface between the Power PC60*x* bus and the 144-bit ECC DRAM (system memory array) and/or ROM/Flash.

fast Ethernet — See 100Base-TX.

FDC — **F**loppy **D**isk **C**ontroller

FIFO — **F**irst-**I**n, **F**irst-**O**ut. A memory that can temporarily hold data so that the sending device can send data faster than the receiving device can accept it. The sending and receiving devices typically operate asynchronously.

firmware — The program or specific software instructions that have been more or less permanently burned into an electronic component, such as a ROM (read-only memory) or an EPROM (erasable programmable read-only memory).

frame	One complete television picture frame consists of 525 horizontal lines with the NTSC system. One frame consists of two Fields.
graphics controller	On EGA and VGA, a section of circuitry that can provide hardware assist for graphics drawing algorithms by performing logical functions on data written to display memory.
HAL	**H**ardware **A**bstraction **L**ayer. The lower level hardware interface module of the Windows NT operating system. It contains platform specific functionality.
hardware	A computing system is normally spoken of as having two major components: hardware and software. Hardware is the term used to describe any of the physical embodiments of a computer system, with emphasis on the electronic circuits (the computer) and electromechanical devices (peripherals) that make up the system.
HCT	**H**ardware **C**onformance **T**est. A test used to ensure that both hardware and software conform to the Windows NT interface.
I/O	**I**nput/**O**utput
IBC	PCI/**I**SA **B**ridge **C**ontroller
IDC	**I**nsulation **D**isplacement **C**onnector
IDE	**I**ntelligent **D**evice **E**xpansion
IEEE	**I**nstitute of **E**lectrical and **E**lectronics **E**ngineers
IQ Signals	Similar to the color difference signals (R-Y), (B-Y) but using different vector axis for encoding or decoding. Used by some USA TV and IC manufacturers for color decoding.
ISA (bus)	**I**ndustry **S**tandard **A**rchitecture (bus). The de facto standard system bus for IBM-compatible computers until the introduction of VESA and PCI. Used in the reference platform specification. (IBM)
ISASIO	**ISA S**uper **I**nput/**O**utput device
ISDN	**I**ntegrated **S**ervices **D**igital **N**etwork. A standard for digitally transmitting video, audio, and electronic data over public phone networks.
LAN	**L**ocal **A**rea **N**etwork
LED	**L**ight-**E**mitting **D**iode
LFM	**L**inear **F**eet per **M**inute

little-endian	A byte-ordering method in memory where the address *n* of a word corresponds to the least significant byte. In an addressed memory word, the bytes are ordered (left to right) 3, 2, 1, 0, with 3 being the most significant byte.
MBLT	**M**ultiplexed **BL**ock **T**ransfer
MCA (bus)	**M**icro **C**hannel **A**rchitecture
MCG	**M**otorola **C**omputer **G**roup
MFM	**M**odified **F**requency **M**odulation
MIDI	**M**usical **I**nstrument **D**igital **I**nterface. The standard format for recording, storing, and playing digital music.
MPC	**M**ultimedia **P**ersonal **C**omputer
MPC750	Motorola's component designation for the PowerPC 750 microprocessor.
MPIC	**M**ulti-**P**rocessor **I**nterrupt **C**ontroller
MPU	**M**icro**P**rocessing **U**nit
MTBF	**M**ean **T**ime **B**etween **F**ailures. A statistical term relating to reliability as expressed in power on hours (poh). It was originally developed for the military and can be calculated several different ways, yielding substantially different results. The specification is based on a large number of samplings in one place, running continuously, and the rate at which failure occurs. MTBF is not representative of how long a device, or any individual device is likely to last, nor is it a warranty, but rather, of the relative reliability of a family of products.
multisession	The ability to record additional information, such as digitized photographs, on a CD-ROM after a prior recording session has ended.
nonvolatile memory	A memory in which the data content is maintained whether the power supply is connected or not.
NTSC	**N**ational **T**elevision **S**tandards **C**ommittee (USA)
NVRAM	**N**on-**V**olatile **R**andom **A**ccess **M**emory
OEM	**O**riginal **E**quipment **M**anufacturer
OMPAC	**O**ver - **M**olded **P**ad **A**rray **C**arrier

OS	**O**perating **S**ystem. The software that manages the computer resources, accesses files, and dispatches programs.
OTP	**O**ne-**T**ime **P**rogrammable
parallel port	A connector that can exchange data with an I/O device eight bits at a time. This port is more commonly used for the connection of a printer to a system.
PBC	Peripheral Bus Controller (PCI-to-ISA Bridge)
PCI (local bus)	**P**eripheral **C**omponent **I**nterconnect (local bus) (Intel). A high-performance, 32-bit internal interconnect bus used for data transfer to peripheral controller components, such as those for audio, video, and graphics.
PCMCIA (bus)	**P**ersonal **C**omputer **M**emory **C**ard **I**nternational **A**ssociation (bus). A standard external interconnect bus which allows peripherals adhering to the standard to be plugged in and used without further system modification.
PCR	**P**CI **C**onfiguration **R**egister
PHB	**P**CI **H**ost **B**ridge
PDS	**P**rocessor **D**irect **S**lot
physical address	A binary address that refers to the actual location of information stored in secondary storage.
PIB	**P**CI-to-**I**SA **B**ridge
PLL	**P**hase-**L**ocked **L**oop
PMC	**P**CI **M**ezzanine **C**ard
POWER	**P**erformance **O**ptimized **W**ith **E**nhanced **R**ISC architecture (IBM)
PowerPC™	The trademark used to describe the **P**erformance **O**ptimized **W**ith **E**nhanced **R**ISC microprocessor architecture for **P**ersonal **C**omputers developed by the IBM Corporation. PowerPC is superscalar, which means it can handle more than one instruction per clock cycle. Instructions can be sent simultaneously to three types of independent execution units (branch units, fixed-point units, and floating-point units), where they can execute concurrently, but finish out of order. PowerPC is used by Motorola, Inc. under license from IBM.

PowerPC 750™ The fourth implementation of the PowerPC family of microprocessors. This CPU incorporates a memory management unit with a 64-entry buffer and a 64KB (instruction and data) cache. It provides a selectable 32-bit or 64-bit data bus and a separate 32-bit address bus. PowerPC 750 is used by Motorola, Inc. under license from IBM.

PowerPC Reference Platform (PRP) A specification published by the IBM Power Personal Systems Division which defines the devices, interfaces, and data formats that make up a PRP-compliant system using a PowerPC processor.

PROM **P**rogrammable **R**ead-**O**nly **M**emory

PS/2 **P**ersonal **S**ystem/**2** (IBM)

QFP **Q**uad **F**lat **P**ackage

RAM **R**andom-**A**ccess **M**emory. The temporary memory that a computer uses to hold the instructions and data currently being worked with. All data in RAM is lost when the computer is turned off.

RAS **R**ow **A**ddress **S**trobe. A clock signal used in dynamic RAMs to control the input of the row addresses.

Raven The PowerPC-to-PCI local bus bridge chip developed by Motorola for the MVME2600 and MVME3600 series of boards. It provides the necessary interface between the PowerPC 60x bus and the PCI bus, and acts as interrupt controller.

Reduced-Instruction-Set Computer (RISC) A computer in which the processor's instruction set is limited to constant-length instructions that can usually be executed in a single clock cycle.

RFI **R**adio **F**requency **I**nterference

RGB The three separate color signals: **R**ed, **G**reen, and **B**lue. Used with color displays, an interface that uses these three color signals as opposed to an interface used with a monochrome display that requires only a single signal. Both digital and analog RGB interfaces exist.

RISC See Reduced Instruction Set Computer (RISC).

ROM **R**ead-**O**nly **M**emory

RTC	**R**eal-**T**ime **C**lock
SBC	**S**ingle **B**oard **C**omputer
SCSI	**S**mall **C**omputer **S**ystems **I**nterface. An industry-standard high-speed interface primarily used for secondary storage. SCSI-1 provides up to 5 Mbps data transfer.
SCSI-2 (Fast/Wide)	An improvement over plain SCSI; and includes command queuing. Fast SCSI provides 10 Mbps data transfer on an 8-bit bus. Wide SCSI provides up to 40 Mbps data transfer on a 16- or 32-bit bus.
serial port	A connector that can exchange data with an I/O device one bit at a time. It may operate synchronously or asynchronously, and may include start bits, stop bits, and/or parity.
SIM	**S**erial **I**nterface **M**odule
SIMM	**S**ingle **I**nline **M**emory **M**odule. A small circuit board with RAM chips (normally surface mounted) on it designed to fit into a standard slot.
SIO	**S**uper **I/O** controller
SMP	**S**ymmetric **M**ulti**P**rocessing. A computer architecture in which tasks are distributed among two or more local processors.
SMT	**S**urface **M**ount **T**echnology. A method of mounting devices (such as integrated circuits, resistors, capacitors, and others) on a printed circuit board, characterized by not requiring mounting holes. Rather, the devices are soldered to pads on the printed circuit board. Surface-mount devices are typically smaller than the equivalent through-hole devices.
software	A computing system is normally spoken of as having two major components: hardware and software. Software is the term used to describe any single program or group of programs, languages, operating procedures, and documentation of a computer system. Software is the real interface between the user and the computer.
SRAM	**S**tatic **R**andom **A**ccess **M**emory
SSBLT	**S**ource **S**ynchronous **BL**ock **T**ransfer

standard(s)	A set of detailed technical guidelines used as a means of establishing uniformity in an area of hardware or software development.
Teletext	One way broadcast of digital information. The digital information is injected in the broadcast TV signal, VBI, or full field, The transmission medium could be satellite, microwave, cable, etc. The display medium is a regular TV receiver.
thick Ethernet	See 10Base-5.
thin Ethernet	See 10Base-2.
twisted-pair Ethernet	See 10Base-T.
UART	**U**niversal **A**synchronous **R**eceiver/**T**ransmitter
Universe	ASIC developed by Tundra in consultation with Motorola, that provides the complete interface between the PCI bus and the 64-bit VMEbus.
USB	Universal Serial Bus
UV	**U**ltra**V**iolet
VESA (bus)	**V**ideo **E**lectronics **S**tandards **A**ssociation (or VL bus). An internal interconnect standard for transferring video information to a computer display system.
virtual address	A binary address issued by a CPU that indirectly refers to the location of information in primary memory, such as main memory. When data is copied from disk to main memory, the physical address is changed to the virtual address.
VL bus	See **V**ESA **L**ocal bus (VL bus).
VMEchip2	MCG second generation VMEbus interface ASIC (Motorola)
VME2PCI	MCG ASIC that interfaces between the PCI bus and the VMEchip2 device.
volatile memory	A memory in which the data content is lost when the power supply is disconnected.
VRAM	**V**ideo (Dynamic) **R**andom **A**ccess **M**emory. Memory chips with two ports, one used for random accesses and the other capable of serial accesses. Once the serial port has been initialized (with a transfer cycle), it can operate independently of the random port.

This frees the random port for CPU accesses. The result of adding the serial port is a significantly reduced amount of interference from screen refresh. VRAMs cost more per bit than DRAMs.

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