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DSP1008
EIGHT CHANNEL PROGRAMMABLE SIGNAL CONDITIONER

1008

TABLE OF CONTENTS

	SECTION
1008 SPECIFICATIONS	1
OPERATIONAL DESCRIPTION A. GENERAL B. FRONT PANEL INDICATORS AND CONTROLS C. FRONT PANEL CONNECTORS D. CAMAC CONTROL	2
CAMAC APPENDIX	3
SCHEMATICS	
ASSEMBLY	

SECTION 2

MODEL 1008

EIGHT CHANNEL PROGRAMMABLE SIGNAL CONDITIONER

FEATURES

- 8 Independent Differential Input Amplifier Channels
- Gain to X1024
- Low Noise, < 2 μV p-p RTI
- Low Pass Filters
- CMRR up to 100 dB
- Programmable and Manual Control
- Battery Backed Control Settings
- High Density, Single Width Module



ACTUAL SIZE

DESCRIPTION

The DSP Technology Model 1008 contains eight high quality instrumentation amplifiers in a fully programmable CAMAC single width package. These differential input amplifiers with gains up to 1024 are well suited to hostile, noisy environments. Low level voltage sources (eg: thermocouples) can be measured accurately in the presence of noisy multikilovolt sources. The complete independence of the channels allow different inputs to be amplified to similar output levels. Gain settings are retained in battery backed RAM.

FRONT PANEL CONTROLS

Each channel is programmed individually. Setting the CHAN/GAIN toggle switch to CHAN and then depressing the ADVANCE pushbutton allows the user to select any channel. The gain is set by changing the CHAN/GAIN switch to GAIN and again using the ADVANCE pushbuttom to step through the GAIN settings.

CAMAC CONTROL

Each of eight registers in the module can be addressed and loaded with the gain for that channel with a single CAMAC command.

TECHNICAL SPECIFICATIONS - MODEL 1008

INPUTS

Channels: 8 fully differential inputs

Input Impedance: ≥ 10M, 30 pf

Gain: 1,2,4,8,16,32,64,128,256,512,1024. Each channel individually programmable.

Bandwidth: ≥ 10 KHz, G = 1024, ≥ 100 KHz, G = 1

Settling Time: 200 μs to .01%

Filter: 50 Hz low pass cutoff. Jumper selectable in each channel.

Noise: < 2 μv p-p, referred to input.

Common Mode Rejection: ≥ 100 dB at 60 Hz for gains > 32 .

Common Mode Range: ± 10 V

Max Input: ± 15 V (special protection to 300 V for 100 μsec with reduced CMRR of 72 dB).

Accuracy: ± .02%

Non linearity: .01% (max)

OUTPUTS

Type: 8 independent single-ended outputs;

Voltage: ± 10 Volts.

Current: ± 5mA.

Drift: 1 μV / °C max, referred to input at gain = 1024 V.

CONTROLS

Channel and Gain selectable by front panel switches or CAMAC command.

Front Panel LED display indicates Channel or Gain depending on position of CHAN/GAIN toggle switch. Channel number or gain incremented by pushbutton switch See CAMAC commands for gain and channel selection.

COMPUTER COMMANDS

F(0)A(i)-N: Reads the Gain of Channel i. (i = 0-7)

F(16)A(i)-N: Writes the Gain into Channel i (i = 0-7)

MATING CONNECTORS

Amp 36 pin connector (P/N MC3016), two per module, are included.

Mating cable assemblies are also available.

DLSPMC - 1.5 is an input cable with 8 differential LEMO connectors.

DLSPMC2-1.5 is a dual output cable with 16 differential LEMO connectors.

TAB is an interconecting cable between the outputs and a Model 2812M Transient Recorder.

PACKAGING

#1 width CAMAC module

221 mm H, 18 mm W, 292 mm D* (8.7" x 0.7" x 11.5")

*Depth front to rear panel. Rear connector 13 mm (0.5")

In conformance with the CAMAC standard for RF shielded Instrumentation modules (IEEE standard #583, European Report # EUR4100e).

POWER REQUIREMENTS

+ 24 V 200 mA.
+ 6 V 250 mA.

TEMPERATURE RANGE:

0° to 40° C (32° F to 104° F) ambient, to operate within specifications (when installed in crate with enough air flow to hold maximum air exit temperature to 55° C (131° F).

SECTION 2

OPERATIONAL DESCRIPTION

A. GENERAL

The DSP Model 1008 is a single width CAMAC module containing eight instrumentation amplifiers with gains independently settable and readable either from the front panel or via the CAMAC interface. Gains are settable from 1 to 1024 volts/volt in 11 steps. Each amplifier is fully differential, with a small signal bandwidth of 10 KHz to 100 KHz, depending on the gain setting.

B. FRONT PANEL INDICATORS AND CONTROLS

LED INDICATORS

1. CHANNEL/GAIN INDICATOR

   This is a 3 digit, seven segment LED display that indicates either the channel displayed or the gain of that channel, depending on the setting of the CHANNEL#/GAIN switch. A gain of 1024 is indicated by a display of 1E3.

2. N

   A single LED which flashes briefly whenever the module is being addressed by the CAMAC interface.

SWITCH CONTROLS

1. CHANNEL#/GAIN SWITCH

   A three position toggle switch controls the source of display for the CHANNEL/GAIN indicator. There is a center OFF position which shuts off the display, which is of the multiplexed switching type, in order to minimize noise injected into the amplifiers when they are set to high gains.

2. ADVANCE SWITCH

   This pushbutton changes either the channel to be displayed or the gain of the amplifier at the displayed channel, depending on the setting of the CHANNEL#/GAIN switch. Pushing the button when the CHANNEL#/GAIN switch is in the OFF position has no effect on either the indicated channel or the gain. Pushing the button results in a single positive increment; when Channel #8 or a gain of 1024 is indicated, the next increment is to Channel 1 or a gain of 1, respectively.

C. FRONT PANEL CONNECTORS

1. INPUT CONNECTOR

The input connector is an AMP type 204731 with 36 sockets in 3 rows of 12 sockets. The socket connection assignments are given in table 1.

TABLE 1

INPUT CONNECTOR SOCKET ASSIGNMENTS

CH#	NON INVERT	INVERT	GND
1	1A	2A	1B
2	1C	2C	2B
3	4A	5A	4B
4	4C	5C	5B
5	8A	9A	8B
6	8C	9C	9B
7	11A	12A	11B
8	11C	12C	12B

The ground sockets indicated above are connected close to their respective channel amplifier inputs to minimize ground loops. Sockets unassigned in the above table are connected together and then connected to ground close to the front of the module.

2. OUTPUT CONNECTOR

The output connector is also an AMP type 204731, with 36 sockets in a 3 rows of 12. Sockets connection assignments are given in table 2 below.

TABLE 2

OUTPUT CONNECTOR SOCKET ASSIGNMENTS

CH#	OUTPUT	GND
1	1A	1B
2	1C	2B
3	3A	3B
4	3C	4B
5	5A	5B
6	5C	6B
7	7A	7B
8	7C	8B

All unassigned sockets in rows 1 through 8 are connected together and then to ground to reduce crosstalk in the connector. Rows 9-12 have not been loaded with sockets.

D. CAMAC CONTROL

The gain of any channel amplifier can be read or set via the CAMAC interface without affecting any other channel. A list of CAMAC commands appears below.

F(0) *A(n) Reads the gain setting of channel n + 1. See Read/Write data table below for gain/data equivalents.

F(3) *A(n) Reads instrument identification number.

F(16) *A(n) Sets the gain of channel n + 1. See Read/Write data table below for gain/data equivalents.

READ/WRITE DATA TABLE

GAIN	CAMAC LINES			
	W4 R4	W3 R3	W2 R2	W1 R1
1	0	0	0	0
2	0	0	0	1
4	0	0	1	0
	0	0	1	1
	0	1	0	0
8	0	1	0	1
16	0	1	1	0
	0	1	1	1
32	1	0	0	0
64	1	0	0	1
128	1	0	1	0
	1	0	1	1
256	1	1	0	0
512	1	1	0	1
1024	1	1	1	0
	1	1	1	1

SECTION 3

September 10,1981

APPENDIX - CAMAC

STATION NUMBER N

Each normal station is addressed by a signal on an individual Station Number line N which comes from a separate contact at the control station. The stations are numbered in decimal from the left-hand end as viewed from the front, beginning with Station 1 (addressed by N1).

SUBADDRESS A8, A4, A2, A1

Different sections of a module are addressed by signals on the four A bus lines. These signals are decoded in the module to select one of up to sixteen subaddresses, numbered in decimal from A(0) to A(15).

The subaddress may be used to select, for example, a register within the module, or a feature that is to control the Response signal Q, or a section of the module that is to be operated on by functions such as Enable, Disable, and Execute.

The subaddress codes are designated A(0), A(1), A(2), A(3), etc., to distinguish them from the individual Subaddress lines A1, A2, A4, and A8. For example, the Subaddress signals A1 = 1, A2 = 1, A4 = 0, and A8 = 0 represent the code A(3).

FUNCTION F16, F8, F4, F2, F1

The function to be performed at the specified subaddress in the selected module or modules is defined by the signals on the five F bus lines. These signals are decoded in the module to select one of up to thirty-two functions, numbered in decimal from F(0) to F(31). The definitions of the thirty-two function codes are summarised in Table 1.

In some systems the controller partially decodes the Function signals in order to determine whether a data transfer is required to a module (writing) or from a module (reading).

The function codes are subdivided into three groups, involving read operations, write operations, and operations with no transfer of data. The standard function codes have defined actions in modules and controllers. There are also reserved codes, for any future additions to the standard codes, and nonstandard codes whose use is not defined in detail.

The function codes are designated F(0), F(1), F(2), F(3), etc., to distinguish them from the individual function lines F1, F2, etc. For example, the Function signals F1 = 1, F2 = 0, F4 = 0, F8 = 1, and F16 = 1 represent the code F(25).

STROBE SIGNALS S1 AND S2.

During each command operation the controller generates two Strobe signals S1 and S2 in sequence on separate bus lines. In response to these timing signals plug-in units initiate various actions appropriate to the command that is present on the Dataway.

Both Strobe signals must be generated during each command operation.

Plug-in units must not take irreversible action based on the command or data signals until the time of S1. Actions concerned with the acceptance of data and status information from the R, W, Q, and X lines must be initiated at the time of S1 (with the possible exception given below). Other actions may also be timed by S1, but must not change the state of signals on the R and W lines.

Any actions that can change the state of Dataway Read or Write signals must be initiated by the second strobe S2. For example, S2 must be used if it is required to clear a register whose output is connected to the Dataway.

DATA

All information carried by the Read and Write lines is conveniently described as data, although it may be information concerned with status or control features in modules. Information that is transferred to or from a control register in a module is thus regarded as data.

Up to 24 b may be transferred in parallel between the controller and the selected module. Independent lines are provided for the read and write directions of transfer.

WRITE LINES W1-W24

The controller generates data signals on the W bus lines during each write operation. The W signals must reach a steady state before S1 and must be maintained until the end of the operation, unless modified by S2. Strobe S1 must be used by the modules to strobe the data unless there are very strong technical reasons for choosing S2.

READ LINES R1-R24

Data signals are set up on the R bus lines by the module during a read operation. The R signals must reach a steady state before S1 and must be maintained for the full duration of the Dataway operation, unless the state of the data source is changed by S2. The controller must initiate action concerned with the acceptance of data from the R lines at the time of the Strobe S1 and must not take irreversible action before this.

STATUS INFORMATION

Status information is conveyed by signals on the Look-at-Me L, Busy B, Response Q, and Command Accepted X lines.

LOOK-AT-ME L

The Look-at-Me lines, like the N lines, are individual connections from each normal station to separate contacts at the control station (L1 from station 1, etc.).

Any module may generate a signal on its individual line L, to indicate that it requires attention. Modules that occupy more than one station may indicate different demands by signals on the appropriate L lines.

The L signal generated by a module may represent demands for attention originating from more than one Look-at-Me source (LAM source) in the module.

Individual bits of the LAM status register are set by the corresponding LAM sources, and are cleared by appropriate commands and by the initialize signal. The internal Look-at-Me signal (L signal), derived from the OR combination of the LAM requests, is tested by the command Test LAM, with subaddress A(k) distinguishing this from tests of individual LAM requests. Finally, the output of this signal as the Dataway L signal is inhibited while the module is addressed by N, possibly in conjunction with certain F and A codes or groups of codes.

LOOK-AT-ME: Clear, Disable, and Test.

Provision must be made for resetting each bit of the LAM status register individually, either by a Clear Look-at-Me operation F(10), or by a Selective Clear Group 2 operation F(23). All LAM status bits must be reset collectively by the Initialize signal.

If the LAM request calls for some specific action (for example, reading the contents of a data register), then the corresponding bit of the LAM status register should also be cleared when the appropriate Dataway operation is performed.

A module that has generated L = 1 must not clear the LAM status register until it receives an appropriate command or the Initialize signal.

Each module that generates L should have a means of enabling and disabling the LAM requests. This may be done by loading and clearing a mask register, or by Enable and Disable commands.

All LAM requests that can be disabled by commands must also be disabled by the Initialize signal Z.

A module that generates L must have a means of testing the L signal by a Test Look-at-Me operation (Function code F(8), with a subaddress distinguishing this from tests of individual LAM requests). If there are several LAM sources, the corresponding LAM requests must also be

capable of being examined either by Test Look-at-Me operations associated with appropriate subaddresses or by reading a LAM request pattern in a read operation.

BUSY B

The Busy signal is used to interlock various aspects of a system that can compete for the use of the Dataway. The signal B = 1 indicates to all units that a Dataway operation is in progress.

The Busy signal B = 1 must be generated during each Dataway command operation (when N signals are also generated).

RESPONSE Q

During every command operation the addressed module may generate a signal on the Q bus line to indicate the status of any selected feature of the module.

The controller must initiate action concerned with the acceptance of the status information from the Q line at the time of Strobe S1 and must not take irreversible action before this.

In read and write operations addressed modules must establish the signal Q = 0 or Q = 1 before Strobe S1 and must maintain it until at least Strobe S2.

In Test Look-at-Me operations addressed modules may initiate the Q signal at any time during a Dataway operation if the status of the appropriate LAM request changes. If Q = 1 has been initiated, it will remain static until the end of the operation since this command is not allowed to reset LAM status.

In all operations other than read, write, and Test Look-at-Me the Q signal is permitted to change at any time. There is a risk that status information will be missed if Q = 1 is initiated between Strobes S1 and S2 during an operation in which the module resets the status condition at the time of Strobe S2.

In any operation the Q signal conveys only one bit of information, which should be clearly defined for each subaddress and function code used by the module.

COMMAND ACCEPTED X

Whenever a module is addressed during a command operation it must generate X = 1 on the Command Accepted bus line if it recognizes the command as one that it is equipped to perform, either within the module or in association with external equipment. The signal on the X line must reach a steady state before S1 and must be maintained until S2. Controllers that accept the X signal must do so at the time of S1.

The signal X = 0 should indicate a serious malfunction, for example, a module that is not present, not powered, lacks external connections, or is not equipped to perform the required action. The action taken by the controller in response to X = 0 may, for example, be to call for intervention by the operator or operating system.

COMMON CONTROLS Z, C, I.

During unaddressed Dataway operations either Initialize Z or Clear C is generated by the controller and received by each unit connected to the appropriate bus line.

The common control signal Inhibit I is not associated with Dataway operations. It may be generated at any time and is received by each unit connected to the I bus line.

INITIALIZE Z

The Initialize signal is intended to be used during system startup.

Initialize must have absolute priority over other signals. In response to Z = 1 all data and control registers must be set to a defined initial state, all LAM status registers must be reset, and, if possible, all LAM requests must be disabled.

INHIBIT I

The signal I = 1 must inhibit any feature to which it is connected in a module.

The designer is free to choose which activities (for example, data taking) within a module are inhibited by this signal. The signal may be gated or routed within the module, for example, as a result of a previous command or by patch wiring.

When any unit generated the Initialize signal Z = 1 it must also generate I = 1.

CLEAR C

The signal C = 1 must clear all registers and bistables to which it is connected.

Units that generate C must also initiate a sequence including Busy and Strobe S2.

The designer is free to choose which registers and bistables are cleared in response to C·S2. The signal may be gated or routed within the module, for example as a result of a previous command or by patch wiring.

Bus line
Bus line
Individual patch contact
Individual patch contact
Individual patch contact
Bus line
Bus line
Bus line
Individual line
Individual line
Bus line
Bus line

Twenty-four Write Bus lines
W1 = least significant bit
W24 = most significant bit

Twenty-four Read Bus lines
R1 = least significant bit
R24 = most significant bit

Power Bus lines

[redacted]
from front of Crate)

Free Bus line	P1	B	Busy	Bus line
Free Bus line	P2	F16	Function	Bus line
	P3	F8	Function	Bus line
	P4	F4	Function	Bus line
	P5	F2	Function	Bus line
Command Accepted	X	F1	Function	Bus line
Inhibit	1	A8	Subaddress	Bus line
Clear	C	A4	Subaddress	Bus line
Station Number	N	A2	Subaddress	Bus line
Look-at-Me	L	A1	Subaddress	Bus line
Strobe 1	S1	Z	Initialize	Bus line
Strobe 2	S2	Q	Response	Bus line
	W24	W23		
	W22	W21		
	W20	W19		
	W18	W17		
	W16	W15		
	W14	W13		
	W12	W11		
	W10	W9		
	W8	W7		
	W6	W5		
	W4	W3		
	W2	W1		
	R24	R23		
	R22	R21		
	R20	R19		
	R18	R17		
	R16	R15		
	R14	R13		
	R12	R11		
	R10	R9		
	R8	R7		
	R6	R5		
	R4	R3		
	R2	R1		
-12 V dc	-12	-24	-24 V dc	
+200 V dc	-200	-6	-6 V dc	
117 V ac Live	ACL	ACN	117 V ac Neutral	
Reserved	Y1	E	Clean Earth	
+12 V dc	+12	+24	+24 V dc	
Reserved	Y2	+6	+6 V dc	
0 V (Power Return)	0	0	0 V (Power Return)	

Individual patch contact	
Individual patch contact	
Individual patch contact	
Individual patch contact	
Individual patch contact	
Bus line	Command Accepted
Bus line	Inhibit
Bus line	Clear
Individual patch contact	
Individual patch contact	
Bus line	Strobe 1
Bus line	Strobe 2

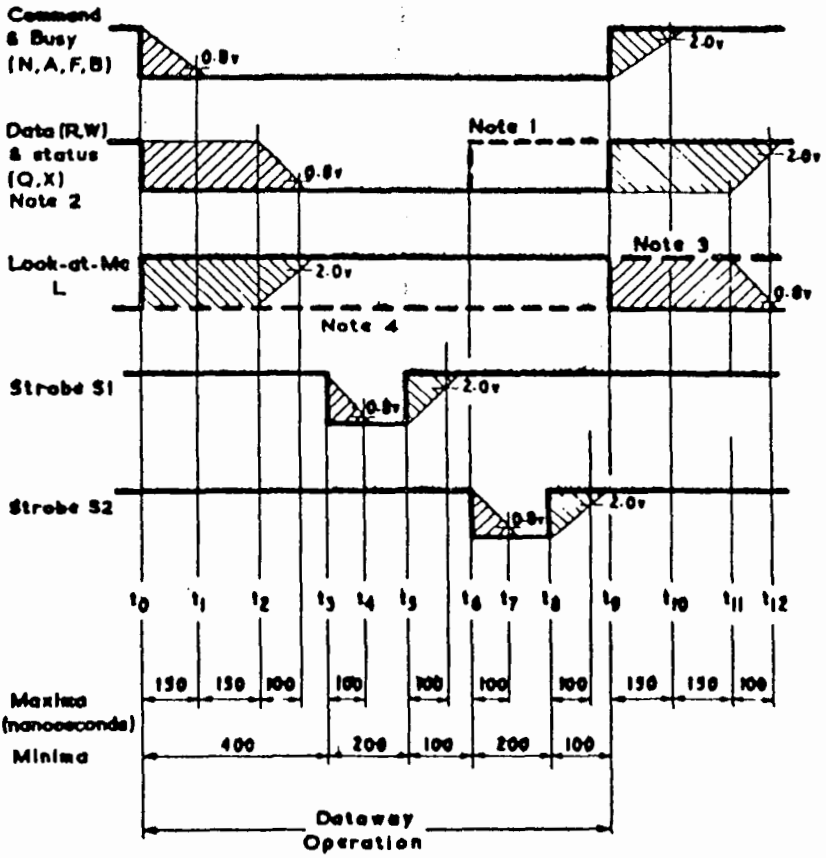
Twenty-four individual Look-at-Me lines L1 from Station 1, etc.

Power Bus lines	-12 V dc
	+200 V dc
	117 V ac Live
	Reserved
	+12 V dc
	Reserved
	0 V (Power Return)

f Crate)

P1	B	Busy	Bus line
P2	F16	Function	Bus line
P3	F8	Function	Bus line
P4	F4	Function	Bus line
P5	F2	Function	Bus line
X	F1	Function	Bus line
I	A8	Subaddress	Bus line
C	A4	Subaddress	Bus line
P6	A2	Subaddress	Bus line
P7	A1	Subaddress	Bus line
S1	Z	Initialize	Bus line
S2	Q	Response	Bus line
L24	N24	Twenty-four individual Station Number lines N1 to Station 1, etc.	
L23	N23		
L22	N22		
L21	N21		
L20	N20		
L19	N19		
L18	N18		
L17	N17		
L16	N16		
L15	N15		
L14	N14		
L13	N13		
L12	N12		
L11	N11		
L10	N10		
L9	N9		
L8	N8		
L7	N7		
L6	N6		
L5	N5		
L4	N4		
L3	N3		
L2	N2		
L1	N1		
-12	-24	-24 V dc	
+200	-6	-6 V dc	
ACL	ACN	117 V ac Neutral	
Y1	E	Clean Earth	
+12	+24	+24 V dc	
Y2	+6	+6 V dc	
0	0	0 V (Power Return)	

Code F( )	Function	Use of R & W Lines	Function Signals F16	F8	F4	F2	F1	Code F( )
0	Read Group 1 register	Functions using the R lines	0	0	0	0	0	0
1	Read Group 2 register		0	0	0	0	1	1
2	Read & Clear Group 1 register		0	0	0	1	0	2
3	Read Complement of Group 1 register		0	0	0	1	1	3
4	Nonstandard		0	0	1	0	0	4
5	Reserved		0	0	1	0	1	5
6	Nonstandard		0	0	1	1	0	6
7	Reserved		0	0	1	1	1	7
8	Test Look-at-Me	Functions using the R or	0	1	0	0	0	8
9	Clear Group 1 register	W lines	0	1	0	0	1	9
10	Clear Look-at-Me		0	1	0	1	0	10
11	Clear Group 2 register		0	1	0	1	1	11
12	Nonstandard		0	1	1	0	0	12
13	Reserved		0	1	1	0	1	13
14	Nonstandard		0	1	1	1	0	14
15	Reserved		0	1	1	1	1	15
16	Overwrite Group 1 register	Functions using the W lines	1	0	0	0	0	16
17	Overwrite Group 2 register		1	0	0	0	1	17
18	Selective Set Group 1 register		1	0	0	1	0	18
19	Selective Set Group 2 register		1	0	0	1	1	19
20	Nonstandard		1	0	1	0	0	20
21	Selective Clear Group 1 register		1	0	1	0	1	21
22	Nonstandard		1	0	1	1	0	22
23	Selective Clear Group 2 register		1	0	1	1	1	23
24	Disable	Functions not using the R	1	1	0	0	0	24
25	Execute	or W lines	1	1	0	0	1	25
26	Enable		1	1	0	1	0	26
27	Test Status		1	1	0	1	1	27
28	Nonstandard		1	1	1	0	0	28
29	Reserved		1	1	1	0	1	29
30	Nonstandard		1	1	1	1	0	30
31	Reserved		1	1	1	1	1	31



NOTES:

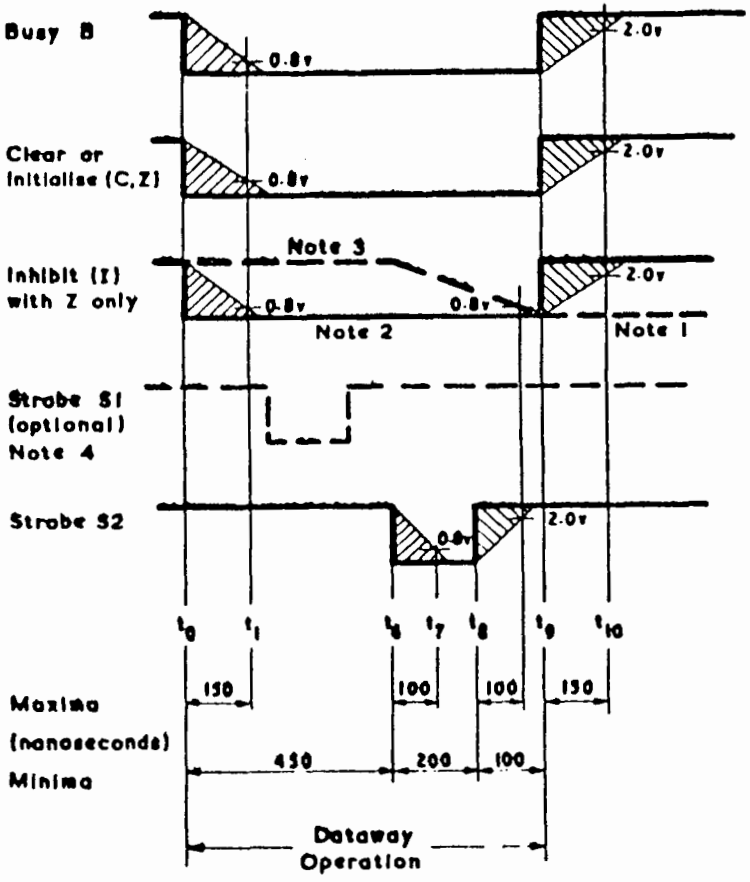
(1) Data and status may change in response to *S2*

(2) During some operations *Q* may change at any time

(3) LAM status may be reset during operation

(4) *L* signal may be maintained during operation

Timing of a Dataway Command Operation

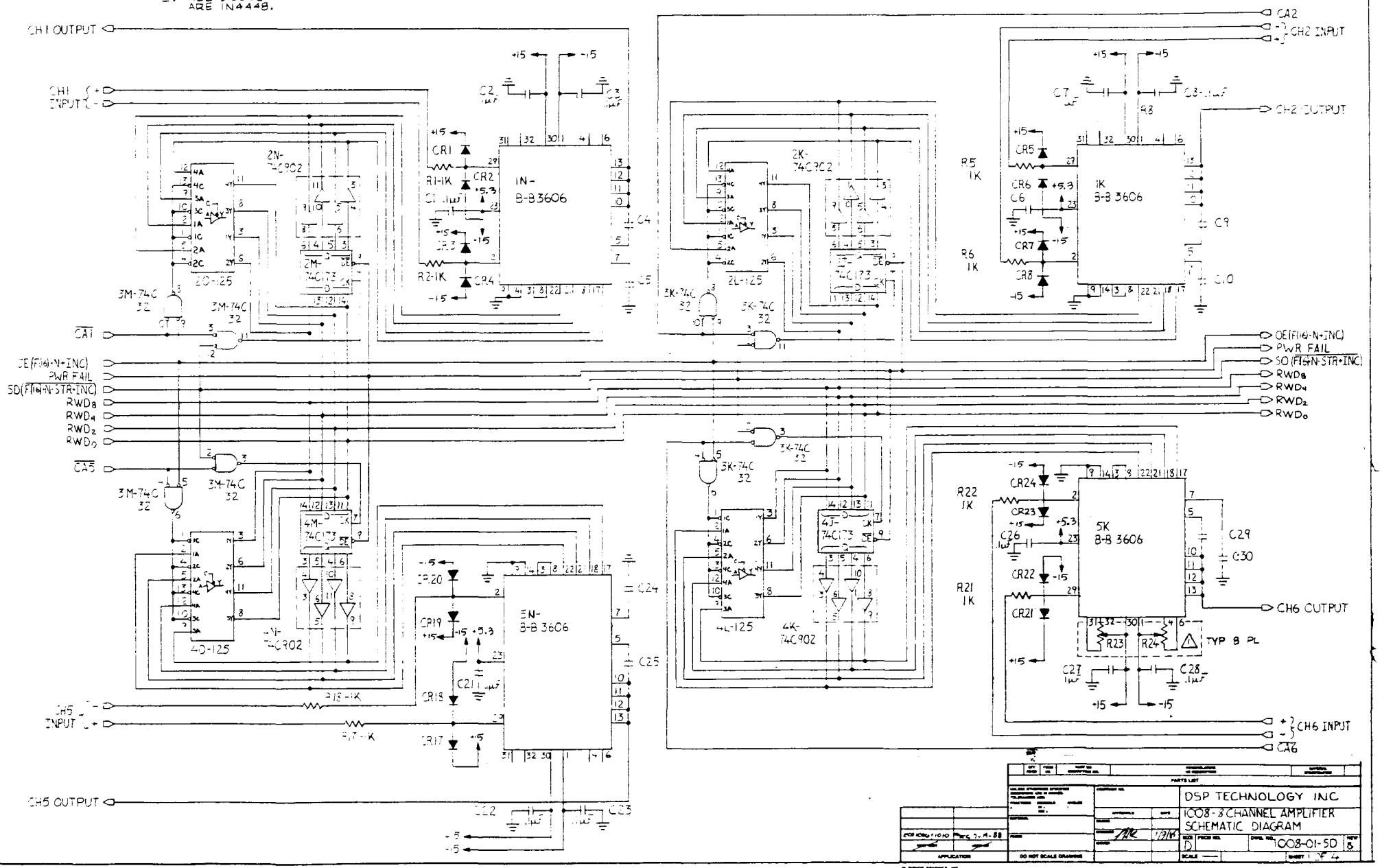


NOTES:
(1) *I* preferably maintained
(2) *I* accompanying *Z*
(3) *I* generated in response to *Z*·*S2*
(4) Other times as in Fig 17

Timing of a Dataway Unaddressed Operation

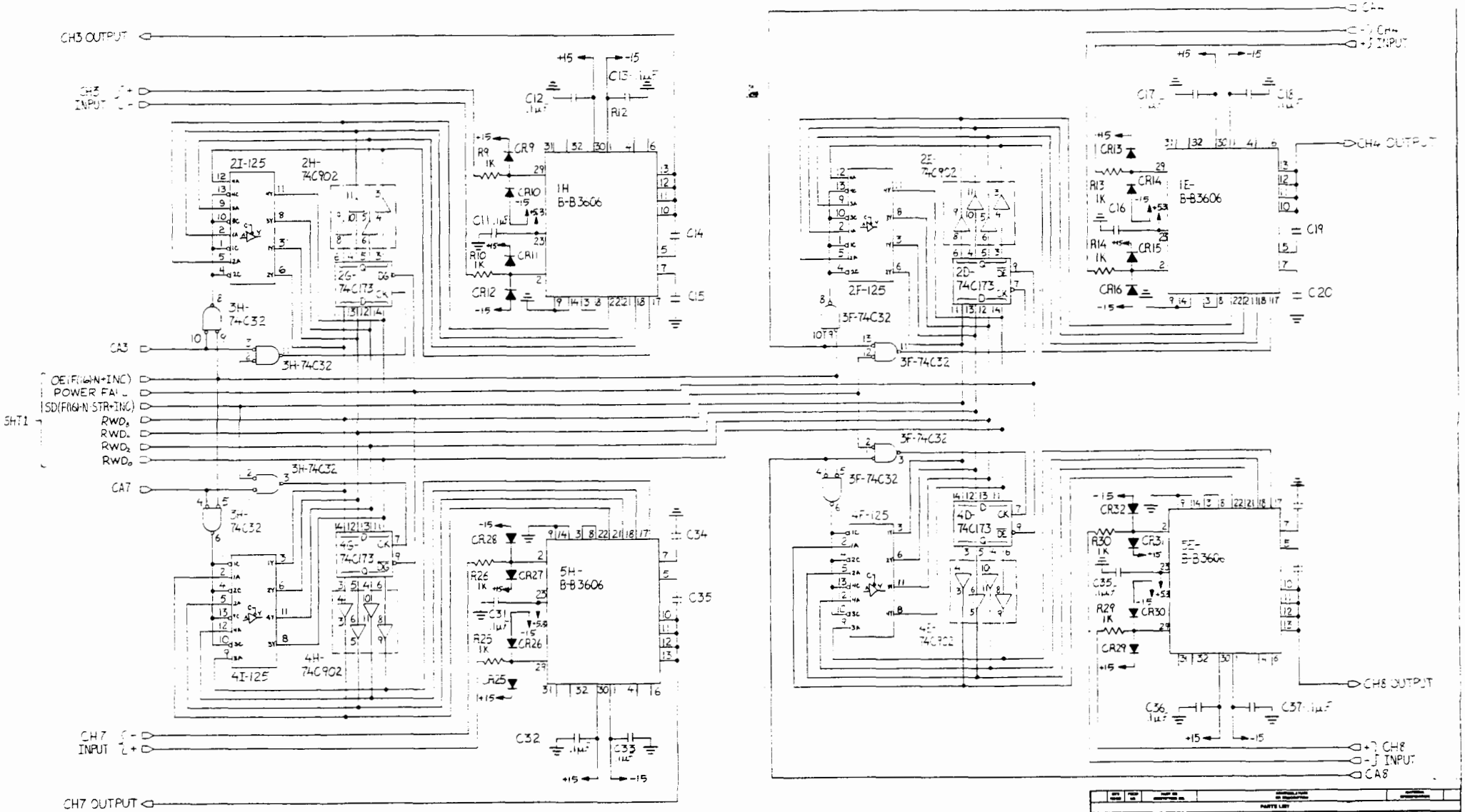
NOTES(UNLESS OTHERWISE SPECIFIED)

1. COMPONENTS DRAWN WITH DASHED LINES ARE OPTIONAL.
2. ALL DIODES ARE IN4448.

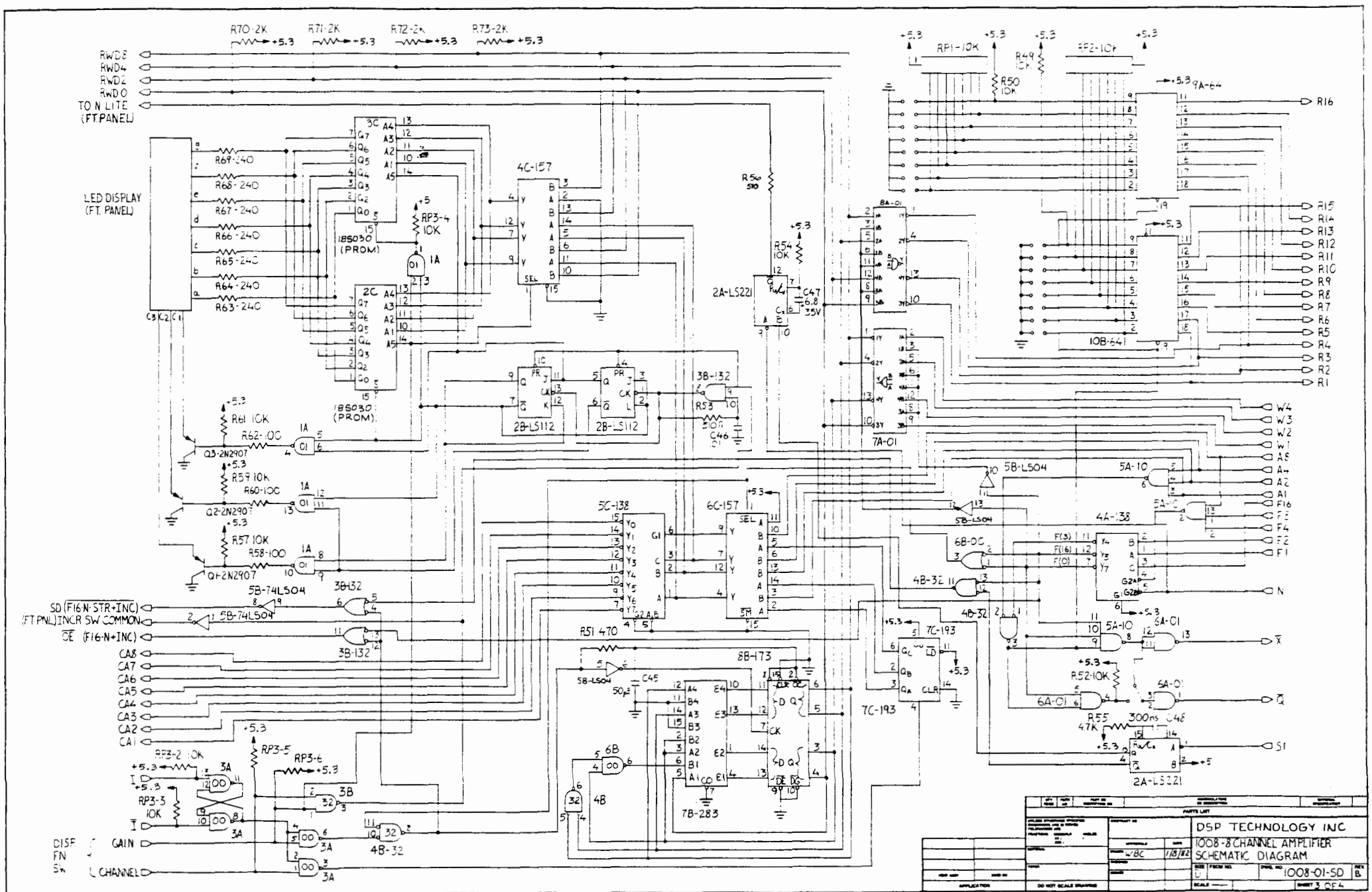


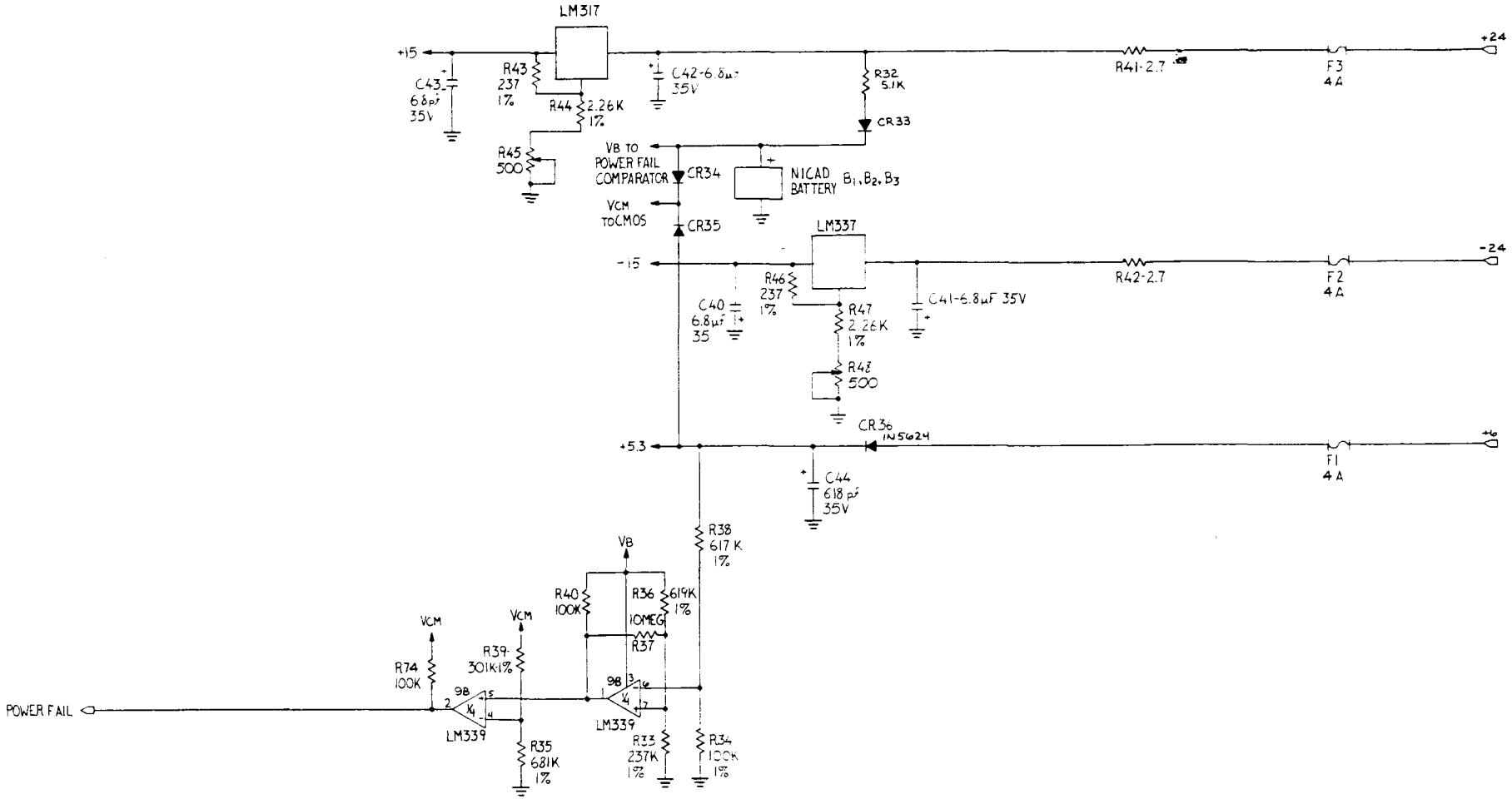
NOTES (UNLESS OTHERWISE SPECIFIED)

1. ALL DIODES ARE IN4448.



			DSP TECHNOLOGY INC
			1008-8 CHANNEL AMPLIFIER SCHEMATIC DIAGRAM
			SIZE D | DWG. NO. 1008-01-SD | REV. B
			SCALE — | SHEET 2 OF 4


R70-2K
R71-2K
R72-2K
R73-2K
+5.3
RWD8
RWD4
RWD2
RWD0
TO N LITE
(FT.PANEL)
LED DISPLAY
(FT. PANEL)
C3 K2 C1
R69-240
R68-240
R67-240
R66-240
R65-240
R64-240
R63-240
3C
2C
4C-157
185030
(PROM)
RP3-4
10K
1A
RP1-10K
RP2-10K
R49
10K
R50
10K
9A-64
10B-641
R16
R15
R14
R13
R12
R11
R10
R9
R8
R7
R6
R5
R4
R3
R2
R1
R56
510
R54
10K
2A-LS221
C47
6.8
35V
8A-01
7A-01
R61 10K
R62-100
Q3-2N2907
R59 10K
R60-100
Q2-2N2907
R57 10K
R58-100
Q1-2N2907
2B-LS112
3B-132
R53
510R
C46
.01
5B-LS04
5A-10
5A-01
4A-138
6B-00
4B-32
F(3)
F(16)
F(0)
W4
W3
W2
W1
A8
A4
A2
A1
F16
F8
F4
F2
F1
N
X
Q
S1
SD (F16-N-STR+INC)
(FT.PNL) INCR SW COMMON
OE (F16-N+INC)
5B-74LS04
CA8
CA7
CA6
CA5
CA4
CA3
CA2
CA1
5C-138
6C-157
8B-173
7C-193
7B-283
R51 470
C45
50pF
R52-10K
R55
4.7K
300ns
C48
2A-LS221
RP3-2 10K
RP3-3
10K
RP3-5
RP3-6
3A
3B
4B
6B
4B-32
DISP
FN
SW
GAIN
CHANNEL
DSP TECHNOLOGY INC
1008-8 CHANNEL AMPLIFIER
SCHEMATIC DIAGRAM
WBC
1/18/82
1008-01-SD
REV B
SHEET 3 OF 4
PARTS LIST
DO NOT SCALE DRAWING



NOTES (UNLESS OTHERWISE SPECIFIED)

1. ALL DIODES ARE IN4448.

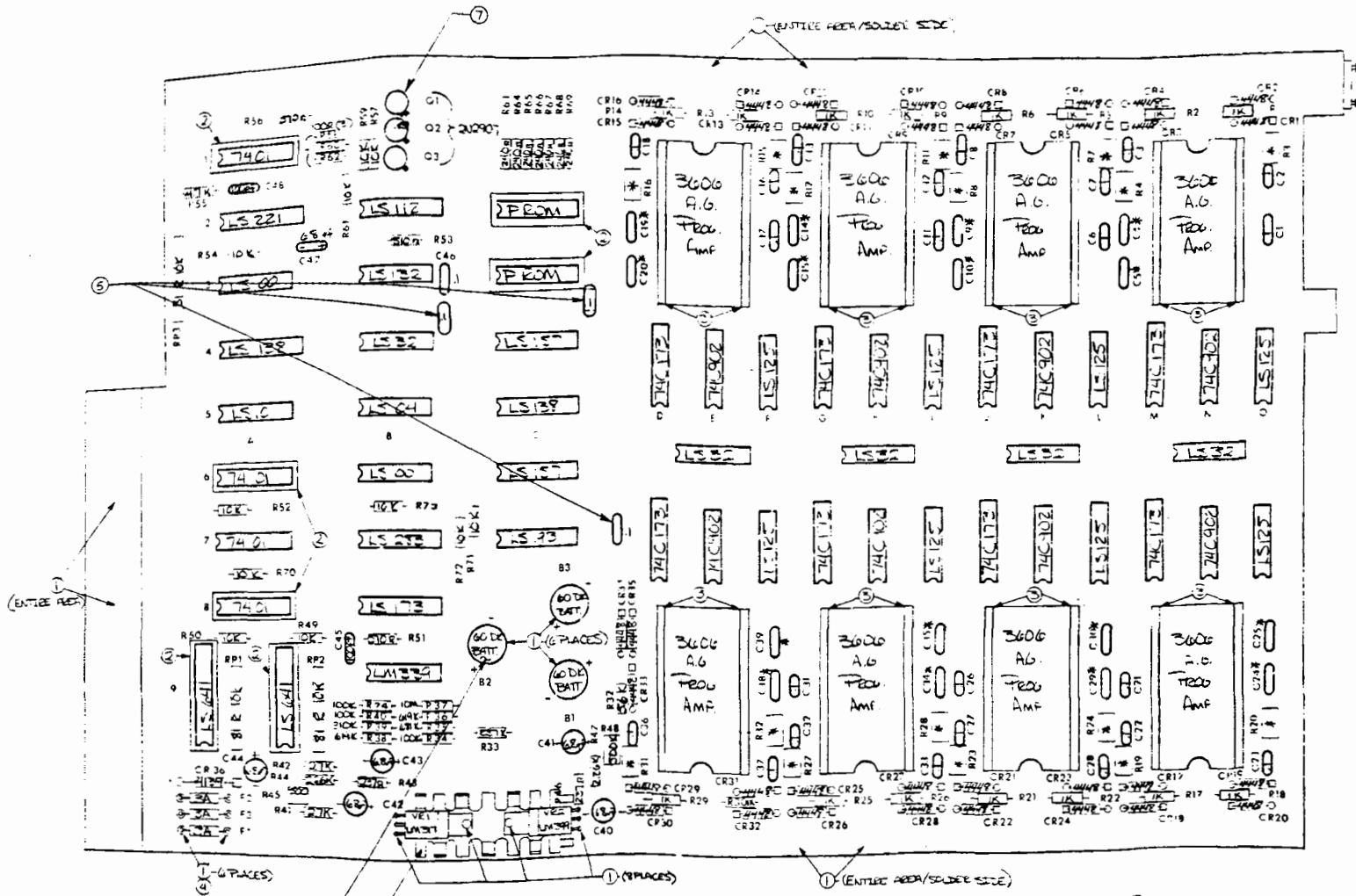
DSP TECHNOLOGY INC

1008-8 CHANNEL AMLIFIER
SCHEMATIC DIAGRAM

WBC 1/8/82

D | 1008-01-SD | REV B

SHEET 4 OF 4

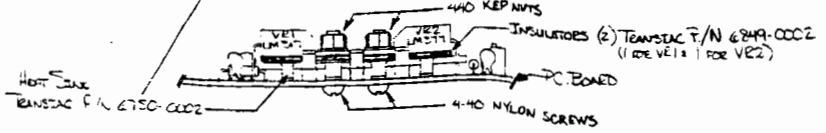


NOTES:

1. MASK DURING WAVE SOLDER.
2. LOAD SOCKET IN THIS POSITION.
3. INSTALL DUAL SOCKET STRIP IN THIS LOCATION (16 PINS PER STRIP) TRANSIAC P/N 5250-0002.
4. INSTALL TRANSIAC P/N 5250-3703 AFTER WAVE SOLDER.
5. INSTALL 0521-0104 HERE (3 PLCS) (THESE 3 CAPACITORS HAVE NO DESIGNATIONS)
6. MOUNT NEG SIDE OF BATTERY FLUSH TO PCB. DO NOT SOLDER THE "-" LEAD OF BATTERY "B2" INTO THE BOARD. INSULATE LEAD WITH LOOSE SHRINK TUBING TO PREVENT IT FROM SHORTING OUT. THIS LEAD WILL BE SOLDERED AFTER TESTING THE UNIT.
7. SILKSCREEN IS WRONG FOR Q1, Q2, Q3. INSTALL Q1, Q2, Q3 AS SHOWN.

NOTE: * INDICATES NO PART REQUIRED

VOLTAGE REG ASSEMBLY DETAIL



	ECO 1008	DSP Technology
		1008 - 8 CHANNEL AMPLIFIER ASSEMBLY DRAWING
	DO NOT SCALE DRAWING	1008-01-A.D.

Assembly: A-1008-01 (ASY 1008:8 CHANNEL AMPLIFIER ASY)
Revision:
As of: 09/30/89

	Component	Description	Qty Per
1.	0100-0101	RES: RC07 100 OHM	3.00
2.	0100-0102	RES: RC07 1K OHM	16.00
3.	0100-0103	RES: RC07 10K OHM	7.00
4.	0100-0104	RES: RC07 100K OHM	2.00
5.	0100-0106	RES: RC07 10M OHM	1.00
6.	0100-0202	RES 5% 1/4W CC RESISTOR R=2K	4.00
7.	0100-0241	RES 5% 1/4W CC RESISTOR R=240	7.00
8.	0100-0279	RES 5% 1/4W CC RESISTOR R=2.7	2.00
9.	0100-0471	RES 5% 1/4W RES R=470	1.00
10.	0100-0472	RES 5% 1/4W CC RESISTOR R=4.7K	1.00
11.	0100-0511	RES 5% 1/4W CC RESISTOR R=510	2.00
12.	0100-0512	RES 5% 1/4W CC RESISTORR R=5.1K	1.00
13.	0150-1003	RES 1% 1/4W MF RESISTOR R=100K	1.00
14.	0150-2261	RES 1% 1/4W MF RESISTOR R=2.26K	2.00
15.	0150-2370	RMF RN55D 1% METAL FILM RES R=237	2.00
16.	0150-2373	RES 1% 1/4W MF RESISTOR R=237K	1.00
17.	0150-3013	RES 1% 1/4W MF RESISTOR R=301K	1.00
18.	0150-6193	RES 1% 1/4W MF RESISTOR R=619K	2.00
19.	0150-6813	RES 1% 1/8W MF RESISTOR R=681K	1.00
20.	0200-0103	RPK RES PK BNS 4308R-101-103	3.00
21.	0350-0501	RES VAR. 12T 1/4" TOP ADJ R=500 BO	2.00
22.	0500-0101	CSM C=100PF CDE # CD5FC101J03	2.00
23.	0521-0104	CMC C=0.1UF MONO CENTRALAB CZ20A104	27.00
24.	0600-0685	CTE C=6.8UF TANT 35WVDC KEMET T361B	6.00
25.	1000-4448	DGS DIODE SIL. SWITCH 1N4448	35.00
26.	1030-5624	DSR: DIODE RECT 3A GE IN5624/BYM56	1.00
27.	1300-2907	TRP TRANSISTOR PNP SIL GP 2N2907	3.00
28.	1750-0001	ICS SN7401	4.00
29.	1760-0000	ICS SN74LS00	2.00
30.	1760-0004	ICS SN74LS04	1.00
31.	1760-0010	ICS SN74LS10	1.00
32.	1760-0032	ICS SN74LS32	5.00
33.	1760-0112	ICS SN74LS112	1.00
34.	1760-0125	ICS SN74LS125	8.00
35.	1760-0132	ICS SN74LS132	1.00
36.	1760-0138	ICS SN74LS138	2.00
37.	1760-0157	ICS SN74LS157	2.00
38.	1760-0173	ICS SN74LS173	1.00
39.	1760-0193	ICS SN74LS193	1.00
40.	1760-0221	ICS SN74LS221	1.00
41.	1760-0283	ICS SN74LS283	1.00
42.	1760-0641	ICS SN74LS641	2.00
43.	1780-0173	IC: 74HCT173	8.00
44.	1780-0902	ICS IC CMOS HEX BUFFER 74C902	8.00
45.	1851-0014	PRM PROM PROG/F 1850-0001 1008-01 2	1.00

Component Description Qty Per

DSP Technology Inc.

BILL OF MATERIAL REPORT

Date: 10/05/89
Page: 1

As of	Until	Reference
01/01/80	12/31/99	R58 R60 R62
01/01/80	12/31/99	R1 R10 R13 R14 R17 R18 R2 R21 R22 R25 R26 R29 R30 R5 R6 R9
01/01/80	12/31/99	R49 R50 R52 R54 R57 R59 R61
01/01/80	12/31/99	R40 R74
01/01/80	12/31/99	R37
02/21/86	12/31/99	R70-R73
02/21/86	12/31/99	R63-R69
01/01/80	12/31/99	R41 R42
05/11/88	12/31/99	R51
01/01/80	12/31/99	R55
01/01/80	12/31/99	R53 R56
01/01/80	12/31/99	R32
01/01/80	12/31/99	R34
01/01/80	12/31/99	R44 R47
01/01/80	12/31/99	R43 R46
01/01/80	12/31/99	R33
01/01/80	12/31/99	R39
01/01/80	12/31/99	R36 R38
01/01/80	12/31/99	R35
02/21/86	12/31/99	RP1-RP3
01/01/80	12/31/99	R45 R48
01/01/80	12/31/99	C45 C48
02/21/86	12/31/99	C1-C3 C6-C8 C11-C13 C16-C18 C21-C23 C26-C28 C31-C33 C36 C37 C46
02/21/86	12/31/99	C40-C44 C47
02/21/86	12/31/99	CR1-CR35
01/01/80	12/31/99	CR36
02/21/86	12/31/99	Q1-Q3
02/21/86	12/31/99	1A 6A-8A
01/01/80	12/31/99	3A 6B
01/01/80	12/31/99	5B
01/01/80	12/31/99	5A
01/01/80	12/31/99	3F 3H 3K 3N 4B
01/01/80	12/31/99	2B
01/01/80	12/31/99	2F 2I 2L 2O 4F 4I 4L 4O
01/01/80	12/31/99	3B
01/01/80	12/31/99	4A 5C
01/01/80	12/31/99	4C 6C
01/01/80	12/31/99	8B
01/01/80	12/31/99	7C
01/01/80	12/31/99	2A
01/01/80	12/31/99	7B
05/15/87	12/31/99	9A 10B
01/01/80	12/31/99	2D 2G 2J 2M 4D 4G 4J 4M
01/01/80	12/31/99	2E 2H 2K 2N 4E 4H 4K 4N
01/07/86	12/31/99	2C

| As of | Until | Reference |

Assembly: A-1008-01 (ASY 1008:8 CHANNEL AMPLIFIER ASY)
Revision:
As of: 09/30/89

	Component	Description	Qty Per	As of	Until
46.	1851-0015	PRM PROM PROG/F 1850-0001 1008-01 3	1.00	01/07/86	12/31/99
47.	2010-0339	ICS QUAD COMPARATOR LM339	1.00	01/01/80	12/31/99
48.	2030-0317	ICS IC VOL REG NAT LM317T	1.00	01/01/80	12/31/99
49.	2030-0337	IC: VOLT REG, NEG ADJ, LM337T	1.00	01/01/80	12/31/99
50.	2050-7433	IC: IC LED DISPLAY HP 5082-7433	1.00	01/01/80	12/31/99
51.	3100-0402	FUS FUSE 4AMP LITTLEFUSE 251004	3.00	01/01/80	12/31/99
52.	5000-0014	SKT CAMBION 703-1314-01-04-10	3.00	01/01/80	12/31/99
53.	5000-0016	SKT CAMBION 703-1316-01-04-10	2.00	01/01/80	12/31/99
54.	5000-0020	SKT CAMBION 703-1320-01-04-10	2.00	09/17/87	12/31/99
55.	5050-0001	SKT 20 STRIP SAMTEC SS120G-2	1.00	02/21/86	12/31/99
56.	5250-0002	FLS COMPONET LEAD SOCKET BERG#7554	256.00	02/21/86	12/31/99
57.	5250-3703	JCK FUS CAMBION 450-3703-01-06-00	6.00	02/21/86	12/31/99
58.	6510-3606	AMP PROG. GAIN AMPLIFIER BB3606AG	8.00	01/01/80	12/31/99
59.	6750-0063	HTSK: 6025B MODIFIED	1.00	06/23/86	12/31/99
60.	6849-0002	INS BERGQUIST 3223-07-FR-54	2.00	02/21/86	12/31/99
61.	6850-0001	RAIL: GUIDE, MDL, 5 HOLE, C-BORE	2.00	01/01/80	12/31/99
62.	7000-0017	PCB DWG# 1008-01-FD	1.00	01/01/80	12/31/99
63.	7010-0013	PCB: LED MTG, 1008/1020	1.00	02/21/86	12/31/99
64.	7303-0500	FLS SCREW 4-40 X 1/2 PAN HD NYLON	2.00	02/21/86	12/31/99
65.	7350-0001	FLS KEPS UNT 4-40 STEEL	2.00	02/21/86	12/31/99
66.	7410-0003	HWD: SWAGE TYPE STANDOFF	6.00	01/01/88	12/31/99
67.	8200-0002	BAT BATTERY NICAD 1.2V VARTA 60DK	3.00	01/01/80	12/31/99
68.	DOCUMENTATION	PER ASSY DWG REFERENCE	1.00	02/21/86	12/31/99

Reference
3C
9B
VR1
VR2
DPL1
F1 F2 F3
1A 6A 8A
2C 3C
9A 10B
DISPLAY PCB
1E 1H 1K 1N 5E 5H 5K 5N
F1 F2 F3
1E 1H 1K 1N 5E 5H 5K 5N
VR1/VR2
VR1 VR2
DISPLAY MNTG PCB
HEATSINK MNTG HDWR
HEATSINK MNTG HDWR
B1 B2 B3
1008-01AD

Assembly: A-1008-02 (ASY 1008:FRONT PANEL ASY)
Revision: A
As of: 09/30/89

	Component	Description	Qty Per
1.	078005	CONN: JUMPER, BUSSCO B5153-100-240T	20.00
2.	1040-0001	DLE LED GREEN LITRONIX#LD37-2	1.00
3.	5601-0002	SKT WIREWRAP AMP #1-205172-1	72.00
4.	5601-0036	CON 36 PIN AMP 204731-1	2.00
5.	6020-0002	CAP FOR 6020-0001 ALCO C-10-1-25	1.00
6.	6020-0003	NUT DRESS ALCO N-40 CTLR-HMMR WNU-	2.00
7.	6020-0004	SWH ON-OFF-ON TOGGLE C&K7103SYZQ	1.00
8.	6025-0001	SPB SWITCH PUSHBTN C&K 8125SHZGE	1.00
9.	6025-0002	CAP:PUSH BUTTON C&K 7089-BROWN	1.00
10.	6851-0008	PNL: FR, 1008	1.00
11.	6852-0001	SCR:FT PNL JCK DEUTCH D7500M4B4	1.00
12.	6852-0004	PNL: RR, 1/25 B	1.00
13.	7710-0001	RML PLASTIC SHEET-RED VENDOR:SAN JO	1.00
14.	A-1008-01	ASY 1008:8 CHANNEL AMPLIFIER ASY	1.00
15.	DOCUMENTATION	PER ASSY DWG REFERENCE	3.00

Component Description Qty Per

Assembly: A-1008-02 (ASY 1008:FRONT PANEL ASY)

[redacted] Technology Inc. [redacted]

BILL OF MATERIAL REPORT

Date: 10/05/89
Page: 1

As of	Until	Reference
04/16/87	12/31/99	
02/21/86	12/31/99	N
02/21/86	12/31/99	INPUT/OUTPUT
02/21/86	12/31/99	INPUT/OUTPUT
02/21/86	12/31/99	CHAN/GAIN
02/21/86	12/31/99	CHAN/GAIN, ADVANCE
02/21/86	12/31/99	CHAN/GAIN
02/21/86	12/31/99	ADVANCE
02/21/86	12/31/99	ADVANCE
01/01/80	12/31/99	
01/01/80	12/31/99	
06/09/86	12/31/99	
02/21/86	12/31/99	WINDOW
01/01/80	12/31/99	
02/21/86	12/31/99	1008-02AD, 1008-02WD, 1008-02WL

As of	Until	Reference

dsp Technology Inc.

PRODUCT WARRANTY

(Excludes Software)

DSP TECHNOLOGY ("DSP") warrants its products to be free from defects in material and workmanship and to meet DSP's performance specifications. The warranty period is one year from the date of shipment to the buyer. The warranty is limited by the paragraphs below.

RETURN TO FACTORY

If a buyer discovers a defect in a DSP product covered by this agreement, buyer's exclusive remedy is to ship the product back to DSP's Fremont factory, where DSP will, at its option, either repair or replace the product. This remedy applies if DSP receives the returned product on or before the tenth day after the expiration of the warranty period and the buyer notifies DSP of the defect before returning the product.

COST TO BUYER OF REPAIRS OR REPLACEMENT

Buyer must prepay freight charges to DSP. DSP will pay standard return freight to buyer. Buyer will be charged for premium freight if that method of transport is requested by buyer. There is no other charge for repair or replacement during the warranty period.

TRANSFERRABLE WARRANTIES

In addition to the foregoing warranty, DSP also provides the buyer the transferrable warranty, if any, provided to DSP by the manufacturers of other products such as terminals and disk systems supplied by SEC as part of a total system.

LIMITATION OF WARRANTY AND LIABILITY

The foregoing constitutes DSP's entire warranty, expressed, implied, and/or statutory (except as to title), and to any other party for any breach of such warranty and for damages, whether direct, special, incidental, or consequential. Other than as expressly provided in this document, no warranties expressed or implied, including any warranty of merchantability or fitness for a particular purpose are made. No employee, representative, or agent or seller has any authority expressed or implied to alter or supplement the terms of this warranty.

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