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DSP TECHNOLOGY INC.

MODEL 1024 TRIGGER MODULE

USER'S MANUAL

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OPERATIONAL DESCRIPTION

Model 1024 is a general purpose analog trigger module which can generate programmable trigger and timing conditions for four input signals. The trigger outputs can be logically gated together to form a master trigger or the individual outputs can be used directly.

The analog input signals can be either :

1) (Factory Default)
Low speed (<2Mhz) differential (NORM mode) with 1 Megohm input impedance, (optional AC coupling), full scale input range is 20 volts (+/- 10 volts) with a common mode rejection range (signal + common mode voltage) of +/- 50 volts. Other full scale ranges can be accommodated by changing the resistor attenuators. Input signals are attenuated by ten to a full scale of +/- 1.0 volts before detection by the trigger circuit.

2) High speed , <25 Mhz, single ended (FAST mode) with 50 ohm input impedance,(optional AC coupling) full scale range of 2 volts (+/- 1.0 volts).

In the NORM mode two options are available for further signal conditioning before trigger detection:

1) A low frequency notch filter with variable Q control. The notch reject frequency is resistor selectable.

2) A true RMS to DC converter with a usable frequency range to 1 Mhz. The converter has typically 5% ripple at 10 hz and < 1% ripple above 100 hz.

Each channel also has a strapable 4 bit code which can be read by the computer to identify how the channel was configured. The analog outputs (+/- 1 volts max) from the signal conditioning circuits are inputted to trigger detection circuits which generate TTL level signals. Each trigger circuit can be programmed for the following:

1) Upper and Lower Threshold: The upper threshold is used for positive/negative edge detection and for window mode. It is programmable over a +/- 1.0 volt interval. The lower threshold is used only for window mode and is also programmable over +/- 1.0 volts. Both levels are programmable with an 8 bit resolution (1 part in 255) over the output range.

2) SLOPE: A trigger can be generated after detection of a signal transition above (positive) or below (negative) the upper threshold level. Once triggered the output will remain active for a programmed time interval (pulsed mode) or until reset (toggled mode). A window mode which generates a trigger any time the signal is above the upper threshold or below the lower threshold is also available. In this mode the trigger is active the entire time the signal is outside the window limits.

3) SELECT: Enables or disables a trigger output.

4) LOGIC:
   a) OR ENABLE: enables the trigger output to be OR'd with the output of other OR ENABLE'd channels or the external OR input.
   b) AND ENABLE: enables the trigger output to be AND'd with the output of other AND ENABLE'd channels or the external AND input.

5) PULSED OR TOGGLED: The output from the trigger detection circuit can be either a pulse of programmable width or a static level which must be reset by the computer or the ARM signal. The window mode is a time over threshold trigger only.

6) PULSE WIDTH: The trigger output pulse width is programmable over a range of 1 to 256 times a clock oscillator period. Each trigger circuit has its own RC clock whose frequency is adjusted by capacitor selection, normally 10ns per period. (Factory Default)

In addition to the above there is a universal ARM signal which must be active to allow any channel to trigger. This signal is a TTL high (an internal pullup resistor will normally ARM the channels if no external signal is being applied) and a low ARM signal will clear all trigger outputs.

The outputs from the trigger detectors are directly available through the front panel connectors (TTL high signals, capable of driving 50 ohms). Also the combinatorial logic outputs OR and AND are available. The OR signal will be TTL high whenever one or more of the 'OR' enabled channels or external 'OR' logic is TTL high. The external OR signal is pulled down by an internal resistor and need not be present to enable 'OR' logic. The AND signal will be TTL high whenever all of the 'AND' enabled channels and external 'AND' logic are TTL high. The external 'AND' signal is pulled high by an internal resistor and need not be present to enable the 'AND' logic. An additional logic feature allow the output of the AND logic to be gated into the OR logic.

A status bit from each of the trigger circuits is available for computer monitoring using the F(2)A(1) command. These bits are set whenever a trigger is generated and remain on until reset by the clear lam command F(10)A(0).

FRONT PANEL INDICATORS & CONTROLS:

N LED: Active whenever the module is addressed with a valid CAMAC command.

FRONT PANEL INPUT SIGNALS:

OR: A TTL high signal (510 ohms to ground), LEMO type connector, which is OR'd with the internal logic OR circuit allows cascading of 1024 modules.

AND: A TTL high signal (10 Kohms to +5.0 volts), LEMO type connector, which is AND'd with the internal logic AND allows cascading of 1024 modules.

ARM: A TTL high signal(10 Kohms to +5.0 volts), LEMO type connector, enables all channels to trigger. Switching the signal to TTL low will clear triggered outputs.

SIGNAL IN: Four analog input signals either differential or single ended.
Connector: Four, two position Lemo connectors. Male pin is positive input.
Signal inputs also available from rear panel flat cable.

FRONT PANEL OUTPUT SIGNALS:

CHANNEL OUT: Four individual trigger outputs, active TTL high level, LEMO type connector, minimum load of 50 ohms.

OR: Active TTL high level whenever OR logic is true, LEMO type connector

AND: Active TTL high level whenever AND logic is true, LEMO type connector.

REAR PANEL INPUT SIGNALS:

CHANNEL IN: Four analog input signals either differential or single ended.
Connector : 40 pin flat cable connector.
See Jumper Location drawing signal pinout. Front Panel inputs available.

CAMAC CONTROL:

The following list describes the response of the 1024 to the CAMAC dataway commands. All commands require N(Station Number) and return X=1 and Q=1 unless stated.

F(0).A(i-1) Read channel(i) upper threshold, on
n = 0..3 R8-R1, see F(16).A(n).

F(0).A(n) Read channel(i) lower threshold, i = n - 3, on
n= 4..7 R8-R1, see F(16).A(n).

F(1).A(n) n = 0..3 — Read trigger channel(i) status, i = 1 + n, on R8-R1, see F(17).A(n).

R2, R 1: Slope selection:
0: Negative slope
1: Positive slope
2: Window mode

R 3: Mode:
0: Single event (toggled mode) - trigger remains on until reset by ARM or F(10).A(0).
1: Multiple event(pulsed mode) - trigger output pulse width is programmable (see F(17).A(n)).

R 4: OR logic:
0: Disable channel's trigger output for OR logic.
1: Enable channel's trigger output for OR logic.

R 5: AND logic:
0: Disable channel's trigger output for AND logic.
1: Enable channel's trigger output for AND logic.

R 6: Trig Enable:
0: Disable channel from triggering.
1: Enable channel for triggering.

R 8: AND/OR logic (channel 1 only).
0: Disable AND/OR logic.
1: Enable AND/OR logic.
(i.e. if R8 is one for channel 1 then the output of the AND logic is gated into the OR logic.)

F(1).A(n) n = 4..7 — Read channel(i) pulse width control, i = n - 3, on R8-R1, see F(17).A(n).

F(2).A(0) — Read ARM status and 'OR','AND' LAM status.

R1: 1 if trigger channels ARMed.
R2: 1 if OR logic triggered.
R3: 1 if AND logic triggered.

F(2).A(1) Read internal LAM status.
R(n) : 1 if channel triggered, n = channel nu.
R5 : 1 if AND logic triggered
R6 : 1 if OR logic triggered

F(3).A(0) Read module I.D.
(R16-R1) = 1024

F(3).A(n) n= 8..11 — Read channel(i) signal conditioning plug-in I.D. for i = n-7.

F(8).A(0) — Read internal LAM status:
Q = 0 of internal LAM not on.
Q = 1 if internal LAM on.
(The internal LAM is on whenever any channel, the 'OR' or 'AND' logic triggers).

F(10).A(0) — Clear internal LAM status; clear triggers and trigger logic.

F(16).A(n) n = 0..3 — Write channel(i) upper threshold, i = n + 1, on W8-W1. Thresholds are programmable over a +\- 1.0 volt range (0 = +1.0 volts, 255 = -1.0 volts). The 1024 is normally delivered with a divide by 10 attenuator for the NORM input.

F(16).A(n) n= 4..7 — Write channel(i) lower threshold ,i= n - 3, on W8-W1. Thresholds are programmable over a +\- 1.0 volt range (0 = +1.0 volts, 255 = -1.0 volts). The 1024 is normally delivered with a divide by 10 attenuator for the NORM input.

F(17).A(n) n = 0..3 — Write channel(i) n trigger status, i = n + 1, on W8-W1,

W2, W 1: Slope selection:
- 0: Negative slope
- 1: Positive slope
- 2: Window mode

W 3: Mode:
- 0: Single event (toggled mode) - trigger remains on until reset by ARM or F(10).A(0).
- 1: Multiple event(pulsed mode) - trigger output pulse width is programmable (see F(17).A(n)).

W 4: OR logic:
- 0: Disable channel's trigger output for OR logic.
- 1: Enable channel's trigger output for OR logic.

W 5: AND logic:
- 0: Disable channel's trigger output for AND logic.
- 1: Enable channel's trigger output for AND logic.

W 6: Trig Enable:
- 0: Disable channel from triggering.
- 1: Enable channel for triggering.

W 8: AND/OR logic (channel 1 only).
- 0: Disable AND/OR logic.
- 1: Enable AND/OR logic.

(i.e. if R8 is one for channel 1 then the output of the AND logic is gated into the OR logic.)

F(17).A(n) n = 4..7 — Write channel(i) (PW) pulse width control ,i = n - 3, on W8-W1.
PW = 254 then triggered output = 10 usec +/- 20%
= 0 then triggered output = 1.5msec +/- 20%
The RC clocks which control the pulse width are factory set to an approximate period of 6 usec. There is an extra 4 usec. turnon delay.

F(24).A(0) — Disable the CAMAC dataway LAM.

F(25).A(n) n = 0..3 — Trigger channel(i), i = n + 1. Requires the channel to be armed and enabled, F(17)A(n)W(6).

F(26).A(0) — Enable the CAMAC dataway LAM.

Z — Clear internal LAM status; clear triggers and trigger logic. Disable CAMAC LAM.

C — Same as Z.

COMPUTER PROGRAMMING THE 1024

The following examples shows how to setup channel 1 for positive slope detection at 0.0 volts threshold, enable channel 1 for the OR logic and detect if the trigger occurred.

Note: the command

a) camo(n,f,a,d,q,x) writes a command to the 1024 module.

b) cami(n,f,a,d,q,x) reads a command from the 1024 module.

c) n=station number

d) f=function commands, a = subaddress

e) $d=data ,binary
d=data ,decimal

f) q,x = q & x response

```
camo(n,17,0,$00101101,q,x);     enable channel1, pulsed mode, OR enabled
                                note- channels 1,2,4 should be disabled.

camo(n,17,8,0        ,q,x);     pulse width = app. 1.5 msec.

camo(n,16,0,128      ,q,x);     upper threshold = 0.0 volts.

camo(n,10,0,0        ,q,x);     clear old triggers, & status bits

camo(n,26,0,0        ,q,x);     enable LAM interrupt;

wait for LAM interrupt
  or do
cami(n,8,0,0 ,q,x);             q =1 if any trigger occurred.

cami(n,2,1,data      ,q,x);     read trigger status bits:
                                     R1 = 1 if channel 1 triggered.
                                     R6 = 1 if channel 1 triggered.

camo(n,10,0,0        ,q,x);     clear triggers and LAM status bits.
```

THEORY OF OPERATION

(refer to FIG 3 and schematics)

Signal conditioning:

Each of the four analog channels is composed of identical circuits. For the FAST mode the single ended signal is terminated to with a 51 ohm resistor and then inputted directly to the comparators. For the NORM mode the differential signals are attenuated through compensated divide by ten circuits composed of R20, R24, C12, C13 and R21, R22, C15, and C14. Capacitors C14 and C13 are adjusted to give the best square wave response. Op amps 1J and 2J convert the differential NORM signals to a single ended signal which can be connected to the signal conditioning circuits or directly to the comparators.

Trigger detection:

I.C. G1 is a dual comparator which sets the thresholds for trigger detection. The upper comparator , pins 1,2, and 4 are used for positive, negative and window detect modes. The lower comparator, pins 11,12 and 9 are used only for the lower window detect mode. The thresholds are programmable over a plus one to minus one volt range. The PAL at 8D contains all the logic necessary for the various detection modes. In the toggle mode, once a trigger is detected then 8D pin 19 will go low to enable the a programmable pulse width to be generated by the RC clock at 5D and counter 7C.

Logic detection:

I.C. 9K contains all logic for the OR and AND logic detection. For OR logic, only channels that are OR enabled will input pulses to 9K. For AND logic, channels that are NOT enabled will ALWAYS be TTL high.

JUMPER OPTIONS and COMPONENT SELECTION
(refer to jumper location drawing and schematics)

JUMPER OPTIONS:

1) Signal inputs from rear connector: (J1)
Up to 8 differential signals [8 signals(+) and their referenced grounds(-)] are available on the forty pin rear connector. Jumpers near J1 allow connecting:

Signal 1 + or Signal 5+ to Channel 1+ ;
Signal 1 - or Signal 5- to Channel 1- ;
Signal 2 + or Signal 6+ to Channel 2+ ;
Signal 2 - or Signal 6- to Channel 2- ;
Signal 3 + or Signal 7+ to Channel 3+ ;
Signal 3 - or Signal 7- to Channel 3- ;
Signal 4 + or Signal 8+ to Channel 4+ ;
Signal 4 - or Signal 8- to Channel 4- ;

This allow two 1024 modules to monitor 8 signals on the same cable.

2) FAST MODE: (high frequency, 50 ohm termination, single ended; signal is inputted through Ch - pin on rear connector.)

D.C. coupling: E16 - E17 (connects Ch + to gnd)
E1 - E7 (connects Ch - to 51 ohm)
E11 - E15 (connects Ch - to comparators)

A.C. coupling: E1 - E3 (connects Ch - to C16)
E5 - E7 (connects C16 to 51 ohm)
E16 - E17 (connects Ch + to gnd)
E11 - E15 (connects Ch - to comparators)

Note: For norm mode, a single ended signal applied to the Ch - input will appear inverted at the comparators.

3) NORM MODE: (low frequency, 1 Mohm termination,differential)

D.C. coupling: E1 - E2 (connects Ch - to attenuator)
A.C. coupling: E1 - E3 (connects Ch - to C16)
E5 - E2 (connects C16 to attenuator)

4) NORM MODE: (low frequency, 1 Mohm termination,single ended)
D.C. coupling: E16 - E17 (connects Ch + to gnd)
A.C. coupling: same as 3

5) SIGNAL CONDITIONING OPTIONS (NORM MODE ONLY):

a) Output of NORM signal conditioning circuit connected to comparators.
: E12 - E15 (output of norm connected to comparators)

b) Output of NORM signal conditioning circuit connected to RMS circuit.
Output of RMS circuit connected to comparators.

: E8 - E9 (output of norm connected to rms circuit
: C18 + E15 (output of RMS connected to comparators)

c) Output of NORM signal conditioning circuit connected to NOTCH filter.
Output of NOTCH filter connected to RMS circuit.
Output of RMS circuit connected to comparators.

: E10 - E9 (output of NOTCH connected to rms circuit)
: C18 + E15 (output of RMS connected to comparators)

COMPONENT SELECTION

1) A.C. COUPLING : C16, user selectable.

2) NORM mode attenuator: Factory set for divide by ten, 1 megohm impedance.. Select R21,R22 and R20,R24 for other attenuation/impedances. For other attenuations C15 and C12 must also be changed. Adjust C13,C14 for correct A.C. responses.

3) Pulse width control : The range of the trigger output pulse width can be changed by selection of C11.

4) RMS detector : The 1024 uses an Analog Devices AD637 RMS detector. The user should refer to the data sheet characteristics which are affected by the value of C18.

5) Notch Filter :

$$F0 = \frac{1}{2\pi L\,(R31)\,(C19)}$$

R31 = R25 = (R32)/2
C19 = C20 = 2(C17)

For 60Hz
C19 = 6800pF
R21 = < 390k

Q Adjustable by R26

THE DSP ISA (Integrated Signal Acquisition) SYSTEM

Multi-channel signal acquisition systems which digitally record many analog signals typically encounter two problems which grow in severity as the number of channels increases:

1) Users need to be assured of system integrity from signal input through to the computer interface.

2) Recording triggers must be reliable and flexibly configured.

Either of these problems can be very costly due to partial or complete data loss. The DSP ISA system has been developed to overcome both of these concerns resulting in data acquisition systems that are highly reliable.

System Integrity:

To insure system integrity at all times the computer must be able to determine that all data channels are operating correctly and are connected properly. The ISA system addresses the problem by designing in front end calibration for each signal conditioning channel (ex: DSP1402). Under computer command the signal conditioner can switch from the input signal to a programmed calibration signal. By digitizing the calibration signals one at a time the computer will determine:

1) That the correct signal conditioning module is connected to the correct ADC channel.

2) That the cabling between the signal conditioner and ADC is operative.

3) That the signal conditioning module is calibrated.

These measurements can be done very quickly and automatically by the computer.

ISA signal conditioners also have a rear panel analog bus which allows buffered, conditioned, signals from selected channels to be sensed by other acquisition modules such as the DSP 1024 (see fig 2 and 3). This allows the user to programmably reconfigure the trigger channels without physically altering the system cabling and possibly introducing errors.

Trigger Reliability:

Reliable recording triggers are perhaps the most difficult problem for multichannel systems. Many measurements can be performed only one time and faulty triggers can be fatal, resulting in complete data loss. The DSP model 1024 is a flexible trigger detection module which overcomes many of these problems.
To insure trigger integrity the trigger signal should be qualified by gating the signal of interest with other signals that must be present at the same time. The qualified signal becomes a 'master' trigger which is then sent to the recording instrumentation. This is similar to a digital logic analyzer which generates a trigger only when a predetermined digital pattern is present except the 1024 uses both analog and digital signals. The 1024 can generate the master trigger by logically gating triggers from four separate analog

channels plus external logic signals. By programming the unit the user can insure that a trigger only appears under the correct conditions (see fig 4). The 1024 capabilities include:

a) generating triggers from four separate analog signals. The user can program the trigger signals to be on permanently (toggle mode) or for a predetermined time duration (pulse mode).

b) logically gating the triggers together to generate a 'master' trigger. There are two logic combinations available: 'OR' and 'AND' gating:

   OR: A master trigger is generated whenever any one of the trigger or external 'OR' signals is present.

   AND: A master trigger is generated only when all of the enabled trigger signals are present. Since the 1024 allows programming the width of the trigger pulses, the user can create a 'trigger window' in which two or more signals must be present before the master trigger is generated. The duration of the shortest pulse will determine the window time (see fig 4).

c) An ARM signal which enables or disables all triggers using an external control signal.

d) Trigger signals can also be generated by a computer command which can simulate trigger timing and check the system response to the master trigger.

REAR PANEL INPUTS CONFIGURATION

1	gnd	
2	Ch1 -	
3	Ch1 +	
4	gnd	
5	Ch2 -	
6	Ch2 +	
7	gnd	
8	Ch3 -	
9	Ch3 +	
10	gnd	
11	Ch4 -	
12	Ch4 +	
13	gnd	Strap Selectable
15	Ch5 -	|/
16	Ch5 +	
17	Ch6 -	
18	Ch6 +	
19	gnd	
20	Ch7 -	
21	Ch7 +	
22	gnd	
23	Ch8 -	
24	Ch8 +	
25	gnd	
26-40	Not Used	

Assembly: A-1024-01 (ASSY: PCB, 1024 4CH SIGNAL CONDITIO)
Revision: C
As of: 04/21/90

	Component	Description	Qty Per
1.	0100-0102	RES: RC07 1K OHM 5% 1/4W	12.00
2.	0100-0103	RES: RC07 10K OHM 5% 1/4W	5.00
3.	0100-0223	RCF 5% 1/4W CF RESISTOR R=22K	1.00
4.	0100-0241	RES 5% 1/4W CC RESISTOR R=240	2.00
5.	0100-0244	RES 5% 1/4W CC RESISTOR R=240K	4.00
6.	0100-0272	RES 5% 1/4W CC RESISTOR R=2.7K	2.00
7.	0100-0511	RES 5% 1/4W CC RESISTOR R=510	5.00
8.	0100-0512	RES 5% 1/4W CC RESISTORR R=5.1K	1.00
9.	0150-0511	RMF RN55D 1% RESISTOR R=5i.1	4.00
10.	0150-1001	RES 1% 1/4W MF RESISTOR R=1.00K	41.00
11.	0150-1004	RMF RN55D 1% METAL FILM RES R=1.00M	8.00
12.	0150-1103	RES: 1%,1/4W,R=110K	8.00
13.	0150-2001	RES RN55D 1% 1/4W R=2.00K	2.00
14.	0150-3011	RMF RN55D 1% METAL FILM RES R=3.01K	1.00
15.	0201-0102	RPK RES PK BNS 4310R-101-102	4.00
16.	0500-0101	CSM C=100PF CDE # CD5FC101J03	1.00
17.	0520-0103	CMC C=0.01UF MONO CENTRALAB CZ20H1	4.00
18.	0520-0104	CMC 0.1UF CNTLB:CZ20H104M2 KEM:C322	74.00
19.	0520-0105	CMC C=1.0UF MONO 50WVDC KEM# C320	1.00
20.	0600-0226	CTE C=22UF 10WVDC TANTALUM	4.00
21.	0600-0475	C TANT 4.7MF 10% 35V	3.00
22.	0750-0003	CCV C=5.5-18PF VAR JOHANSON JFD D	8.00
23.	1000-4448	DGS DIODE SIL. SWITCH 1N4448	32.00
24.	1010-2811	DSS DIODE H.P.5000-2811	2.00
25.	1030-4003	DSR 1AMP 1N4003	1.00
26.	1030-5624	DSR: DIODE RECT 3A GE 1N5624/BYM56	1.00
27.	1750-0001	ICS SN7401	1.00
28.	1750-0128	ICS SN74128	2.00
29.	1750-0154	ICS SN74154	1.00
30.	1760-0000	ICS SN74L500	1.00
31.	1760-0004	ICS SN74LS04	2.00
32.	1760-0074	ICS SN74LS74	1.00
33.	1760-0132	ICS SN74LS132	2.00
34.	1760-0138	ICS SN74LS138	2.00
35.	1760-0221	ICS SN74LS221	1.00
36.	1760-0244	ICS SN74LS244	1.00
37.	1760-0374	ICS SN74LS374	4.00
38.	1760-0393	ICS SN74LS393	4.00
39.	1760-0640	ICS SN74LS640	1.00
40.	1760-0642	ICS SN74LS642	1.00
41.	1760-0643	ICS SN74LS643	4.00
42.	1770-0004	ICS IC LSTTL HEX INV SN74S04	1.00
43.	1851-0037	PRM: PROG/F 1850-0001,1024-01 5A	1.00
44.	1851-0038	PRM: PROG/F 1850-0001, 1024-01 10A	1.00
45.	1857-0020	PAL: PROG/F 1856-4104, 1024-01 8D,F	4.00
46.	1857-0021	PAL: PROG/F 1856-4010, 1024-01 5K	1.00

| | Component | Description | Qty Per |

Assembly: A-1024-01 (ASSY: PCB, 1024 4CH SIGNAL CONDITIO)

DSP Technology Inc.

B I L L O F M A T E R I A L R E P O R T

Date: 04/24/90
Page: 1

As of	Until	Reference
08/19/87	12/31/99	R36,R37,R41
07/02/87	12/31/99	R7,R9,R16,R43,R44
02/22/87	12/31/99	R11
02/21/87	12/31/99	R13,R14
07/22/87	12/31/99	R42
02/21/87	12/31/99	R12,R15
03/08/87	12/31/99	R5,R6,R17-R19
02/21/87	12/31/99	R8
02/21/87	12/31/99	R23
08/19/87	12/31/99	R2,R27-R30,R33-R35 R38-R40
02/22/87	12/31/99	R20,R21
05/20/87	12/31/99	R22,R24
08/19/87	12/31/99	R1,R4
02/21/87	12/31/99	R3
02/21/87	12/31/99	RP1-RP4
05/20/87	12/31/99	C2
08/19/87	12/31/99	C8-C11
07/22/87	12/31/99	C23,C24
02/21/87	12/31/99	C3
05/20/87	12/31/99	C18
08/19/87	12/31/99	C1,C4-C7
02/21/87	12/31/99	C13,C14
02/21/87	12/31/99	CR6-CR13
05/20/87	12/31/99	CR3,CR4
02/21/87	12/31/99	CR1
02/21/87	12/31/99	CR2
02/21/87	12/31/99	7H
02/21/87	12/31/99	5G,10K
02/21/87	12/31/99	9F
02/21/87	12/31/99	4H
03/08/87	12/31/99	5E,5J
02/21/87	12/31/99	11K
02/21/87	12/31/99	5D,5H
02/21/87	12/31/99	9E,10E
02/21/87	12/31/99	9D
02/21/87	12/31/99	9H
02/21/87	12/31/99	7D,7F,7H,7K
02/21/87	12/31/99	7C,7E,7G,7J
02/21/87	12/31/99	8H
02/21/87	12/31/99	11H
02/21/87	12/31/99	8C,8E,8G,8J
03/08/87	12/31/99	5C
05/20/87	12/31/99	9H
05/20/87	12/31/99	10H
05/20/87	12/31/99	8D,8F,8H,8K
05/20/87	12/31/99	9K

As of	Until	Reference

Assembly: A-1024-01 (ASSY: PCB, 1024 4CH SIGNAL CONDITIO)
Revision: 2
As of: 04/21/90

	Component	Description	Qty Per	As of	Until
47.	1857-0022	PAL: PROG/F 1856-0106, 1024-01 9G	1.00	05/20/87	12/31/99
48.	1857-0023	PAL: PROG/F 1856-4102, 1024-01 9C	1.00	05/20/87	12/31/99
49.	1857-0024	PAL: PROG/F 1856-4008, 1024-01 6A	1.00	05/20/87	12/31/99
50.	1857-0025	PAL: PROG/F 1856-4102, 1024-01 5A	1.00	05/20/87	12/31/99
51.	1910-0005	IC: CMOS, HM6264ALSP-12	1.00	02/21/87	12/31/99
52.	2000-0082	ICS DUAL OP AMP FET TI TL082CP	13.00	05/20/87	12/31/99
53.	2010-0521	ICA IC SIGNETICS NE521N	4.00	02/21/87	12/31/99
54.	2020-0002	ICA VOLTAGE REF PMI REF02AHP	1.00	02/21/87	12/31/99
55.	2030-0317	ICS IC VOL REG NAT LM317T	1.00	02/21/87	12/31/99
56.	2030-0337	IC: VOLT REG, NEG ADJ, LM337T	1.00	02/21/87	12/31/99
57.	3100-0402	FUS FUSE 4AMP LITTLEFUSE 251004	4.00	05/20/87	12/31/99
58.	5000-0008	SKT CAMBION 703-1308-01-04-10	8.00	05/20/87	12/31/99
59.	5000-0014	SKT CAMBION 703-1314-01-04-10	4.00	08/19/87	12/31/99
60.	5000-0016	SKT CAMBION 703-1316-01-04-10	10.00	05/20/87	12/31/99
61.	5000-0020	SKT CAMBION 703-1320-01-04-10	1.00	05/20/87	12/31/99
62.	5250-3703	JCK FUS CAMBION 450-3703-01-08-00	32.00	08/19/87	12/31/99
63.	5251-0001	JMP CAMBION 481-2251-01-03-10	8.00	01/01/88	12/31/99
64.	5500-0018	HDR 40 PIN R/A 4 WALL 3M#3595-5002	1.00	02/22/87	12/31/99
65.	6520-7226	DAC: 8BIT,QUAD,CMOS, AD7226KN	2.00	02/21/87	12/31/99
66.	6849-0002	INS BERGQUIST 3223-07-FR-54	2.00	08/19/87	12/31/99
67.	6850-0001	RAIL: GUIDE, MDL, 5 HOLE, C-BORE	2.00	05/20/87	12/31/99
68.	7000-0058	PCB DWG# 1024-01-PD	1.00	05/20/87	12/31/99
69.	7410-0003	HWD: SWAGE TYPE STANDOFF	6.00	05/20/87	12/31/99
70.	8200-0001	BAT BATTERY DURACELL DL 1/3N W TABS	1.00	05/20/87	12/31/99
71.	DOCUMENTATION	PER ASSY DWG REFERENCE	2.00	04/16/87	12/31/99

Component	Description	Qty Per	As of	Until

Assembly: A-1024-01 (ASSY: PCB, 1024 4CH SIGNAL CONDITIO)

Reference

9G
9C
6A
5A
11C
3B, 1C, 2C, 3D, 1E, 2E, 3F 1G, 2G, 3H, 1J, 2J, 3K
4D, 4F, 4H, 4K
3A
VR1
VR2
F1-F4
8D, 8F, 8H, 8K, 5A, 6A, 9C 9K
3C, 3E, 3G, 3J
9A, 10A, 8D, 8F, 8H, 8K 5A, 6A, 9C, 9K
9G
F1-F4 CH1-CH4
CH1 THRU CH4
J1
5F, 5K
VR1, VR2

BAT
1024-01 AD 1024-01 CD

Reference

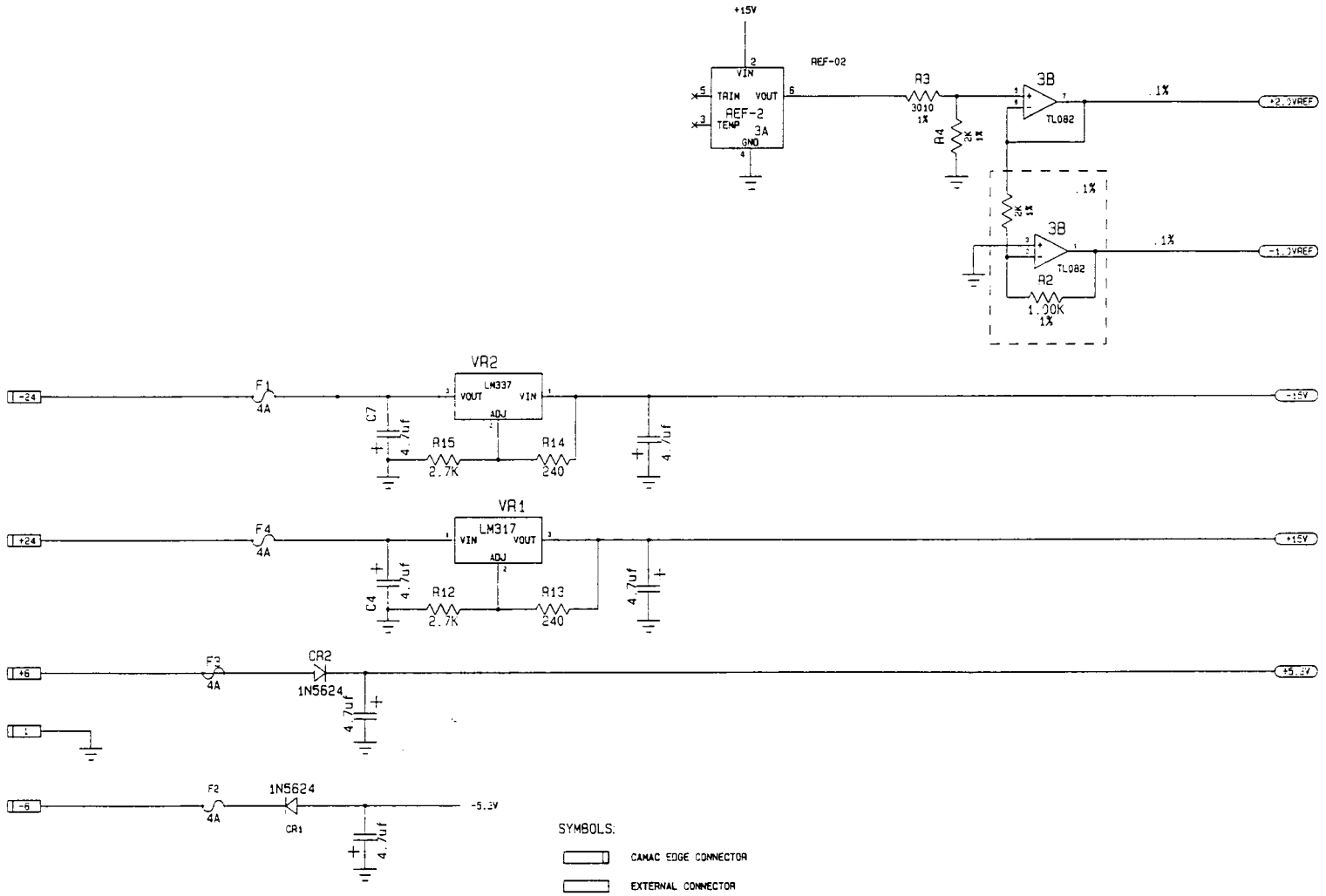
SINGLE LEVEL BILL OF MATERIAL
AS OF 06/28/88

ASSEMBLY P/N A-1024-02 REV A
DESCRIPTION ASSY: F/P MECH, 4CH SIGNAL CONDITIO

PART NUMBER	DESCRIPTION	QTY PER	AS OF	UNTIL	REFERENCE
1040-0001	DLE LED GREEN LITRONIX#LD37-2	1	3/08/87	12/31/99	
5510-0004	CON RT ANGLE LEMO RPL00.250TEF	9	3/08/87	12/31/99	J2-J8, P2, P5
5511-0001	CON PNL MT 2P LEMO RA0.302NYL	4	12/01/87	12/31/99	
5511-0004	HDW GND LUG 2P LEMO #RA0.251	4	12/01/87	12/31/99	
6851-0073	PNL: FR, 1024	1	12/01/87	12/31/99	
6852-0001	SCR:FT PNL JCK DEUTCH D7500-4MM-B4	1	7/22/87	12/31/99	
6852-0031	PNL REAR #1 DWG #2812-03-FD	1	7/22/87	12/31/99	
8030-0003	CBL: TWIST,SHLD PAIR,TEFLON INS, 83	3	12/01/87	12/31/99	
A-1024-01	ASSY: PCB, 1024 4CH SIGNAL CONDITIO	1	5/11/87	12/31/99	

SINGLE LEVEL BILL OF MATERIAL - by Part Number - for Assembly A-1024-02

PART NUMBER DESCRIPTION QTY PER AS OF UNTIL REFERENCE



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL CAPACITORS ARE IN uf.
2. ALL RESISTORS ARE IN OHMS.

REV	DESCRIPTION	DATE
A	ECO1001	3/89
A	PROD. RELEASE	1/89

REVISIONS

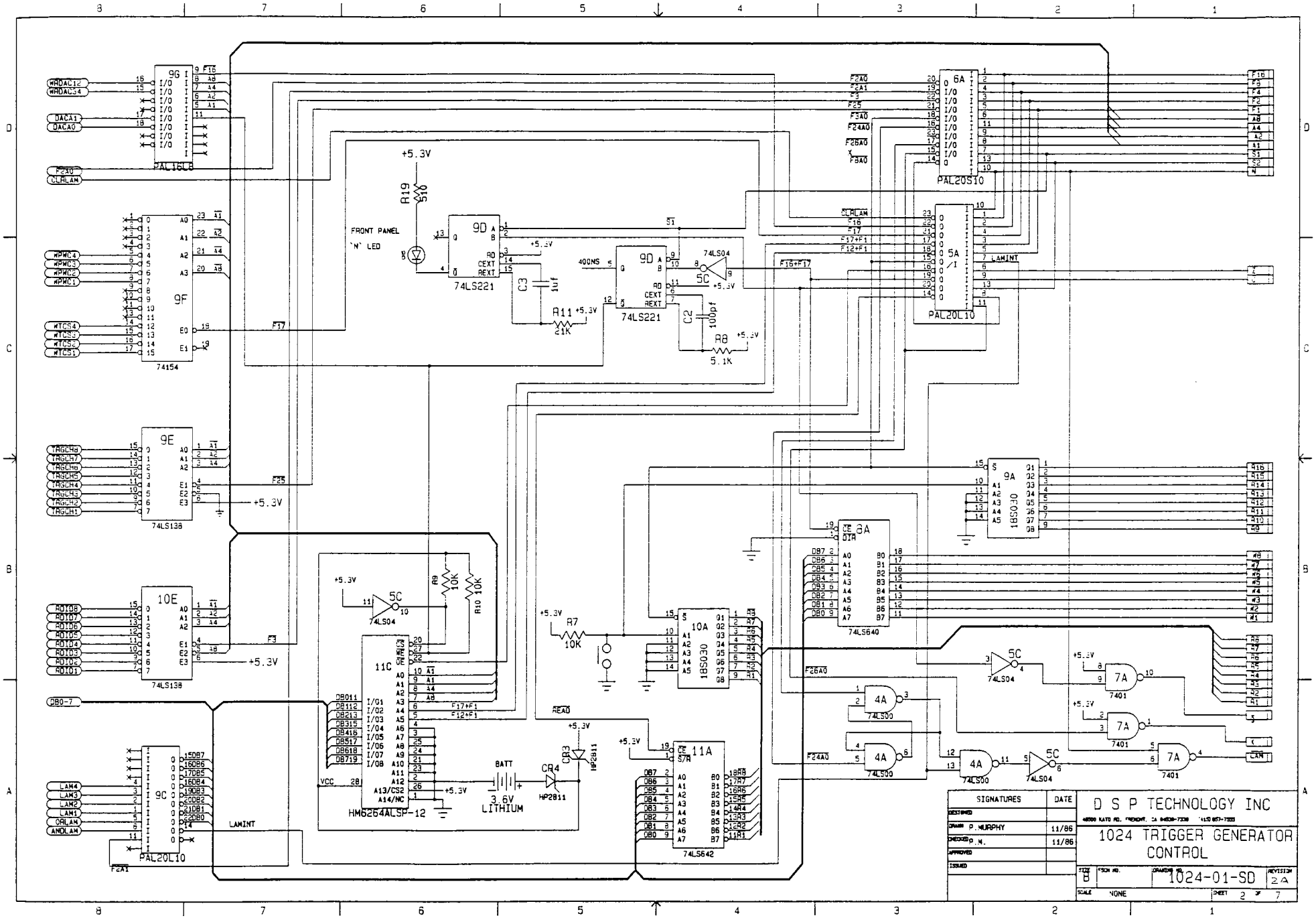
SIGNATURES		DATE
DESIGNED		
DRAWN	PATRICK MURPHY	11/86
CHECKED		
APPROVED	Pat Murphy	5/89
ISSUED		

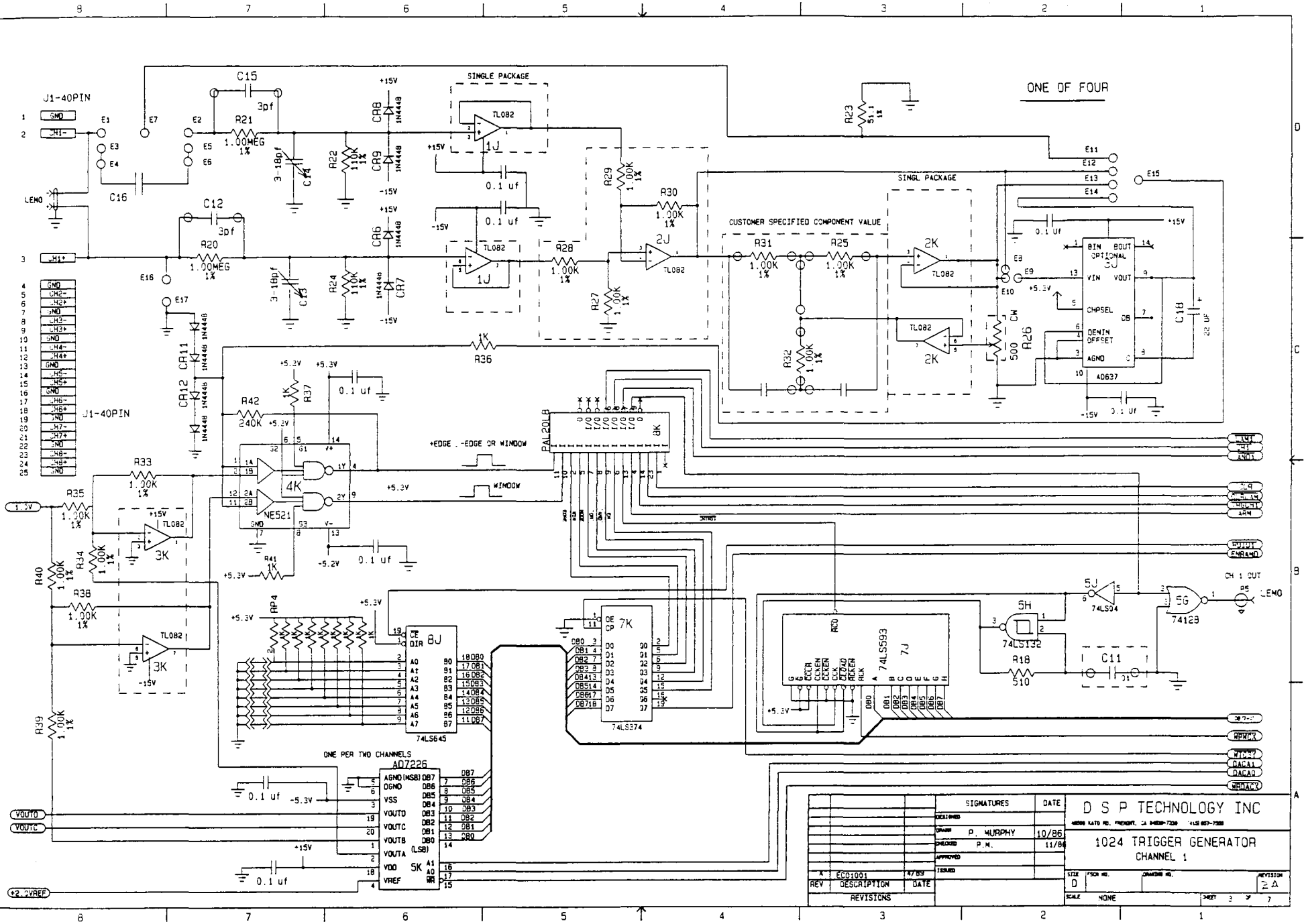
D S P TECHNOLOGY INC

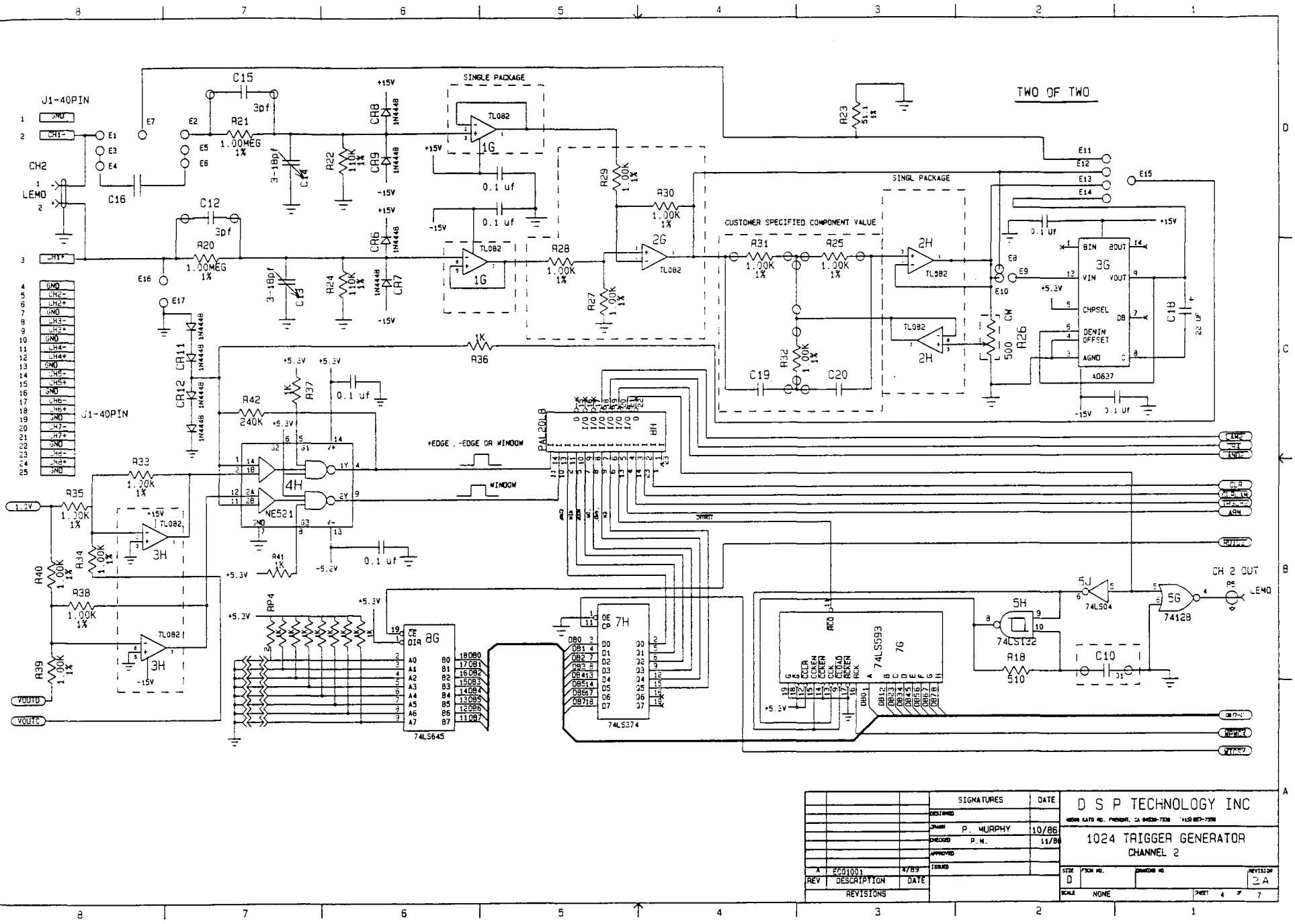
1024 TRIG GENERATOR

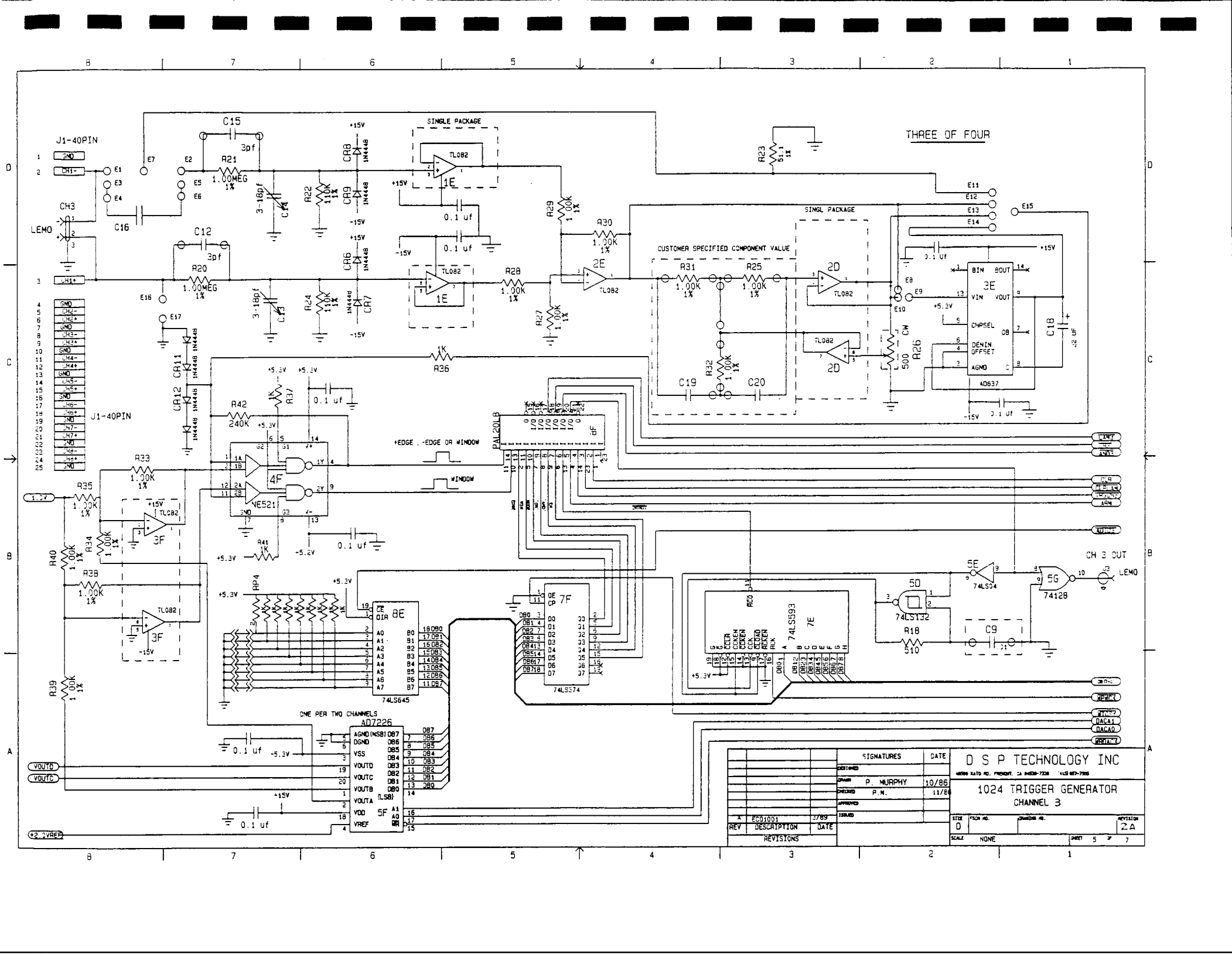
SIZE	SCH NO.	DRAWING NO.	REVISION
	01	1024-01-SD	2A

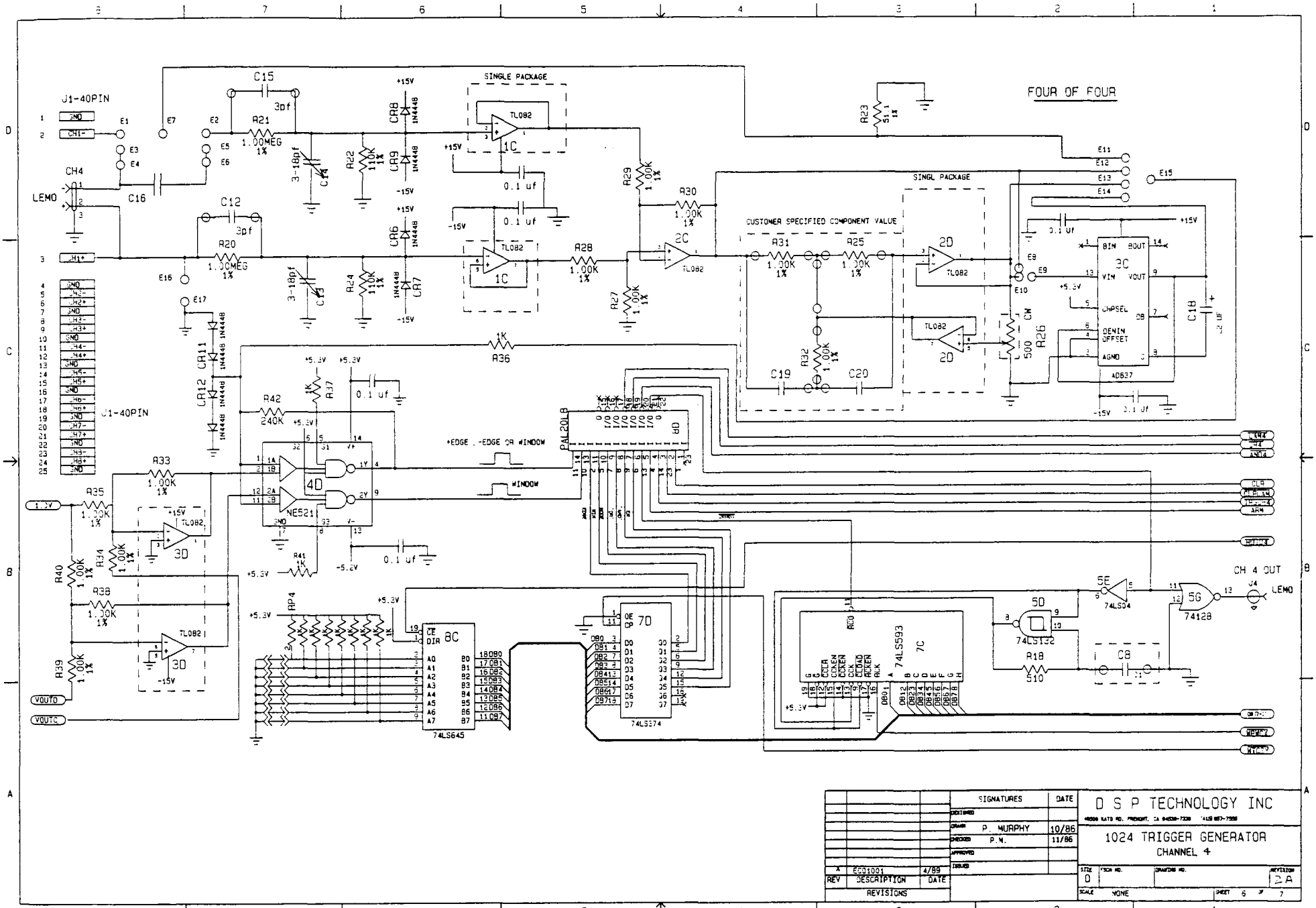
SCALE NONE SHEET 1 OF 7

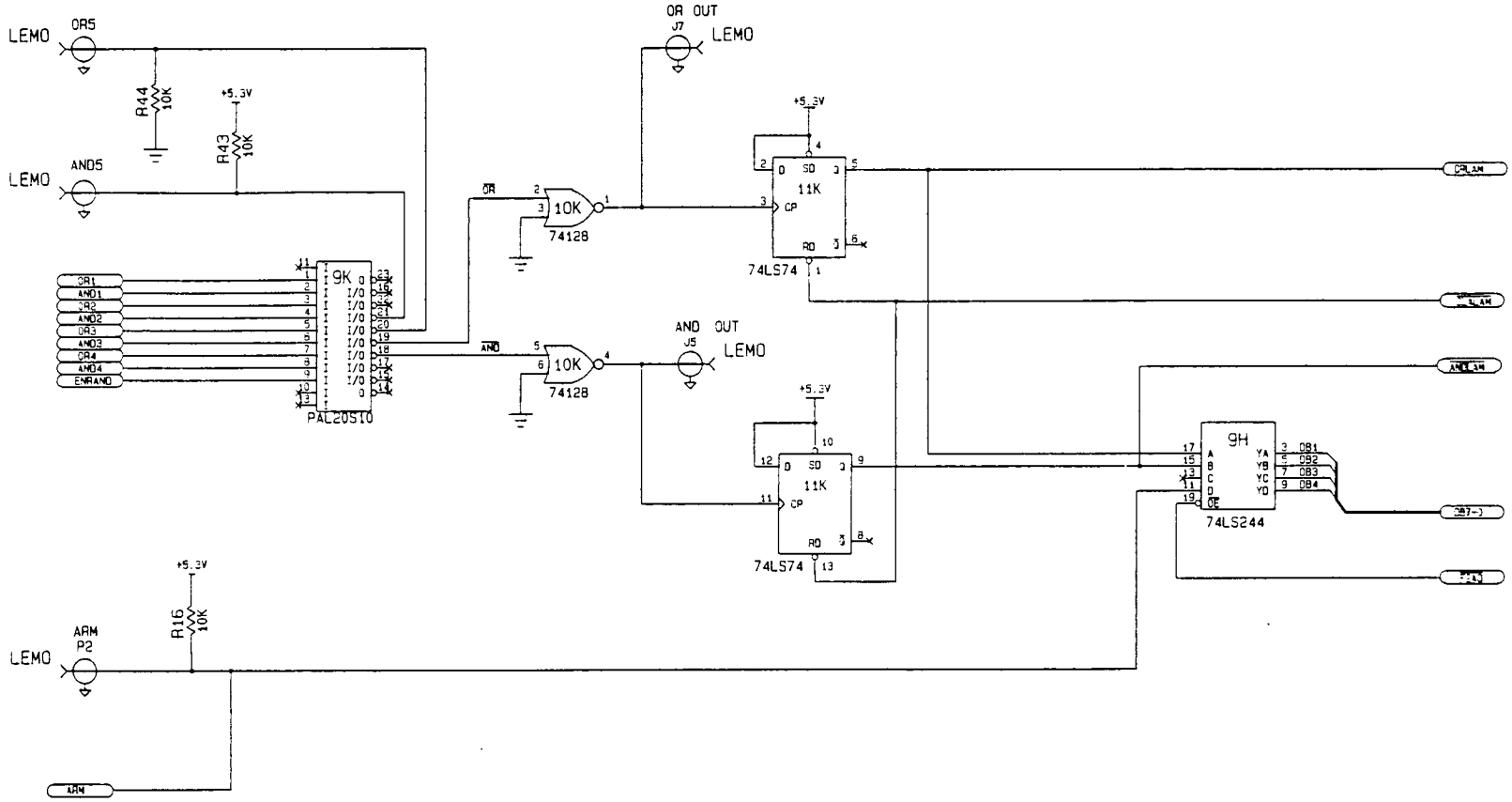

PAL16L8
74154
74LS138
74LS138
PAL20L10
PAL20S10
PAL20L10
74LS221
74LS221
74LS04
74LS640
74LS642
HM6264ALSP-12
3.6V LITHIUM
HP2811
FRONT PANEL LED
74LS00
7401
D S P TECHNOLOGY INC
1024 TRIGGER GENERATOR CONTROL
1024-01-SD
SIGNATURES
DATE
P. MURPHY
11/86
11/86
SIZE B
SCALE NONE
SHEET 2 OF 7


ONE OF FOUR
SINGLE PACKAGE
SINGL PACKAGE
CUSTOMER SPECIFIED COMPONENT VALUE
J1-40PIN
LEMO
TL082
NE521
PAL20L8
74LS645
74LS374
74LS593
74LS04
74128
74LS132
AD7226
AD637
ONE PER TWO CHANNELS
+EDGE . -EDGE OR WINDOW
WINDOW
CH 1 OUT
D S P TECHNOLOGY INC
1024 TRIGGER GENERATOR
CHANNEL 1
P. MURPHY
10/86
11/86
ECO1001
4/89
REVISIONS
SIGNATURES
DATE
SIZE
D
REVISION
2A
SCALE
NONE


TWO OF TWO
J1-40PIN
CH2
LEMO
SINGLE PACKAGE
SINGL PACKAGE
CUSTOMER SPECIFIED COMPONENT VALUE
TL082
AD637
PAL20L8
NE521
74LS645
74LS374
74LS593
74LS132
74LS04
74128
+EDGE . -EDGE OR WINDOW
WINDOW
CH 2 OUT
D S P TECHNOLOGY INC
1024 TRIGGER GENERATOR
CHANNEL 2
SIGNATURES
DATE
P. MURPHY
10/86
11/86
REVISIONS
ECO1001
4/89
SIZE D
SCALE NONE
REVISION 2A


THREE OF FOUR
J1-40PIN
CH3
LEMO
SINGLE PACKAGE
TL082
CUSTOMER SPECIFIED COMPONENT VALUE
SINGL PACKAGE
AD637
PAL20L8
+EDGE , -EDGE OR WINDOW
WINDOW
NE521
74LS645
74LS374
74LS593
74LS132
74LS04
74128
CH 3 OUT
LEMO
ONE PER TWO CHANNELS
AD7226
VOUTD
VOUTC
+2.2VREF
SIGNATURES
DATE
P. MURPHY
10/86
P.M.
11/86
REVISIONS
ECO1001
3/89
D S P TECHNOLOGY INC
1024 TRIGGER GENERATOR
CHANNEL 3
SIZE
D
REVISION
2A
SCALE
NONE


FOUR OF FOUR
J1-40PIN
LEMO
CH4
SINGLE PACKAGE
SINGL PACKAGE
CUSTOMER SPECIFIED COMPONENT VALUE
TL082
AD637
PAL20L8
74LS593
74LS374
74LS645
74LS132
74LS04
74128
NE521
CH 4 OUT
VOUTD
VOUTC
+EDGE, -EDGE OR WINDOW
WINDOW
1024 TRIGGER GENERATOR
CHANNEL 4
D S P TECHNOLOGY INC
P. MURPHY
10/86
P.M.
11/86
ECO1001
4/89
REVISIONS



REV	DESCRIPTION	DATE
A	ECO1001	4/89
A	PROD. RELEASE	4/89

REVISIONS

SIGNATURES	DATE
DESIGNED	
DRAWN J.CHURCH	4/89
CHECKED	
APPROVED	
ISSUED	

D S P TECHNOLOGY INC

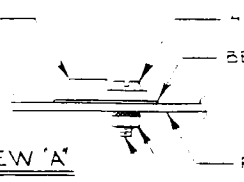
1024 TRIGGER GENERATOR
TRIGGER LOGIC

SIZE	FSCM NO.	DRAWING NO.	REVISION
		1024-01-SD	2A

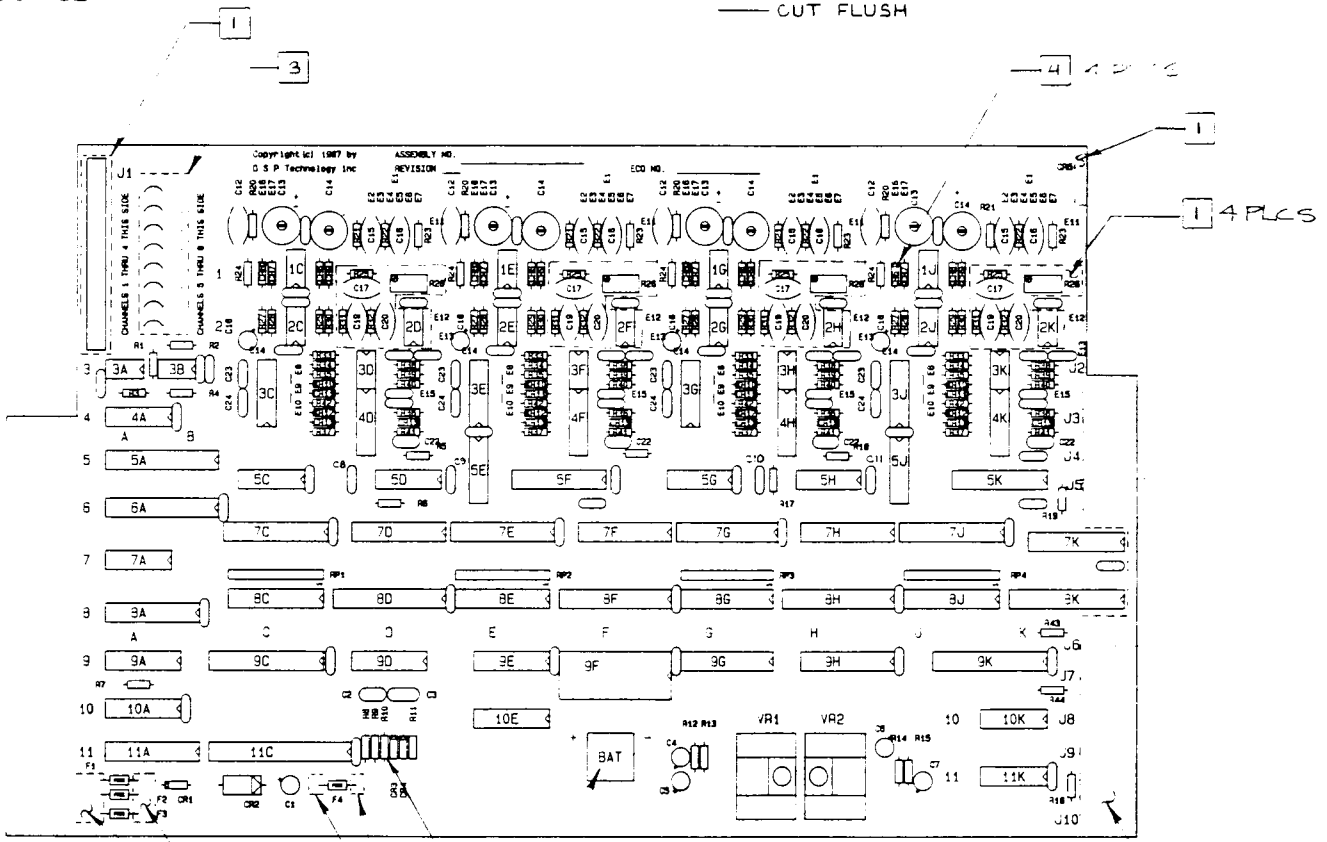
SCALE NONE SHEET 7 OF 7

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. MASK AREAS
2. MASK ALL "E" HOLES.
3. INSTALL ITEM (6) (CAMBION JACKS)
4. CR6 INSTALL IN REVERSE POLARITY INDICATED ON PCB.
5. INSTALL JUMPERS:
   E1 TO E2
   E12 TO E15
   CHANNELS 1 TO 4
6. DO NOT SOLDER POSITIVE TERMINAL
7. NO LOADS



VIEW 'A'
SCALE: NONE



MODEL 1024
PART NO. 7000-0058
REV. 2

SILKSCREEN (BODY)
SILKSCREEN COMP. SIDE

VIEW 'A'

SYM	DESCRIPTION	DATE	APPROVAL
A	ECO 00		

REVISIONS

MATERIAL: FR4
HEAT TREAT:
WEIGHT:
MISC.

FINISH:
DIMENSIONAL TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ANG.
XX± XXX± ±
SCALE NO REQ'D
NEXT ASSY

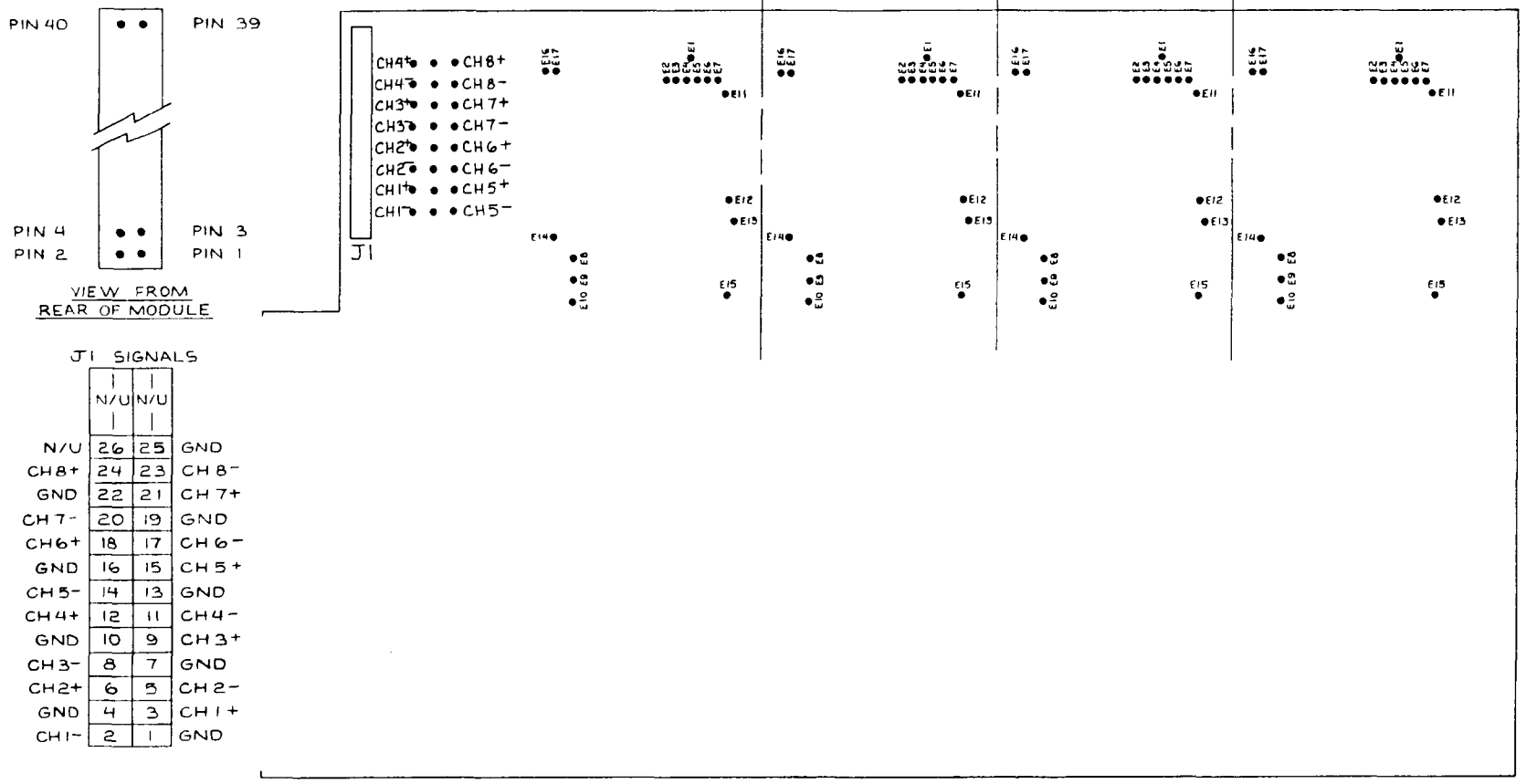
TITLE: ASSEMBLY 1024

DESIGN | DATE
DETAIL | DATE 10-30-87
CHECK | DATE
APPRO | DATE 3-24-88

dsp Technology

JOB NO.
SIZE | DRAWING NUMBER | ISSUE
C | A-1024-01-AD | 2

SHT 1 of 2



J1 SIGNALS

	N/U	N/U	
N/U	26	25	GND
CH8+	24	23	CH 8-
GND	22	21	CH 7+
CH 7-	20	19	GND
CH6+	18	17	CH 6-
GND	16	15	CH 5+
CH5-	14	13	GND
CH4+	12	11	CH4-
GND	10	9	CH3+
CH3-	8	7	GND
CH2+	6	5	CH2-
GND	4	3	CH1+
CH1-	2	1	GND

COMPONENT SIDE

SYM	DESCRIPTION	DATE	APPROVAL
	REVISIONS		

MATERIAL
HEAT TREAT
WEIGHT
MISC

FINISH
DIMENSIONAL TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL | ANG.
XX± | XXX± | ±
SCALE | NO REQ'D
NEXT ASS'Y

TITLE
1024,
JUMPER LOCATIONS

DESIGN		DATE	
DETAIL		DATE	3-13-87
CHECK		DATE	3-13-87
APPRO		DATE	

dsp Technology Inc

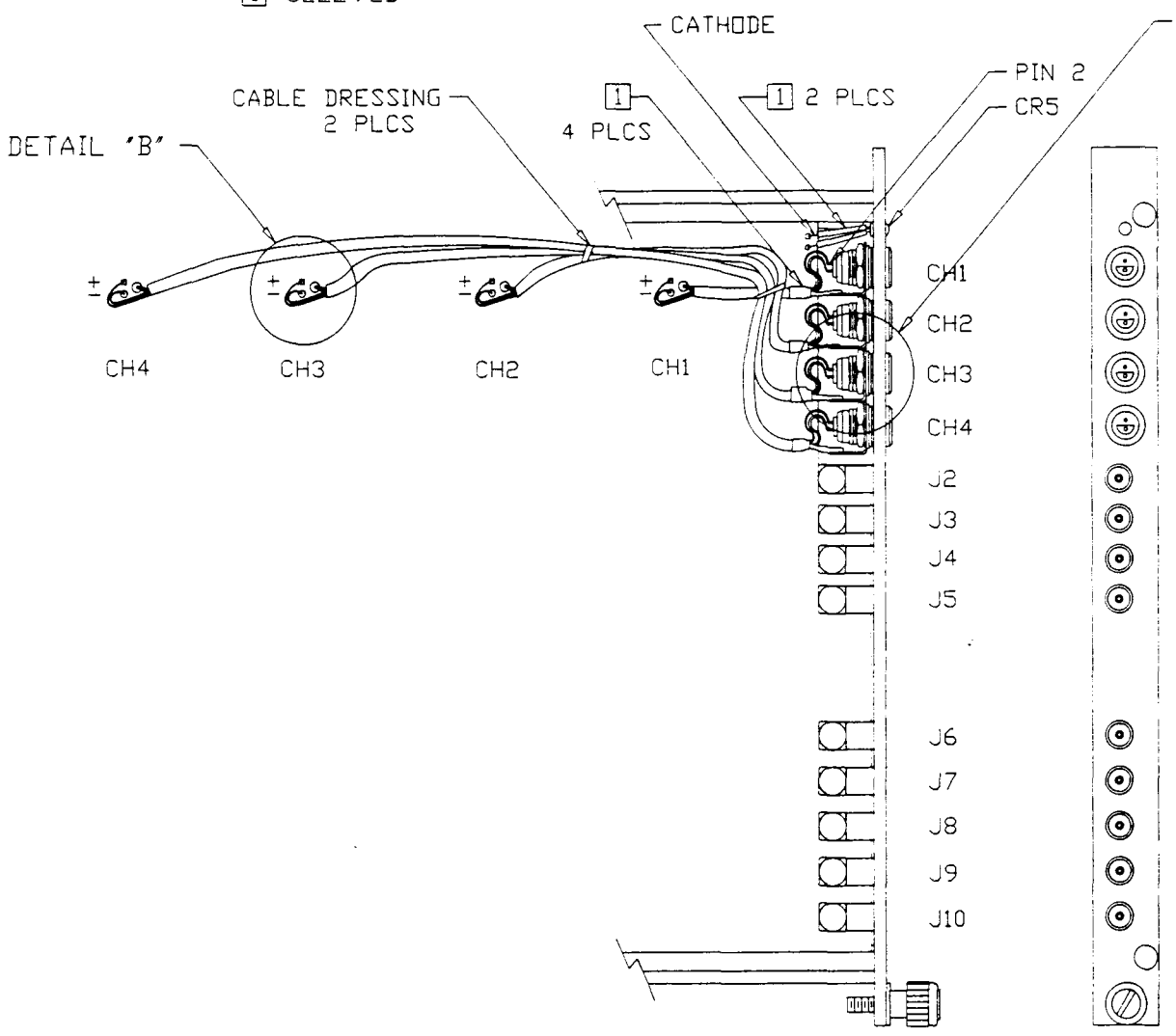
SHEET 2 of 2

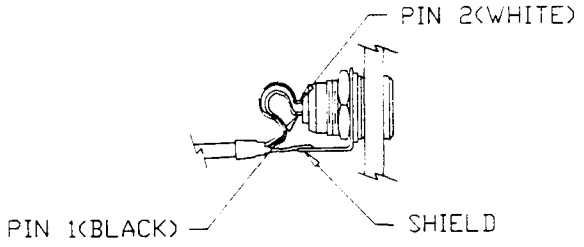
SIZE	DRAWING NUMBER	ISSUE
C	1024-01-AD	2

ST R2+2

NOTES: (UNLESS OTHERWISE SPECIFIED)

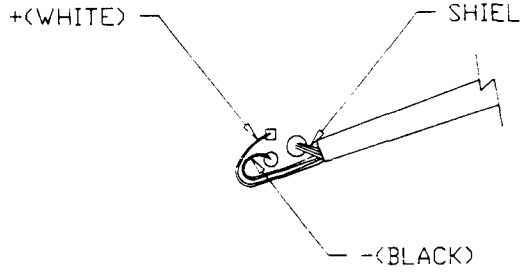
[1] SLEEVED





DETAIL A

SCALE: NONE



DETAIL B

SCALE: NONE

		MATERIAL	FINISH	TITLE: PANEL, FRONT, ASSEMBLY, 1024	dsp technology		
		HEAT TREAT	DIMENSIONAL TOLERANCES UNLESS OTHERWISE NOTED				
		WEIGHT	DECIMAL: XX± XXX± ANG. ±				
		MISC	SCALE NONE NO REQ'D	DESIGN	DATE	JOB NO	
			NEXT ASS'Y	DETAIL	DATE 2-22-97	SIZE: C	DRAWING NUMBER: 024-02-AD
SYM	DESCRIPTION	DATE / APPROVAL		CHECK	DATE		ISSUE: A
REVISIONS				APPRO	DATE		

REVISION HISTORY

DATE	BY	DESCRIPTION
06/20/89	PM	Added Notch Filter

dsp Technology Inc.

PRODUCT WARRANTY

(Excludes Software)

DSP TECHNOLOGY ("DSP") warrants its products to be free from defects in material and workmanship and to meet DSP's performance specifications. The warranty period is one year from the date of shipment to the buyer. The warranty is limited by the paragraphs below.

RETURN TO FACTORY

If a buyer discovers a defect in a DSP product covered by this agreement, buyer's exclusive remedy is to ship the product back to DSP's Fremont factory, where DSP will, at its option, either repair or replace the product. This remedy applies if DSP receives the returned product on or before the tenth day after the expiration of the warranty period and the buyer notifies DSP of the defect before returning the product.

COST TO BUYER OF REPAIRS OR REPLACEMENT

Buyer must prepay freight charges to DSP. DSP will pay standard return freight to buyer. Buyer will be charged for premium freight if that method of transport is requested by buyer. There is no other charge for repair or replacement during the warranty period.

TRANSFERRABLE WARRANTIES

In addition to the foregoing warranty, DSP also provides the buyer the transferrable warranty, if any, provided to DSP by the manufacturers of other products such as terminals and disk systems supplied by SEC as part of a total system.

LIMITATION OF WARRANTY AND LIABILITY

The foregoing constitutes DSP's entire warranty, expressed, implied, and/or statutory (except as to title), and to any other party for any breach of such warranty and for damages, whether direct, special, incidental, or consequential. Other than as expressly provided in this document, no warranties expressed or implied, including any warranty of merchantability or fitness for a particular purpose are made. No employee, representative, or agent or seller has any authority expressed or implied to alter or supplement the terms of this warranty.

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