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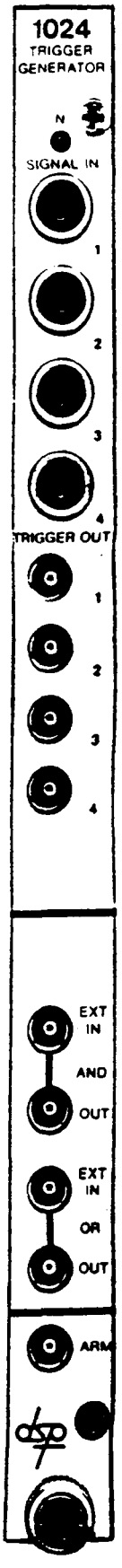
MODEL 1024 TRIGGER MODULE

USER'S MANUAL

MODEL 1024
MULTICHANNEL, PROGRAMMABLE TRIGGER GENERATOR/QUALIFIER

FEATURES

- High Density - four channels in a single CAMAC width.
- Separate trigger output for each channel.
- Very High Integrity Triggering via AND, OR and AND/OR qualification of Trigger Sources
- Programmable output pulse width control for each trigger channel.
- Two independent programmable amplitude thresholds for each channel.
- Positive or Negative edge detection.
- Norm or Fast trigger modes.
- Selectable sensitivity, notch filtering, impedance and coupling.
- True RMS to dc level converter option.



ACTUAL SIZE

DESCRIPTION

The Model 1024 is a four channel, fully programmable, general purpose module which can generate triggers from analog signals. The trigger outputs can be logically gated together to form a master trigger or the individual outputs can be used directly.

Generating reliable recording triggers is perhaps the most difficult problem for multichannel signal acquisition instruments and systems that digitally record multiple analog signals. Many measurements can only be performed one time. Faulty triggers can be fatal. In ADC configurations where all digitizer channels share a common trigger, the loss of data can be total. The Model 1024 can improve trigger integrity by qualifying a potential trigger with other signal conditions that must be present at the same time. This is similar to a digital logic analyzer which generates a trigger only when a predetermined digital pattern is present except that the Model 1024 can use both analog and digital input signals. A qualified master trigger can be generated using the programmable internal logic to combine triggers from up to four separate analog channels (plus external logic signals if desired). Multiple Model 1024 modules can be interconnected to perform the same function for a larger number of channels.

As one example of how a Model 1024 can be used to improve trigger integrity, suppose that two different trigger sources are ORed together. Now a failure of either source to generate the expected trigger won't prevent the system from receiving it's trigger as it would have if the faulty source were the only source. Still further trigger reliability improvements can be achieved by using the AND logic to combine the output of two ro more ORed trigger source pairs. This will prevent a false trigger such as might be caused by a noise spike in one of the sources from triggering the system.

The time of occurance of two or more events relative to each other can be selected as a condition for triggering. The maximum time interval within which one or more events must follow another event is set by programming the width of the trigger output pulse from the individual channels and then using the ANDed output of the selected channels as a master trigger. The programmable trigger pulse width feature can also be utilized as a trigger delay generator.

Multichannel transient recording application sometimes require that the time interval during which data is recorded be determined separately for each channel rather than being the same interval for all channels. The four channels of the Model 1024 can be used independently (i.e., without activating the combinational logic) to generate a separate trigger for each ADC channel.

Trigger points can be set separately for each analog channel by programming the amplitude threshold and slope, or by using the window mode.Each trigger input has independent selection of full scale range, Q tunable line frequency notch filtering, coupling and impedance. The ability to enable each channel separately, and to arm all channels commonly, add to the user's degree of control. A true RMS detector option provides the capability of triggering on the RMS value of a signal. Battery backed-up memory allows a computer to read and reset controls after a power interrupt.

TECHNICAL SPECIFICATIONS - MODEL 1024

INPUTS (analog)

Channels: 4

Bandwidth: dc to 2 MHz (Norm) or dc to 25 MHz (Fast), strap selectable.

Mode: Single (Fast) or differential (Norm). Common mode rejection of 60 db at 60 Hz, 48 db at 1 kHz. Common mode voltage range of ± 50 V, referenced to module ground, including signal + common mode voltage.

Impedance: 50 Ω (Fast) or 1 MΩ (Norm). Other impedances available by resistor substitution.

Full Scale: ± 10 V (Norm), ± 2 % accuracy ± 1.0 V (Fast), ± 1 % accuracy. Other full scale ranges available by resistor substitution.

Input Protection: ± 250 V dc, ± 1 kV for 1 ms (1 MΩ channels). ± 25 V dc, ± 100 V for 1 ms (50 Ω channels).

Notch Filter: Rejection 60 dB @ 60 Hz. (strap selectable, Norm only). Frequency adjustable by component value changes, Q variable from 10 to 50 by potentiometer adjustment.

RMS detector: True RMS to DC converter, (purchase option), strap selectable, Norm only. 5 % ripple at 10 Hz, 1 % ripple at 100 Hz and above. Usable frequency range to 1 MHz.

Identifier: User strappable, 4 bit computer readable code for each channel to identify how the channel is configured.

Connector: 4 differential LEMO connectors on the front panel. A 40 pin flat cable connector on the rear panel allows connection to the rear panel signal outputs of the Model 1402 Amplifier and Antialiasing Filter. The front and rear panel connectors are parallel input lines.

INPUTS (digital)

OR: A TTL high signal is OR'd with the internal logical OR circuit to allow cascading of Model 1024 modules. 510 Ω to ground.

AND: A TTL high signal is AND'd with the internal logical AND circuit to allow cascading of Model 1024 modules. Input is connected to + 5 V through a 10 kΩ resistor (internal AND circuitry of module is normally enabled).

ARM: TTL input, must be at TTL high to allow triggering of channels. Switching the signal to TTL low will clear the triggered channel outputs in the toggled mode. Input is connected to + 5 V through a 10 kΩ resistor (module is normally in the ARM'd mode). Note: module must be computer enabled as well as armed before triggers can be generated.

TRIGGER CONDITIONS (independently programmable for each channel)

LEVEL: (upper and lower threshold), The upper threshold is used for positive/negative edge detection and for window mode, the lower threshold is used only for window mode. Both levels are separately programmable with 8 bit resolution (1 part in 256) over a range of ± 10 V (Norm) or ± 1 V (Fast), ± 3 %.

SLOPE: A trigger can be generated upon detection of a signal transition above (positive) or below (negative) the upper threshold level. The minimum time over threshold for trigger detection is 15 ns. A window mode which generates a trigger whenever the signal is above the upper threshold or below the lower threshold is also available.

ENABLE: Enables or disables a trigger output.

LOGIC:

OR Enable: enables the trigger output to be OR'd with the output of other OR Enabled channels and/or the external OR input.

AND Enable: enables the trigger output to be AND'd with the output of other AND enabled channels and/or the external AND input.

AND/OR Enable: the output of the AND logic is *inputted* into the OR logic.

PULSED OR TOGGLED: The output from the trigger detection circuit can be either a pulse of programmable width or a static level which must be reset by the computer or the ARM signal. The window mode is a time over threshold trigger only.

PULSE WIDTH: The trigger output pulse width is programmable over a range of 1 to 256 times 6 µs. Other time intervals are available by capacitor selection.

COUPLING: ac or dc, strap selectable.

OUTPUTS: 4 trigger (one from each channel), OR, and AND. Active TTL high level, minimum 50 Ω load.

COMPUTER COMMANDS

All commands require N(Station Number) and return X = 1 and Q = 1 unless otherwise stated.

F(0)A(n), n = 0..3, Read channel(i) upper threshold, i = 1 + n, on R8..R1, see F(16)A(n).

F(0)A(n), n = 4..7, Read channel(i) lower threshold, i = n – 3, on R8..R1, see F(16)A(n).

F(1)A(n), n = 0..3, Read trigger channel(i) status, i = 1 + n, on R8..R1, see F(17)A(n).

R2, R1 (Slope) 0 = neg. 1 = positive, 2 = window.

R3 (Mode) 0 = Single event (toggled mode) trigger remains on until reset by ARM or F(10)A(0). 1 = Multiple event(pulsed mode) trigger output pulse width is programmable (see F(17)A(n)).

R4 (OR logic) 0 = disable, 1 = enable.

R5 (AND logic) 0 = disable, 1= enable.

R6 (Trigger) 0= disable, 1 = enable.

R8 (AND/OR logic, channel 1 only) 0 = disable, 1 = enable. (i.e. if R8 is one for channel 1 then the output of the AND logic for all AND enabled channels is gated into the OR logic.)

F(1)A(n), n = 8..11, Read channel (i) pulse width control, i = n – 3 on R8..R1, see F(17)A(n).

X & Q response not available.

F(2)A(0), Read internal LAM register.
R1 = 1 if trigger channels ARMed.
R2 = 1 if OR logic triggered.
R3 = 1 if AND logic triggered.

F(2)A(1), Read internal LAM register.
R(n) = 1 if channel triggered, n = channel number.
R5 = 1 if AND logic triggered.
R6 = 1 if OR logic triggered.

F(3)A(0), Read module I.D. (R16..R1) = 1024

F(3)A(n), n = 8..9, Read channel(i, j) configuration identifier, i = n – 7, j = n – 6, on R8..R1.

F(8)A(0), Read internal LAM status: Q = 1 if LAM on. (The internal LAM is on whenever any channel, the OR or AND logic triggers).

F(10)A(0), Clear internal LAM registers and status; clear triggers and trigger logic.

F(16)A(n), n = 0..3, Write channel (i) upper threshold, i = n + 1, on W8..W1. Thresholds are programmable over a ± 1.0 V range (0 = + 1.0 V, 255 = – 1.0 V). The 1024 is normally delivered with a divide by 10 attenuator installed for the NORM input.

F(16)A(n), n = 4..7, Write channel(i) lower threshold, i = n – 3, on W8..W1. Thresholds are programmable over a ± 1.0 V range (0 = + 1.0 V, 255 = – 1.0 V).

F(17)A(n), n = 0..3, Write channel(i) trigger status, i = n + 1, on W8..W1,
W2,W1(Slope) 0 = neg., 1 = positive, 2 = window
W3 (Mode): 0 = Single event (toggled mode) trigger remains on until reset by ARM or F(10)A(0). 1 = Multiple event(pulsed mode) trigger output pulse width is programmable (See F(17)A(n)).
W4 (OR logic) 0 = disable, 1 = enable.
W5 (AND logic) 0 = disable, 1 = enable.
W6 (Trigger) 0 = disable, 1 = enable.
W8 (AND/OR logic, channel 1 only) 0 = disable, 1 = enable. (i.e. if W8 = 1 for channel 1, then the output of the AND logic is gated into the OR logic).

F(17)A(n), n = 8..11, Write channel(i) Pulse Width control, i = n – 7, on W8..W1.
X & Q response not available
Pulse Width = 255 when trigger output = 10 µs ± 20 %, = 0 when trigger output = 1.5 ms ± 20 %. The RC clocks which control the pulse width are factory set to an approximate period of 6 µs. There is an extra 4 µs turn on delay.

F(24)A(0) Disable the CAMAC dataway LAM.

F(25)A(n), n = 0..3, Trigger channel(i), i = n + 1. Requires the channel to be armed and enabled, F(17)A(n)W(6).

F(26)A(0) Enable the CAMAC dataway LAM.

Z Clear internal LAM status; clear triggers and trigger logic. Disable CAMAC LAM.

C Same as Z.

CAMAC STATUS BITS

X Command Acknowledgement (See F(1)A(n) & F(17) A(n) exceptions)
0 = Invalid NFA command
1 = Valid NFA command

Q Data Acknowledgement (See F(1)A(n) & F(17) A(n) exceptions)
0 = Invalid data (see F(8)A(0) exception)
1 = Valid data

LAM Service Request
NOTE: State of trigger enables, LAM enable and trigger outputs are indeterminate at time of power-up.

CURRENT REQUIREMENTS

+ 6 V = 2 A
– 6 V = 20 mA
+ 24 V = 10 mA
– 24 V = 75 mA

ORDERING INFORMATION

Model 1024 does not include the RMS detector; Model 1024RMS does.

A Notch filter is not factory installed unless requested when ordering. Specify 50 Hz, 60 Hz or 400 Hz rejection frequency.

Coupling (ac/dc), Mode (Norm/Fast) and channel configuration identifier are strap selectable choices. Modules are normally shipped from the factory strapped for dc coupling, Norm mode, and identifier 1111 (no straps installed). Other strap configurations are available by special order.

MATING CONNECTORS

The rear panel 40 pin input connector mates with an ADCBUS-N cable assembly (N = number of connectors on the cable).

When Model 1024 is ordered at the same time as Model 1402 Programmable Amplifier and Antialias Filter, the proper cable assembly for interconnections is included.

Cable assemblies LCOB (LEMO-BNC) and LCOL (LEMO-LEMO) are compatible with the coaxial front panel connectors (LEMO). DLSPDL (Diff. LEMO - Diff. LEMO)and DLSPB(Diff. LEMO-BNC) cable assemblies mate with the front panel signal input differential LEMO connectors. The cable asssemblies in this paragraph are not included.

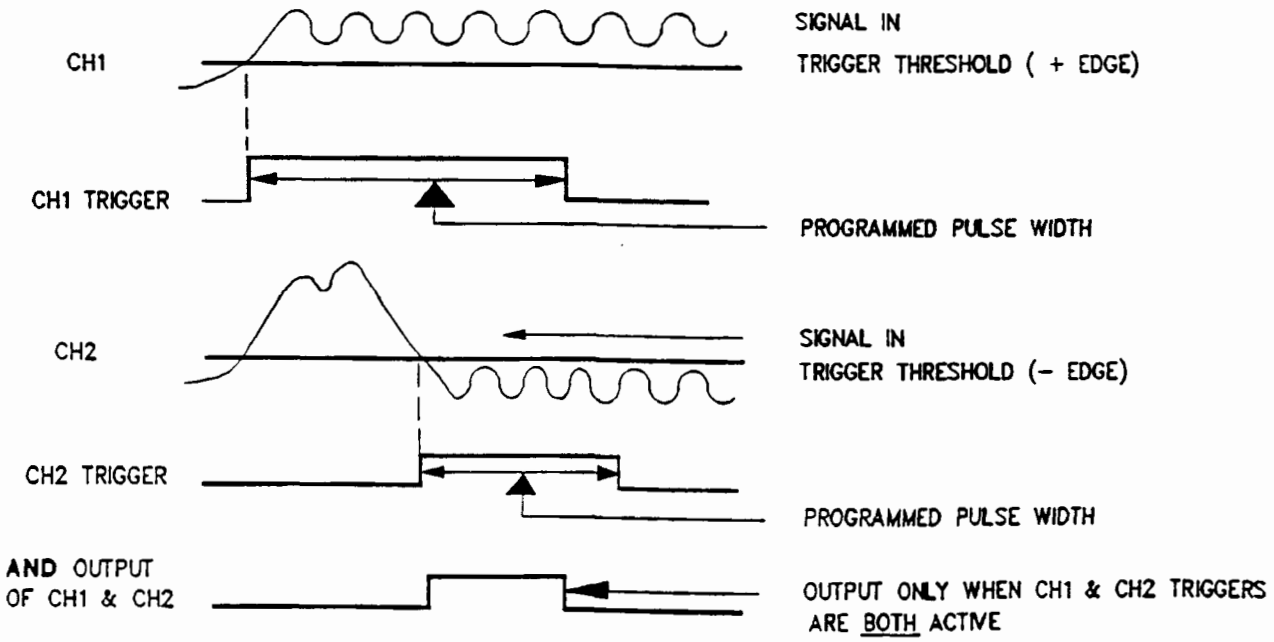
PACKAGING

1 width CAMAC module
221 mm H, 18 mm W, 292 mm D* (8.7" X 0.7" X 11.5")
*Depth front to rear panel. Rear connector 13 mm (0.5").In conformance with the CAMAC standard for RF shielded instrumentation modules (IEEE standard 583, European Esone Report #EUR4100e).

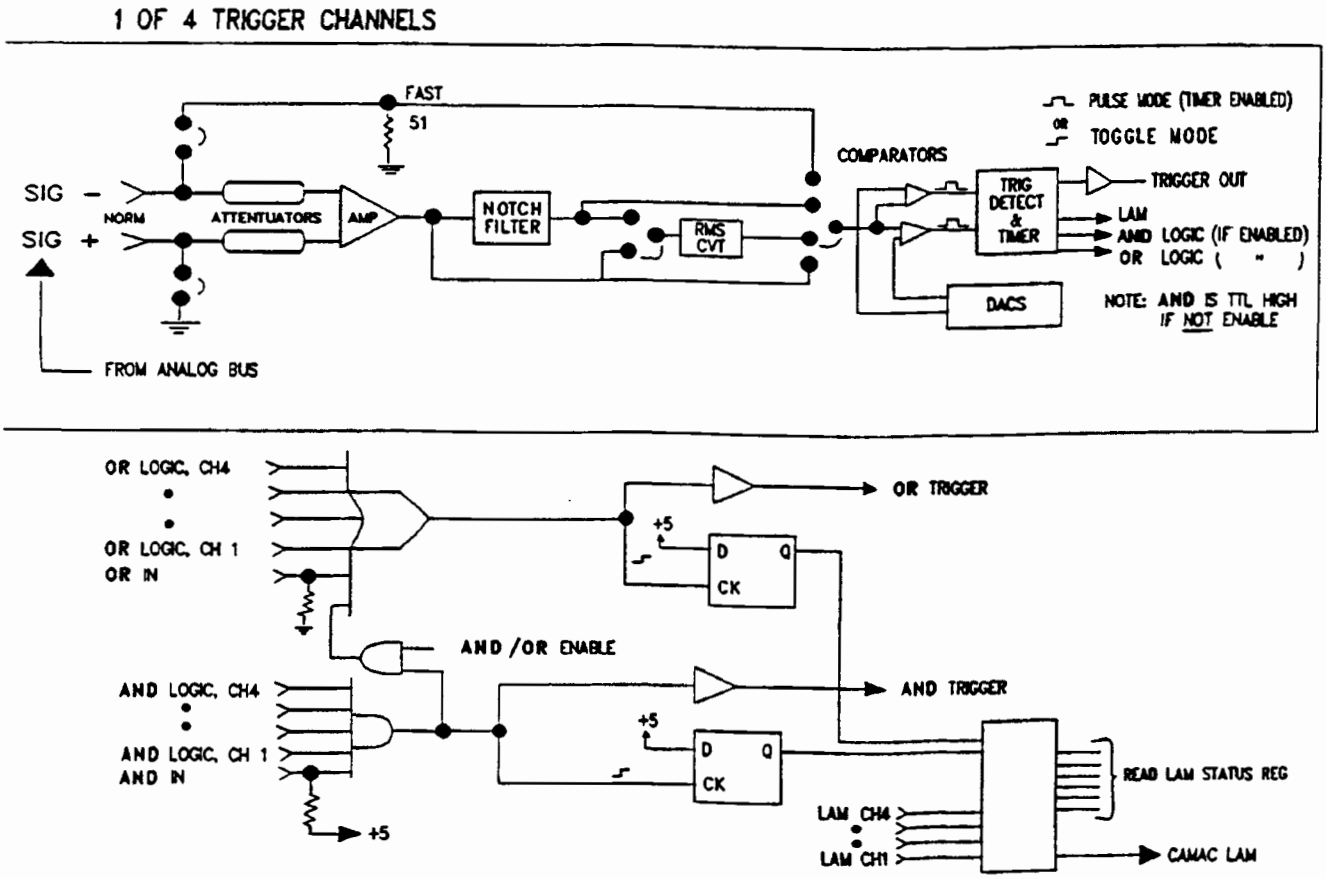
TEMPERATURE RANGE

0°C to 40°C (32°F to 104°F) ambient to operate within specifications (when installed in crate with enough air flow to hold maximum air exit temperature to 55°C (131°F).

TECHNICAL SPECIFICATIONS (cont.) - MODEL 1024



Master Trigger Generation



1024 Block Diagram

PROPRIETARY STATEMENT

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OPERATIONAL DESCRIPTION

Model 1024 is a general purpose analog trigger module which can generate programmable trigger and timing conditions for four input signals. The trigger outputs can be logically gated together to form a master trigger or the individual outputs can be used directly.

The analog input signals can be either :

1)(Factory Default)
Low speed (<2Mhz) differential (NORM mode) with 1 Megohm input impedance, (optional AC coupling), full scale input range is 20 volts (+/- 10 volts) with a common mode rejection range (signal + common mode voltage) of +/- 50 volts. Other full scale ranges can be accommodated by changing the resistor attenuators. Input signals are attenuated by ten to a full scale of +/- 1.0 volts before detection by the trigger circuit.

2) High speed , <25 Mhz, single ended (FAST mode) with 50 ohm input impedance,(optional AC coupling) full scale range of 2 volts (+/- 1.0 volts).

In the NORM mode two options are available for further signal conditioning before trigger detection:

1) A low frequency notch filter with variable Q control. The notch reject frequency is resistor selectable.

2) A true RMS to DC converter with a usable frequency range to 1 Mhz. The converter has typically 5% ripple at 10 hz and < 1% ripple above 100 hz.

Each channel also has a strapable 4 bit code which can be read by the computer to identify how the channel was configured. The analog outputs (+/- 1 volts max) from the signal conditioning circuits are inputted to trigger detection circuits which generate TTL level signals. Each trigger circuit can be programmed for the following:

1) Upper and Lower Threshold: The upper threshold is used for positive/negative edge detection and for window mode. It is programmable over a +/- 1.0 volt interval. The lower threshold is used only for window mode and is also programmable over +/- 1.0 volts. Both levels are programmable with an 8 bit resolution (1 part in 255) over the output range.

2) SLOPE: A trigger can be generated after detection of a signal transition above (positive) or below (negative) the upper threshold level. Once triggered the output will remain active for a programmed time interval (pulsed mode) or until reset (toggled mode). A window mode which generates a trigger any time the signal is above the upper threshold or below the lower threshold is also available. In this mode the trigger is active the entire time the signal is outside the window limits.

3) SELECT: Enables or disables a trigger output.

4) LOGIC:
   a) OR ENABLE: enables the trigger output to be OR'd with the output of other OR ENABLE'd channels or the external OR input.
   b) AND ENABLE: enables the trigger output to be AND'd with the output of other AND ENABLE'd channels or the external AND input.

5) PULSED OR TOGGLED: The output from the trigger detection circuit can be either a pulse of programmable width or a static level which must be reset by the computer or the ARM signal. The window mode is a time over threshold trigger only.

6) PULSE WIDTH: The trigger output pulse width is programmable over a range of 1 to 256 times a clock oscillator period. Each trigger circuit has its own RC clock whose frequency is adjusted by capacitor selection, normally 6 microsec. per period. (Factory Default)

In addition to the above there is a universal ARM signal which must be active to allow any channel to trigger. This signal is a TTL high (an internal pullup resistor will normally ARM the channels if no external signal is being applied) and a low ARM signal will clear all trigger outputs.

The outputs from the trigger detectors are directly available through the front panel connectors (TTL high signals, capable of driving 50 ohms). Also the combinatorial logic outputs OR and AND are available. The OR signal will be TTL high whenever one or more of the 'OR' enabled channels or external 'OR' logic is TTL high. The external OR signal is pulled down by an internal resistor and need not be present to enable 'OR' logic. The AND signal will be TTL high whenever all of the 'AND' enabled channels and external 'AND' logic are TTL high. The external 'AND' signal is pulled high by an internal resistor and need not be present to enable the 'AND' logic. An additional logic feature allow the output of the AND logic to be gated into the OR logic.

A status bit from each of the trigger circuits is available for computer monitoring using the F(2)A(1) command. These bits are set whenever a trigger is generated and remain on until reset by the clear lam command F(10)A(0).

NOTE: Model 1024 registers are volatile and need to be initialized after powering up the module.

FRONT PANEL INDICATORS & CONTROLS:

N LED: Active whenever the module is addressed with a valid CAMAC command.

FRONT PANEL INPUT SIGNALS:

OR: A TTL high signal (510 ohms to ground), LEMO type connector, which is OR'd with the internal logic OR circuit allows cascading of 1024 modules.

AND: A TTL high signal (10 Kohms to +5.0 volts), LEMO type connector, which is AND'd with the internal logic AND allows cascading of 1024 modules.

ARM: A TTL high signal(10 Kohms to +5.0 volts), LEMO type connector, enables all channels to trigger. Switching the signal to TTL low will clear triggered outputs.

SIGNAL IN: Four analog input signals either differential or single ended. Connector: Four, two position Lemo connectors. Male pin is positive input. Signal inputs also available from rear panel flat cable.

FRONT PANEL OUTPUT SIGNALS:

CHANNEL OUT: Four individual trigger outputs, active TTL high level, LEMO type connector, minimum load of 50 ohms.

OR: Active TTL high level whenever OR logic is true, LEMO type connector

AND: Active TTL high level whenever AND logic is true, LEMO type connector.

REAR PANEL INPUT SIGNALS:

CHANNEL
IN: Four analog input signals either differential or single ended.
Connector : 40 pin flat cable connector.
See Jumper Location drawing signal pinout. Front Panel inputs available.

CAMAC CONTROL:

The following list describes the response of the 1024 to the CAMAC dataway commands. All commands require N(Station Number) and return X=1 and Q=1 unless stated. Note that registers are volatile and need to be programmed after power up.

F(0).A(i-1) Read channel(i) upper threshold, on
n = 0..3 R8-R1, see F(16).A(n).

F(0).A(n) Read channel(i) lower threshold, i = n - 3, on
n= 4..7 R8-R1, see F(16).A(n).

F(1).A(n) Read trigger channel(i) status, i = 1 + n, on
n = 0..3 R8-R1, see F(17).A(n).

R2, R1: Slope selection:
- 0: Negative slope
- 1: Positive slope
- 2: Window mode

R3: Mode:
- 0: Single event (toggled mode) - trigger remains on until reset by ARM or F(10).A(0).
- 1: Multiple event(pulsed mode) - trigger output pulse width is programmable (see F(17).A(n)).

R4: OR logic:
- 0: Disable channel's trigger output for OR logic.
- 1: Enable channel's trigger output for OR logic.

R5: AND logic:
- 0: Disable channel's trigger output for AND logic.
- 1: Enable channel's trigger output for AND logic.

R6: Trig Enable:
0: Disable channel from triggering.
1: Enable channel for triggering.

R8: AND/OR logic (channel 1 only).
0: Disable AND/OR logic.
1: Enable AND/OR logic.
(i.e. if R8 is one for channel 1 then the output of the AND logic is gated into the OR logic.)

F(1).A(n) n = 8..1 Read channel(i) pulse width control, i = n - 3, on R8-R1, see F(17).A(n). NOTE: No X & Q response available

F(2).A(0) Read ARM status and 'OR','AND' LAM status.

R1: 1 if trigger channels ARMed.
R2: 1 if OR logic triggered.
R3: 1 if AND logic triggered.

F(2).A(1) Read internal LAM status.
R(n) : 1 if channel triggered, n = channel nu.
R5 : 1 if AND logic triggered
R6 : 1 if OR logic triggered

F(3).A(0) Read module I.D.
(R16-R1) = 1024

F(3).A(n) n= 8..11 Read channel(i) signal conditioning plug-in I.D. for i = n-7.

F(8).A(0) Read internal LAM status:
Q = 0 of internal LAM not on.
Q = 1 if internal LAM on.
(The internal LAM is on whenever any channel, the 'OR' or 'AND' logic triggers).

F(10).A(0) Clear internal LAM status; clear triggers and trigger logic.

F(16).A(n) n = 0..3 Write channel(i) upper threshold, i = n + 1, on W8-W1. Thresholds are programmable over a +\- 1.0 volt range (0 = +1.0 volts, 255 = -1.0 volts). The 1024 is normally delivered with a divide by 10 attenuator for the NORM input.

F(16).A(n) Write channel(i) lower threshold ,i= n - 3, on
n= 4..7 W8-W1. Thresholds are programmable over a +\- 1.0 volt range (0 = +1.0 volts, 255 = -1.0 volts). The 1024 is normally delivered with a divide by 10 attenuator for the NORM input.

F(17).A(n) Write channel(i) n trigger status, i = n + 1, on
n = 0..3 W8-W1,

W2, W 1: Slope selection:
- 0: Negative slope
- 1: Positive slope
- 2: Window mode

W 3: Mode:
- 0: Single event (toggled mode) - trigger remains on until reset by ARM or F(10).A(0).
- 1: Multiple event(pulsed mode) - trigger output pulse width is programmable (see F(17).A(n)).

W 4: OR logic:
- 0: Disable channel's trigger output for OR logic.
- 1: Enable channel's trigger output for OR logic.

W 5: AND logic:
- 0: Disable channel's trigger output for AND logic.
- 1: Enable channel's trigger output for AND logic.

W 6: Trig Enable:
- 0: Disable channel from triggering.
- 1: Enable channel for triggering.

W 8: AND/OR logic (channel 1 only).
- 0: Disable AND/OR logic.
- 1: Enable AND/OR logic.

(i.e. if R8 is one for channel 1 then the output of the AND logic is gated into the OR logic.)

F(17).A(n) Write channel(i) (PW) pulse width control ,i = n - 3,
n = 8..11 on W8-W1. NOTE: No X & Q response available
PW = 254 then triggered output = 10 usec +/- 20%
= 0 then triggered output = 1.5msec +/- 20%
The RC clocks which control the pulse width are factory set to an approximate period of 6 usec. There is an extra 4 usec. turnon delay.

F(24).A(0) Disable the CAMAC dataway LAM.

F(25).A(n) Trigger channel(i), i = n + 1. Requires the

n = 0..3 channel to be armed and enabled, F(17)A(n)W(6).

F(26).A(0) Enable the CAMAC dataway LAM.

Z Clear internal LAM status; clear triggers and trigger logic. Disable CAMAC LAM.

C Same as Z.

COMPUTER PROGRAMMING THE 1024

The following examples shows how to setup channel 1 for positive slope detection at 0.0 volts threshold, enable channel 1 for the OR logic and detect if the trigger occurred.

Note: the command a) camo(n,f,a,d,q,x) writes a command to the 1024 module.

b) cami(n,f,a,d,q,x) reads a command from the 1024 module.

c) n=station number

d) f=function commands, a = subaddress

e) $d=data ,binary
d=data ,decimal

f) q,x = q & x response

camo(n,17,0,$00101101,q,x);	enable channel1, pulsed mode, OR enabled note- channels 1,2,4 should be disabled.
camo(n,17,8,0 ,q,x);	pulse width = app. 1.5 msec.
camo(n,16,0,128 ,q,x);	upper threshold = 0.0 volts.
camo(n,10,0,0 ,q,x);	clear old triggers, & status bits
camo(n,26,0,0 ,q,x);	enable LAM interrupt;
wait for LAM interrupt or do	
cami(n,8,0,0 ,q,x);	q =1 if any trigger occurred.
cami(n,2,1,data ,q,x);	read trigger status bits: R1 = 1 if channel 1 triggered. R6 = 1 if channel 1 triggered.
camo(n,10,0,0 ,q,x);	clear triggers and LAM status bits.

THEORY OF OPERATION

(refer to FIG 3 and schematics)

Signal conditioning:

Each of the four analog channels is composed of identical circuits. For the FAST mode the single ended signal is terminated to with a 51 ohm resistor and then inputted directly to the comparators. For the NORM mode the differential signals are attenuated through compensated divide by ten circuits composed of R20, R24, C12, C13 and R21, R22, C15, and C14. Capacitors C14 and C13 are adjusted to give the best square wave response. Op amps 1J and 2J convert the differential NORM signals to a single ended signal which can be connected to the signal conditioning circuits or directly to the comparators.

Trigger detection:

I.C. G1 is a dual comparator which sets the thresholds for trigger detection. The upper comparator , pins 1,2, and 4 are used for positive, negative and window detect modes. The lower comparator, pins 11,12 and 9 are used only for the lower window detect mode. The thresholds are programmable over a plus one to minus one volt range. The PAL at 8D contains all the logic necessary for the various detection modes. In the toggle mode, once a trigger is detected then 8D pin 19 will go low to enable the a programmable pulse width to be generated by the RC clock at 5D and counter 7C.

Logic detection:

I.C. 9K contains all logic for the OR and AND logic detection. For OR logic, only channels that are OR enabled will input pulses to 9K. For AND logic, channels that are NOT enabled will ALWAYS be TTL high.

JUMPER OPTIONS and COMPONENT SELECTION

(refer to jumper location drawing and schematics)

JUMPER OPTIONS:

1) Signal inputs from rear connector: (J1)
Up to 8 differential signals [8 signals(+) and their referenced grounds(-)] are available on the forty pin rear connector. Jumpers near J1 allow connecting:

Signal 1 + or Signal 5+ to Channel 1+ ;
Signal 1 - or Signal 5- to Channel 1- ;
Signal 2 + or Signal 6+ to Channel 2+ ;
Signal 2 - or Signal 6- to Channel 2- ;
Signal 3 + or Signal 7+ to Channel 3+ ;
Signal 3 - or Signal 7- to Channel 3- ;
Signal 4 + or Signal 8+ to Channel 4+ ;
Signal 4 - or Signal 8- to Channel 4- ;

This allow two 1024 modules to monitor 8 signals on the same cable.

2) FAST MODE: (high frequency, 50 ohm termination, single ended; signal is inputted through Ch - pin on rear connector.)

D.C. coupling:
E16 - E17 (connects Ch + to gnd)
E1 - E7 (connects Ch - to 51 ohm)
E11 - E15 (connects Ch - to comparators)

A.C. coupling:
E1 - E3 (connects Ch - to C16)
E5 - E7 (connects C16 to 51 ohm)
E16 - E17 (connects Ch + to gnd)
E11 - E15 (connects Ch - to comparators)

Note: For norm mode, a single ended signal applied to the Ch - input will appear inverted at the comparators.

3) NORM MODE: (low frequency, 1 Mohm termination,differential)

D.C. coupling: E1 - E2 (connects Ch - to attenuator)
A.C. coupling: E1 - E3 (connects Ch - to C16)
E5 - E2 (connects C16 to attenuator)

4) NORM MODE: (low frequency, 1 Mohm termination,single ended)
D.C. coupling: E16 - E17 (connects Ch + to gnd)
A.C. coupling: same as 3

5) SIGNAL CONDITIONING OPTIONS (NORM MODE ONLY):

a) Output of NORM signal conditioning circuit connected to comparators.
: E12 - E15 (output of norm connected to comparators)

b) Output of NORM signal conditioning circuit connected to RMS circuit.
Output of RMS circuit connected to comparators.

: E8 - E9 (output of norm connected to rms circuit
: C18 + E15 (output of RMS connected to comparators)

c) Output of NORM signal conditioning circuit connected to NOTCH filter.
Output of NOTCH filter connected to RMS circuit.
Output of RMS circuit connected to comparators.

: E10 - E9 (output of NOTCH connected to rms circuit)
: C18 + E15 (output of RMS connected to comparators)

COMPONENT SELECTION

1) A.C. COUPLING	:	C16, user selectable.
2) NORM mode attenuator	:	Factory set for divide by ten, 1 megohm impedance. Select R21,R22 and R20,R24 for other attenuation/impedances. For other attenuations C15 and C12 must also be changed. Adjust C13,C14 for correct A.C. responses.
3) Pulse width control	:	The range of the trigger output pulse width can be changed by selection of C11.
4) RMS detector	:	The 1024 uses an Analog Devices AD637 RMS detector. The user should refer to the data sheet for this device to understand the ripple characteristics which are affected by the value of C18.
5) Notch Filter	:	C17, C19 and C20 determine the NOTCH frequency.

THE DSP ISA (Integrated Signal Acquisition) SYSTEM

Multi-channel signal acquisition systems which digitally record many analog signals typically encounter two problems which grow in severity as the number of channels increases:

1) Users need to be assured of system integrity from signal input through to the computer interface.

2) Recording triggers must be reliable and flexibly configured.

Either of these problems can be very costly due to partial or complete data loss. The DSP ISA system has been developed to overcome both of these concerns resulting in data acquisition systems that are highly reliable.

System Integrity:

To insure system integrity at all times the computer must be able to determine that all data channels are operating correctly and are connected properly. The ISA system addresses the problem by designing in front end calibration for each signal conditioning channel (ex: DSP1402). Under computer command the signal conditioner can switch from the input signal to a programmed calibration signal. By digitizing the calibration signals one at a time the computer will determine:

1) That the correct signal conditioning module is connected to the correct ADC channel.

2) That the cabling between the signal conditioner and ADC is operative.

3) That the signal conditioning module is calibrated.

These measurements can be done very quickly and automatically by the computer.

ISA signal conditioners also have a rear panel analog bus which allows buffered, conditioned, signals from selected channels to be sensed by other acquisition modules such as the DSP 1024 (see fig 2 and 3). This allows the user to programmably reconfigure the trigger channels without physically altering the system cabling and possibly introducing errors.

Trigger Reliability:

Reliable recording triggers are perhaps the most difficult problem for multichannel systems. Many measurements can be performed only one time and

faulty triggers can be fatal, resulting in complete data loss. The DSP model 1024 is a flexible trigger detection module which overcomes many of these problems.
To insure trigger integrity the trigger signal should be qualified by gating the signal of interest with other signals that must be present at the same time. The qualified signal becomes a 'master' trigger which is then sent to the recording instrumentation. This is similar to a digital logic analyzer which generates a trigger only when a predetermined digital pattern is present except the 1024 uses both analog and digital signals. The 1024 can generate the master trigger by logically gating triggers from four separate analog channels plus external logic signals. By programming the unit the user can insure that a trigger only appears under the correct conditions (see fig 4). The 1024 capabilities include:

a) generating triggers from four separate analog signals. The user can program the trigger signals to be on permanently (toggle mode) or for a predetermined time duration (pulse mode).

b) logically gating the triggers together to generate a 'master' trigger. There are two logic combinations available: 'OR' and 'AND' gating:

OR: A master trigger is generated whenever any one of the trigger or external 'OR' signals is present.

AND: A master trigger is generated only when all of the enabled trigger signals are present. Since the 1024 allows programming the width of the trigger pulses, the user can create a 'trigger window' in which two or more signals must be present before the master trigger is generated. The duration of the shortest pulse will determine the window time (see fig 4).

c) An ARM signal which enables or disables all triggers using an external control signal.

d) Trigger signals can also be generated by a computer command which can simulate trigger timing and check the system response to the master trigger.

REAR PANEL INPUTS CONFIGURATION

1	gnd
2	Ch1 -
3	Ch1 +
4	gnd
5	Ch2 -
6	Ch2 +
7	gnd
8	Ch3 -
9	Ch3 +
10	gnd
11	Ch4 -
12	Ch4 +
13	gnd
15	Ch5 -
16	Ch5 +
17	Ch6 -
18	Ch6 +
19	gnd
20	Ch7 -
21	Ch7 +
22	gnd
23	Ch8 -
24	Ch8 +
25	gnd
26-40	Not Used

Strap Selectable



DSP Technology Inc.

SINGLE LEVEL BILL OF MATERIAL REPORT

Assembly: 1024 (4 CH TRIG GENERATOR/QUALIFIER)
Revision: A
As of: 11/10/90

Date: 11/13/90
Page: 1

	Component	Description	Qty Per	As of	Until	Reference
1.	6852-0002	PNL: CAMAC SIDE STD	2.00	03/08/87	12/31/99	
2.	A-1024-02	ASSY: F/P MECH, 4CH SIGNAL CONDITIO	1.00	03/08/87	12/31/99	

Component	Description	Qty Per	As of	Until	Reference

Assembly: 1024 (4 CH TRIG GENERATOR/QUALIFIER)

Assembly: A-1024-01 (ASSY: PCB, 1024 4CH SIGNAL CONDITIO)
Revision: 2
As of: 11/10/90

	Component	Description	Qty Per	As of
1.	0100-0102	RES: RC07 1K OHM 5% 1/4W	12.00	08/19/87
2.	0100-0103	RES: RC07 10K OHM 5% 1/4W	5.00	07/02/87
3.	0100-0223	RCF 5% 1/4W CF RESISTOR R=22K	1.00	02/22/87
4.	0100-0241	RES 5% 1/4W CC RESISTOR R=240	2.00	02/21/87
5.	0100-0244	RES 5% 1/4W CC RESISTOR R=240K	4.00	07/22/87
6.	0100-0272	RES 5% 1/4W CC RESISTOR R=2.7K	2.00	02/21/87
7.	0100-0511	RES 5% 1/4W CC RESISTOR R=510	5.00	03/08/87
8.	0100-0512	RES 5% 1/4W CC RESISTORR R=5.1K	1.00	02/21/87
9.	0150-0511	RMF RN55D 1% RESISTOR R=51.1	4.00	02/21/87
10.	0150-1001	RES 1% 1/4W MF RESISTOR R=1.00K	41.00	08/19/87
11.	0150-1004	RMF RN55D 1% METAL FILM RES R=1.00M	8.00	02/22/87
12.	0150-1103	RES: 1%,1/4W,R=110K	8.00	05/20/87
13.	0150-2001	RES RN55D 1% 1/4W R=2.00K	2.00	08/19/87
14.	0150-3011	RMF RN55D 1% METAL FILM RES R=3.01K	1.00	02/21/87
15.	0201-0102	RPK RES PK BNS 4310R-101-102	4.00	02/21/87
16.	0500-0101	CSM C=100PF CDE # CD5FC101J03	1.00	05/20/87
17.	0520-0103	CMC C=0.01UF MONO CENTRALAB CZ20A1	4.00	08/19/87
18.	0520-0104	CMC 0.1UF CNTLB:CZ20A104M2 KEM:C322	74.00	07/22/87
19.	0520-0105	CMC C=1.0UF MONO 50WVDC KEM# C320	1.00	02/21/87
20.	0600-0226	CTE C=22UF 10WVDC TANTALUM	4.00	05/20/87
21.	0600-0475	C TANT 4.7MF 10% 35V	5.00	08/19/87
22.	0750-0003	CCV C=5.5-18PF VAR JOHANSON JFD D	8.00	02/21/87
23.	1000-4448	DGS DIODE SIL. SWITCH 1N4448	32.00	02/21/87
24.	1010-2811	DSS DIODE H.P.5082-2811	2.00	05/20/87
25.	1030-4005	DSR 1AMP 1N4005	1.00	02/21/87
26.	1030-5624	DSR: DIODE RECT 3A GE IN5624/BYM56	1.00	02/21/87
27.	1750-0001	ICS SN7401	1.00	02/21/87
28.	1750-0128	ICS SN74128	2.00	02/21/87
29.	1750-0154	ICS SN74154	1.00	02/21/87
30.	1760-0000	ICS SN74LS00	1.00	02/21/87
31.	1760-0004	ICS SN74LS04	2.00	03/08/87
32.	1760-0074	ICS SN74LS74	1.00	02/21/87
33.	1760-0132	ICS SN74LS132	2.00	02/21/87
34.	1760-0138	ICS SN74LS138	2.00	02/21/87
35.	1760-0221	ICS SN74LS221	1.00	02/21/87
36.	1760-0244	ICS SN74LS244	1.00	02/21/87
37.	1760-0374	ICS SN74LS374	4.00	02/21/87
38.	1760-0593	ICS SN74LS593	4.00	02/21/87
39.	1760-0640	ICS SN74LS640	1.00	02/21/87
40.	1760-0642	ICS SN74LS642	1.00	02/21/87
41.	1760-0645	ICS SN74LS645	4.00	02/21/87
42.	1770-0004	ICS IC LSTTL HEX INV SN74S04	1.00	03/08/87
43.	1851-0057	PRM: PROG/F 1850-0001,1024-01 9A	1.00	05/20/87
44.	1851-0058	PRM: PROG/F 1850-0001, 1024-01 10A	1.00	05/20/87
45.	1857-0020	PAL: PROG/F 1856-4104, 1024-01 8D,F	4.00	05/20/87
46.	1857-0021	PAL: PROG/F 1856-4010, 1024-01 9K	1.00	05/20/87

Component	Description	Qty Per	As of

Until	Reference
12/31/99	R36,R37,R41
12/31/99	R7,R9,R16,R43,R44
12/31/99	R11
12/31/99	R13,R14
12/31/99	R42
12/31/99	R12,R15
12/31/99	R5,R6,R17-R19
12/31/99	R8
12/31/99	R23
12/31/99	R2,R27-R30,R33-R35 R38-R40
12/31/99	R20,R21
12/31/99	R22,R24
12/31/99	R1,R4
12/31/99	R3
12/31/99	RP1-RP4
12/31/99	C2
12/31/99	C8-C11
12/31/99	C23,C24
12/31/99	C3
12/31/99	C18
12/31/99	C1,C4-C7
12/31/99	C13,C14
12/31/99	CR6-CR13
12/31/99	CR3,CR4
12/31/99	CR1
12/31/99	CR2
12/31/99	7A
12/31/99	5G,10K
12/31/99	9F
12/31/99	4A
12/31/99	5E,5J
12/31/99	11K
12/31/99	5D,5H
12/31/99	9E,10E
12/31/99	9D
12/31/99	9H
12/31/99	7D,7F,7H,7K
12/31/99	7C,7E,7G,7J
12/31/99	8A
12/31/99	11A
12/31/99	8C,8E,8G,8J
12/31/99	5C
12/31/99	9A
12/31/99	10A
12/31/99	8D,8F,8H,8K
12/31/99	9K

Assembly: A-1024-01 (ASSY: PCB, 1024 4CH SIGNAL CONDITIO)
Revision: 2
As of: 11/10/90

	Component	Description	Qty Per
47.	1857-0022	PAL: PROG/F 1856-0106, 1024-01 9G	1.00
48.	1857-0023	PAL: PROG/F 1856-4102, 1024-01 9C	1.00
49.	1857-0024	PAL: PROG/F 1856-4008, 1024-01 6A	1.00
50.	1857-0025	PAL: PROG/F 1856-4102, 1024-01 5A	1.00
51.	1910-0005	IC: CMOS, HM6264ALSP-12	1.00
52.	2000-0082	ICS DUAL OP AMP FET TI TL082CP	13.00
53.	2010-0521	ICA IC SIGNETICS NE521N	4.00
54.	2020-0002	ICA VOLTAGE REF PMI REF02HP	1.00
55.	2030-0317	ICS IC VOL REG NAT LM317T	1.00
56.	2030-0337	IC: VOLT REG, NEG ADJ, LM337T	1.00
57.	3100-0402	FUS FUSE 4AMP LITTLEFUSE 251004	4.00
58.	5000-0008	SKT CAMBION 703-1308-01-04-10	8.00
59.	5000-0014	SKT CAMBION 703-1314-01-04-10	4.00
60.	5000-0016	SKT CAMBION 703-1316-01-04-10	10.00
61.	5000-0020	SKT CAMBION 703-1320-01-04-10	1.00
62.	5250-3703	JCK FUS CAMBION 450-3703-01-06-00	32.00
63.	5251-0001	JMP CAMBION 461-2251-01-03-10	8.00
64.	5500-0018	HDR 40 PIN R/A 4 WALL 3M#3595-5002	1.00
65.	6520-7226	DAC: 8BIT,QUAD,CMOS, AD7226KN	2.00
66.	6849-0002	INS BERGQUIST 3223-07-FR-54	2.00
67.	6850-0001	RAIL: GUIDE, MDL, 5 HOLE, C-BORE	2.00
68.	7000-0058	PCB DWG# 1024-01-FD	1.00
69.	7410-0003	HWD: SWAGE TYPE STANDOFF	6.00
70.	8200-0001	BAT BATTERY DURACELL DL 1/3N W TABS	1.00
71.	DOCUMENTATION	PER ASSY DWG REFERENCE	2.00

As of	Until	Reference
05/20/87	12/31/99	9G
05/20/87	12/31/99	9C
05/20/87	12/31/99	6A
05/20/87	12/31/99	5A
02/21/87	12/31/99	11C
05/20/87	12/31/99	3B,1C,2C,3D,1E,2E,3F 1G,2G,3H,1J,2J,3K
02/21/87	12/31/99	4D,4F,4H,4K
02/21/87	12/31/99	3A
02/21/87	12/31/99	VR1
02/21/87	12/31/99	VR2
05/20/87	12/31/99	F1-F4
05/20/87	12/31/99	8D,8F,8H,8K,5A,6A,9C 9K
08/19/87	12/31/99	3C,3E,3G,3J
05/20/87	12/31/99	9A,10A,8D,8F,8H,8K 5A,6A,9C,9K
05/20/87	12/31/99	9G
08/19/87	12/31/99	F1-F4 CH1-CH4
01/01/88	12/31/99	CH1 THRU CH4
02/22/87	12/31/99	J1
02/21/87	12/31/99	5F,5K
08/19/87	12/31/99	VR1,VR2
05/20/87	12/31/99	
05/20/87	12/31/99	
05/20/87	12/31/99	
05/20/87	12/31/99	BAT
04/16/87	12/31/99	1024-01 AD 1024-01 CD

As of	Until	Reference

REVISION HISTORY

DATE	BY	DESCRIPTION
06/20/89	PM	Added Notch Filter

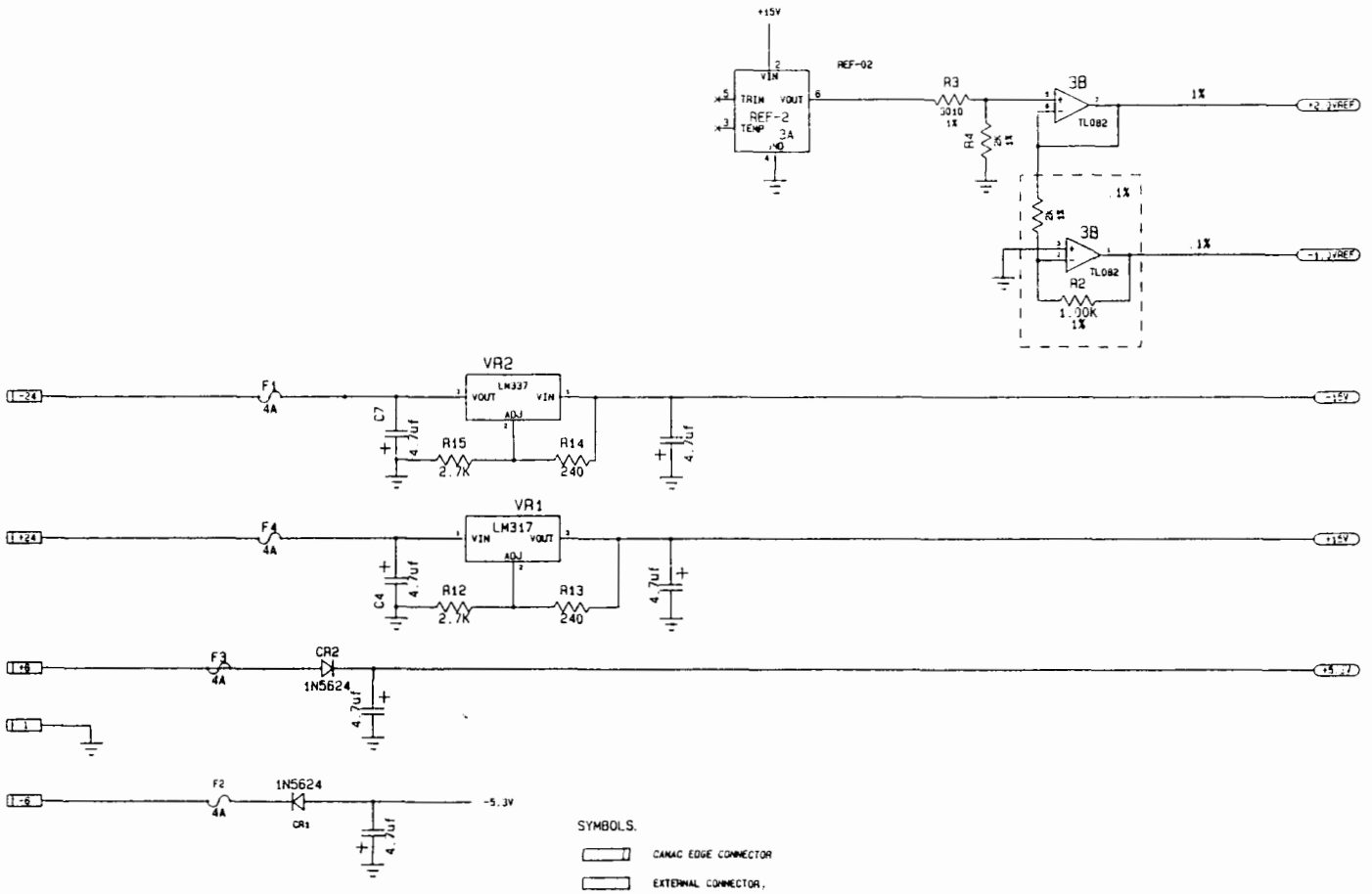
DSP Technology Inc.

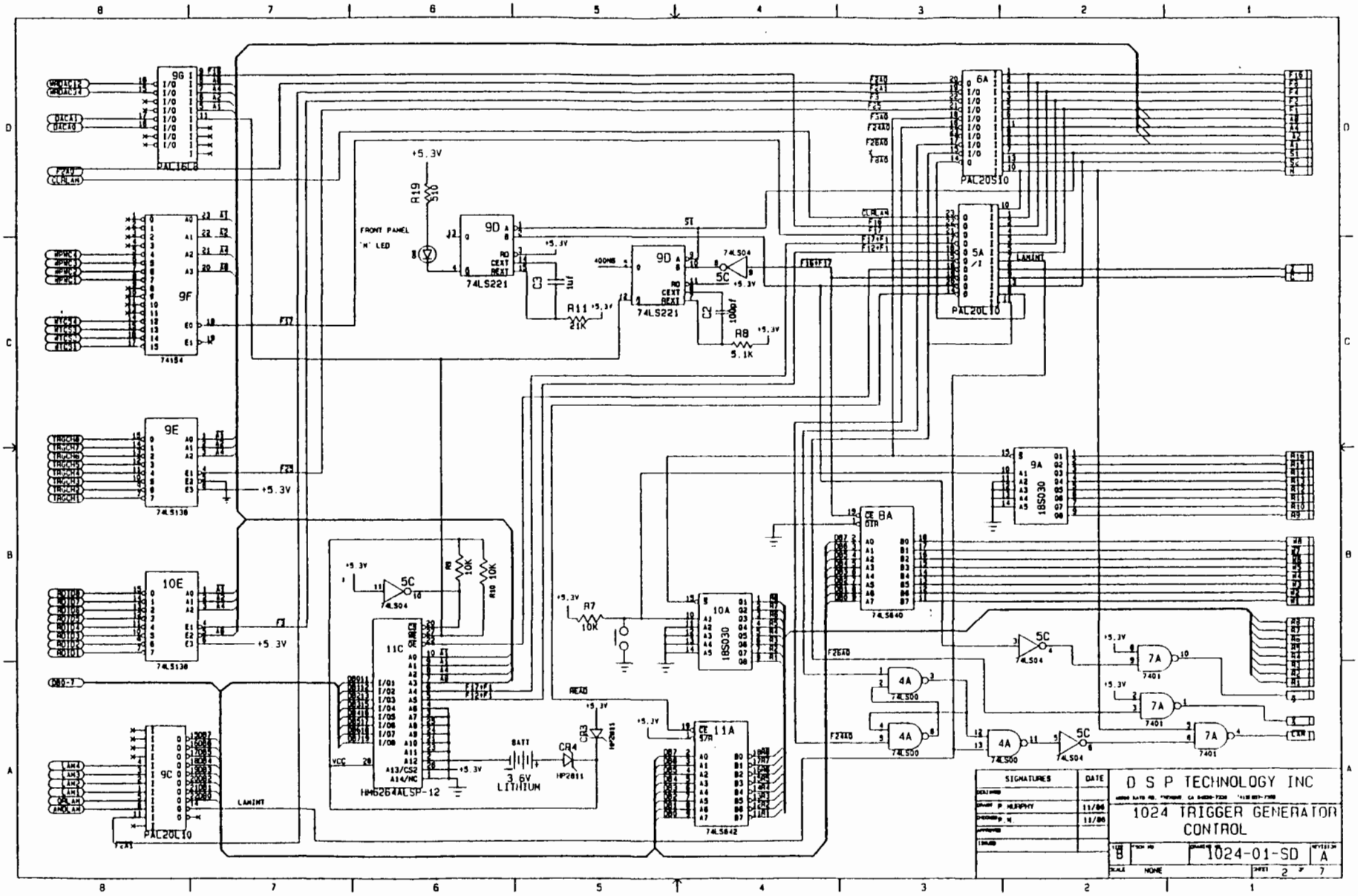
SINGLE LEVEL BILL OF MATERIAL REPORT

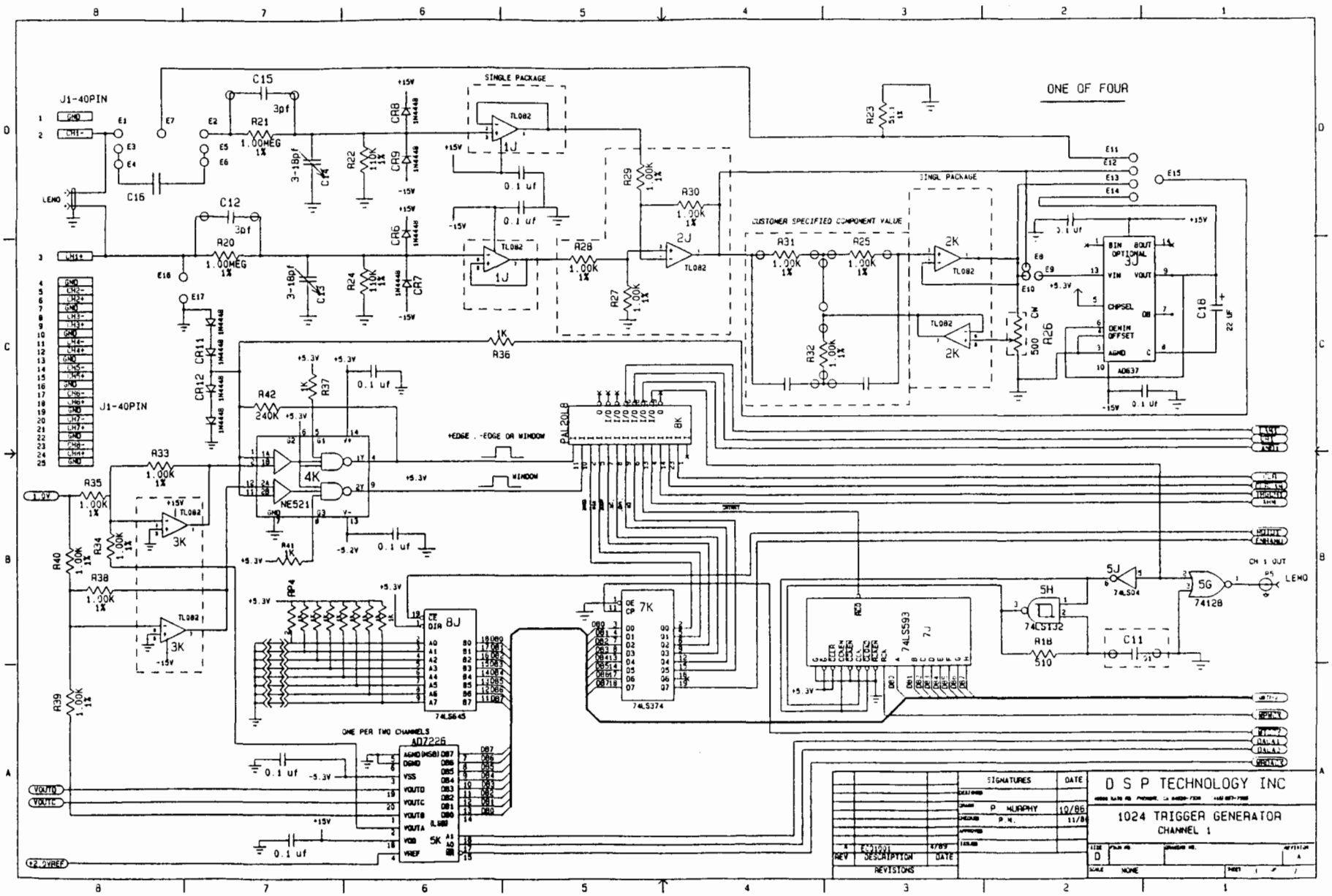
Assembly: A-1024-02 (ASSY: F/P MECH, 4CH SIGNAL CONDITIO)
Revision: A
As of: 11/10/90

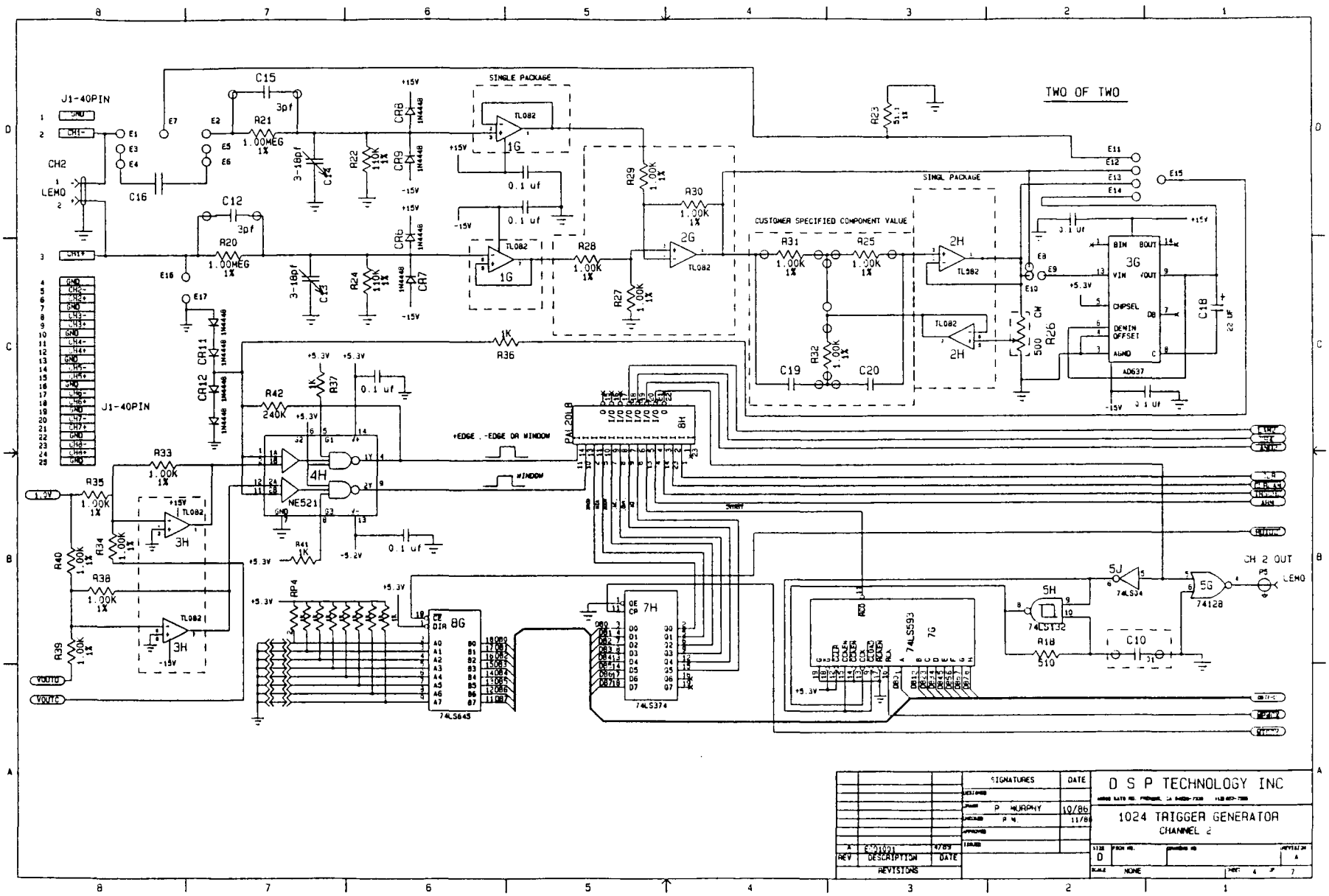
Date: 11/13/90

	Component	Description	Qty Per	As of	Until	Reference
1.	1040-0001	DLE LED GREEN LITRONIX LDG1152	1.00	03/08/87	12/31/99	
2.	5510-0004	CON RT ANGLE LEMO EPL 00 250 NTN	9.00	03/08/87	12/31/99	J2-J10
3.	5511-0001	CONN: PNL MT 2P LEMO ERA 0S 302 CNL	4.00	12/01/87	12/31/99	
4.	5511-0004	HDW GND LUG 2P LEMO GCA 0S 255 LT	4.00	12/01/87	12/31/99	
5.	6851-0073	PNL: FR, 1024	1.00	12/01/87	12/31/99	
6.	6852-0001	SCR:FT PNL JCK DEUTCH 07500M484	1.00	07/22/87	12/31/99	
7.	6852-0031	PNL REAR #1 DWG #2812-03-FD	1.00	07/22/87	12/31/99	
8.	8030-0003	CBL:SHLD PAIR,TW,24 AWG,TYPE E	3.00	12/01/87	12/31/99	
9.	A-1024-01	ASSY: PCB, 1024 4CH SIGNAL CONDITIO	1.00	05/11/87	12/31/99	


+15V
REF-02
REF-2
TEMP
TRIM
VOUT
VIN
GND
3A
3B
TL082
R3
3010
1%
R4
25
1%
R2
1.00K
1%
+2.2VREF
-1.2VREF
VR2
LM337
VOUT
VIN
ADJ
VR1
LM317
VIN
VOUT
ADJ
F1
F4
F3
F2
4A
C7
C4
4.7uf
R15
2.7K
R14
240
R12
R13
CR2
CR1
1N5624
-15V
+15V
+5.2V
-5.3V
SYMBOLS.
CAMAC EDGE CONNECTOR
EXTERNAL CONNECTOR,
CONTINUE ON SAME SHEET
CONTINUE ON DIFFERENT SHEET
UNUSED PIN
JUMPERS
SINGLE PIN SOCKET
NOTES. (UNLESS OTHERWISE SPECIFIED)
1. ALL CAPACITORS ARE IN uf.
2. ALL RESISTORS ARE IN OHMS.
SIGNATURES
DATE
PATRICK MURPHY
11/86
D S P TECHNOLOGY INC
1024 TRIG GENERATOR
1024-01-SD
REVISIONS
REV
DESCRIPTION
DATE


9G
PAL16L8
9F
74184
9E
74LS138
10E
74LS138
9C
PAL20L10
9D
74LS221
9D
74LS221
R19
510
FRONT PANEL
'H' LED
1uf
R11
21K
100pf
R8
5.1K
5C
74LS04
6A
PAL20S10
5A
PAL20L10
9A
IBS030
8A
74LS640
10A
IBS030
11C
HM6264ALSP-12
11A
74LS642
R7
10K
R9
10K
R10
10K
BATT
3.6V
LITHIUM
CR3
CR4
HP2811
4A
74LS00
7A
7401
+5.3V
+5.3 V
READ
LAMINT
SIGNATURES
DATE
11/86
11/86
D S P TECHNOLOGY INC
1024 TRIGGER GENERATOR CONTROL
1024-01-SD
A
NONE
2
7


ONE OF FOUR
J1-40PIN
SINGLE PACKAGE
CUSTOMER SPECIFIED COMPONENT VALUE
+EDGE, -EDGE OR WINDOW
WINDOW
ONE PER TWO CHANNELS
AD7226
PAL20L8
74LS645
74LS374
74LS593
74LS132
74LS04
74128
AD637
D S P TECHNOLOGY INC
1024 TRIGGER GENERATOR
CHANNEL 1
SIGNATURES
DATE
P. MURPHY
10/86
REVISIONS

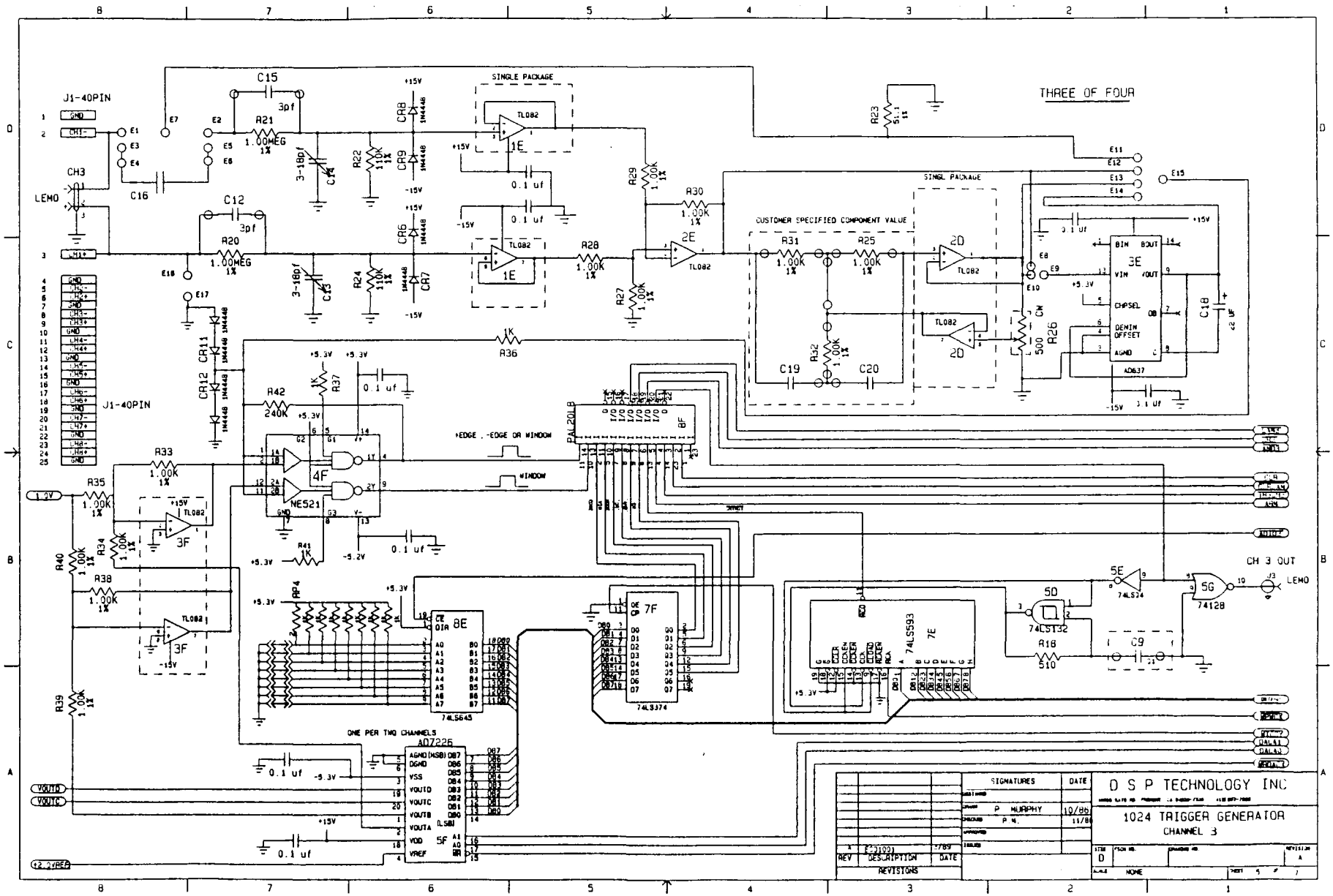


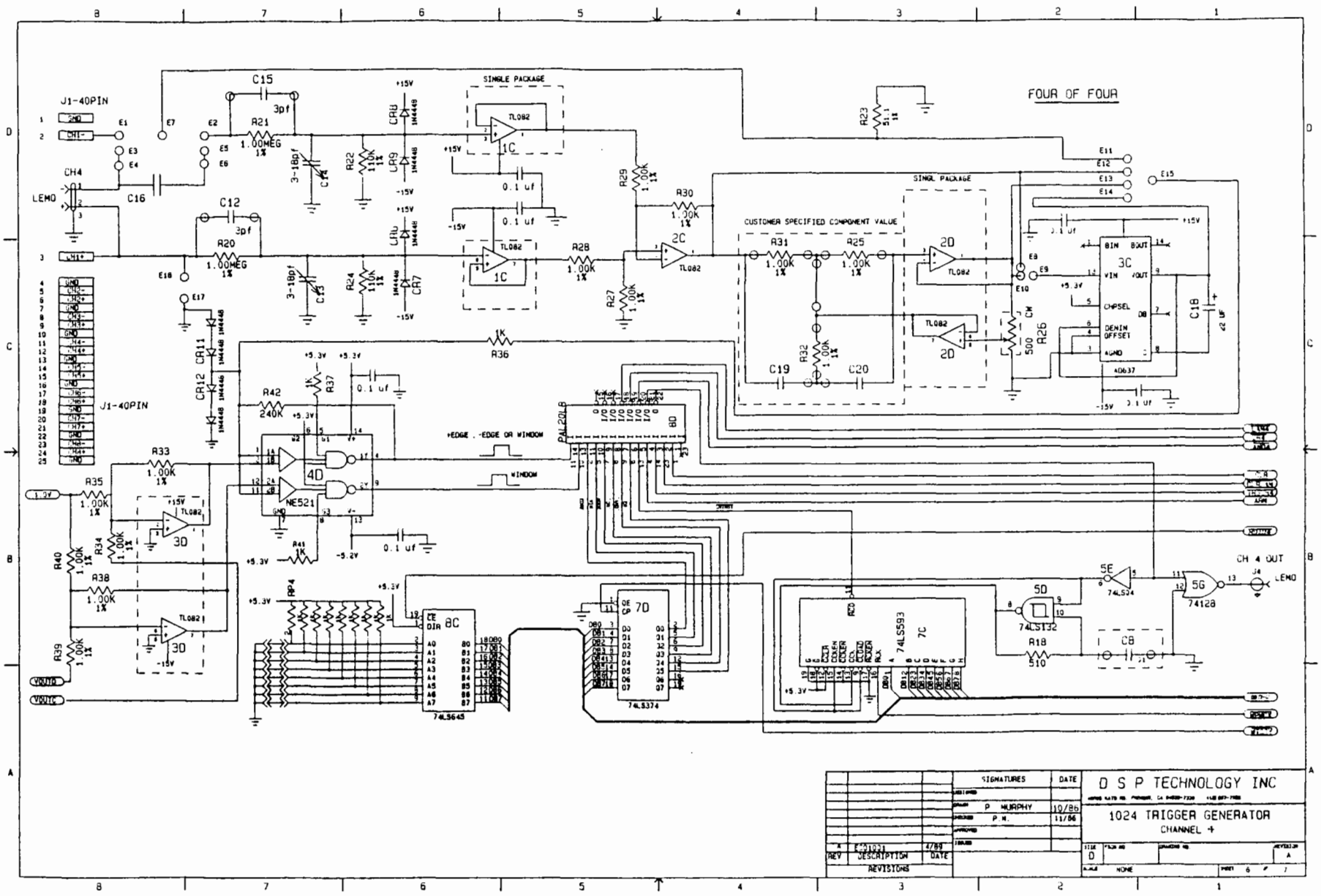
REVISIONS				SIGNATURES	DATE
REV	DESCRIPTION	DATE			
A	E.C.O.1021	4/89		P MURPHY	10/86
					11/86

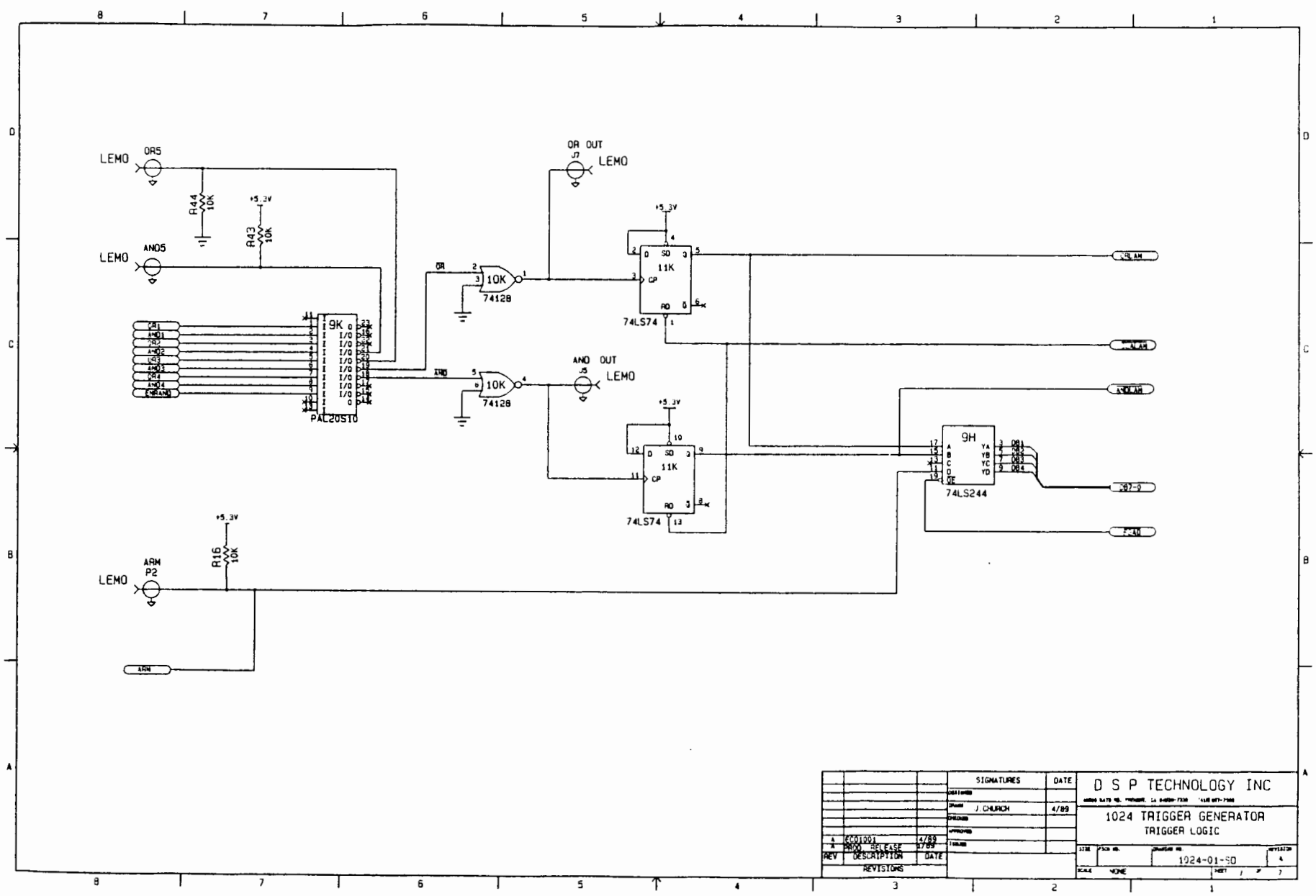
D S P TECHNOLOGY INC

1024 TRIGGER GENERATOR
CHANNEL 2

SIZE D | SCALE NONE


THREE OF FOUR
J1-40PIN
LEMO
CH3
SINGLE PACKAGE
CUSTOMER SPECIFIED COMPONENT VALUE
TL082
NE521
PAL20L8
74LS645
74LS374
74LS593
74LS32
74LS24
74128
AD7226
AD637
ONE PER TWO CHANNELS
+EDGE , -EDGE OR WINDOW
+WINDOW
CH 3 OUT
D S P TECHNOLOGY INC
1024 TRIGGER GENERATOR
CHANNEL 3
SIGNATURES
DATE
P MURPHY
10/86
11/86
REVISIONS
DESCRIPTION
NONE


FOUR OF FOUR
J1-40PIN
CH4
LEMO
SINGLE PACKAGE
TL082
CUSTOMER SPECIFIED COMPONENT VALUE
+EDGE , -EDGE OR WINDOW
WINDOW
PAL20L8
NE521
74LS374
74LS593
74LS645
74LS32
74LS04
74128
AD637
CH 4 OUT
LEMO
D S P TECHNOLOGY INC
1024 TRIGGER GENERATOR
CHANNEL +
SIGNATURES
DATE
P MURPHY
10/86
11/86
REVISIONS
REV
DESCRIPTION
DATE


LEMO
OR5
R44
10K
+5.3V
R43
10k
LEMO
AND5
OR
10K
74128
OR OUT
J7
LEMO
+5.3V
11K
74LS74
AND
10K
74128
AND OUT
J5
LEMO
+5.3V
11K
74LS74
9K
PAL20S10
9H
74LS244
+5.3V
R16
10K
ARM
P2
LEMO
ARM
SIGNATURES
DATE
J. CHURCH
4/89
D S P TECHNOLOGY INC
1024 TRIGGER GENERATOR
TRIGGER LOGIC
1024-01-SD
REVISIONS
REV
DESCRIPTION
DATE
SCALE NONE

dsp Technology Inc.

PRODUCT WARRANTY

(Excludes Software)

DSP TECHNOLOGY ("DSP") warrants its products to be free from defects in material and workmanship and to meet DSP's performance specifications. The warranty period is one year from the date of shipment to the buyer. The warranty is limited by the paragraphs below.

RETURN TO FACTORY

If a buyer discovers a defect in a DSP product covered by this agreement, buyer's exclusive remedy is to ship the product back to DSP's Fremont factory, where DSP will, at its option, either repair or replace the product. This remedy applies if DSP receives the returned product on or before the tenth day after the expiration of the warranty period and the buyer notifies DSP of the defect before returning the product.

COST TO BUYER OF REPAIRS OR REPLACEMENT

Buyer must prepay freight charges to DSP. DSP will pay standard return freight to buyer. Buyer will be charged for premium freight if that method of transport is requested by buyer. There is no other charge for repair or replacement during the warranty period.

TRANSFERRABLE WARRANTIES

In addition to the foregoing warranty, DSP also provides the buyer the transferrable warranty, if any, provided to DSP by the manufacturers of other products such as terminals and disk systems supplied by SEC as part of a total system.

LIMITATION OF WARRANTY AND LIABILITY

The foregoing constitutes DSP's entire warranty, expressed, implied, and/or statutory (except as to title), and to any other party for any breach of such warranty and for damages, whether direct, special, incidental, or consequential. Other than as expressly provided in this document, no warranties expressed or implied, including any warranty of merchantability or fitness for a particular purpose are made. No employee, representative, or agent or seller has any authority expressed or implied to alter or supplement the terms of this warranty.

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