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DSP1030

4 CHANNEL PROGRAMMABLE AMPLIFIER

USER REFERENCE MANUAL

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SECTION 1

INTRODUCTION

The DSP model 1030 is a 4 channel wideband amplifier packaged in a single width CAMAC module. Input voltage ranges are selectable from +/-25mv to +/-25V in 1-2-5 steps. The input impedance of each channel can be selected to be either 50 ohms or 1 megohm. Coupling for each channel can be either AC or DC. Each channel's output can be offset +/-250mv in 2mv steps. These parameters can be selected for each channel independently via the CAMAC dataway. All setup parameters for each amplifier are stored in battery backed up memory.

SECTION 2

SPECIFICATIONS

ANALOG INPUTS

Connector:	Lemo coaxial
Impedance:	1 megohm or 50 ohms, programmable via CAMAC dataway
Full scale:	50 mv p-p to 50 V p-p 1-2-5 steps
Gains:	.01, .025, .05, .1, .25, .5, 1, 2.5, 5, 10
Maximum input voltage:	a) With 1 megohm input impedance selected: $\pm$50 V at input sensitivities of $\pm$25mv to $\pm$500mv. $\pm$250 V (DC + peak AC) for other range settings. b) With 50 ohm input impedance selected: 7 VDC (50mv to 10 V range)
Bandwidth:	-3db at $\geq$ 100 MHz minimum for all gain settings.

ANALOG OUTPUTS

Connector:	Lemo coaxial
Impedance:	50 ohms, $\pm$2%
Output range:	+/-250mv max; includes +/-250mv signal + offset (output terminated into 50 ohms)
Offset range:	+/-250mv, settable in approx. 2mv steps via the CAMAC dataway

CAMAC COMMANDS

F(0) .A(0) .N:	Read channel one control register (R1-R8)
F(0) .A(1) .N:	Read channel two control register (R1-R8)
F(0) .A(2) .N:	Read channel three control register (R1-R8)
F(0) .A(3) .N:	Read channel four control register (R1-R8)
F(0) .A(4) .N:	Read channel one offset register (R1-R8)
F(0) .A(5) .N:	Read channel two offset register (R1-R8)
F(0) .A(6) .N:	Read channel three offset register (R1-R8)
F(0) .A(7) .N:	Read channel four offset register (R1-R8)
F(3) .A(0) .N:	Read module identifier (R1-R16)
F(16) .A(0) .N:	Write channel one control register (R1-R8)
F(16) .A(1) .N:	Write channel two control register (R1-R8)
F(16) .A(2) .N:	Write channel three control register (R1-R8)
F(16) .A(3) .N:	Write channel four control register (R1-R8)
F(16) .A(4) .N:	Write channel one offset register (R1-R8)
F(16) .A(5) .N:	Write channel two offset register (R1-R8)
F(16) .A(6) .N:	Write channel three offset register (R1-R8)
F(16) .A(7) .N:	Write channel four offset register (R1-R8)

CONTROLS AND INDICATORS

LED INDICATORS

N — Indicates that the module is being addressed by the computer.

SELECTED CHANNEL — Four LED lamps one for each channel, indicating which channel's status is being displayed on the front panel status lights.

GAIN — Four LED lamps that indicate the gain of the amplifier in the selected channel, according to the encoding shown below:

LED 3	LED 2	LED 1	LED 0	GAIN	VFS
OFF	OFF	OFF	OFF	10	50mv
OFF	OFF	OFF	ON	5	100mv
OFF	OFF	ON	OFF	2.5	200mv
OFF	OFF	ON	ON	1	500mv
OFF	ON	OFF	OFF	.5	1v
OFF	ON	OFF	ON	.25	2v
OFF	ON	ON	OFF	.1	5v
OFF	ON	ON	ON	.05	10v
ON	OFF	OFF	OFF	.025	20v
ON	OFF	OFF	ON	.01	50v

GND — When this lamp is on, the selected amplifier's input is disconnected from its input connector and connected to ground through a 50 ohm resistor.

AC — When this lamp is on, the selected amplifier's input is AC coupled.

HIZ — When this lamp is on, the selected amplifier's input impedance is 1 megohm; when it is off, the impedance is 50 ohms.

CONTROLS

SELECT — This pushbutton increments the selected channel by one each time it is pushed. When the selected channel is channel 4, the next push of the SELECT button selects channel 1.

CONNECTORS

INPUT — Each of the four channels has a LEMO coaxial input connector.

OUTPUT — Each of the four channels has a LEMO coaxial output connector.

CAMAC CONTROL

F(0) A(0) N Read channel 1 controls. This command reports amplifier status regarding gain setting, coupling, input impedance and enabled/ground state. Data on the R lines reports the status according to the table below:

R4	R3	R2	R1	GAIN	VFS
0	0	0	0	10	50mv
0	0	0	1	5	100mv
0	0	1	0	2.5	200mv
0	0	1	1	1	500mv
0	1	0	0	.5	1v
0	1	0	1	.25	2v
0	1	1	0	.1	5v
0	1	1	1	.05	10v
1	0	0	0	.025	20v
1	0	0	1	.01	50v

R5 = 0: Channel input impedance is 1 megohm
R5 = 1: Channel input impedance is 50 ohms
R6 = 0: Channel is DC coupled
R6 = 1: Channel is AC coupled
R7 = 0: Channel is enabled
R7 = 1: Channel is disabled and grounded

F(0) A(1) N Read channel 2 controls. This command reports amplifier status regarding gain setting, coupling, input impedance and enabled/grounded state. Data on the R lines reports the status according to the table shown for F(0) A(0) N.

F(0) A(2) N Read channel 3 controls. This command reports amplifier status regarding gain setting, coupling, input impedance and enabled/grounded state. Data on the R lines reports the status according to the table shown for F(0) A(0) N.

F(0) A(3) N Read channel 4 controls. This command reports amplifier status regarding gain setting, coupling, input impedance and enabled/grounded state. Data on the R lines reports the status according to the table shown for F(0) A(0) N.

F(0) A(4) N Read channel 1 offset setting (R1-R8). R1-R8 represent a binary code, with R1 being the LSB. A code of 0 indicates that the output of this channel (terminated in 50 ohms), with no signal, will be offset -.25 volts. A code of 255 indicates that the offset is +.25 volts.

F(0) A(5) N Read channel 2 offset setting (R1-R8). R1-R8 represent a binary code, with R1 being the LSB. A code of 0 indicates that the output of this channel (terminated in 50 ohms), with no signal, will be offset -.25 volts. A code of 255 indicates that offset is +.25 volts.

F(0) A(6) N Read channel 3 offset setting (R1-R8). R1-R8 represent a binary code, with R1 being the LSB. A code of 0 indicates that the output of this channel (terminated in 50 ohms), with no signal, will be offset -.25 volts. A code of 255 indicates that the offset is +.25 volts.

F(0) A(7) N Read channel 4 offset setting (R1-R8). R1-R8 represent a binary code, with R1 being the LSB. A code of 0 indicates that the output of this channel (terminated in 50 ohms), with no signal, will be offset -.25 volts. A code of 255 indicates that the offset is +.25 volts.

F(3) A(0) N Read module identifier (R1-R16).

F(16) A(0) N Write channel 1 controls. This command sets amplifier gain, coupling, input impedance and enabled/grounded state. W1-W7 control the status according to the table below:

W4	W3	W2	W1	GAIN	VFS
0	0	0	0	10	50mv
0	0	0	1	5	100mv
0	0	1	0	2.5	200mv
0	0	1	1	1	500mv
0	1	0	0	.5	1v
0	1	0	1	.25	2v
0	1	1	0	.1	5v
0	1	1	1	.05	10v
1	0	0	0	.025	20v
1	0	0	1	.01	50v

W5 = 0: Channel input impedance is 1 megohm
W5 = 1: Channel input impedance is 50 ohms
W6 = 0: Channel is DC coupled
W6 = 1: Channel is AC coupled
W7 = 0: Channel is enabled
W7 = 1: Channel is disabled and grounded

F(16) A(1) N Write channel 2 controls. This command sets amplifier gain, coupling, input impedance and enabled/grounded state. W1-W7 control the status according to the table for F(16) A(0) N.

F(16) A(2) N Write channel 3 controls. This command sets amplifier gain, coupling, input impedance and enabled grounded state. W1-W7 control the status according to the table for F(16 A(0) N.

F(16) A(3) N Write channel 4 controls. This command sets amplifier gain, coupling, input impedance and enabled/grounded state. W1-W7 control the status according to the table for F(16) A(0) N.

F(16) A(4) N Write channel 1 offset DAC. This command writes data on W1-W8 to the offset DAC. W1 is the LSB. A code of 0 offsets the output to -.25v. A code of 255 offsets the output to +.25v. The output can be offset in 2mv steps using the following expression.

V offset = (0.500/256) * (code-128)

F(16) A(5) N Write channel 2 offset DAC. This command writes data on W1-W8 to the offset DAC. W1 is the LSB. A code of 0 offsets the output to -.25v. A code of 255 offsets the output to +.25v The output can be offset in 2mv steps using the following expression.

V offset = (0.500/256) * (code-128)

F(16) A(6) N Write channel 3 offset DAC. This command writes data on W1-W8 to the offsets DAC. W1 is the LSB. A code of 0 offsets the output to -.25v. A code of 255 offsets the output to +.25v. The output can be offset in 2mv steps using the following expression.

V offset = (0.500/256) * (code-128)

F(16) A(7) N Write channel 4 offset DAC. This command writes data on W1-W8 to the offset DAC. W1 is the LSB. A code of 0 offsets the output to -.25v. The output can be offset in 2mv steps using the following expression.

V offset = (0.500/256) * (code-128)

FUNCTIONAL DESCRIPTION

GENERAL

Refer to Fig.1, 1030 Block Diagram. The 1030 module contains four independent wideband amplifiers, each with seperate controls for coupling, termination, gain, offset, and enable/disable. These controls are accessible only from the CAMAC dataway. However, the status of each amplifier (except for offset) can be viewed on front panel indicator lights. These lights indicate the status of one channel, which is selected by operating the SELECT pushbutton. The channel currently being displayed is also shown on the front panel LEDs.

In addition to the four amplifier channels, the module contains a block of logic to decode and implement CAMAC commands, another block of logic to retain the setup information when the power is shut down (battery backup), and a power supply and reference voltage section.

To isolate the amplifier channels from crosstalk and power supply noise, each amplifier has its own ground plane as well as the liberal use of ferrite beads to reduce RF signals on power planes.

AMPLIFIER

GENERAL

Each amplifier has two stages. The first stage sets the coupling, enable/disable, and termination parameters, and also does coarse signal attenuation and impedance transformation for the second stage. Input protection is provided here also. The second stage provides gain, fine signal attenuation and signal offsetting.

INPUT STAGE

Refer to Fig 2, 1030 Input Stage Diagram. Signals entering the amplifier go to terminals on two relays. The first connects the input to a 50 ohm termination resistor, if desired; The second either connects the amplifier proper to the signal input or to a 50 ohm termination, providing the enable/disable function. Assuming that the amplifier is enabled, the signal next encounters the AC coupling capacitor, with its shorting relay (for DC coupling). Next the signal encounters two parallel 2 megohm attenuators, with a voltage attenuation factor of 1/10 or 1/100. A one-of three analog multiplexer selects either the X 1, X 0.1, or X 0.01 attenuation to the following circuitry. The signal thus selected is applied to the input of a FET voltage follower, which supplies a low impedance drive to the output stage. The X 1 multiplexer relay, switchs in a capacitor to replace the input capacitance of the FET follower in order to maintain a constant capacitance in the attenuator input node.

INPUT STAGE DETAILS

Refer to Sheet 2 of the Schematic Diagram. Only channel 1 will be described; All other channels are identical. Signals enter via J1 on the front panel. K8 selects the 50 ohm termination, formed by the parallel combination of R47 and R48. Relay K9 selects either the input signal or terminating resistor R46. C54 is the AC coupling capacitor, in parallel with shorting relay K7. R44 provides a current limit to the overload protection circuitry at the amplifier input when the X 1 attenuation is selected by K6. C49 maintains compensation for the following RC attenuator networks. The 1/10 attenuator is formed by R37-R40, C47, C50 and C51. The variable capacitor C51 adjusts the low frequency peaking of the attenuator section. The 1/100 attenuator is formed by R35, R36, R42, R43, C42, C43 and C46. The variable capacitor C45 adjusts the low frequency peaking of the attenuator section.

The X 1 switch on the 1-of-3 multiplexer is relay K6. Both contact sets are used to provide extra "off" state isolation. C49 connects to the input terminal whenever the amplifier is switched elsewhere, to assure that the amplifier input capacitance remains constant at all gain settings. The X 0.1 switch is K5. K4 selects the X 0.01 setting on the multiplexer.

Dual low-leakage diode D5 prevents the amplifier input from swinging more than about +/-6 volts when overdriven, to protect the amplifier input and following circuitry. 1F is a FET-input unity-gain buffer, which provides a very high load impedance for the input attenuator and very low driving impedance to the following amplifier stage. R31 and R32 provides offset adjustment for the input stage.

Note that the relay coils and the amplifier power terminals are decoupled by RC on RC networks. These networks protect the input circuitry from system noise and also prevent crosstalk between the compoments.

OUTPUT STAGE

Refer to Fig. 3, 1030 Output Stage Block Diagram. Signals from the input stage drive two parallel attenuators. One attenuates by 0.5, and the second by 0.2. The multiplexer selects the 1-2-5 portion of the inverting input of the amplifier connects to gain switching and offset bias circuitry.

OUTPUT STAGE DETAILS

Refer to Sheet 3 of the 1030 Schematic Diagram. Only channel 1 will be described in detail; all the other channels are identical. Signal from the input stage connects to two parallel attenuators. The X 1 signal flow is from the buffer output thru RX2 and K2 to the amplifier's positive input. The X.5 attenuator is made up of RX3 and R29. The X.2 attenuator uses the X.5 attenuator plus K3 and R27. R30 and C31 are high frequency compensation for the X.5 attenuator. The variable capacitor C31 adjusts the peaking of the X.5 attenuator. The output of the 1-2-5 attenuator is applied to the positive input of the amplifier. The programmable offset voltage is applied to the inverting side of the amplifier. Also there is a gain switch for the X 10 range on the inverting input.

The amplifier has an internal 1K feedback resistor, which is connected by a trace between pins 4 and 11. Gain of the amplifier is set by this resistor and the parallel combination of the resistors connected to the inverting input pin of the amplifier. R18, R19, R20 and R23 are the primary gain-setting resistors. Relay K1 increases the amplifier gain for the X 10 gain setting only, and R19 provides overall adjustment for this gain setting. R18 adjusts overall amplifier gain for all other settings. R24 sets the scale factor for the voltage from the offset D/A convertor. Since the offset convertor is unipolar in nature, an offset current must be provided to make it bipolar; R25 and the 1V reference provide that offset current. R17 sets the output impedance of the amplifier channel.

A fine offset adjustment to compensate for the amplifier bias current error is formed by R81 and R82. The error is unipolar and therefore so is the compensation.

CAMAC DECODING LOGIC

Refer to Sheet 10 of the 1030 Schematic Diagram. There is an internal 8-bit read/write bus to reduce wiring complexity. 7A provides a write path from the CAMAC dataway W lines to this bus, and 8A serves a similar purpose for the CAMAC R lines. These ICs are controlled by 6A, which also generates some CAMAC-originated signals that do not require strobing with S1. 8B generates all signals that require the S1 strobe, as well as some other unstrobed CAMAC signals (such as X and Q). 1A stretches the S1 pulse to blink the N light, and 6B adds some extra channel decoding. 9A and 6A generate the unit ID that is read by F(3) A(0). They drive the R lines independently, because the ID is a 16-bit word. 6D-2 and 6D-4 provide open collector drive to the CAMAC dataway for X and Q.

BATTERY BACKUP LOGIC AND CHANNEL CONTROL DECODING

Refer to Sheet 11 of the 1030 Schematic Diagram. Amplifier status except for offset control is stored in a CMOS register for each channel. These registers are 2A-5A, for channels 1, 2, 3 and 4 respectively. These ICs have a readback feature; i.e. when pin 1 is brought low, data in the registers is presented on the D inputs without disturbing the register Q outputs. 7B prevents operation of the clock inputs to the registers when the power is down. 7D prevents data strobing of the offset D/A convertor (see sheet 13).

2B-5B are small PROMs that further decode the channel setup data contained in the battery backup registers. 6D provides drive power for some of the control relay coils.

FRONT PANEL DISPLAY LOGIC

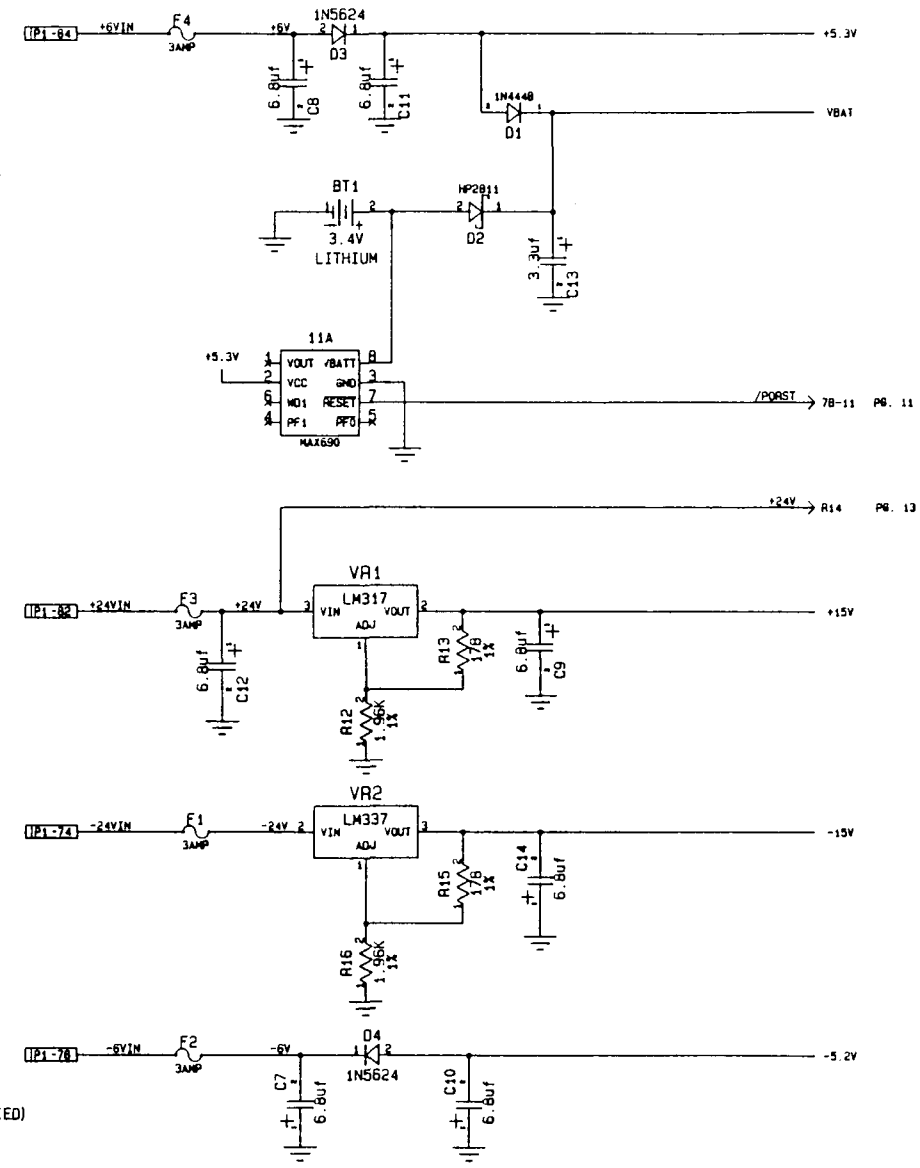
Refer to Sheet 12 of the 1030 Schematic Diagram. The front panel SELECT button is debounced by 1B. Each time the button is pressed, the 2-bit counter formed by 1C increments one count. The counter outputs go to the selection PAL 8B and also are decoded by 1D, which drives the LEDs that indicate the selected channel. The channel status LEDs are driven directly from the 8-bit read/write bus.

POWER SUPPLY

Refer to Sheet 1 of the 1030 Schematic Diagram. D3 drops the 6 volts from the CAMAC connector to near 5 volts, as does D4 for the -6 volts to near -5 volts. Lithium battery BT1 provides powerdown voltage for the backup registers through D2, while D1 supplies the same registers when power is on, saving battery power. 11A serves as a power fail detector and power on reset generator. VR1 and VR2 provide +15 volts and -15 volts, respectively, to the input stage buffers on the amplifiers.

REFERENCE VOLTAGES

Refer to Sheet 13 of the 1030 Schematic Diagram. Precision reference 11B is the master voltage standard for the 1030. 11C derives from it a 1 volt reference, which is used both as a reference for the D/A convertor and as unipolar/bipolar conversion offset for the amplifiers. The D/A convertor 8D is a quad CMOS device with internal latches that can be read back through its input data bus. Its power terminal is connected to the backup battery voltage, thus preserving its settings when power is off. 10B is a quad operational amplifier that that buffers the output of each D/A convertor section, providing drive current for the amplifier offset inputs.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL CAPACITORS ARE IN uf.
2. ALL RESISTORS ARE 1/4W 5% IN OHMS.

REVISIONS

ECO#	REV	BY	DATE	DESCRIPTION	APPRV	DATE
1003	A	JR		PROD RELEASE		
1001	A	JR	12/89	BATTERY CURRENT DRAIN		
1002	B	JR	10/89	BATTERY CURRENT DRAIN		

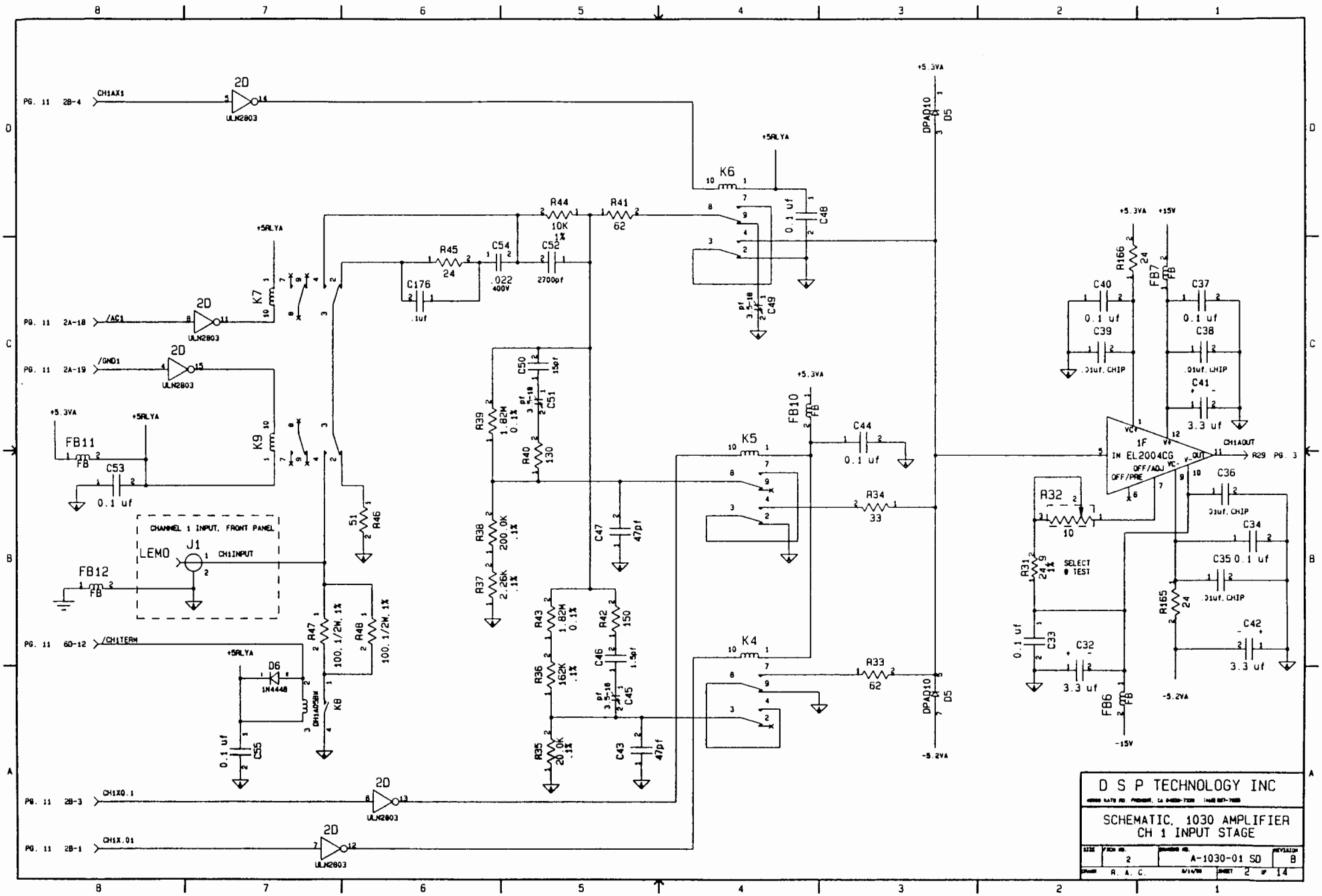
SIGNATURES	DATE
DEL RASMUSSON	

D S P TECHNOLOGY INC

SCHEMATIC, 1030 AMPLIFIER POWER SUPPLY

SIZE	TECH NO.	DRAWING NO.	REVISION
B	01	A-1030-01 SD	B

SCALE NONE SHEET 1 OF 14

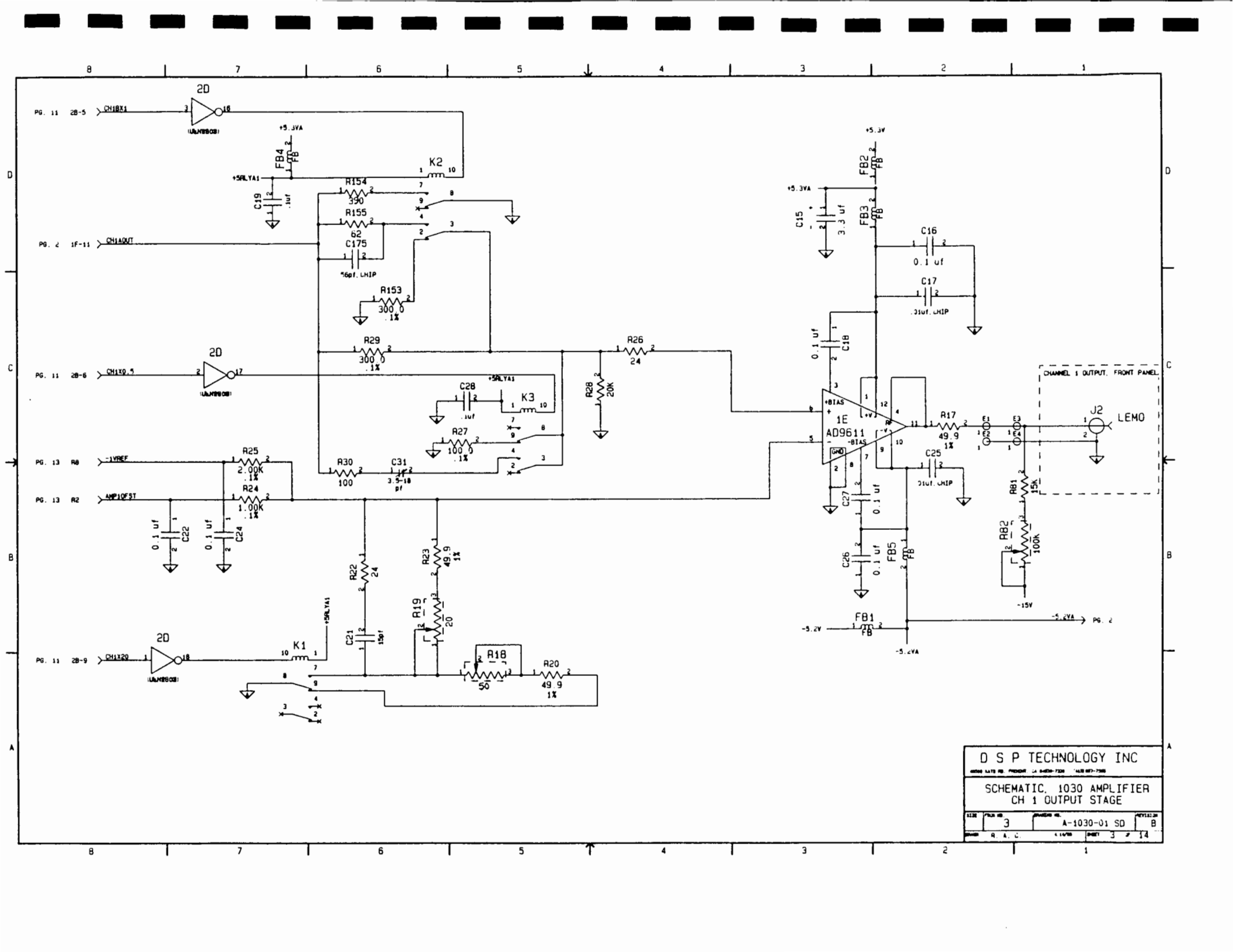


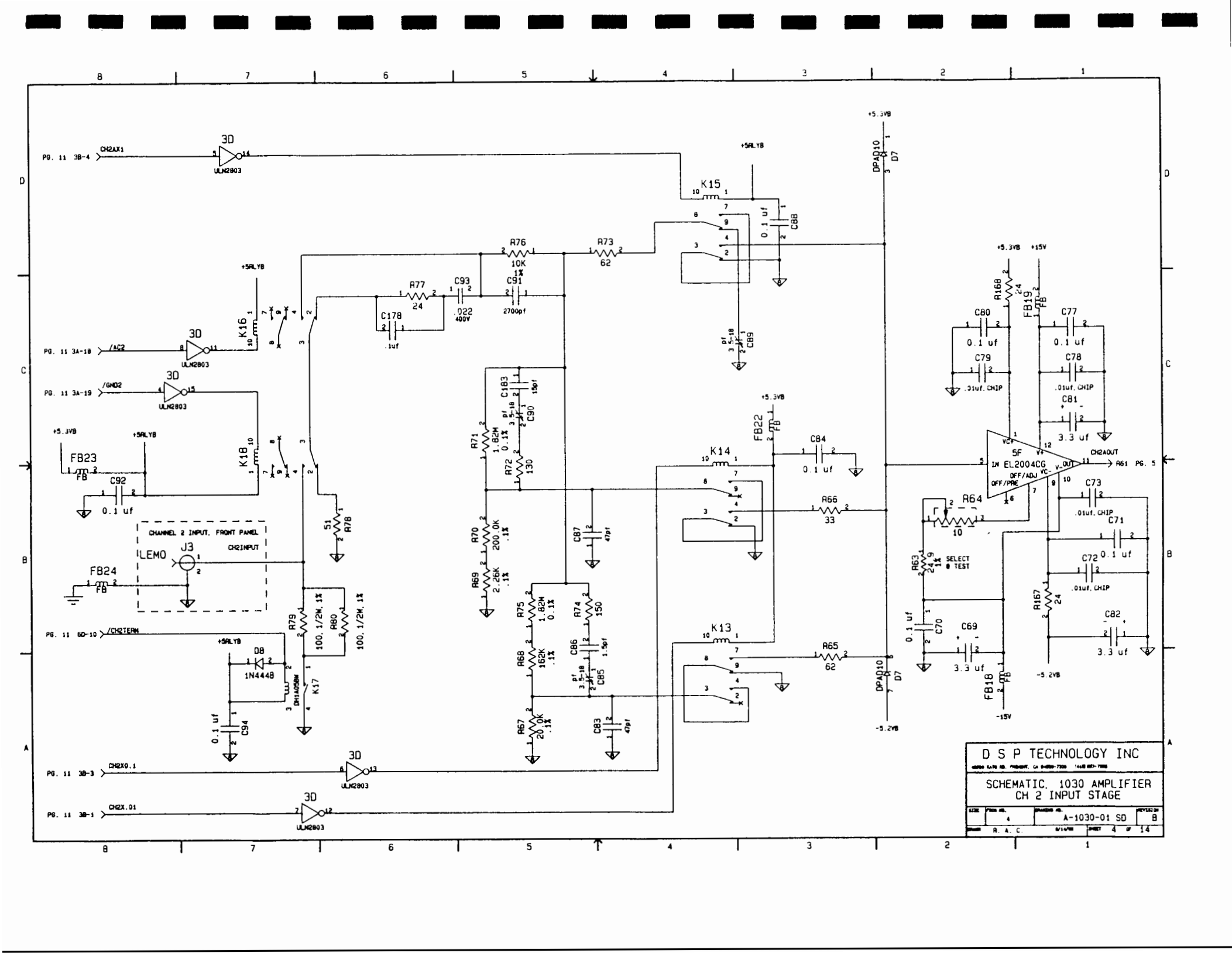
D S P TECHNOLOGY INC

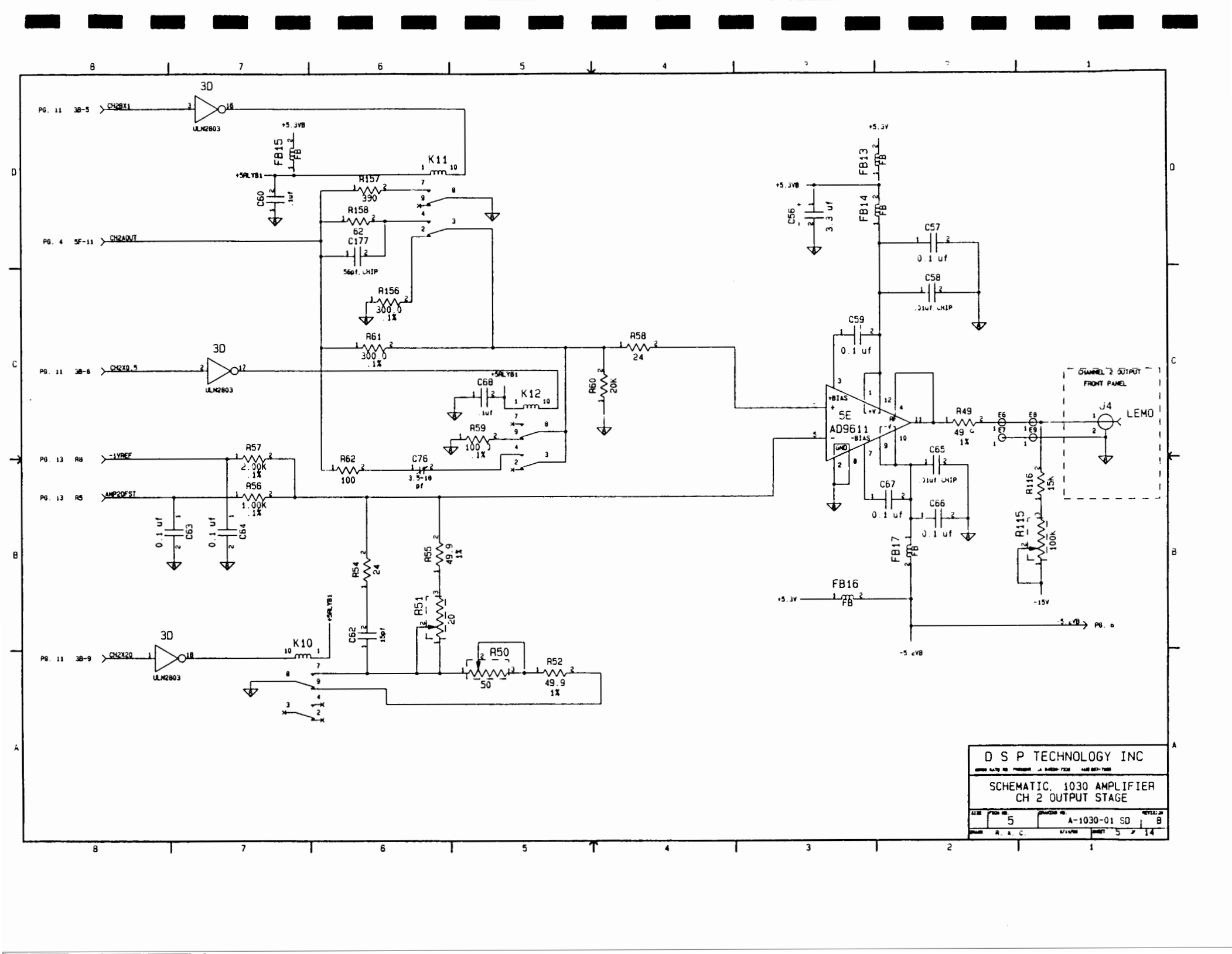
SCHEMATIC, 1030 AMPLIFIER
CH 1 INPUT STAGE

SIZE	FSCM NO.	DRAWING NO.	REVISION
	2	A-1030-01 SD	B

DRAWN R. A. C. 8/14/98 SHEET 2 OF 14


2D
PG. 11 2B-5
CH1BX1
+5.3VA
FB4
K2
+5RLYA1
C19
.1uf
R154
390
R155
62
C175
56pf, CHIP
PG. 2 1F-11
CH1AOUT
R153
300.0
.1%
2D
PG. 11 2B-6
CH1X0.5
R29
300.0
.1%
R26
24
R28
20K
C28
.1uf
K3
R27
100.0
.1%
PG. 13 R8
-1VREF
R25
2.00K
.1%
R30
100
C31
3.5-18
pf
PG. 13 R2
AMP1OFST
R24
1.00K
.1%
0.1 uf
C22
0.1 uf
C24
R22
24
R23
49.9
1%
R19
20
C21
15pf
2D
PG. 11 2B-9
CH1X20
K1
+5RLYA1
R18
50
R20
49.9
1%
+5.3V
FB2
+5.3VA
C15
3.3 uf
FB3
C16
0.1 uf
C17
.01uf, CHIP
0.1 uf
C18
+BIAS
1E
AD9611
-BIAS
GND
CHANNEL 1 OUTPUT, FRONT PANEL
R17
49.9
1%
E1
E3
J2
LEMO
C25
.01uf, CHIP
C27
0.1 uf
R81
15K
R82
100K
-15V
C26
0.1 uf
FB5
FB1
-5.2V
-5.2VA
PG. 2
D S P TECHNOLOGY INC
SCHEMATIC, 1030 AMPLIFIER
CH 1 OUTPUT STAGE
3
A-1030-01 SD
B
SHEET 3 OF 14

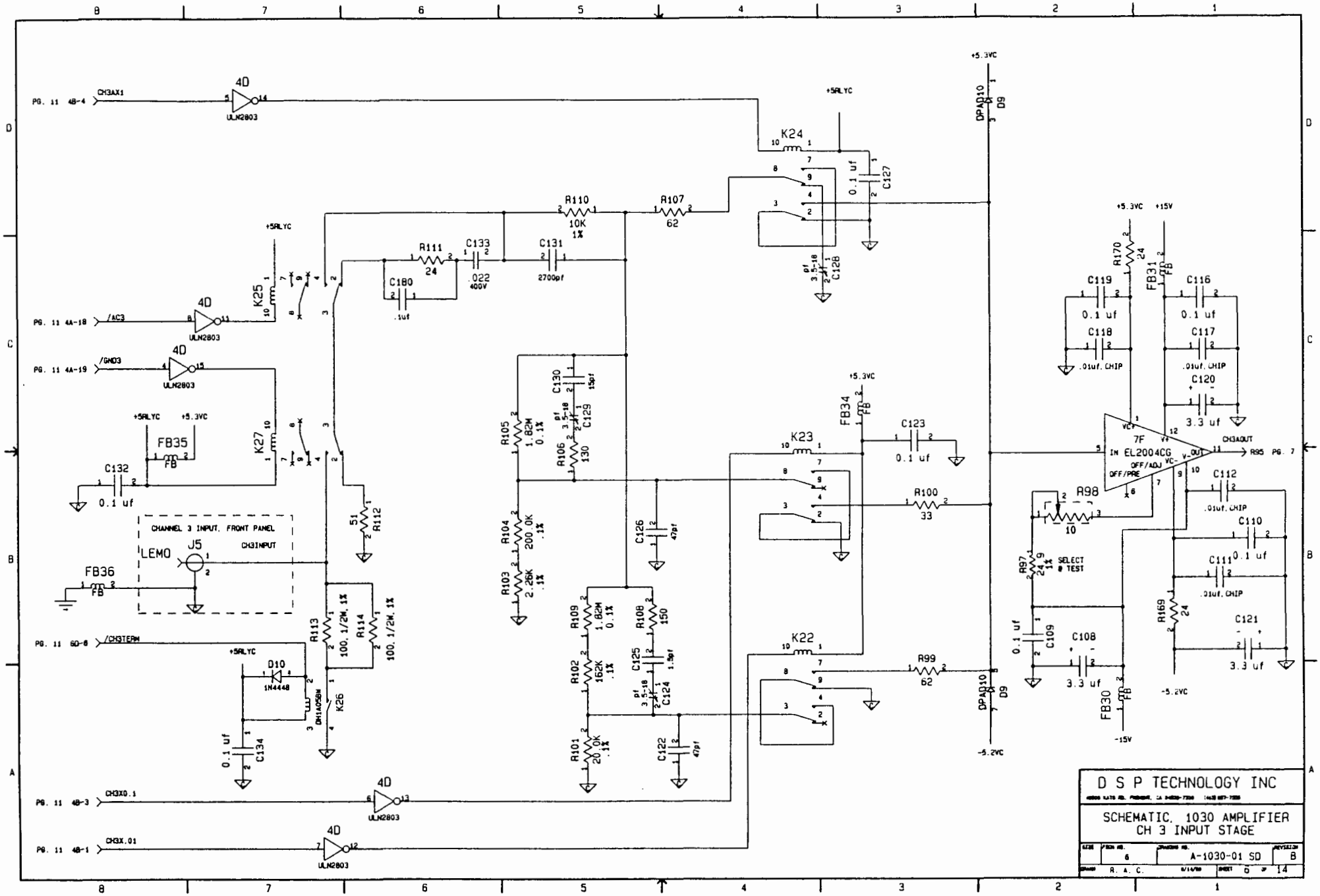

D S P TECHNOLOGY INC
SCHEMATIC, 1030 AMPLIFIER
CH 2 INPUT STAGE
A-1030-01 SD
B
4
R. A. C.
4 OF 14
CHANNEL 2 INPUT, FRONT PANEL
CH2INPUT
LEMO
J3
FB24
FB23
FB22
FB19
FB18
K15
K14
K13
K18
K16
K17
DH1A05BM
1N4448
D8
ULN2803
3D
+5RLYB
+5.3VB
+15V
-15V
-5.2VB
DPAD10
D7
5F
EL2004CG
CH2AOUT
SELECT
B TEST
R64
10
R66
33
R65
62
R76
10K
1%
R73
62
R77
24
C93
.022
400V
C91
2700pf
C178
.1uf
C92
0.1 uf
C88
0.1 uf
C89
C90
C183
15pf
C84
0.1 uf
C87
47pf
C86
1.5pf
C85
C83
47pf
C94
0.1 uf
C80
0.1 uf
C79
.01uf, CHIP
C77
0.1 uf
C78
.01uf, CHIP
C81
3.3 uf
C73
.01uf, CHIP
C71
0.1 uf
C72
.01uf, CHIP
C82
3.3 uf
C69
3.3 uf
C70
0.1 uf
R168
24
R167
24
R71
1.82M
0.1%
R72
130
R70
200.0K
.1%
R69
2.26K
.1%
R75
1.82M
0.1%
R74
150
R68
162K
.1%
R67
20.0K
.1%
R79
100, 1/2W, 1%
R80
100, 1/2W, 1%
R78
51
R63
24.9
1%
PG. 11 3B-4
CH2AX1
PG. 11 3A-18
/AC2
PG. 11 3A-19
/GND2
PG. 11 6D-10
/CH2TERM
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CH2X0.1
PG. 11 3B-1
CH2X.01
PG. 5

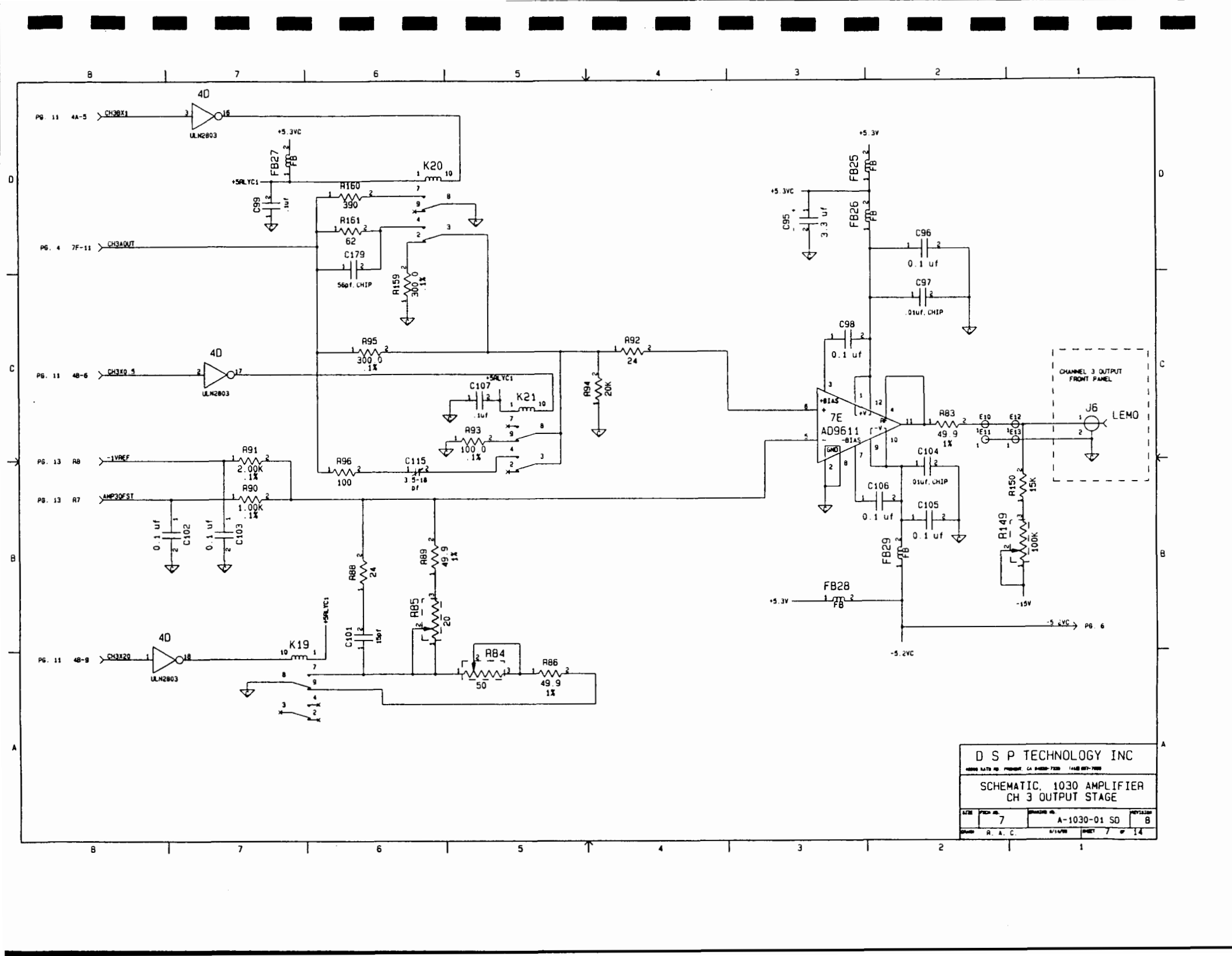


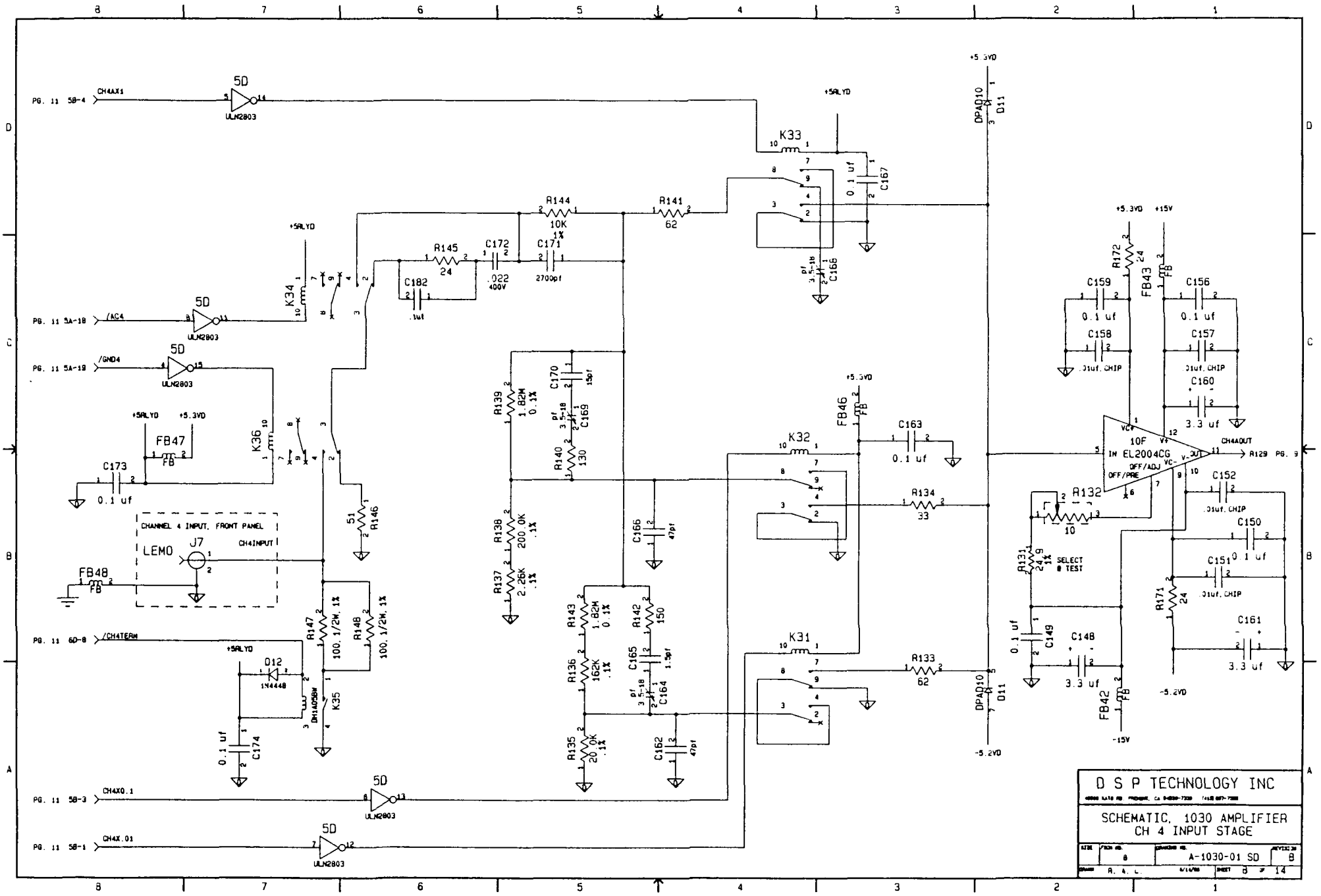
D S P TECHNOLOGY INC

SCHEMATIC, 1030 AMPLIFIER
CH 2 OUTPUT STAGE

SIZE	DRAWING NO.	REVISION
5	A-1030-01 SD	B
DRAWN R. A. C.		SHEET 5 OF 14


CH3AX1
PG. 11 4B-4
4D
ULN2803
+5RLYC
K24
R110
10K
1%
R107
62
0.1 uf
C127
C128
+5.3VC
DPAD10
D9
R111
24
C133
.022
400V
C131
2700pf
C180
.1uf
K25
/AC3
PG. 11 4A-18
/GND3
PG. 11 4A-19
+5.3VC
FB35
FB
C132
0.1 uf
K27
C130
15pf
R105
1.82M
0.1%
R106
130
R104
200.0K
.1%
R103
2.26K
.1%
C126
47pf
FB34
C123
0.1 uf
K23
R100
33
R112
51
CHANNEL 3 INPUT, FRONT PANEL
CH3INPUT
LEMO
J5
FB36
FB
R113
100, 1/2W, 1%
R114
100, 1/2W, 1%
/CH3TEPM
PG. 11 6D-6
D10
1N4448
DH114D05BW
K26
C134
0.1 uf
R109
1.82M
0.1%
R108
150
R102
162K
.1%
C125
1.5pf
C124
47pf
R101
20.0K
.1%
C122
47pf
K22
R99
62
CH3X0.1
PG. 11 4B-3
CH3X.01
PG. 11 4B-1
+5.3VC
+15V
R170
24
FB31
FB
C119
0.1 uf
C118
.01uf, CHIP
C116
0.1 uf
C117
.01uf, CHIP
C120
3.3 uf
7F
EL2004CG
IN
OUT
OFF/ADJ
OFF/PRE
VC+
VC-
CH3AOUT
R95
PG. 7
R98
10
C112
.01uf, CHIP
C110
0.1 uf
C111
.01uf, CHIP
R97
24.9
1%
SELECT
@ TEST
C109
0.1 uf
C108
3.3 uf
R169
24
C121
3.3 uf
FB30
FB
-15V
-5.2VC
D S P TECHNOLOGY INC
SCHEMATIC, 1030 AMPLIFIER
CH 3 INPUT STAGE
A-1030-01 SD
B
R. A. C.
SHEET 6 OF 14


4D
PG. 11 4A-5
CH3BX1
ULN2803
+5.3VC
FB27
FB
K20
+5RLYC1
R160
390
C99
.1uf
R161
62
PG. 4 7F-11
CH3AOUT
C179
56pf. CHIP
R159
300.0
1%
4D
PG. 11 4B-6
CH3X0.5
ULN2803
R95
300.0
1%
C107
.1uf
K21
R93
100.0
1%
R96
100
C115
3.5-18
pf
R92
24
R94
20K
PG. 13 A8
-1VREF
R91
2.00K
1%
PG. 13 A7
AMP3OFST
R90
1.00K
1%
0.1 uf
C102
0.1 uf
C103
R88
24
R89
49.9
1%
R85
20
C101
15pf
4D
PG. 11 4B-9
CH3X20
ULN2803
K19
+5RLYC1
R84
50
R86
49.9
1%
+5.3V
FB25
FB26
FB
C95
3.3 uf
C96
0.1 uf
C97
.01uf. CHIP
C98
0.1 uf
+BIAS
7E
AD9611
-BIAS
GND
+V
-V
R83
49.9
1%
CHANNEL 3 OUTPUT
FRONT PANEL
J6
LEMO
C104
.01uf. CHIP
C106
0.1 uf
C105
0.1 uf
R150
15K
R149
100K
FB29
FB28
-15V
-5.2VC
-5.2VC PG. 6
D S P TECHNOLOGY INC
SCHEMATIC, 1030 AMPLIFIER
CH 3 OUTPUT STAGE
7
A-1030-01 SO
B
R. A. C.
7 OF 14

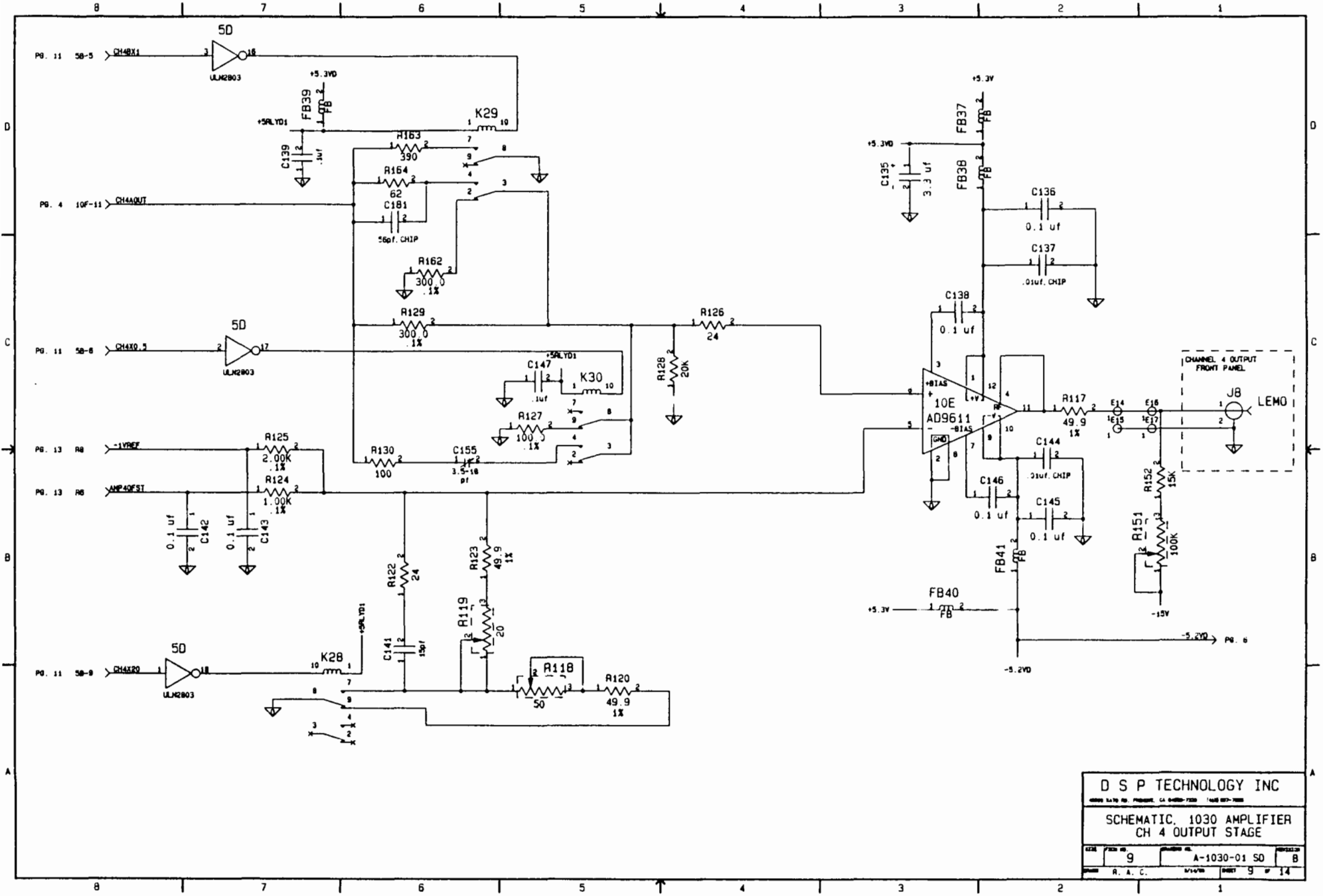


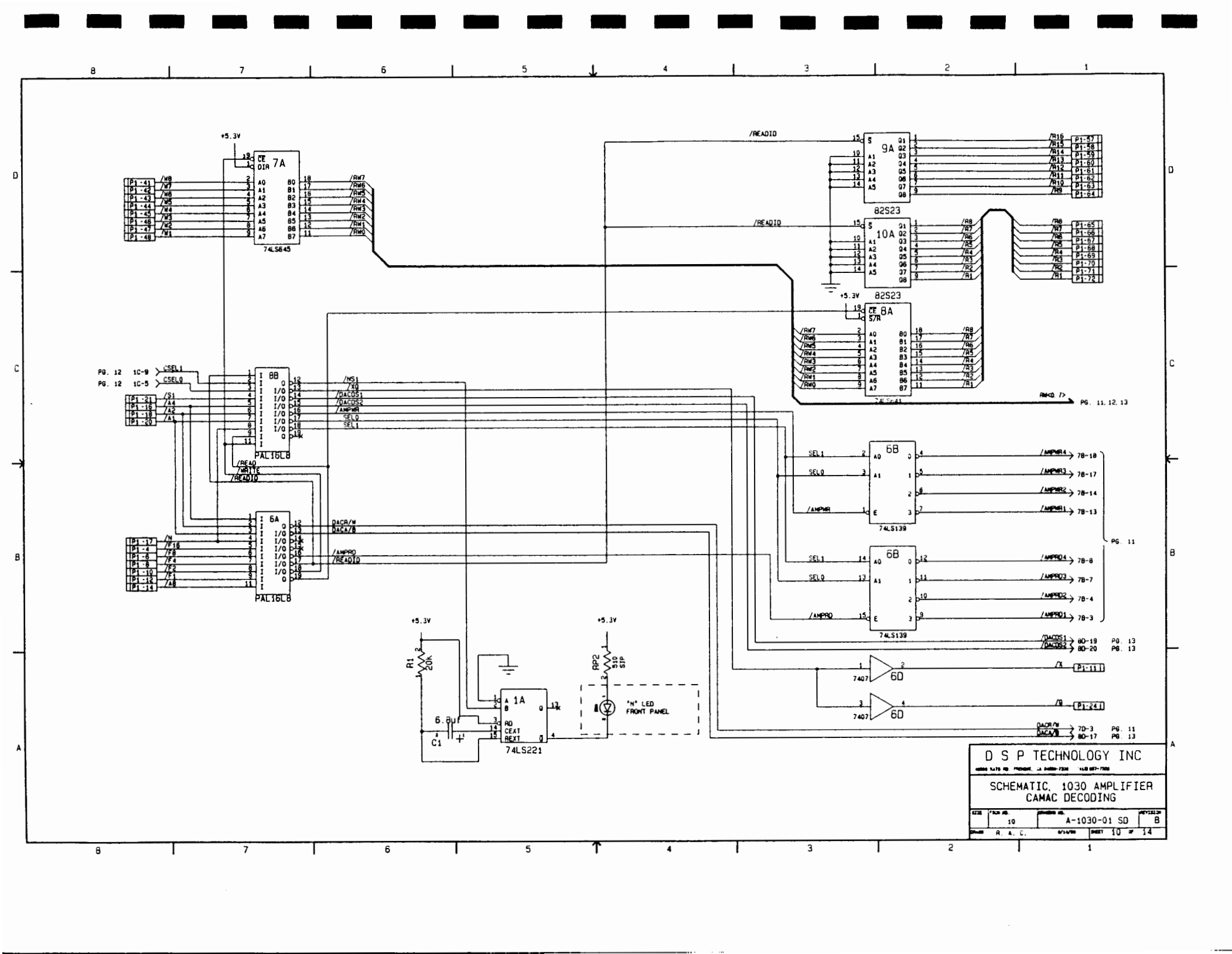
D S P TECHNOLOGY INC

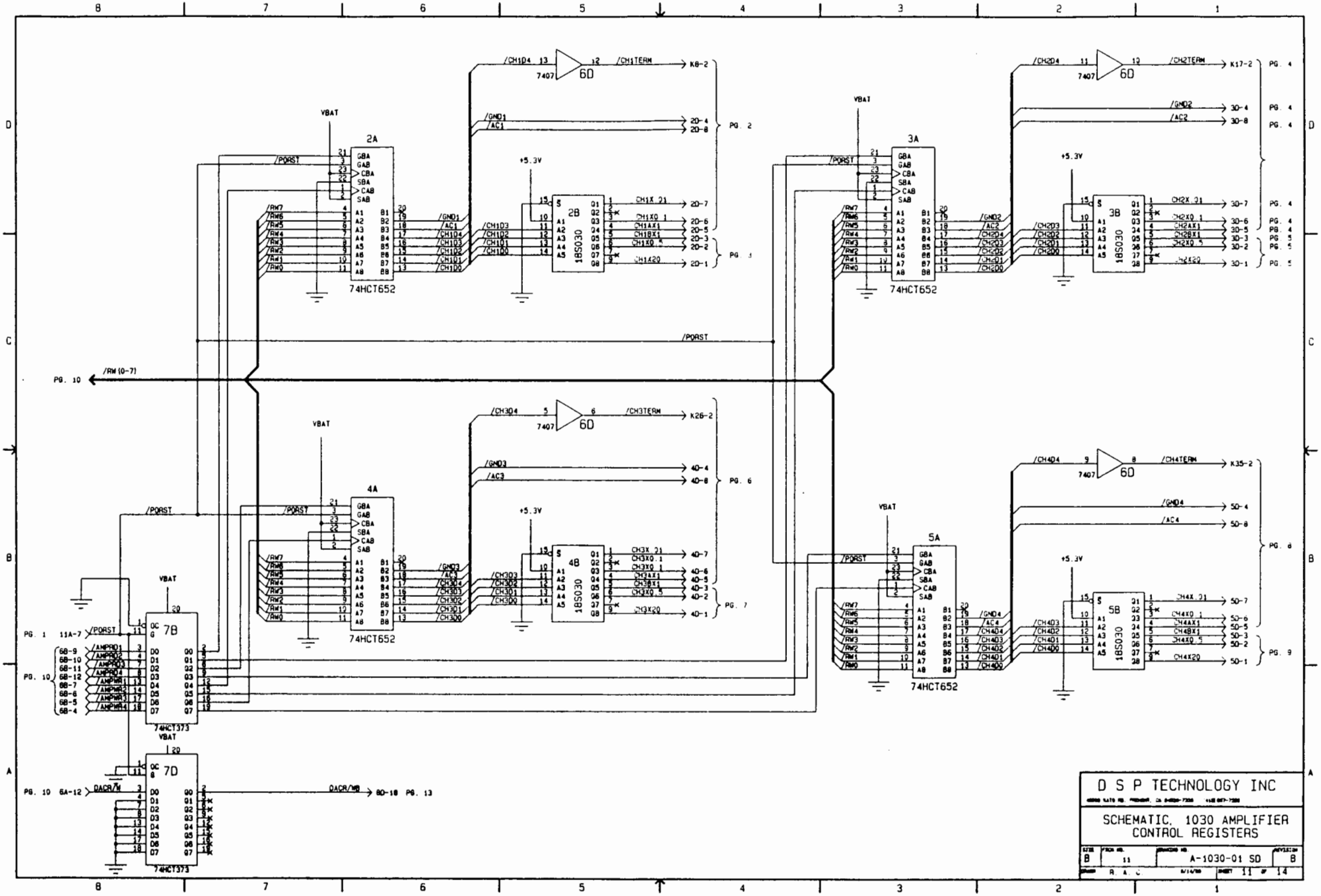
SCHEMATIC, 1030 AMPLIFIER
CH 4 INPUT STAGE

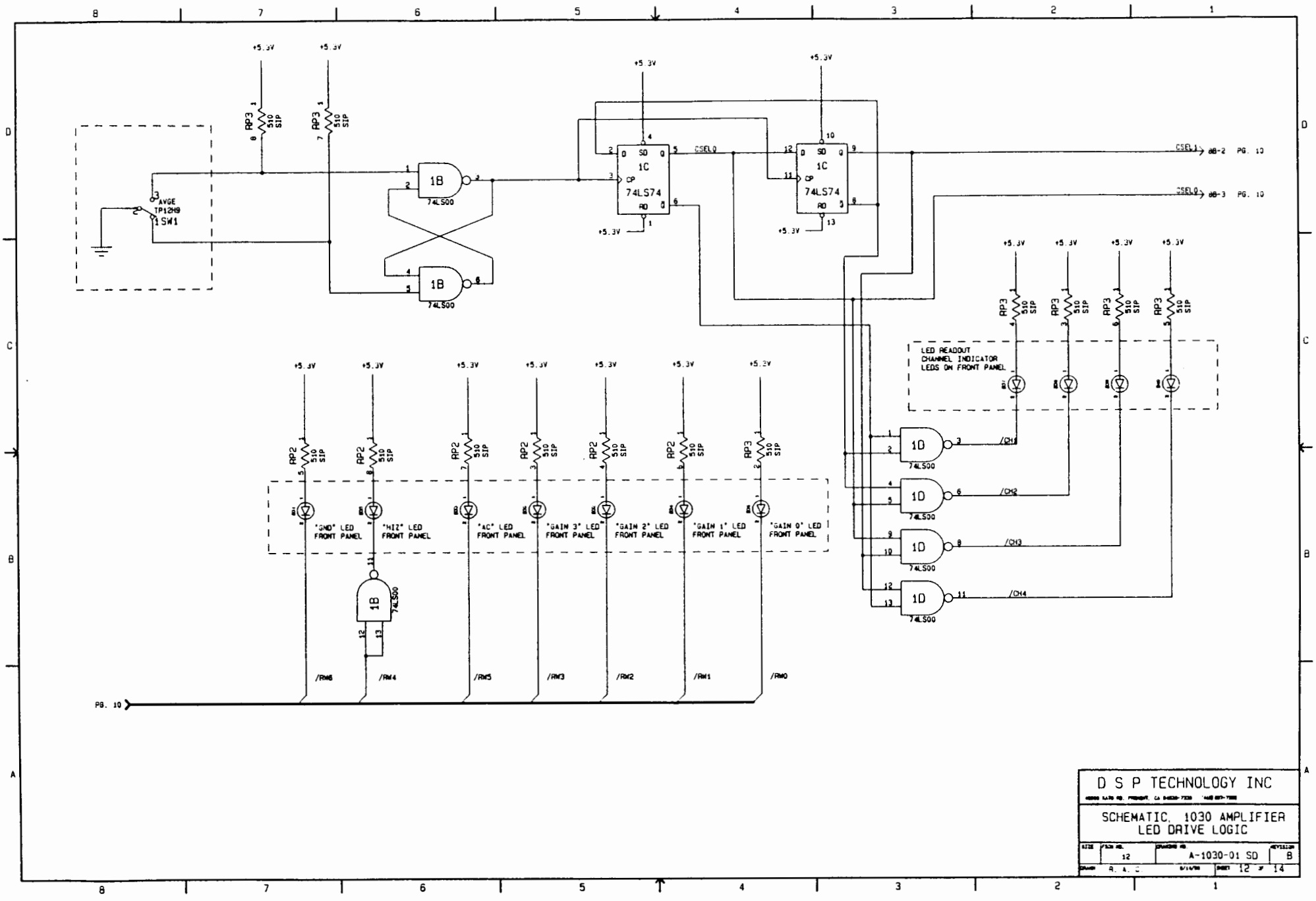
A-1030-01 SD B

R. A. L. 8/14/96 SHEET 8 OF 14


5D
PG. 11 5B-5
CH4BX1
ULN2803
+5.3VD
FB39
+5RLYD1
K29
C139
.1uf
R163
390
R164
62
PG. 4 10F-11
CH4AOUT
C181
56pf. CHIP
R162
300.0
.1%
5D
PG. 11 5B-8
CH4X0.5
ULN2803
R129
300.0
.1%
R126
24
R128
20K
C147
.1uf
K30
R127
100
.1%
+5RLYD1
PG. 13 R8
-1VREF
R125
2.00K
.1%
PG. 13 R8
AMP40FST
R124
1.00K
.1%
R130
100
C155
3.5-18
pf
0.1 uf
C142
0.1 uf
C143
R122
24
R123
49.9
1%
R119
20
C141
15pf
5D
PG. 11 5B-9
CH4X20
ULN2803
K28
+5RLYD1
R118
50
R120
49.9
1%
+5.3V
FB37
+5.3VD
FB38
C135
3.3 uf
C136
0.1 uf
C137
.01uf. CHIP
C138
0.1 uf
+BIAS
10E
AD9611
-BIAS
R117
49.9
1%
CHANNEL 4 OUTPUT
FRONT PANEL
J8
LEMO
C144
.01uf. CHIP
C146
0.1 uf
C145
0.1 uf
R152
15K
R151
100K
FB41
FB40
+5.3V
-15V
-5.2VD
-5.2VD
PG. 6
D S P TECHNOLOGY INC
SCHEMATIC, 1030 AMPLIFIER
CH 4 OUTPUT STAGE
9
A-1030-01 SO
8
R. A. C.
9 OF 14


D S P TECHNOLOGY INC
SCHEMATIC, 1030 AMPLIFIER
CAMAC DECODING
A-1030-01 SD
B
10
R. A. C.
10 OF 14
74LS645
74LS139
74LS221
82S23
PAL16L8
'N' LED
FRONT PANEL
/READID
+5.3V

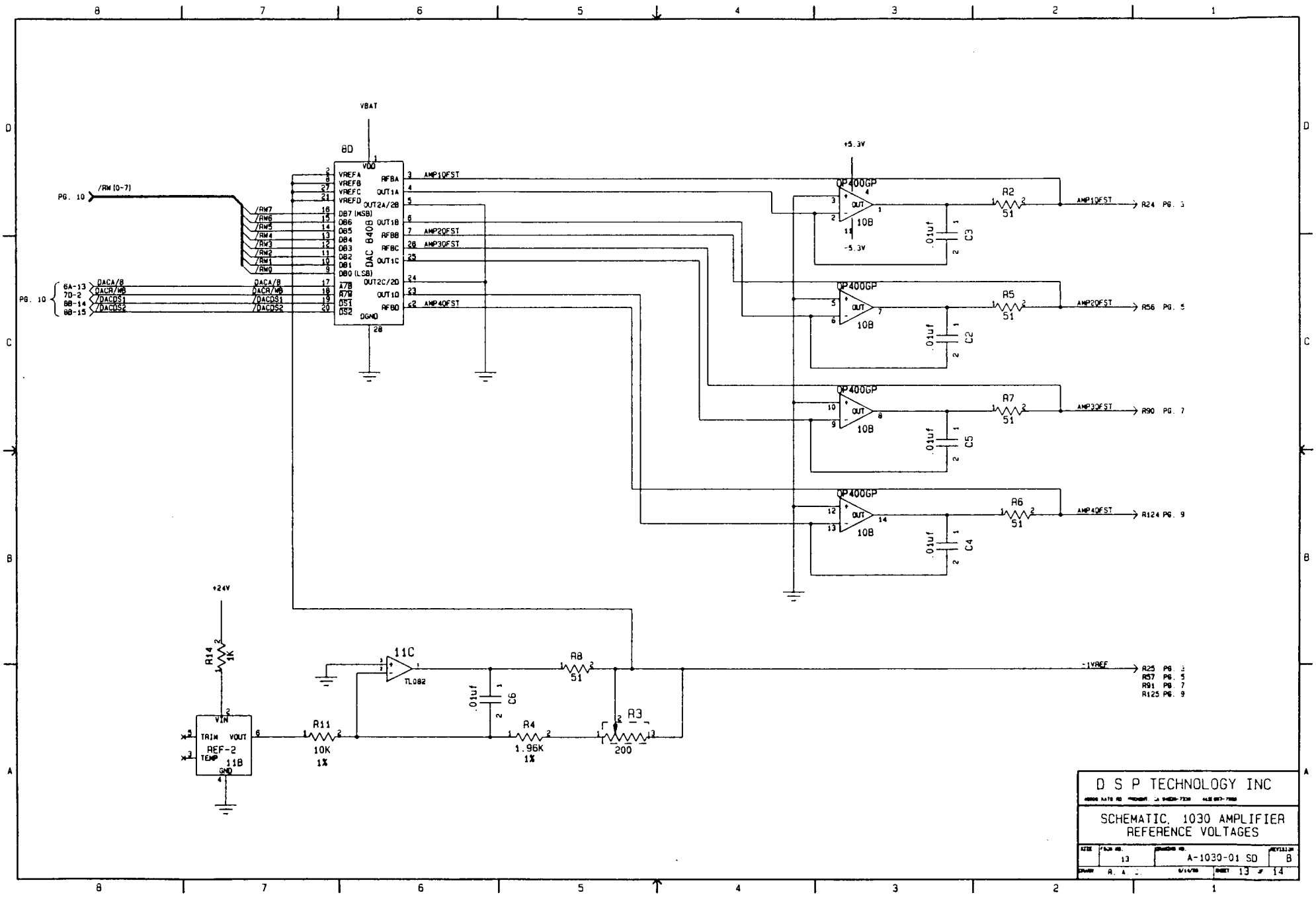

D S P TECHNOLOGY INC
SCHEMATIC, 1030 AMPLIFIER CONTROL REGISTERS
A-1030-01 SD
B
11
R. A. C.
11 OF 14
74HCT652
74HCT373
185030
7407
/PORST
/RW(0-7)
VBAT
+5.3V
/GND1
/GND2
/GND3
/GND4
/AC1
/AC2
/AC3
/AC4
/CH1D4
/CH2D4
/CH3D4
/CH4D4
/CH1TERM
/CH2TERM
/CH3TERM
/CH4TERM
/CH1X 21
/CH1X0 1
/CH1AX1
/CH1BX1
/CH1X0 5
/CH1X20
/CH2X 21
/CH2X0 1
/CH2AX1
/CH2BX1
/CH2X0 5
/CH2X20
/CH3X 21
/CH3X0 1
/CH3AX1
/CH3BX1
/CH3X0 5
/CH3X20
/CH4X 21
/CH4X0 1
/CH4AX1
/CH4BX1
/CH4X0 5
/CH4X20
/CH1D3
/CH1D2
/CH1D1
/CH1D0
/CH2D3
/CH2D2
/CH2D1
/CH2D0
/CH3D3
/CH3D2
/CH3D1
/CH3D0
/CH4D3
/CH4D2
/CH4D1
/CH4D0
/AMPRD1
/AMPRD2
/AMPRD3
/AMPRD4
/AMPWR1
/AMPWR2
/AMPWR3
/AMPWR4
DACR/W
DACR/WB
2A
2B
3A
3B
4A
4B
5A
5B
6D
7B
7D
PG. 1
PG. 2
PG. 4
PG. 5
PG. 6
PG. 7
PG. 9
PG. 10
PG. 13



D S P TECHNOLOGY INC

SCHEMATIC, 1030 AMPLIFIER
LED DRIVE LOGIC

SIZE	PLAN NO.	DRAWING NO.	REVISION
	12	A-1030-01 SD	B
DRAWN R. A. C.	8/14/98	SHEET 12 OF 14	



D S P TECHNOLOGY INC

SCHEMATIC, 1030 AMPLIFIER
REFERENCE VOLTAGES

SIZE	FILE NO.	DRAWING NO.	REVISION
	13	A-1030-01 SD	B
DRAWN A. A.		SHEET 13 OF 14	

POWER TABLE							
DEVICE	REF. DESIGNATION	VBAT	+15V	-15V	+5.3V	-5.2V	DIGITAL GROUND
74HCT652	2A-5A	24					12
18S030	2B-5B				16		8
74HCT373	7B, 7D	20					10
74LS74	1C				14		7
74LS00	1B, 1D				14		7
7407	6D				14		7
74LS645	7A				20		10
16L8	6A, 8B				20		10
74LS641	8A				20		10
74LS139	6B				16		8
74LS221	1A				16		8
8408	8D	1					28
82S23	9A, 10A				16		8

D S P TECHNOLOGY INC

SCHEMATIC, 1030 AMPLIFIER POWER SUPPLY

SIZE	TECH NO.	DRAWING NO.	REVISION
B	14	A-1030-01 SD	B
SCALE NONE		SHEET 14 OF 14	

Assembly: 1030-B (ASSY: 4CHNL 100MHZ PRG AMP TRACH)

Revision: B

As of: 02/10/90

	Component	Description	Qty Per	As of	Until	Reference
1.	0100-0101	RES: RC07 100 OHM 5% 1/4W	4.00	06/01/89	12/31/99	R30,R62,R96,R130
2.	0100-0102	RES: RC07 1K OHM 5% 1/4W	1.00	07/28/88	12/31/99	R14
3.	0100-0131	RES 5% 1/4W CC RESISTOR R=130	4.00	10/16/89	12/31/99	R40,R72,R106,R140
4.	0100-0151	RES 5% 1/4W CC RESISTOR R=150	4.00	07/01/89	12/31/99	R42,R74,R108,R142
5.	0100-0153	RES 5% 1/4 W CF RESISTOR R=15K	4.00	06/01/89	12/31/99	R82,R116,R150,R182
6.	0100-0203	RES 5% 1/4W CC RESISTOR R=20K	8.00	07/28/88	12/31/99	R1,R38,R60,R94,R128
7.	0100-0240	RES 5% 1/4W CC RESISTOR R=24	20.00	06/01/89	12/31/99	R26,R58,R92,R126,R45,R47,R111,R145,R165-R172,R22,R54,R88,R122
8.	0100-0330	RES: 5% 1/4W CC R=33	4.00	10/16/89	12/31/99	R34,R66,R100,R134
9.	0100-0331	RES 5% 1/4W CC RESISTOR R=330	4.00	01/01/90	12/31/99	R154,R157,R162,R163
10.	0100-0510	RES 5% 1/4W CC RESISTOR R=51	8.00	07/28/88	12/31/99	R46,R76,R112,R146,R2,R5-R8
11.	0100-0620	RES 5% 1/4W R=62 OHM	12.00	07/01/89	12/31/99	R33,R41,R65,R73,R99,R107,R133,R141,R155,R158,R161,R164
12.	0150-0499	RMF RN55D 1% MF RES R=49.9	12.00	07/28/88	12/31/99	R23,R55,R89,R123,R17,R49,R83,R117,R20,R52,R86,R120
13.	0150-1002	RES 1% 1/4W MF RESISTOR R=10.0K	5.00	07/28/88	12/31/99	R44,R76,R110,R144,R11
14.	0150-1623	RMF RN55D 1% R=162K	4.00	07/01/89	12/31/99	R36,R68,R102,R136
15.	0150-1630	RES 1% RES 1.63 OHM	2.00	07/28/88	12/31/99	R10,R15
16.	0150-1961	RMF RN55D 1% MF RES R=1.96K	3.00	07/28/88	12/31/99	R4,R16,R18
17.	0150-2151	RES 1% 1/4W MF RESISTOR R=2.15K	4.00	06/01/89	12/31/99	R37,R69,R103,R137
18.	0150-2499	RMF RN55D24R9F 24.9 OHM 1%	4.00	07/28/88	12/31/99	R31,R63,R97,R131
19.	0150??	CAP:.022MF 400VDC,PLESSE/60C223J400	4.00	07/28/88	12/31/99	C54,C93,C133,C172
20.	0152-1000	RMF: RN55C 0.1% R=100	4.00	07/01/89	12/31/99	R27,R59,R93,R127
21.	0152-1001	RES: RN55C 0.1% R=1.00K	4.00	07/28/88	12/31/99	R24,R56,R90,R124
22.	0152-1824	RMF: RN55C 0.1% R=1.82M	8.00	06/01/89	12/31/99	R39,R43,R71,R75,R105,R109,R113,R143
23.	0152-2001	RMF RN55C 0.1% MF RES R=2.00K	4.00	07/28/88	12/31/99	R25,R57,R91,R125
24.	0152-2002	RMF RN55C 0.1% MF RESISTOR R=20.0K	4.00	06/01/89	12/31/99	R35,R67,R101,R135
25.	0152-2003	RES: RN55C 0.1% R=200K	4.00	06/01/89	12/31/99	R38,R70,R104,R138
26.	0152-3000	RMF: RN55C 0.1% R=300	8.00	06/01/89	12/31/99	R29,R61,R129,R95,R153,R156,R159,R162
27.	0152-3000	RES 1% 1/2W MF RESISTOR R=100	8.00	06/01/89	12/31/99	R42,R43,R73,R80,R111,R114,R147,R149
28.	0200-0511	RPK RES PK BNS +308R-101-511	3.00	06/01/89	12/31/99	RP2,RP3
29.	0350-0100	RES:VAR,15T,10 OHM,BURNSRJ26FW100	4.00	10/16/89	12/31/99	R32,R64,R98,R132
30.	0350-0104	RES VAR. 12T 1/4" TOP ADJ BOURNS 3	4.00	07/01/89	12/31/99	R81,R115,R149,R151
31.	0350-0200	RES: VAR,12T,R=20,BOURNS RJ26FW200	4.00	06/01/89	12/31/99	R19,R51,R85,R119
32.	0350-0201	POT 1/4" RT R=200 BOURNS RJ26FW2	1.00	07/28/88	12/31/99	R3
33.	0350-0500	POT 1/4" 15T TOP ADJ R=50 BOURNS RJ	4.00	01/01/90	12/31/99	R13,R50,R84,R115
34.	0500-0153	CSM C=15PF 5% RADIO CD6C150J03	4.00	07/01/89	12/31/99	C51,C62,C101,C141
35.	0500-0470	CSM C=47PF 5% RADIO CM05-470J03	8.00	07/01/89	12/31/99	C47,C48,C83,C87,C111,C115,C165,C166
36.	0510-0103	CAP CER CHIP .01UF	24.00	07/01/89	12/31/99	SOLDER SIDE
37.	0510-0150	CAP CER, CHIP, 15PF	4.00	07/01/89	12/31/99	C50,C130,C170,C183 (SOLDER SIDE)
38.	0510-0159	CAP CER CHIP 0805 1.5PF	4.00	07/01/89	12/31/99	C46,C86,C125,C165 (SOLDER SIDE)
39.	0510-0560	CAP CER CHIP 0805 56PF	4.00	08/08/89	12/31/99	C175,C177,C179,C181 SOLDER SIDE
40.	0520-0103	CMC C=0.01UF MONO CENTRALAB CZ20A1	5.00	07/28/88	12/31/99	C3-C6
41.	0520-0272	CAP C=2700PF CER COG 100V LS=.2	4.00	01/01/90	12/31/99	C52,C91,C131,C171
42.	0521-0104	CMC C=0.1UF MONO CENTRALAB CZ20A104	90.00	06/01/89	12/31/99	C16,18,19,22,24,33,34,37,40,44,48,53,55,57,59,26,27,60,63,64 C66-C68,70,71,77,80,84,88,92,94,96,98,176,178,180,182,102, C103,C105-C107,110,116,119,123,127,132,134,136,28,109,138, C139,142,143,C145-147,149,150,156,159,163,167,173,174,39

Component	Description	Qty Per	As of	Until	Reference

Assembly: 1030-B (ASSY: 4CHNL 100MHZ PRG AMP TRACH)

Assembly: 1030-B (ASSY: 4CHNL 100MHZ PRG AMP TRAQH) Date: 3/13/90
Revision: B Page: 2
As of: 02/10/90

	Component	Description	Qty Per	As of	Until	Reference
43.	0600-0335	CTE C=3.3UF TANT KEMET T362B335K03	17.00	07/28/88	12/31/99	C13,C15,C32,C41,C42,C56,C69,C81,C82,C95,C108,C120,C121,C135, C148,C160,C161
44.	0600-0685	CTE C=6.8UF TANT 35WVDC KEMET T361B	8.00	07/28/88	12/31/99	C1,C7-C12,C14
45.	0750-9373	CCV CAP CER VAR SCHAFFNER 9373	12.00	07/28/88	12/31/99	C31,C49,C76,C85,C89,C45,C51,C90,C1.5,C124,C128,C129,C155, C164,C168,C169
46.	0870-0003	FBD FERROXCUBE WIRED BEAD 11+13-4B	40.00	07/01/89	12/31/99	FB1-FB7,FB10-FB19,FB22-FB31,FB34-FB43,FB46-FB48
47.	1000-4448	DGS DIODE SIL. SWITCH IN4448	5.00	07/28/88	12/31/99	D1,D6,D8,D10,D12
48.	1005-0010	DLL DUAL LO LKG DIODE SIL DPAD10	4.00	07/28/88	12/31/99	D5,D7,D9,D11
49.	1010-2811	DSS DIODE H.P.5000-2811	1.00	07/28/88	12/31/99	D2
50.	1030-5824	DSR: DIODE REC 3A 3E MR824/STMDE	2.00	07/28/88	12/31/99	D3,D4
51.	1040-0002	DLE LED RED HP HLMP-1301	12.00	07/28/88	12/31/99	D38,D39-D40
52.	122045	HDW: 4-40 KEP NUT ZINC	8.00	07/01/89	12/31/99	
53.	123046	HDW: WASHER #4 FLAT NYLON	2.00	07/01/89	12/31/99	
54.	1705-2803	IC INTFC ULN2803A OCTAL RLY DRV	4.00	06/01/89	12/31/99	2D-5D
55.	1750-0007	ICS SN7407	1.00	07/28/88	12/31/99	6D
56.	1750-0030	ICS SN74LS30	2.00	07/28/88	12/31/99	7E,7F
57.	1760-0074	ICS SN74LS74	1.00	07/28/88	12/31/99	1C
58.	1760-0139	ICS SN74LS139	1.00	07/28/88	12/31/99	6B
59.	1760-0221	ICS SN74LS221	1.00	07/28/88	12/31/99	1A
60.	1760-0641	ICS SN74LS641	1.00	07/28/88	12/31/99	8A
61.	1760-0645	ICS SN74LS645	1.00	07/28/88	12/31/99	7A
62.	1780-0373	IC: 74HCT373	2.00	07/28/88	12/31/99	7B,7D
63.	1780-0652	IC: 74HCT652	4.00	10/16/89	12/31/99	2A-5A
64.	1851-0097	PROM: M/F 1850-0003 1030 ID HIGH	1.00	07/01/89	12/31/99	9A
65.	1851-0098	PROM: M/F 1850-0003 1030 ID LOW	1.00	07/01/89	12/31/99	10A
66.	1851-0099	PROM: M/F 1850-0001 1030 CONTROL	4.00	07/01/89	12/31/99	2B-5B
67.	1857-0140	PAL: M/F 1856-0106 1030 CAMAC1	1.00	07/01/89	12/31/99	8B
68.	1857-0141	PAL: M/F 1856-0106 1030 CAMAC2	1.00	07/01/89	12/31/99	8A
69.	2000-0082	ICS DUAL OP AMP FET TI TL082CP	1.00	07/28/88	12/31/99	11C
70.	2000-0400	IC: OP AMP QUAD LOW VOS OP400	1.00	07/01/89	12/31/99	10B
71.	2000-2004	IC: FET, 350MHZ, ELANTEC EL2004CG	4.00	07/28/88	12/31/99	1F,3F,7F,10F
72.	2000-9611	IC:OP AMP, I FB WB,AD9611BH	4.00	07/28/88	12/31/99	1E,3E,7E,10E
73.	2020-0002	ICA VOLTAGE REF PMI REF02HP	1.00	07/28/88	12/31/99	11B
74.	2020-0690	IC: V MON, 5V, E30CPA	1.00	07/28/88	12/31/99	11A
75.	2030-0317	ICS IC VOL REG NAT LM317T	1.00	07/28/88	12/31/99	VR1
76.	2030-0337	IC: VOLT REG, NEG ADJ, LM337T	1.00	07/28/88	12/31/99	VR2
77.	2060-8408	DAC: QUAD 8BIT PMI # DAC8408GP	1.00	07/28/88	12/31/99	8D
78.	3000-0005	RLY AROMAT TQ2EDC-5V RELAY DIP	32.00	07/28/88	12/31/99	K1-K7,K9-K16,K18-K25,K27-K34,K36
79.	3001-0001	RLY: ALEPH DH1A05BW GORDO 4705	4.00	07/28/88	12/31/99	K8,K17,K26,K35
80.	3100-0302	FUSE 3AMP LITTLEFUSE 251003	4.00	07/28/88	12/31/99	F1-F4
81.	5000-0016	SKT CAMBION 703-1316-01-04-10	6.00	07/28/88	12/31/99	9A,12A,2B-5B
82.	5000-0020	SKT CAMBION 703-1320-01-04-10	3.00	07/28/88	12/31/99	6A,8A,8B
83.	5001-0028	SKT CAMBION 703-1328-01-04-10	1.00	07/28/88	12/31/99	8D
84.	5250-3703	JCK FUS CAMBION 450-3703-01-06-00	8.00	07/28/88	12/31/99	F1-F4
85.	5510-0004	CON RT ANGLE LEMO RPL00.250TEF	8.00	07/28/88	12/31/99	J1-J8
86.	8035-0003	SW: PCB MTG, SPDT, C&K TP12H3AVGE	1.00	07/28/88	12/31/99	SW1

DSP Technology Inc.

SINGLE LEVEL BILL OF MATERIAL REPORT

Assembly: 1030-B (ASSY: 4CHNL 100MHZ PRG AMP TRAQH)

Revision: B

As of: 02/10/90

	Component	Description	Qty Per	As of	Until	Reference
87.	6850-0001	RAIL: GUIDE, MDL, 5 HOLE, C-BORE	2.00	07/28/88	12/31/99	
88.	6851-0079	PNL: FR, 1030	1.00	07/28/88	12/31/99	FRONT PANEL
89.	6852-0002	PNL: CAMAC SIDE STD	2.00	07/01/89	12/31/99	
90.	6852-0004	PNL: RR, 1/2E S	1.00	07/28/88	12/31/99	
91.	7000-0076	PCB DWG # 1030-01-PD	1.00	07/22/88	12/31/99	PCB
92.	7303-0500	FLS SCREW 4-40 X 1/2 PAN HD PHLSH	8.00	07/01/89	12/31/99	
93.	7410-0003	HWD: SWAGE TYPE STANDOFF	5.00	07/28/88	12/31/99	
94.	8200-0001	BAT BATTERY DURACELL DL 1/3N W TABS	1.00	07/28/88	12/31/99	BT1

Component | Description | Qty Per | As of | Until | Reference

Assembly: 1030-B (ASSY: 4CHNL 100MHZ PRG AMP TRAQH)

REVISION HISTORY

Date	By	Description
8/15/89	jh	Major corrections

dsp technology inc.

PRODUCT WARRANTY

(Excludes Software)

DSP TECHNOLOGY ("DSP") warrants its products to be free from defects in material and workmanship and to meet DSP's performance specifications. The warranty period is one year from the date of shipment to the buyer. The warranty is limited by the paragraphs below.

RETURN TO FACTORY

If a buyer discovers a defect in a DSP product covered by this agreement, buyer's exclusive remedy is to ship the product back to DSP's Fremont factory, where DSP will, at its option, either repair or replace the product. This remedy applies if DSP receives the returned product on or before the tenth day after the expiration of the warranty period and the buyer notifies DSP of the defect before returning the product.

COST TO BUYER OF REPAIRS OR REPLACEMENT

Buyer must prepay freight charges to DSP. DSP will pay standard return freight to buyer. Buyer will be charged for premium freight if that method of transport is requested by buyer. There is no other charge for repair or replacement during the warranty period.

TRANSFERRABLE WARRANTIES

In addition to the foregoing warranty, DSP also provides the buyer the transferrable warranty, if any, provided to DSP by the manufacturers of other products such as terminals and disk systems supplied by SEC as part of a total system.

LIMITATION OF WARRANTY AND LIABILITY

The foregoing constitutes DSP's entire warranty, expressed, implied, and/or statutory (except as to title), and to any other party for any breach of such warranty and for damages, whether direct, special, incidental, or consequential. Other than as expressly provided in this document, no warranties expressed or implied, including any warranty of merchantability or fitness for a particular purpose are made. No employee, representative, or agent or seller has any authority expressed or implied to alter or supplement the terms of this warranty.

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