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DSP2904

SPINCODER
TIMER & COUNTER MODULE

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MODEL 2904

SPINCODER

FEATURES:

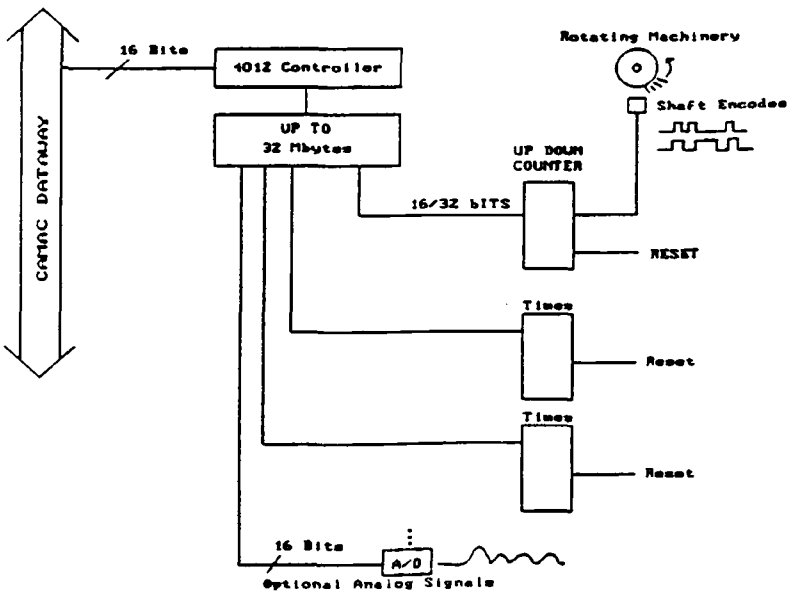
- Quadrature Input for Optical Encoders
- Built-in Timer
- 32 Bit Timer and Counter Resolution
- TRAQ P Compatible

DESCRIPTION

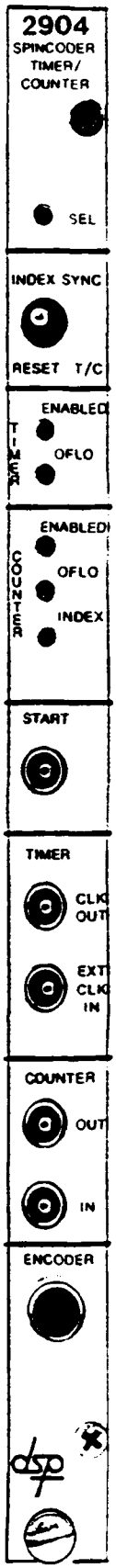
The 2904 is a general purpose timer and counter that has the ability to store digital data from a shaft encoder. The 2904 can be used to log rotation or position and correlate that data to analog events and time. The module is compatible with TRAQ P Real Time Signal Processing System. This allows analog measurements to be taken synchnonously to rotation and time measurements.

APPLICATION

The 2904 is used for measuring rotation as a function of time such as for centrifuge and engine analysis. The 2904 can also be used for general timing measurement and to enhance real time processing applications.



2904 Block Diagram



ACTUAL SIZE

INTRODUCTION

The DSP2904 combines a digital TIMER and COUNTER in a single module. It may be used as a stand-alone module or within a TRAQ data acquisition subsystem.

Features:

* Timer and Counter Module for TRAQ Multi-channel Waveform Recorder
* 32 Bit, 10 MHz Timer and Counter Resolution
* Time Automatically stored on each Sample Clock
* Quadrature input to Counter for connection to shaft encoders
* Up/Down Counter
* Counter Clock Out available for Crank Angle Sampling clock

Both the TIMER and COUNTER channels are independently programmable and readable. Each may be configured for either 16 or 32 bits maximum range (64K or 2**32). Actual range can be programmed, allowing for modulo 360, 720 or other user specified ranges.

Flexible modes of gating and data storage permit rate of change, elapsed time, or interval measurements.

USER NOTE

FACTORY SUPPLIED SETTINGS

1. TRAQ Users : The DSP2904 is supplied from the factory with the following TRAQ Channel assignments:

Timer Low word	TRAQ Channel #9
Counter Low word	TRAQ Channel #10
Timer High word	TRAQ Channel #127 (not used)
Counter High word	TRAQ Channel #127 (not used)

2. Use with ENCODERS : The DSP2904 Index (Reset) input is supplied from the factory set for EDGE detect INDEX mode. This causes the 2904 counter to reset on the first counter clock following the rising edge of the INDEX input. In this mode there is NOT a requirement that the INDEX input pulse overlap a single clock cycle.

Users requiring a LEVEL detect INDEX mode may select this mode by moving the E4 - E5 jumper to E5 - E6.

DSP2904 VERSION COMPATIBILITY

Users of DSP2904s with serial numbers 101 through 140 should refer to Appendix B for information specific to those units. Internal switch settings and modes of operation are selected differently.

CONTROLS AND INDICATORS

This section describes the DSP2904 controls and indicators that are directly accessable to the user.

FRONT PANEL

The DSP2904 Front Panel is divided into 3 major sections

Start / Stop Control

Timer Control and Status

Counter Control and Status

SEL

Indicates module is selected for data readout into a TRAQ subsystem.

Type : LED - Green

INDEX SYNC

Sets Counter channel's Index Divider. Refer to INSTALLATION section for description of the Index Divider.

Type : Switch - Momentary action

RESET T/C

Reset Timer and Counter channels. Loads Timer and Counter channels with contents of PRESET registers. Starts (Enables) both channels.

Type : Switch - Momentary action

TIMER ENABLED

Indicates Timer channel is Enabled (started).

Type : LED - Green

TIMER OFLO

Indicates that the Timer channel has overflowed (maximum time reached).

Type : LED - Red

COUNTER ENABLED

Indicates Counter channel is Enabled (started).

Type : LED - Green

COUNTER OFLO

Indicates that the Counter channel has overflowed (maximum count reached).

Type : LED - Red

START

Accepts an external control pulse to Start (Enable) Timer and Counter channels.

Type: LEMO. TTL rising edge sensitive. Minimum pulse width 50 nSec. 1 KOhm, protected input impedance.

TIMER CLK OUT

Timer timebase output. Corresponds to timebase used to increment timer. Active only when Timer is enabled.

Type: LEMO. TTL pulse train. Rising edge corresponds to timer increment (+/-50 nSec). Drives 50 Ohm load.

TIMER CLK IN

Accepts an external pulse train for TIMER timebase when an External rate code has been selected.

Type: LEMO. TTL pulse. Rising edge increments TIMER channel when enabled and external timebase selected. Input is 1KOhm and is protected. Minimum pulse width 35 nSec. Maximum pulse rate 10 MHz.

COUNTER CLK OUT

Counter clock output. Corresponds to clock used to increment or decrement the COUNTER channel. Active only when COUNTER is enabled.

Type: LEMO. TTL pulse train. Rising edge corresponds to COUNTER increment or decrement (+/-50 nSec). Drives 50 Ohm load.

COUNTER CLK IN

Accepts an external pulse train for COUNTER increment.

Type: LEMO. TTL pulse. Rising edge increments COUNTER channel when enabled. Input is 1KOhm and is protected. Minimum pulse width 35 nSec. Maximum pulse rate 10 MHz.

NOTE: This input is connected directly to the ENCODER ACIk input. If the ENCODER input is being used do NOT apply a signal to the COUNTER CLK IN connector. Doing so may result in damage to the attached encoder.

ENCODER

Accepts output from a quadrature type encoder for control of the COUNTER channel.

Type: LEMO 4PIN.

1: +5 Volt out. Used for powering encoder. Protected at 500mA maximum.

2: INDEX (Z). Index pulse from encoder. Used to reset COUNTER channel.

3: BCLK. Phase B quadrature clock from encoder

4: ACLK. Phase A quadrature clock from encoder

SIDE PANEL CONTROLS

TRAQ ID SELECT

Each channel (TIMER and COUNTER) in the DSP2904 may be assigned an individual TRAQ ID. Both the TIMER and COUNTER may be configured as 16 or 32 bits long. The 32 bit configuration requires 2 TRAQ channels. Therefore there are two (2) TRAQ ID switches for each of the DSP2904 channels - corresponding to the HIGH (bits 17..32) and the LOW (bits 1..16) bits. Refer to the TRAQ User Manual for further details on TRAQ channel IDs.

SW1 : COUNTER LOW TRAQ ID

Assigns COUNTER bits 1..16 to a TRAQ channel assignment.

Type: 8 DIP Switches. Accessed from top of module. Refer to ID switch setting table.

SW3 : COUNTER HIGH TRAQ ID

Assigns COUNTER bits 17..32 to a TRAQ channel assignment.

Type: 8 DIP Switches. Accessed from top of module. Refer to ID switch setting table.

SW2 : TIMER HIGH TRAQ ID

Assigns TIMER bits 17..32 to a TRAQ channel assignment.

Type: 8 DIP Switches. Accessed from top of module. Refer to ID switch setting table.

SW4 : TIMER LOW TRAQ ID

Assigns TIMER bits 1..16 to a TRAQ channel assignment.

Type: 8 DIP Switches. Accessed from top of module. Refer to ID switch setting table.

DSP2904 CONTROLS AND INDICATORS

TRAQ ID SELECT

TRAQ Channel assignment is determined by 4 separate 8 position switches.

> NOTE: Early versions of the DSP2904 (serial numbers 101 through 140) have nonstandard switch setting. Refer to Appendix B.

Positions 1 through 7 of each switch is the binary encoded TRAQ ID number of the desired channel. The TRAQ ID number is always 1 less than the TRAQ CHANNEL.
Therefore:

> POS1 (MSB) ...POS7 (LSB) = TRAQ CHANNEL - 1

Note Position 8 is NOT used and should be left Open/Off.

The following table lists the correct settings.
0 corresponds to the OFF or OPEN position
1 corresponds to the ON or CLOSED position

TRAQ CHAN	SWITCH POSITION 1 2 3 4 5 6 7	TRAQ CHAN	SWITCH POSITION 1 2 3 4 5 6 7
1	0 0 0 0 0 0 0	33	0 1 0 0 0 0 0
2	0 0 0 0 0 0 1	34	0 1 0 0 0 0 1
3	0 0 0 0 0 1 0	35	0 1 0 0 0 1 0
4	0 0 0 0 0 1 1	36	0 1 0 0 0 1 1
5	0 0 0 0 1 0 0	37	0 1 0 0 1 0 0
6	0 0 0 0 1 0 1	38	0 1 0 0 1 0 1
7	0 0 0 0 1 1 0	39	0 1 0 0 1 1 0
8	0 0 0 0 1 1 1	40	0 1 0 0 1 1 1
9	0 0 0 1 0 0 0	41	0 1 0 1 0 0 0
10	0 0 0 1 0 0 1	42	0 1 0 1 0 0 1
11	0 0 0 1 0 1 0	43	0 1 0 1 0 1 0
12	0 0 0 1 0 1 1	44	0 1 0 1 0 1 1
13	0 0 0 1 1 0 0	45	0 1 0 1 1 0 0
14	0 0 0 1 1 0 1	46	0 1 0 1 1 0 1
15	0 0 0 1 1 1 0	47	0 1 0 1 1 1 0
16	0 0 0 1 1 1 1	48	0 1 0 1 1 1 1
17	0 0 1 0 0 0 0	49	0 1 1 0 0 0 0
18	0 0 1 0 0 0 1	50	0 1 1 0 0 0 1
19	0 0 1 0 0 1 0	51	0 1 1 0 0 1 0
20	0 0 1 0 0 1 1	52	0 1 1 0 0 1 1
21	0 0 1 0 1 0 0	53	0 1 1 0 1 0 0
22	0 0 1 0 1 0 1	54	0 1 1 0 1 0 1
23	0 0 1 0 1 1 0	55	0 1 1 0 1 1 0
24	0 0 1 0 1 1 1	56	0 1 1 0 1 1 1
25	0 0 1 1 0 0 0	57	0 1 1 1 0 0 0
26	0 0 1 1 0 0 1	58	0 1 1 1 0 0 1
27	0 0 1 1 0 1 0	59	0 1 1 1 0 1 0
28	0 0 1 1 0 1 1	60	0 1 1 1 0 1 1
29	0 0 1 1 1 0 0	61	0 1 1 1 1 0 0
30	0 0 1 1 1 0 1	62	0 1 1 1 1 0 1
31	0 0 1 1 1 1 0	63	0 1 1 1 1 1 0
32	0 0 1 1 1 1 1	64	0 1 1 1 1 1 1

INSTALLATION

TRAQ SYSTEMS

This section describes DSP2904 installation in a TRAQ subsystem. Detailed TRAQ configuration information may be found in the TRAQ User's Manual.

PHYSICAL INSTALLATION

CAUTION

> Always turn-off the CAMAC Crate power before installing or removing modules. Failure to do so may cause permanent damage to modules in the system.

Install the DSP2904 in an available (open) CAMAC station adjacent to the TRAQ Controller and ADCs.

Connect the unit to the TRAQ ADCBus located at the rear of the module. Note that in systems with other TRAQ data acquisition modules the TRAQ ADCBus connects to each module and then to the TRAQ Controller. Check that these connections have not been removed.

INITIAL SETUP AND MODULE ID

Power-up the system and initialize the TRAQ Controller (setting desired number of channels, memory size etc).

In order for the TRAQ Controller to access the DSP2904, the latter's address or channel ID must be assigned correctly. A single DSP2904 may occupy either 1,2,3 or 4 TRAQ channels - based on using either 16 or 32 bit word sizes for either the TIMER or COUNTER sections. Refer to the CONTROLS and INDICATORS section for a description of the module ID switches. In general it is most straight forward to assign ADC channels first and then set the DSP2904 channel IDs.

Example:

> 16 Bit TIMER and 16 Bit COUNTER with 8 Channel 2812
>
> Assign DSP2812 Channels to 1..8 within TRAQ. This requires that the DSP2812 Module ID = 0.

Assign the DSP2904 TIMER to channel #9. Since only 16 bits are being used the section to assign is TIMER LOW (bits 1..16). According to the CONTROLs and INDICATOR section the appropriate ID switch is SW4. For TRAQ Channel #9 :

SW4-6 = OPEN	SW4-4 = CLOSED	SW4-2 = OPEN	SW4-1 = OPEN
SW4-3 = OPEN	SW4-5 = OPEN	SW4-7 = OPEN	SW4-8 = OPEN

Assign the DSP2904 COUNTER to channel #10. Again only bits are being used so the COUNTER LOW ID switch (SW1) is used. For TRAQ channel #10 :

SW1-6 = OPEN	SW1-4 = CLOSED	SW1-2 = OPEN	SW1-1 = OPEN
SW1-3 = OPEN	SW1-5 = OPEN	SW1-7 = CLOSED	SW1-8 = OPEN

TRAQ CONTROLLER SETUP

Set the TRAQ Controller NOC (Number of Channels) to include the DSP2904 channel assignments. Correct installation and setup can be verified by manually STARTing the TRAQ Controller. Confirm that all data acquisition modules' CVT and SEL indicators are ON.

If a module's SEL indicator is OFF, the probable cause is an incorrect ID assignment. Because a Module ID error will cause the system to "hang" or halt data transfers, an invalid ID in one module can inhibit ALL units from being SELECTED. Therfore, all modules should be checked for their corresponding IDs.

ENCODER INSTALLATION

The DSP2904 Counter channel is designed to be used with an incremental shaft encoder for angular measurements. Connection to the encoder is made be means of the four (4) position ENCODER connector on the DSP2904 front panel.

Quadrature Encoder Overview

An incremental shaft encoder provides three (3) signals from which angular position and direction of rotation can be determined. Angular position is determined by counting pulses generated as the encoder shaft turns (Channels A and B in Figure 1). A typical encoder may produce a pulse for every degree (angle) i.e. 360 per revolution. Encoders are available that provide over 5000 counts per revolution.

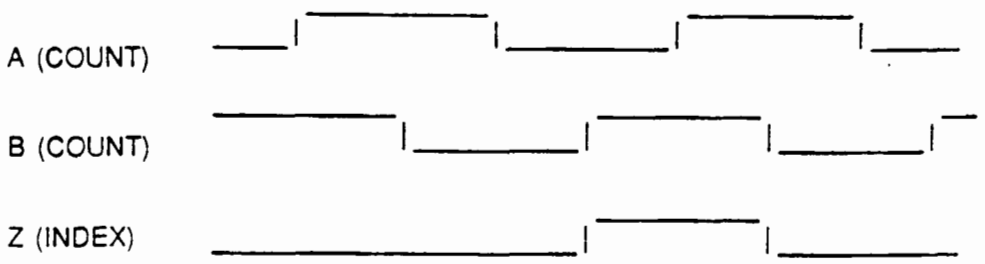


Figure 1 Quadrature Encoder Signals

Direction is sensed by measuring the phase difference between the two encoder count channels A and B (Figure 1). If Channel A leads channel B the shaft is turning in the opposite direction than when channel B leads.

Once every revolution an INDEX pulse is generated. This defines zero (0) degrees to the DSP2904 and allows angle measurements relative to a fixed shaft position.

DSP2904 - ENCODER CONNECTION

The DSP2904 ENCODER connector has the following pin assignments:

DSP PIN NUMBER	SIGNAL	SOURCE
4	Channel A (Up)	Encoder
3	Channel B (Down)	Encoder
2	Index	Encoder
1	+5 Volt	DSP2904

As viewed at the DSP2904 front panel, the connector numbering is:

4	3	
P	P	P : Pin (Male)
S	S	S : Socket (Female)
1	2	Connector case is ground.

The connector mates with Kings p/n 1095-1 (DSP p/n 5511-0003.

A maximum of 250 mA of +5 Volts is available at the DSP2904 ENCODER pin 1 for powering the shaft encoder. The power return is made using the shell of the connector. An internal fuse protects the DSP2904 from excessive current drawn at this connector.

The INDEX timing relative to Channel A is important for reliable reseting (zeroing) of the DSP2904 counter. As shown in Figure 1 the INDEX pulse must overlap the Channel A pulse. Specifically, the DSP2904 will reset if and only if the INDEX signal is HIGH (>2 volts) when the Channel A signal makes its transition from LOW (<0.5 volts) to HIGH (>2 volts).

Note that if the INDEX pulse overlaps multiple channel A encoder pulses, the DSP2904 is repeatedly reset to zero. It is important therefore that both the timing and duration of the Index signal from the encoder be consistent with these requirements. In general optical quadrature encoders are directly compatible with the DSP2904. Magnetic pick-off or other types of encoders may require signal conditioning prior to connection to the DSP2904.

Use with ENCODERS : The DSP2904 Index (Reset) input is supplied from the factory set for EDGE detect INDEX mode. This causes the 2904 counter to reset on the first counter clock following the rising edge of the INDEX input. In this mode there is NOT requirement that the INDEX input pulse overlap a single clock cycle.

Users requiring a LEVEL detect INDEX mode may select this mode by moving the E4 - E5 jumper to E5 - E6.

PROGRAMMING

The DSP2904 consists of two channels, Timer and Counter. Each must be programmed via CAMAC in order to configure their mode of operation. In general the Timer and Counter channels are very similar, having equivalent modes. The chief distinction is the source of the clock - in the case of the Timer, either an internal timebase or an external source may be selected. The Counter is clocked only by an external source. It will count up (increment) or down (decrement) by controlling the nature of the clock (refer to INSTALLATION section).

Either channel may be read out via CAMAC or by a DSP TRAQ family controller. In the latter case the DSP2904 appears to the TRAQ subsystem as multiple data acquisition channels. Because both the Timer and Counter may be configured as either 16 or 32 bit channels, the module can occupy upto 4 channels (16 bits each) on TRAQ. Refer to the INSTALLATION section for more information concerning use with TRAQ. Observe that CAMAC operations other than setup of a DSP2904 channel may conflict with simultaneous TRAQ operation.

MODE Register

In Timer and Counter is controlled by a mode register. This determines the number of bits (size) of the counter, enabling of the timer/counter source, and the action taken when the timer/counter overflows.

GATED

With this mode the Counter is gated (conditionally enabled) by the enable of the Timer. If the timer is programmed to halt after a preset time interval, the counter will also halt. This allows using the counter to measure the frequency (rate) of an external source.

Gating has a similar use with the timer. A gated timer is controlled by the enable of the Counter. When the Counter is programmed to halt after a preset count, the gated timer will contain elapsed time (period) of the counting interval.

In most cases the GATED mode is used in conjuction with WRAP = OFF of the channel determining the gate condition (f.i. Timer GATED and Counter WRAP=OFF) and a preset value for the gating channel. See also WRAP, Channel PRESET.

MOD32

Both the Timer and Counter have either 16 or 32 bit size. Selection of a 16 bit length allows for a maximum of 65535 clocks before the channel overflows. A 32 bit size allows upto (2**32) -1 clocks. The selection of a channel's bit size is independent of reading the channel. Hence, a 32 bit size can be selected but only the lower 16 bits read out in which case the data would appear to overflow at a count of 65535. See also MOD32, Channel PRESET.

WRAP

When the Timer or Counter overflows, the channel may be programmed to stop (WRAP = OFF) or reload with its preset value and resume counting (WRAP = ON). Overflow occurs when the channel reaches its maximum count. If configured for 16 bits, the maximum is at 65535, and for 32 bits at (2**32)-1 counts. WRAP = OFF is used in conjunction with the GATE mode for measuring time intervals or counter frequency.

The Counter channel will also underflow when decrementing (counting down) and it reaches a count of zero (0). WRAP mode affects the action on underflow in a similar manner to overflow. See also GATED, Channel PRESET, MOD32.

TIME OF COUNT

The Timer channel contents can be stored when the Counter channel overflows by setting the Timer in the Time of Count mode. Provided the the Counter channel is set in the WRAP mode, reading the Timer will yield an elapsed time between successive counter overflows. By preseting the Counter channel, the time can be used to calculate Count rate on a continuous basis. This contrasts to the GATED Timer mode which requires re-starting both channels following a single reading.

See also WRAP, Channel PRESET

TIMEBASE RATE

The Timer Channel includes a programmable timebase clock. As the Timer contents increment on each clock cycle, reading the channel's contents provides a measure of elapsed time. The resolution of this measure is determined by the timebase period - a fast clock will yield better timing resolution whereas a slower clock allows measuring a greater total elapsed time.

Timebase periods are programmed by means of a rate code. The resulting timebase is:

TimeBase Interval = 100 nSec * (2 ** Rate Code)

An external timebase clock can be used by selecting the External Rate Code. The maximum external rate is 10 MHz (100 nSec).

PERIOD	CODE	PERIOD	CODE	PERIOD	CODE	PERIOD	CODE
100 nS	0	25.6 uS	8	6.4- mS	16	1.6- Sec	24
200 nS	1	51.2 uS	9	12.8- mS	17	3.2- Sec	25
400 nS	2	102.4 uS	10	25.6- mS	18	6.4- Sec	26
800 nS	3	204.8 uS	11	51.2- mS	19	12.8- Sec	27
1.6 uS	4	409.6 uS	12	102.4- mS	20	25.6- Sec	28
3.2 uS	5	819.3 uS	13	204.8- mS	21	51.2- Sec	29
6.4 uS	6	1.6684 mS	14	409.6- mS	22	10.24- Sec	30
12.8 uS	7	3.2568 mS	15	819.2- mS	23	20.48- Sec	31

External 32

- = use formula for exact value

INDEX DIVIDER

The Counter channel can be re-loaded with the PRESET value by means of a signal at the INDEX input during a counter clock. If the INDEX signal occurs once for every "n" clock cycles, the Counter becomes a modulo-N counter. The INDEX DIVIDER mode inhibits alternate INDEX signals. This results in a modulo-2N counter. Typical applications are with shaft encoders where every 2 revolutions may indicate a full cycle.

PROGRAMMING

PRESET Registers

Each channel can be preset to a count prior to being enabled. This preset value is also used if the channel overflows and the WRAP mode is set. The preset value is loaded as two 16 bit words- High and Low. The High word is required only if the channel is being used in the 32 bit mode (see MOD32).

CHANNEL CONTROL

The DSP2904 Channels can be STARTED (Enabled), READ (contents accessed), and STOPPED (Disabled) by CAMAC control. These functions are also performed by a TRAQ controller if it is attached. Refer to CAMAC COMMAND Summary for detailed definitions.

CHANNEL READOUT

TRAQ

When the DSP2904 is used in a TRAQ subsystem, the TRAQ 4012A controls readout of the Timer and/or Counter channels. These channels are stored and accessed through TRAQ in an identical manner to other TRAQ channels.

CAMAC

Readout of the 2904 channels via CAMAC is a two (2) step process.

The STORE command (F[18]A[0]) transfers the current Counter and Timer contents into separate buffers within the 2904. At this point the buffers can be accessed from CAMAC and will reflect the Time and Count at the time of the STORE command.

The Timer and/or Counter buffers are divided between high and low words. Each section may be readout independently and in any order.

Timer Buffer (High Word)	F[2] A[0]
Timer Buffer (Low Word)	F[2] A[1]
Counter Buffer (High Word)	F[2] A[2]
Counter Buffer (Low Word)	F[2] A[3]

The buffer contents are static and are only updated by the STORE command.

NOTE

CAMAC 2904 Channel STORE and READOUT commands should NOT be used when the 2904 is in a TRAQ system during the TRAQ CONVERT mode. In this case the 2904 channel buffers are used for data transfers to the TRAQ system. Unpredictable data readout behavior will occur if CAMAC STORE commands are also issued.

PROGRAMMING EXAMPLES

1. READOUT OF COUNTER / TIMER PRESET

INITIALIZE DSP2904 Loads Counter and Timer with Preset Register contents	F[27] A[0]
STORE COUNTER and TIMER Stores Counter and Timer into channel buffers.	F[18] A[0]
READOUT CHANNELS	F[2] A[0] F[2] A[1] F[2] A[2] F[2] A[3]

TIMER AND COUNTER SETUP EXAMPLES

1. 32 Bit Timer. 1.6uS Resolution. Continuous mode.
   16 Bit Counter. Reload every 1000 counts.

Stop both channels	F[27] A[0]
Set Counter Mode GATE OFF WRAP ON (continuous mode) MOD32 OFF (16 bit) INDEX OFF	F[16] A[0] D = 2
Set Timer Mode GATE OFF WRAP ON (continuous mode) MOD32 ON (32 bit)	F[16] A[1] D = 6
Set Timer Rate Code = 4 (1.6uS)	F[16] A[1] D = 4
Preset 32 Bit Timer High Word = 0 Low Word = 0	F[17] A[0] D = 0 F[17] A[1] D = 0
Preset 16 Bit Counter Low Word = (overflow after 1000 cnts)	F[17] A[3] D = 64436
Start both Channels	F[9] A[0]

2. 32 Bit Timer. 1.6 uS resolution. Gated by Counter
   16 Bit Counter. Halt after 100 counts.

Stop both channels	F[27] A[0]

Set Counter Mode GATE OFF WRAP OFF (continuous mode) MOD32 OFF (16 bit) INDEX OFF	F[16] A[0] D = 0
Set Timer Mode GATE ON WRAP ON (continuous mode) MOD32 ON (32 bit) (note timer can overflow)	F[16] A[1] D = 7
Set Timer Rate Code = 4 (1.6uS)	F[16] A[1] D = 4
Preset 32 Bit Timer High Word = 0 Low Word = 0	F[17] A[0] D = 0 F[17]A[1] D = 0
Preset 16 Bit Counter Low Word = (overflow after 100 cnts)	F[17] A[3] D = 65435
Start both Channels	F[9] A[0]

3. 16 Bit Timer. 1.6 uS resolution.
Measure interval of 720 counts repeatedly.
16 Bit Counter. 720 counts. Reset on alternate INDEX pulses

Stop both channels	F[27] A[0]
Set Counter Mode GATE OFF WRAP ON (continuous mode) MOD32 OFF (16 bit) INDEX ON (alternate INDEX pulses)	F[16] A[0] D = 10
Set Timer Mode GATE OFF WRAP ON (continuous mode) MOD32 OFF (16 bit) TOFCNT ON (Time of Count mode)	F[16] A[1] D = 10
Set Timer Rate Code = 4 (1.6uS)	F[16] A[1] D = 4
Preset 16 Bit Timer Low Word = 0	F[17] A[1] D = 0
Preset 16 Bit Counter Low Word = 0 (Index Pulse reset after 720)	F[17] A[3] D = 0
Start both Channels	F[9] A[0]

PROGRAMMING

CAMAC COMMAND SUMMARY

Module conforms to CAMAC (IEEE 583) standard protocol. All valid commands are acknowledged with CAMAC X=1. Q=1 is returned on all commands unless otherwise noted.

F[0] A[0] Read Counter Mode Register

R1 = 0 Gate Mode OFF
1 Gate Mode ON

R2 = 0 Wrap Mode OFF
1 Wrap Mode ON

R3 = 0 16 Bit Counter
1 32 Bit Counter

R4 = Reserved

R5 = 0 Reload on INDEX
1 Reload on INDEX div 2

R6..R8 Reserved

R9 = 0 INDEX divider reset
1 INDEX divider set

F[0] A[1] Read Timer Mode Register

R1 = 0 Gate Mode OFF
1 Gate Mode ON

R2 = 0 Wrap Mode OFF
1 Wrap Mode ON

R3 = 0 16 Bit Counter
1 32 Bit Counter

R4 = 0 Time of Count Mode OFF
1 Time of Count Mode ON

F[0] A[0] Read Timer Clock Rate

R1..R5 Rate Code

R6 = 0 Internal Clock
1 External Clock

F[2] A[0] Read Timer Buffer High Word

R1..R16 = Timer Buffer T17..T32

F[2] A[1] Read Timer Buffer Low Word

R1..R16 = Timer Buffer T1..T16

F[2] A[2] Read Counter Buffer High Word

R1..R16 = Counter Buffer C17..C32

F[2] A[3] Read Counter Buffer Low Word

R1..R16 = Counter Buffer C1..C16

F[3] A[0] Read ID
R1..R16 = 2904

F[8] A[0] Read Timer Overflow LAM Status

Q = 1 Timer Overflowed
0 Timer not overflowed

F[8] A[1] Read Counter Overflow LAM Status

Q = 1 Counter Overflowed
0 Counter not overflowed

F[9] A[0] Start Timer and Counter

F[10] A[0] Clear Timer Overflow LAM

F[10] A[1] Clear Counter Overflow LAM

F[16] A[0] Load Counter Mode Register

W1 = 0 Gate Mode OFF
1 Gate Mode ON

W2 = 0 Wrap Mode OFF
1 Wrap Mode ON

W3 = 0 16 Bit Counter
1 32 Bit Counter

W4 = Reserved

W5 = 0 Reload on INDEX
1 Reload on INDEX div 2

F[16] A[1] Load Timer Mode Register

W1 = 0 Gate Mode OFF
1 Gate Mode ON

W2 = 0 Wrap Mode OFF
1 Wrap Mode ON

W3 = 0 16 Bit Counter
1 32 Bit Counter

CAMAC COMMAND SUMMARY

F[16] A[1]

W4 = 0 Time of Count Mode OFF
1 Time of Count Mode ON

F[16] A[2] Load Timer Rate Register

W1..W5 Rate Code

W6 = Internal Clock
1 External Clock

F[17] A[0] Load Timer Preset Register High Word

W1..W16 = Timer Preset TP17..TP32

F[17] A[1] Load Timer Preset Register Low Word

W1..W16 = Timer Preset TP1..TP16

F[17] A[2] Load Counter Preset Register High Word

W..1W16 = Counter Preset CP17..CP32

F[17] A[3] Load Counter Reset Register Low Word

W1..W16 = Timer Preset CP1..CP16

F[18] A[0] Store current Time and Count
Stores Timer and Counter contents into internal buffers T1..T32 and C1..C32

F[19] A[0] Write Module ID W = 2904 No "Q" or "X" response

F[24] A[0] Disable Timer Overflow LAM

F[24] A[1] Disable Counter Overflow LAM

F[25] A[0] Stop Timer and Scaler

F[26] A[0] Enable Timer Overflow LAM

F[26] A[1] Enable Counter Overflow LAM

F[27] A[0] Reset Timer and Scaler

APPENDIX A

PROGRAMMING EXAMPLES

The following pages describe a number of utility routines for controlling the DSP2904. All routines are written in PASCAL (TURBO) and call DSP CAMAC driver routines for the DSP6001 IBM/PC Crate Controller.

```
{=================================================================
MODULE    :u2904
PURPOSE   :utility programs for 2904
FILE      :u2904.pas
CONTENTS :
-----------------------------------------------------------------
REVISION HISTORY

10/11/87 miller created
=================================================================}

{*****************************************************************************************************************}
procedure u2904Init;
{ issues init command to uN}
begin
  uF := 27; uA := 0;
  camo(uN,uF,uA,uD,uQ,uX) ;
end;
{*****************************************************************************************************************}
procedure u2904 Start;
{ issues START command to uN}
begin
  uF := 9; uA := 0;
  camo (uN,uF,uA,uD,uQ,uX) ;
end;
{*****************************************************************************************************************}
procedure u2904Stop;
{ issues STOP command to uN}
begin
  uF := 25; uA := 0;
  camo(uN,uF,uA,uD,uQ,uX) ;
end;
{*****************************************************************************************************************}
Function u2904LAMQ : boolean;
{tests if 2610 LAM via F8 Q}
begin
  uF := 8; uA := 0;
  cami (uN,uF,uA,uD,uQ,uX);

  if (uQ<>NONE) then u2904 LamQ := TRUE else u2904LamQ := FALSE;
end;
{*****************************************************************************************************************}
procedure u2904IDGet( var id :integer) ;
{returns unit ID register}
begin
  uF := 3; uA := 0;
  cami (uN,uF,uA,uD,uQ,uX) ;
  id := uD;
  end;
```

```
{*****************************************************************************************************************}
procedure u2904TimerClockSet(code: integer) ;
{sets 2904 clock register}
begin
  uF := 16; uA := 2; uD := code;
  camo(uN,uF,uA,uD,uQ,uX) ;
{ showcamacstatus; PAUSE;}
end;
{*****************************************************************************************************************}
procedure u2904TimerClockGet(var code: integer;
                             var rcode : integer) ;
{gets 2904 clock register}
const
  CLMASK =$00FF;
begin
  rcode := NONE;
  uF := 0; uA := 2;
  cami(uN,uF,uA,uD,uQ,uX) ;
  if uQ<>None the code := uD AND CLKMASK else Rcode := INVALID;
end;
{*****************************************************************************************************************}
procedure u2904TimerModeSet(Gate, Wrap, Mod32, TofS : boolean) ;
{sets 2904 Timer Mode register}
begin
  uF := 16; uA := 1;
  uD ;= 0;
  if (Gate) then uD := uD OR 1;
  if (Wrap) then uD := uD OR 2;
  if (Mod32) then uD := uD OR 4;
  if (TofS) then uD := uD OR 8;
  camo (uN,uF,uA,uD,uQ,uX) ;
end;
{*****************************************************************************************************************}
procedure u2904TimerModeGet(var Gate, Wrap, Mod32, TofS : boolean;
                            var rcode :integer);
{gets 2904 Timer Mode register}
begin
  rcode := NONE;
  uF := 0; uA := 1;
  uD := 0;
  cami (uN,uF,uA,uD,uQ,uX) ;
  if (uQ<>NONE) then
   begin
   if ((uD AND 1)=0) then Gate := FALSE else Gate := TRUE;
   uD := uD shr 1;
   if ((uD AND 1)=0) then Wrap := FALSE else Wrap := TRUE;
   uD := uD shr 1;
   if ((uD AND 1)=0) then Mod32 := FALSE else Mod32 := TRUE;
   uD := uD shr 1;
   if ((uD AND 1)=0) then TofS := FALSE else TofS := TRUE;
   end
  else RCode := INVALID;
end;

{*****************************************************************************************************************}
procedure u2904 ScalerModeSet(Gate, Wrap, Mod32, SofT, PI4 : boolean) ;
```

```
{sets 2904 Scaler Mode register}
begin
   uF := 16; uA := 0;
   uD := 0;
   if (Gate) then uD := uD OR 1;
   if (Wrap) then uD := uD oR 2:
   if (Mod32) then uD := uD OR 4;
   if (SofT) then uD := uD OR 8;
   if (PI4) then UD := uD OR 16;
   camo(uN,uF,uA,uD,uQ,uX) ;
end;
{*****************************************************************************************************************}
procedure u2904 ScalerModeGet(var Gate, Wrap, Mod32, SofT, PI4 : boolean;
                              var rcode :integer) ;
{gets 2904 Scaler Mode register}
begin
  rcode := NONE;
  uF := 0; uA := 0;
  uD := 0;
  cami(uN,uF,uA,uD,uQ,uX) ;
  if (uQ<>NONE) then
   begin
   if ((uD AND 1)=0) then Gate := FALSE else Gate := TRUE;
   uD := uD shr 1;
   if ((uD AND 1)=0) then Wrap := FALSE else Wrap := TRUE;
   uD := uD shr 1;
   if ((uD AND 1)=0) the Mod32 : FALSE else Mod32 := TRUE;
   uD := uD shr 1;
   if ((uD AND 1)=0) then SofT := FALSE else SofT := TRUE;
   uD := uD shr 1;
   if ((uD AND 1)=0) then PI4 := FALSE else PI4 := TRUE;
   end
  else RCode := INVALID;
end;
{*****************************************************************************************************************}
procedure u2904TimerPreset(PresetHi, PresetLo : integer; var
rcode : integer);

{Load Timer Preset Register}

begin
  rcode := NONE;
  uF := 17;
  uA := 0;
  camo(uN,uF,uA,PresetHi,uQ,uX) ;
  uA := 1;
  camo(uN,uF,uA,PresetLo,uQ,uX) ;
end;
{*****************************************************************************************************************}
procedure u2904 ScalerPreset(PresetHi, PresetLo : integer; var
rcode : integer) ;
{Load Counter Preset Register}
begin
  rcode := NONE;
  uF := 17;
  uA := 2;
  camo(uN,uF,uA,PresetHi,uQ,uX) ;
```

```
  uA := 3;
  camo(uN,uF,uA,PresetLo,uQ,uX) ;
end;
{*****************************************************************************************************************}
procedure u2904Store;
{Store 2904 counter contents in internal buffer}
begin
  uF := 18; uA := 0; uD := 0;
  camo(uN,uF,uA,uD,uQ,uX) ;
end;
{*****************************************************************************************************************}
procedure u2904Read(var TimeHi, TimeLo, ScalerHi, ScalerLo :
integer;
                    var RCode : integer) ;
var
  i : integer;
  F,A,D : integer;

begin
  RCode : INVALID;
  u2904Store;                    {capture counter contents}
  RCode := NONE;
  uF := 2;
  for uA := 0 to 3 do
   begin
   cami(uN,uF,uA,uD,uQ,uX) ;  {CAMAC Request}
{  showcamacstatus;pause; }
   if (uQ<>NONE) then

    case uA of
    0 : TimeHi := uD;
    1 : TimeLo := uD;
    2 : ScalerHi := uD;
    3 : ScalerLo := uD;
    else end
  else RCode := INVALID;
  end;
end;
{*****************************************************************************************************************}
procedure u2904CfgShow;
{display 2904 registers}

label Xit;

ver
  1              : integer;
  obj            : string[8];
  Gate           : boolean;
  Wrap           : boolean;
  Mod32          : boolean;
  Interval       : boolean;
  PI4            : boolean;
  Rate           : integer;
  THi,TLo,Chi,Clo : integer;
begin
  write('DSP2904/N=',uN:2,' CONFIGURATION ') ;
  write(' ID=') ;
```

```
  u2904IdGet(i) ;
  write1n(i:5) ;
  u2904TimerModeGet(Gate,Wrap,Mod32,Interval,rcode) ;
  if (RCode<>NONE) then
   begin
   ErrorMsg := 'ERROR: Unit at Station '+itos(uN)+' not
responding';
   goto XIT;
   end;

  u2904Read(Thi,Tlo,Clo,rcode) ;
  writeln(thi:6,tlo:6,Chi:6,rcode:4) ;
  write('TIMER :GATE=');
  if (Gate) then write('ON') else write('OFF') ;
  write(' BITS=') ;
  if (Mod32) then write('32') else write('16') ;
  write(' WRAP=') ;
  if (Wrap) then write('ON') else write ('OFF') ;
  write('TOFS=') ;
  if (Interval) then write('ON') else write('OFF') ;
  u2904TimerClockGet(Rate,rcode) ;
  write(' CLOCK=',Rate:2) ;
  writeln(' HI=',thi:6,' LO=',tlo:6) ;

  u2904ScalerModeGet(Gate,Wrap,Mod32,Interval,PI4,rcode) ;
  write('COUNTER :GATE=') ;
  if (Gate) then write('ON') else write('OFF') ;
  write(' BITS=') ;
  if (Mod32) then write('32') else write('16') ;
  write(' WRAP=') ;
  if (Wrap) then write('ON') else write('OFF') ;
  write(' SATT=') ;
  if (Interval) then write('ON') else write('OFF') ;
  write('PI4=') ;
  if (Pi4) then write('ON') else write('OFF') ;
  writeln(' HI=',chi:6,' LO=',clo:6) ;
Xit:
end;
{**********************************************************************************************************
*****************************************}
{**********************************************************************************************************
*****************************************}
```

APPENDIX B

DSP2904 VERSION DIFFERENCES

This section describes differences in early DSP2904 unit (s/n 101 - 140) from the description in the manual. Early version DSP2904 can be identified by the PCB Revision number silkscreened to the right of SW4 on the component side. This number is "1" for such units.

TIMER/COUNTER TRAQ ID SELECT

Four switches are used to determine the TRAQ channel assignment of the four Timer/Counter registers. The assignments are as described in the CONTROLS and INDICATORS section of the manual.

TRAQ ID SELECT

TRAQ channel assignment is determined by 4 individual 8 position switches. Note the 8 positions are interleaved.

TRAQ CHAN	SWITCH POSITION 1 2 3 4 5 6 7	TRAQ CHAN	SWITCH POSITION 1 2 3 4 5 6 7
1	0 0 0 0 0 0 0	33	0 0 0 1 0 0 0
2	0 0 0 0 0 0 1	34	0 0 0 1 0 0 1
3	0 0 0 0 1 0 0	35	0 0 0 1 1 0 0
4	0 0 0 0 1 0 1	36	0 0 0 1 1 0 1
5	0 0 1 0 0 0 0	37	0 0 1 1 0 0 0
6	0 0 1 0 0 0 1	38	0 0 1 1 0 0 1
7	0 0 1 0 1 0 0	39	0 0 1 1 1 0 0
8	0 0 1 0 1 0 1	40	0 0 1 1 1 0 1
9	1 0 0 0 0 0 0	41	1 0 0 1 0 0 0
10	1 0 0 0 0 0 1	42	1 0 0 1 0 0 1
11	1 0 0 0 1 0 0	43	1 0 0 1 1 0 0
12	1 0 0 0 1 0 1	44	1 0 0 1 1 0 1
13	1 0 1 0 0 0 0	45	1 0 1 1 0 0 0
14	1 0 1 0 0 0 1	46	1 0 1 1 0 0 1
15	1 0 1 0 1 0 0	47	1 0 1 1 1 0 0
16	1 0 1 0 1 0 1	48	1 0 1 1 1 0 1
17	0 1 0 0 0 0 0	49	0 1 0 1 0 0 0
18	0 1 0 0 0 0 1	50	0 1 0 1 0 0 1
19	0 1 0 0 1 0 0	51	0 1 0 1 1 0 0
20	0 1 0 0 1 0 1	52	0 1 0 1 1 0 1
21	0 1 1 0 0 0 0	53	0 1 1 1 0 0 0
22	0 1 1 0 0 0 1	54	0 1 1 1 0 0 1
23	0 1 1 0 1 0 0	55	0 1 1 1 1 0 0
24	0 1 1 0 1 0 1	56	0 1 1 1 1 0 1
25	1 1 0 0 0 0 0	57	1 1 0 1 0 0 0
26	1 1 0 0 0 0 1	58	1 1 0 1 0 0 1
27	1 1 0 0 1 0 0	59	1 1 0 1 1 0 0
28	1 1 0 0 1 0 1	60	1 1 0 1 1 0 1
29	1 1 1 0 0 0 0	61	1 1 1 1 0 0 0
30	1 1 1 0 0 0 1	62	1 1 1 1 0 0 1
31	1 1 1 0 1 0 0	63	1 1 1 1 1 0 0
32	1 1 1 0 1 0 1	64	1 1 1 1 1 0 1
		65	0 0 0 0 0 1 0

If a 2904 channel is not to be used the TRAQ Channel assignment should be set to an unused TRAQ channel - for example all switches CLOSED.

INDEX (Reset)INPUT REQUIREMENTS

Early DSP2904 units support LEVEL detect INDEX mode only. As described in the OPERATIONS section of the manual this requires an overlap of the INDEX input pulse with a Counter clock cycle. If the overlap extends across two or more clock cycles multiple Resets will occur.

DSP Technology Inc.
SINGLE LEVEL BILL OF MATERIAL REPORT

Date: 8/30/89
Page: 1

Assembly: A-2904-01 (ASSY: PCB, 2904)
Revision: A
As of: 6/29/89

Component	Description	Qty Per	As of	Until	Reference
0100-0101	RES: RC07 100 OHM	3.00	1/09/89	12/31/99	R23-R25
0100-0102	RES: RC07 1K OHM	9.00	8/25/87	12/31/99	R9-R12, R15, R16, R18, R19, R21
0100-0103	RES: RC07 10K OHM	5.00	6/30/87	12/31/99	R1-R3, R8, R14
0100-0153	RES 5% 1/4 W CF RESISTOR R=15K	2.00	1/09/89	12/31/99	R5, R6
0100-0223	RCF 5% 1/4W CF RESISTOR R=22K	1.00	4/01/88	12/31/99	R13
0100-0271	RES RC07 270 OHM 1/4W 5%	2.00	8/25/87	12/31/99	R20, R22
0100-0473	RES CF, 5% 1/4W R=47K	1.00	11/23/87	12/31/99	R4
0100-0511	RES 5% 1/4W CC RESISTOR R=510	1.00	4/01/88	12/31/99	R17
0200-0102	RPK RES PK BNS 4308R-101-102	1.00	8/25/87	12/31/99	RP1
0201-0102	RPK RES PK BNS 4310R-101-102	1.00	4/01/88	12/31/99	RP2
0500-0100	CSM C=10PF 5% CD6CD100D03	1.00	12/01/87	12/31/99	C3
0500-0200	CSM C=20PF 5% ARCO DM05-200J0	1.00	11/23/87	12/31/99	C4
0520-0104	CMC 0.1UF CNTLB:CZ20A104M2 KEM	43.00	8/25/87	12/31/99	
0600-0335	CTE C=3.3UF TANT KEMET T362B3	2.00	4/01/88	12/31/99	C2, C5
0600-0685	CTE C=6.8UF TANT 35WVDC KEMET	1.00	8/25/87	12/31/99	C1
1000-4448	DGS DIODE SIL. SWITCH 1N4448	10.00	8/25/87	12/31/99	CR8-CR17
1010-2811	DSS DIODE H.P.5000-2811	2.00	8/25/87	12/31/99	CR18, CR19
1030-5624	DSR: DIODE RECT 3A GE IN5624/	1.00	8/25/87	12/31/99	CR1
1750-0001	ICS SN7401	1.00	8/25/87	12/31/99	9A
1750-0032	ICS SN7432	1.00	8/25/87	12/31/99	4B
1750-0128	ICS SN74128	1.00	8/25/87	12/31/99	9H
1760-0000	ICS SN74LS00	1.00	12/01/87	12/31/99	4C
1760-0002	ICS SN74LS02	1.00	8/25/87	12/31/99	7A
1760-0004	ICS SN74LS04	1.00	8/25/87	12/31/99	8B
1760-0010	ICS SN74LS10	1.00	8/25/87	12/31/99	8A
1760-0038	ICS SN74LS38	1.00	8/25/87	12/31/99	1A
1760-0074	ICS SN74LS74	5.00	8/25/87	12/31/99	5C, 3D, 3H, 2H, 14G
1760-0139	ICS SN74LS139	2.00	8/25/87	12/31/99	7C, 8C
1760-0174	ICS SN74LS174	1.00	8/25/87	12/31/99	4D
1760-0221	ICS SN74LS221	2.00	8/25/87	12/31/99	2F, 2G
1760-0279	ICS SN74LS279	1.00	8/25/87	12/31/99	9C
1760-0292	ICS SN74LS292	1.00	8/25/87	12/31/99	5H
1760-0374	ICS SN74LS374	8.00	8/25/87	12/31/99	5D, 7D-10D, 12D-14D
1760-0469	ICS SN74LS469	8.00	8/25/87	12/31/99	4E, 4F, 7E, 7F, 10E, 10F 13E, 13F
1760-0534	ICS SN74LS534	1.00	8/25/87	12/31/99	2A
1760-0640	ICS SN74LS640	2.00	12/01/87	12/31/99	12A, 12B
1760-0644	ICS SN74LS644	2.00	12/01/87	12/31/99	14A, 14B
1760-0645	ICS SN74LS645	4.00	8/25/87	12/31/99	3A, 4A, 10C, 12C
1760-0682	ICS SN74LS682	4.00	8/25/87	12/31/99	2B, 2C, 2D, 2E
1762-0574	ICS SN74ALS574	8.00	8/25/87	12/31/99	3E, 3F, 6E, 6F, 9E, 9F 12E, 12F
1770-0004	ICS IC LSTTL HEX INV SN74S04	1.00	8/25/87	12/31/99	10B
1770-0074	ICS IC STTL DUAL D FF SN74S7	2.00	8/25/87	12/31/99	8H, 13H
1772-0008	ICD 74AS08	1.00	8/25/87	12/31/99	3C
1780-0014	IC: 74HCT14	2.00	5/01/89	12/31/99	12H, 9J
1780-0074	IC: 74HCT74	1.00	8/25/87	12/31/99	10G
1780-0174	IC: MM74HCT174	3.00	8/25/87	12/31/99	5G, 6G, 9G
1780-0574	IC: 74HCT574	8.00	8/25/87	12/31/99	5E, 5F, 8E, 8F, 11E, 11F 14E, 14F
1851-0071	PRM:M/F 1850-0001, 2904 CLK COD	1.00	4/01/88	12/31/99	6H
1857-0058	PAL:M/F 1856-4000, 2904 ENABLE	1.00	4/01/88	12/31/99	10H

DSP Technology Inc.
SINGLE LEVEL BILL OF MATERIAL REPORT

Date: 6/30/89

Assembly: A-2904-01 (ASSY: PCB, 2904)
Revision: A
As of: 6/29/89

Component	Description	Qty Per	As of	Until	Reference
1857-0059	PAL:M/F 1856-0106,2904 COUNTER	1.00	4/01/88	12/31/99	12G
1857-0060	PAL:M/F 1856-0100,2904 COUNTER	1.00	4/01/88	12/31/99	13G
1857-0061	PAL:M/F 1856-0106,2904 TRAQ LO	1.00	4/01/88	12/31/99	3B
1857-0062	PAL:M/F 1856-0106,2904 TIMER C	1.00	4/01/88	12/31/99	3G
1857-0063	PAL:M/F 1856-0106,2904 CMAC DC	1.00	4/01/88	12/31/99	5B
1857-0064	PAL:M/F 1856-0106,2904 CAMAC N	1.00	4/01/88	12/31/99	7B
1857-0065	PAL:M/F 1856-0106,2904 TIMER C	1.00	4/01/88	12/31/99	8G
1857-0066	PAL:M/F 1856-4008,2904 CAMAC L	1.00	4/01/88	12/31/99	9B
1910-0005	IC: CMOS, HM6264ALSP-12	1.00	8/25/87	12/31/99	10A
2350-0206	OSC XTAL CLOCK 20.0MHZ 0.01%	1.00	8/25/87	12/31/99	Y1
3100-0102	FUSE: PICO, 1AMP LITTLEFUSE 2	1.00	8/25/87	12/31/99	F2
3100-0402	FUS FUSE 4AMP LITTLEFUSE 25100	1.00	8/25/87	12/31/99	F1
5000-0008	SKT CAMBION 703-1308-01-04-10	11.00	8/25/87	12/31/99	10A,9B,4E,7E,10E,13E 4F,7F,10F,13F,10H
5000-0014	SKT CAMBION 703-1314-01-04-10	3.00	8/25/87	12/31/99	9A,8H,13H
5000-0016	SKT CAMBION 703-1316-01-04-10	13.00	8/25/87	12/31/99	9B,4E,7E,10E,13E,4F 7F,10F,13F,5G,6G,6H,10H
5000-0020	SKT CAMBION 703-1320-01-04-10	29.00	8/25/87	12/31/99	10A,12A,14A,3B,5B,7B,13B,14B,3E,5E,6E,8E,9E,11E,12E,14E,3F, 5F,6F,8F,9F,11F,12F,14F,3G,8G,12G,13G,1H
5250-3703	JCK FUS CAMBION 450-3703-01-06	8.00	8/25/87	12/31/99	E1-E3,F1,F2
5251-0001	JMP CAMBION 461-2251-01-03-10	1.00	4/01/88	12/31/99	E2
5500-0018	HDR 40 PIN R/A 4 WALL 3M#3595-	1.00	8/25/87	12/31/99	J1
6000-0004	SWD DIP SWT GRYHL ONLY 76SB08	4.00	8/25/87	12/31/99	SW1-SW4
6850-0001	RAIL: GUIDE, MDL, 7 HOLE, C-BO	2.00	8/25/87	12/31/99	
7000-0064	PCB DWG# 2904-01-FD	1.00	8/25/87	12/31/99	
7410-0003	HWD: SWAGE TYPE STANDOFF	6.00	8/25/87	12/31/99	

** E N D O F R E P O R T **

SYMBOLS.


CAMAC EDGE CONNECTOR


EXTERNAL CONNECTOR


CONTINUE ON SAME SHEET

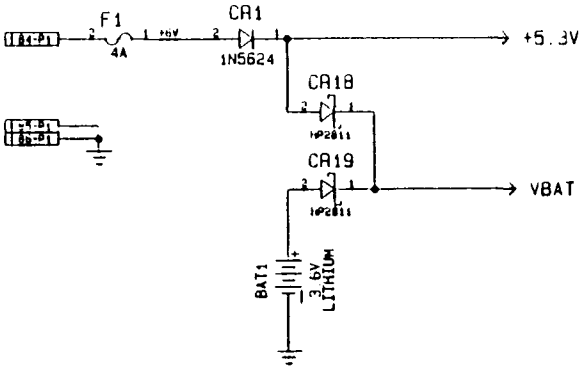

PC BOARD TERMINAL PAD


UNUSED PIN


JUMPERS

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL CAPACITORS ARE IN uf.
2. ALL RESISTORS ARE IN OHMS.



REV	DESCRIPTION	DATE
	REVISIONS	

SIGNATURES | DATE

DRAWN N. PERALTA

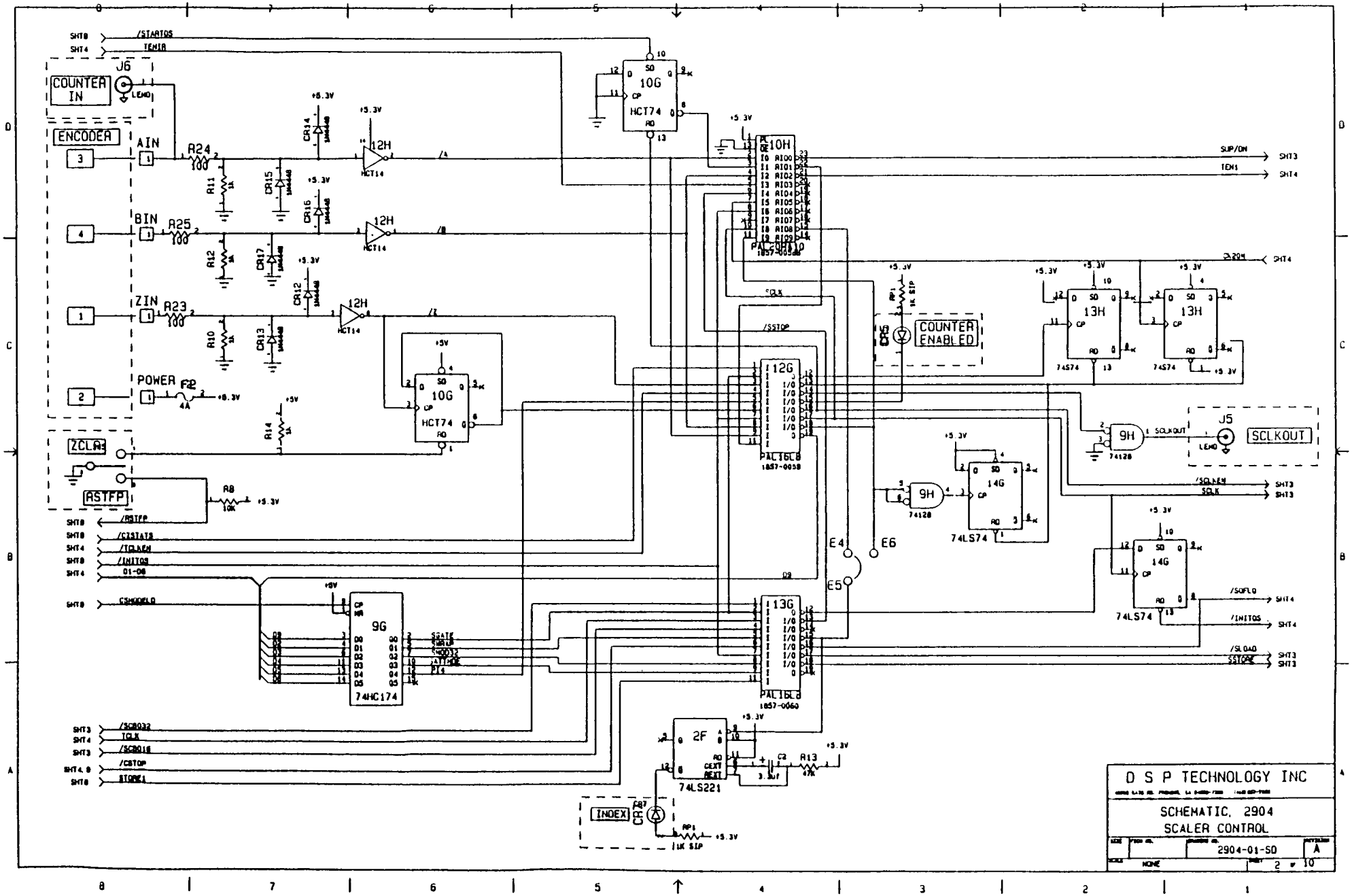
D S P TECHNOLOGY INC

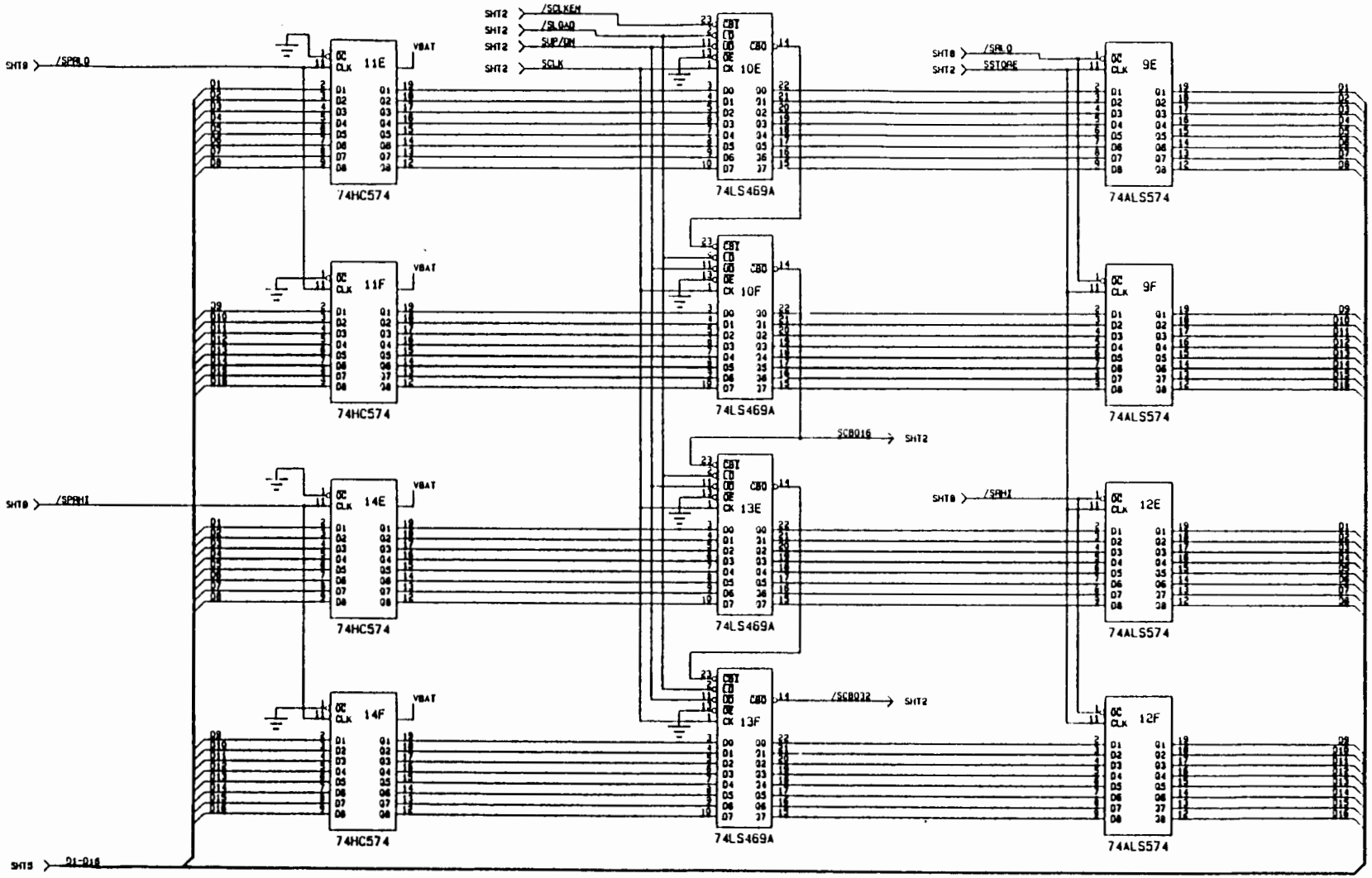
SCHEMATIC, 2904

POWER

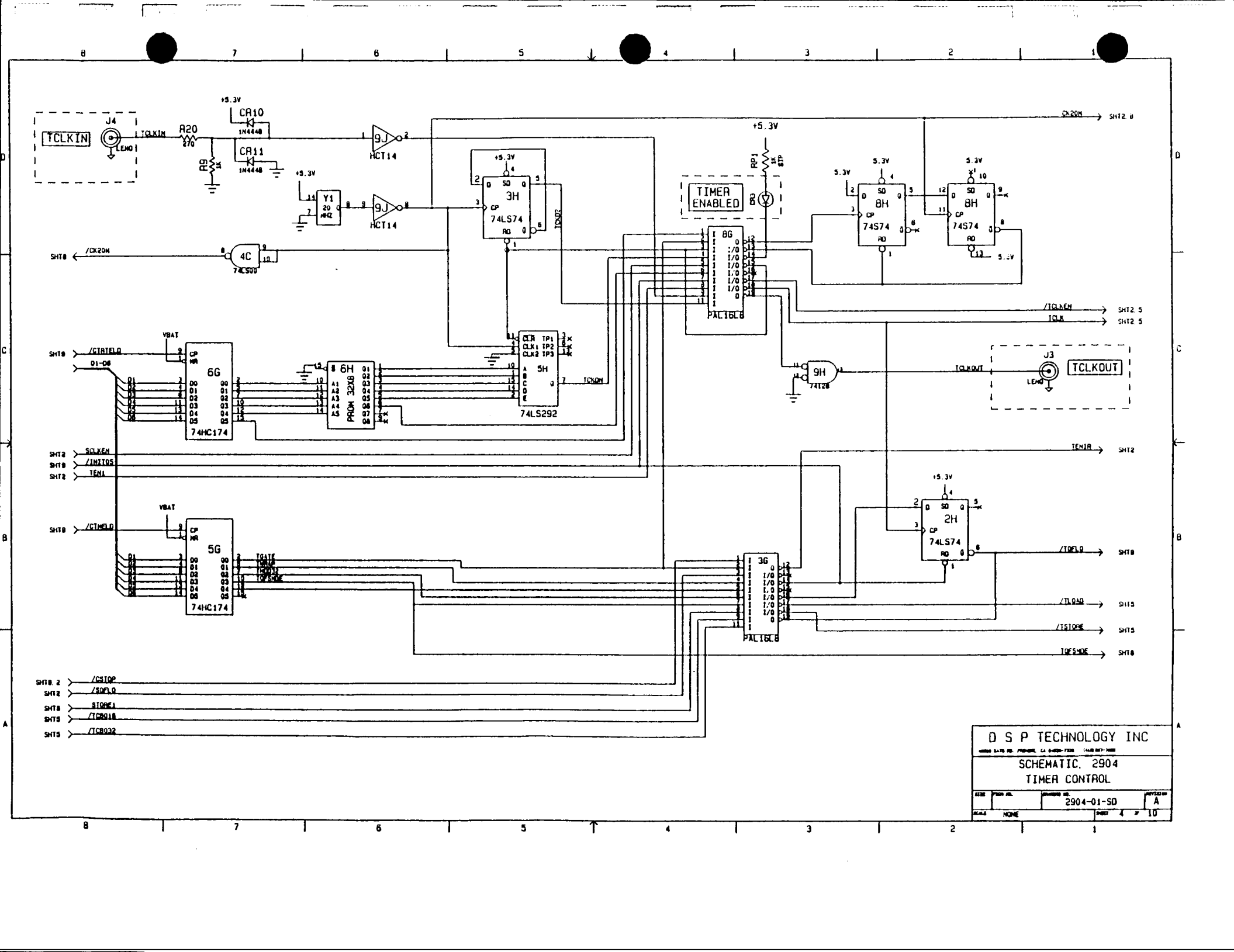
SIZE A | DWG NO. 01 | 2904-01-SD | REV A

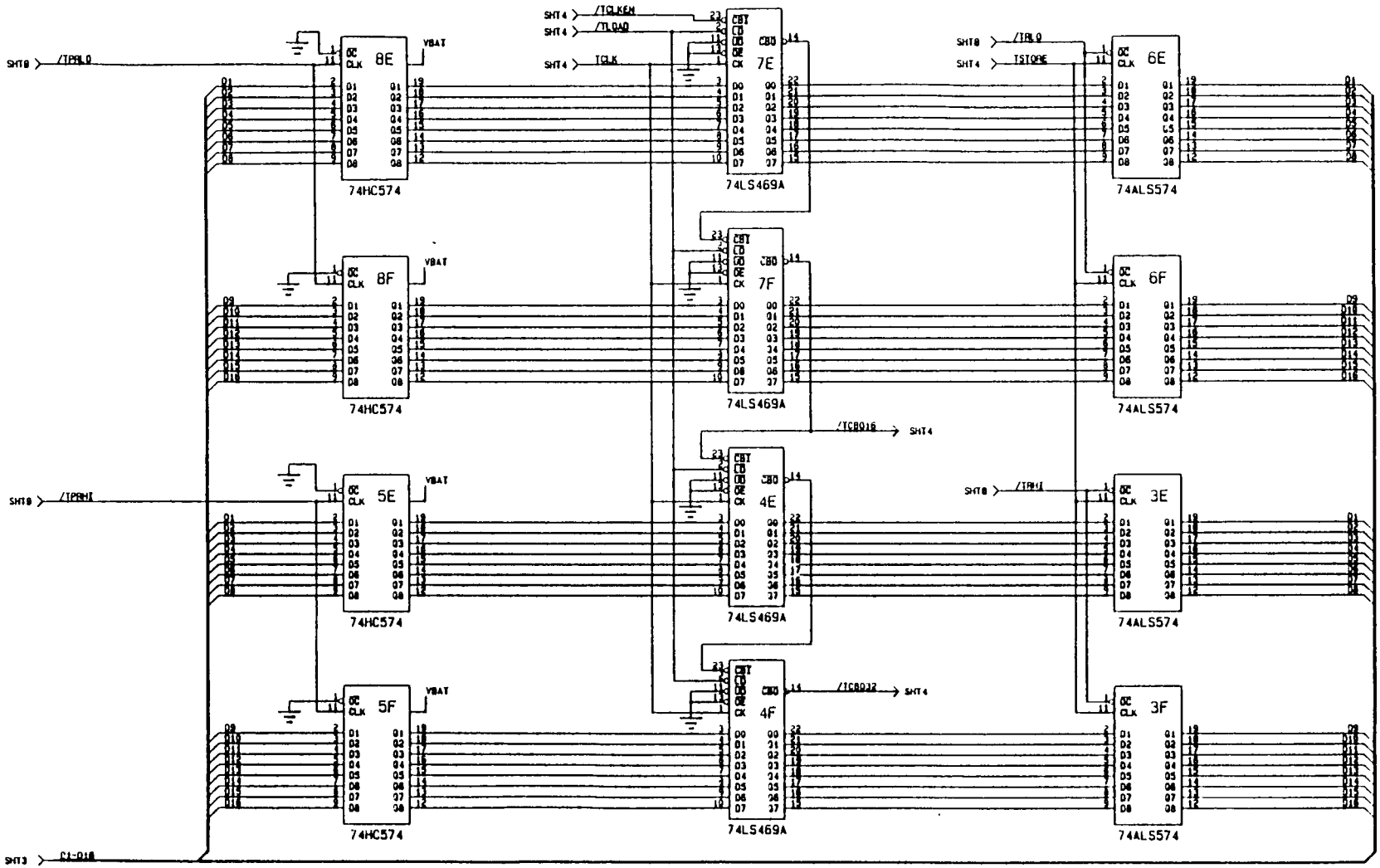
SCALE NONE | SHEET 1 OF


COUNTER IN
J6
ENCODER
AIN
BIN
ZIN
POWER
F2
4A
ZCLR
ASTFP
R24
R25
R23
R11
R12
R10
R14
R8
CR14
CR15
CR16
CR17
CR12
CR13
12H
HCT14
10G
HCT74
12G
13G
PAL16L8
10H
PAL20H10
9G
74HC174
13H
74LS74
14G
9H
74128
2F
74LS221
C2
3.3uF
R13
47K
COUNTER ENABLED
INDEX
1K SIP
J5
SCLKOUT
E4
E5
E6
/STARTOS
TENIR
/A
/B
/Z
/SSTOP
SUP/DN
TEN1
/SCLKEN
SCLK
/SOFLO
/INITOS
/SLOAD
SSTOAE
/RSTFP
/CSTATS
/TCLKEN
/INITOS
01-06
CSHOOKLD
/SCB032
TCLK
/SCB016
/CSTOP
STORE1
D S P TECHNOLOGY INC
SCHEMATIC, 2904
SCALER CONTROL
2904-01-SD
A
NONE
2 OF 10



D S P TECHNOLOGY INC			
SCHEMATIC, 2904 SCALER COUNTER			
SIZE	DSP NO.	DRAWING NO.	REVISION
	03	2904-01-SD	A
SCALE NONE		SHEET 3 OF 10	

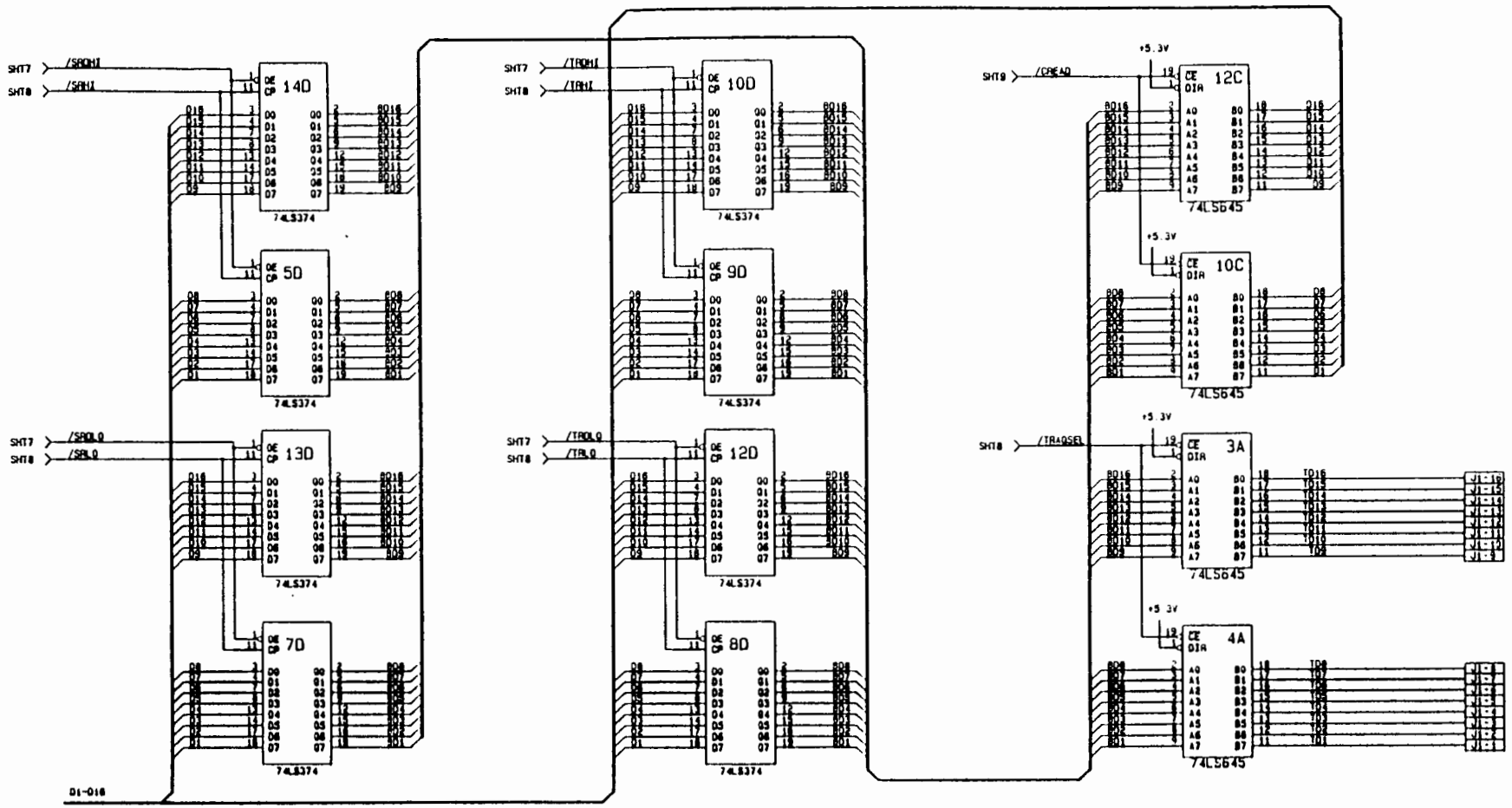

TCLKIN
J4
LEMO
TCLKIN
R20
270
R9
1K
+5.3V
CR10
1N4448
CR11
1N4448
9J
HCT14
Y1
20
MHZ
3H
74LS74
TCNTR
/CK20M
SHT2, 8
4C
74LS00
SHT8
TIMER ENABLED
RP1
1K
6TP
8G
PAL16L8
8H
74S74
/TCLKEN
TCLK
SHT2, 5
9H
74T28
TCLKOUT
J3
TCLKOUT
/CTIMFLG
D1-D8
VBAT
6G
74HC174
6H
PROM 32X8
5H
74LS292
TCKON
SCLKEN
/INITOS
TENI
TENIR
SHT2
SHT8
/CTIMFLG
5G
74HC174
3G
PAL16L8
2H
74LS74
/TOFLG
/TLOAD
/TSTOPE
TOFSYDE
SHT5
SHT8, 2
/CSTOP
/SOFLG
STOPEJ
/TCB01B
/TCB03Z
D S P TECHNOLOGY INC
SCHEMATIC, 2904
TIMER CONTROL
2904-01-SD
A
NONE
4
10



D S P TECHNOLOGY INC

SCHEMATIC. 2904
TIMER COUNTER

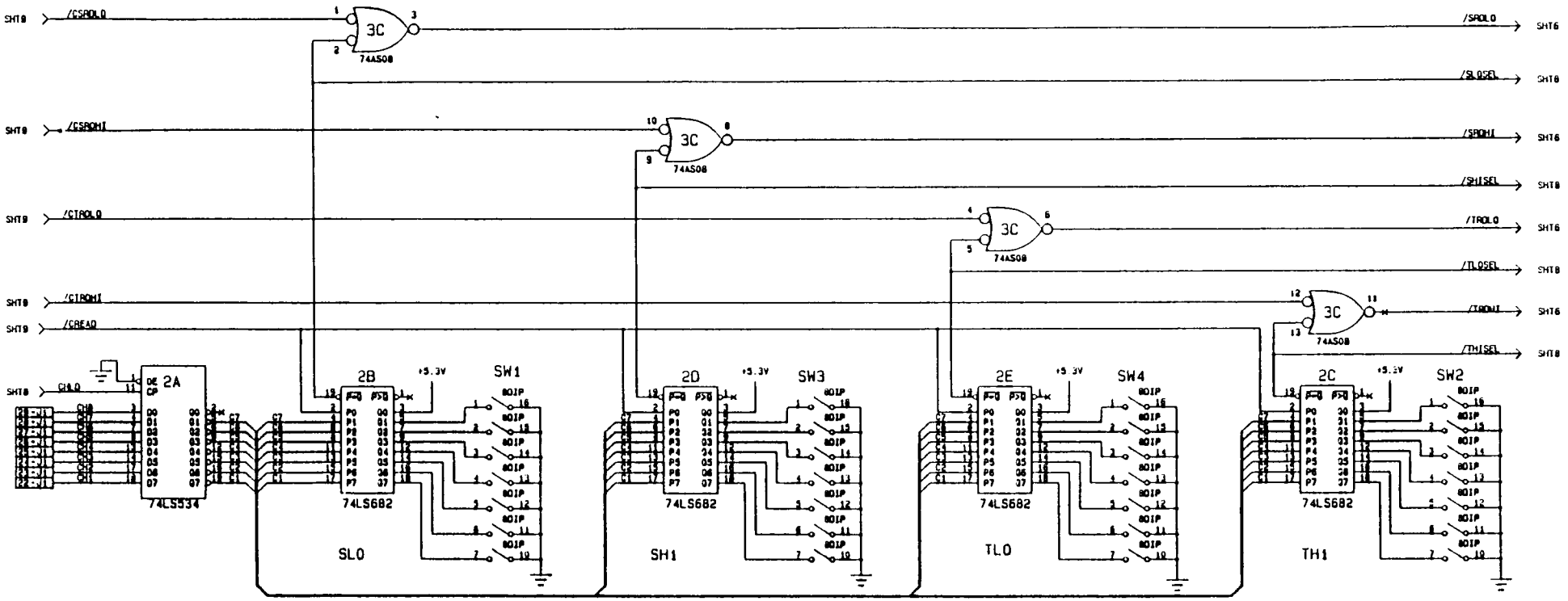
SIZE	FSCM NO.	DRAWING NO.	REVISION
	05	2904-01-SD	A
SCALE: NONE		SHEET 5 OF 10	



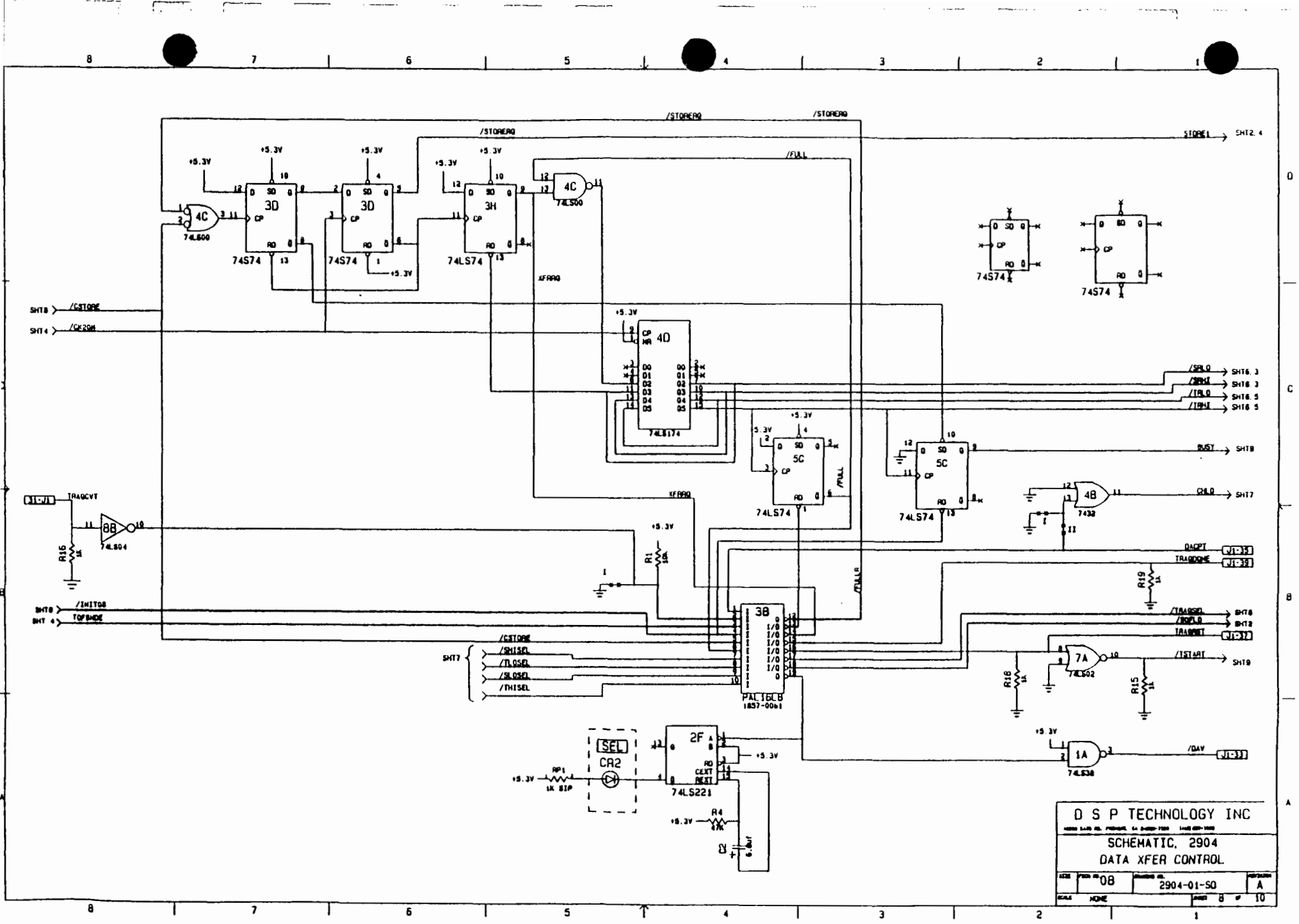
D S P TECHNOLOGY INC

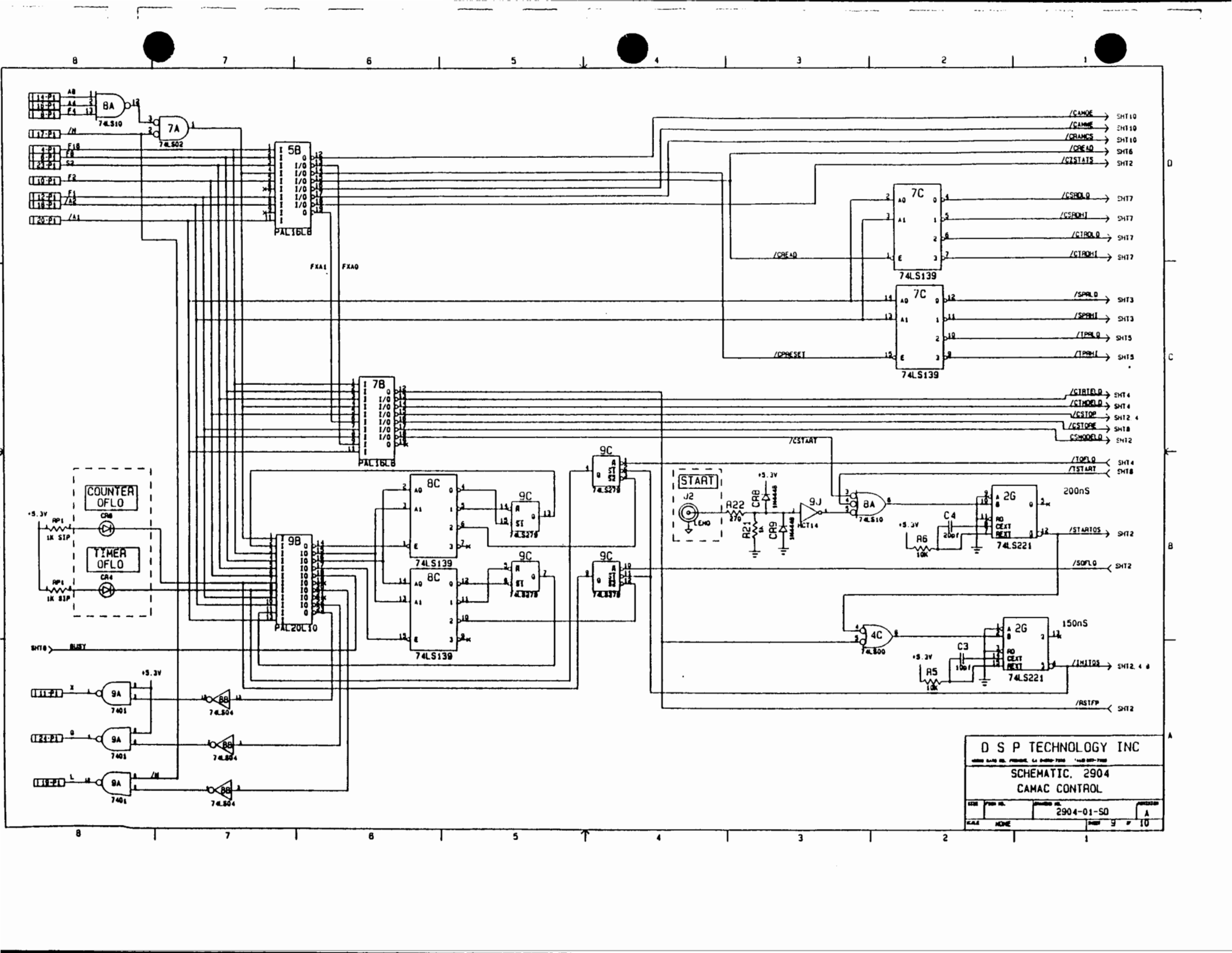
SCHEMATIC, 2904
DATA BUFFER

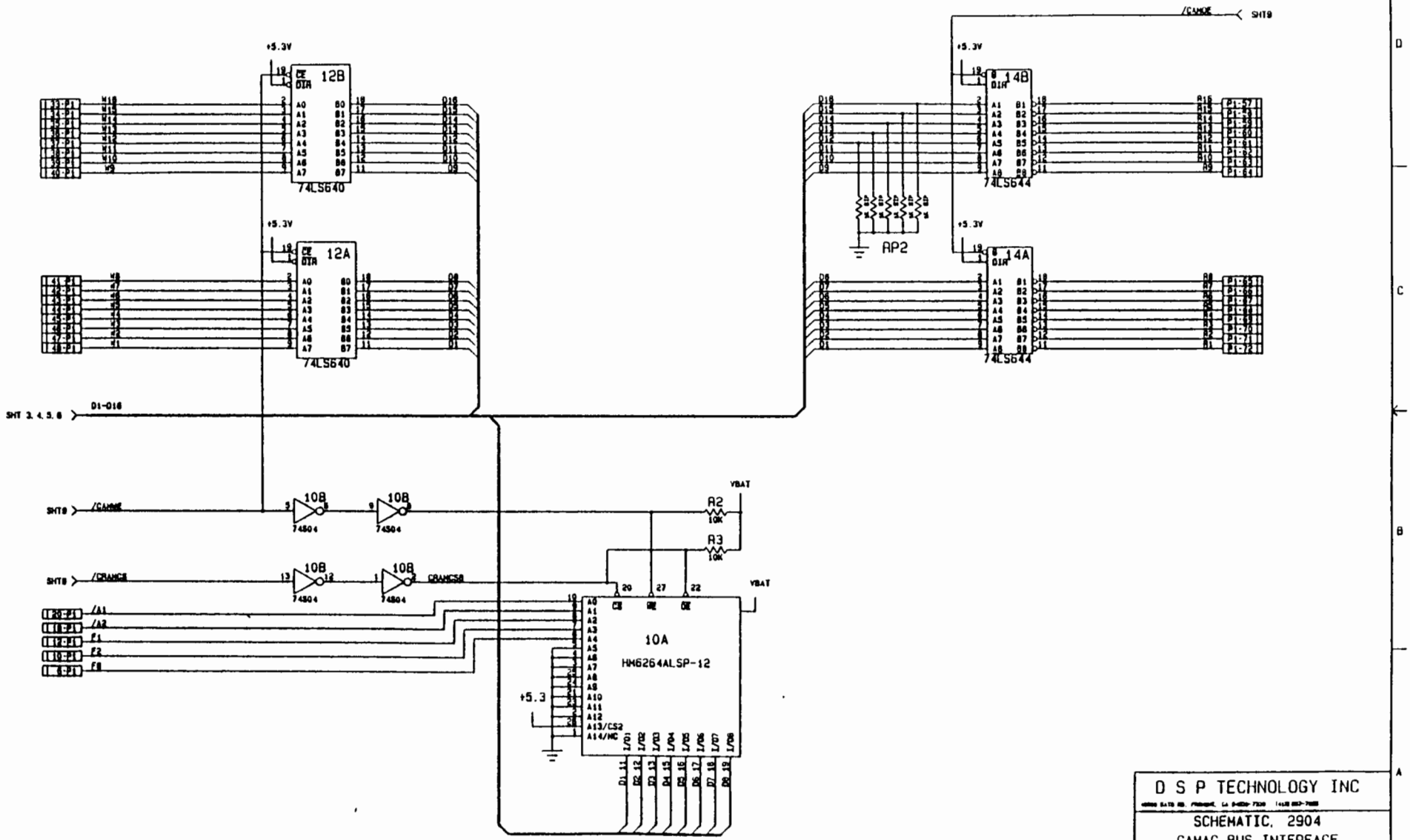
SIZE	DWG NO.	REVISION
	06 2904-01-SD	A
SCALE NONE	SHEET 6 OF 10	



D S P TECHNOLOGY INC	
SCHEMATIC, 2904	
DATA BUFFER SELECT	
2904-01-SD	A
NONE	7 OF 10


/STOREAQ
/FULL
XFRAQ
74S74
74LS74
74LS00
74LS04
74LS174
74LS221
74LS38
74LS02
7432
PAL16L8
SEL
CR2
/CSTORE
/CK20M
/INITQB
TQFSHDE
TRAQCVT
/SHISEL
/TLOSEL
/SLOSEL
/THISEL
/SRLQ
/SRHI
/TRLQ
/TRHI
BUSY
CRLQ
DACPT
TRAQDONE
/TRASSEL
/TRAQRET
/ISTART
/DAV
D S P TECHNOLOGY INC
SCHEMATIC, 2904
DATA XFER CONTROL
2904-01-SO
A
NONE


D S P TECHNOLOGY INC
SCHEMATIC, 2904
CAMAC CONTROL
2904-01-SD
A
9 OF 10
74LS139
74LS221
74LS10
74LS02
74LS00
74LS04
74LS279
74S1
PAL16L8
PAL20L10
COUNTER OFLO
TIMER OFLO
START
200nS
150nS
/CAMOE
/CAMWE
/CRAMCS
/CREAD
/CSTATS
/CSRDLO
/CSRDHI
/CTRDLO
/CTRDHI
/SPRLO
/SPRHI
/TPRLO
/TPRHI
/CTRTELO
/CTMODLO
/CSTOP
/CSTORE
CSMODELO
/CSTART
/TOFLO
/TSTART
/STARTOS
/SOFLO
/INITOS
/RSTFP
BUSY
/CPRESET
/CREAD
FXA1
FXA0



D S P TECHNOLOGY INC			
SCHEMATIC, 2904 CAMAC BUS INTERFACE			
SIZE	DWG NO. 10	2904-01-SO	REV A
SCALE NONE		SHEET 10 OF 10	

MANUAL REVISION HISTORY

DATE	BY	DESCRIPTION
11/02/87	Miller	Released
11/12/87	Miller	Corrected 64K-1 = 65535
03/10/88	Miller	Added CHANNEL READOUT section
		Miscellaneous corrections
		Updated Appendix A - Program Examples
06Jun88	Miller	Installation section
		Corrected Timebase table
30Jun88	Miller	Low/High Counter ID switch
06Jul88	Miller	Merged u2904.inc programming examples
		Reference mating connector for encoder
10Jul89	Miller	Corrected TRAQ ID select
		Encoder connector pin assignment
29Nov89	Miller	Expanded TRAQ ID Table
		Corrected installation example
15Jan90	Miller	Corrected switch labels
		Encoder connector pinout

dsp Technology Inc.

PRODUCT WARRANTY

(Excludes Software)

DSP TECHNOLOGY ("DSP") warrants its products to be free from defects in material and workmanship and to meet DSP's performance specifications. The warranty period is one year from the date of shipment to the buyer. The warranty is limited by the paragraphs below.

RETURN TO FACTORY

If a buyer discovers a defect in a DSP product covered by this agreement, buyer's exclusive remedy is to ship the product back to DSP's Fremont factory, where DSP will, at its option, either repair or replace the product. This remedy applies if DSP receives the returned product on or before the tenth day after the expiration of the warranty period and the buyer notifies DSP of the defect before returning the product.

COST TO BUYER OF REPAIRS OR REPLACEMENT

Buyer must prepay freight charges to DSP. DSP will pay standard return freight to buyer. Buyer will be charged for premium freight if that method of transport is requested by buyer. There is no other charge for repair or replacement during the warranty period.

TRANSFERRABLE WARRANTIES

In addition to the foregoing warranty, DSP also provides the buyer the transferrable warranty, if any, provided to DSP by the manufacturers of other products such as terminals and disk systems supplied by SEC as part of a total system.

LIMITATION OF WARRANTY AND LIABILITY

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