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DSP 2932

32 BIT DIGITAL INPUT MODULE

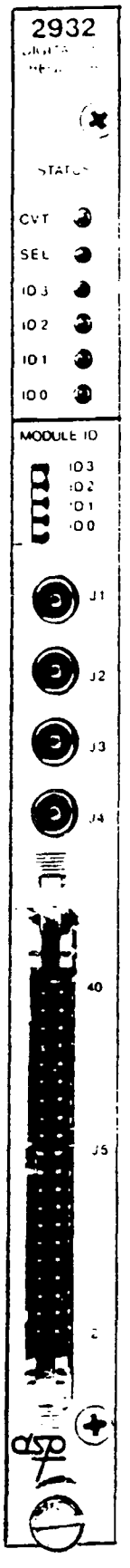
TRAQ MANUAL ADDENDUM
June 24,1986

MODEL 2932

HIGH SPEED DIGITAL INPUT MODULE

FEATURES

- 32 Bits of Input
- 4 MHz Data Rate
- Buffered - up to 32 Mbytes
- TTL Inputs
- TRAQ P Compatible

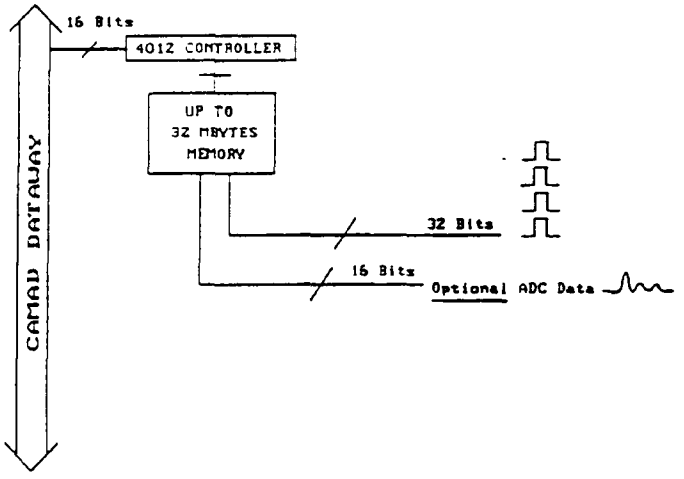


DESCRIPTION

The 2932 is a high speed digital data logging module that is part of the TRAQ P signal processing system. The 2932 is used to take digital data and store it in real time without computer supervision. The stored data can then be retrieved for computer analysis. The 2932 is system compatible with the TRAQ P A/D modules. This allows digital data taking to be synchrounous to A/D measurements. For example, the status of switch closures can be related to the analog response of a system. The 2932 can also supply digital information to the TRAQ P Real Time processor. This allows high speed processing of digital data.

APPLICATION

High speed autonomous digital data logging. Real time digital information processing.



2932 Block Diagram

ACTUAL SIZE

2932 FUNCTIONAL DESCRIPTION

INTRODUCTION

The DSP2932 is a general purpose data input module for the TRAQ Data Acquisition system. A single width module, it contains a complete TRAQ ADCBUS interface and control logic, a 40 pin header and 3 LEMO style coaxial front panel connectors all user definable, a general CAMAC read/write interface, and a voltage regulator section. The remainder of the module is available for integration of specific user designs.

TRAQ CONTROL LOGIC

All data transfer and control logic for connection of the DSP2932 to a DSP4012 series TRAQ controller is provided. Figure x.y defines the electrical interface. Physical connection to the TRAQ controller is via the rear panel 40 wire ADCBUS connector. Control signal sequencing and data timing is shown in Figure x.y.

When the 4012 START CONVERSION command is processed, the 4012 asserts RST (reset). This initializes all data input modules connected on the ADCBUS and may also be used elsewhere in the user specific section (USS) of the DSP2932.

Next the 4012 places the highest valid CHANADDR (Channel Address), corresponding to NOC-1 in the 4012, on the ADCBUS and issues a DACCPT (Data Accept) pulse. All modules latch and decode the CHANADDR on the leading edge of DACCPT. Valid decoding results in IDSEL (ID Selected) asserting. The channel selected will be the first to be read out (transferred to the 4012) when data transfers start. Note that only one module should decode a valid ID on each DACCPT.

Following the DACCPT signal, the 4012 immediately decrements the channel address, allowing the address to stabalize on the ADCBUS prior to the next DACCPT.

Each CVT (Convert Command) pulse begins an acquisition cycle for all channels within each data input module. The exact sequence is a function of the specific module. A typical process is shown in Fig x.y consisting of a signal setup or hold period, followed by conversion or decoding, and terminated with latching of the acquired data (end of conversion).

At the end of the acquisition cycle an EOC (End Of Conversion) signal must be provided to the ADCBUS control logic. When all channels within the module have asserted their EOCs, a latch clock LTCHCLK is generated, strobing the data from each channel into local latches. This sets the FULL (buffer Full) state which

in turn inhibits future loading of the latches until their contents have been emptied.

The DSP2932 supports 2 channels directly via SEL0 and SEL1 control lines. Upto 6 more channels may be added by installing the channel latches and connecting the SEL2 thru SEL7 control lines.

When the CHANADDR channel address CHB1-CHB4 match the module's ID ID3-ID0 lines, IDSEL asserts and the selected channel's data buffer is enabled (SEL0 - SEL7) onto the ADCBUS. Data Available (DAV) is then asserted, signaling the attached TRAQ controller that valid data is available. The controller acknowledges with DACPT.

DACPT inturn updates CHANADDR and the DAV/DACPT sequence repeats until all channels within the module are transferred. This sequence continues until all modules have been accessed.

In response to transferring the final channel (Channel 0), the TRAQ controller returns DONE. This is used to reset the Buffer FULL state, permitting the channel buffers to be updated on the next cycle.

As shown in Fig x.y, the CVT command, and hence the data acquisition/conversion cycle, may overlap the data transfer process. This allows a data sample to be formed/decoded concurrent with data transfer of the previous sample. The fundamental constraint is that the time required for data transfer of all channels must be no longer than the time between CVT commands.

SIGNAL DEFINITIONS

NAME	SOURCE	DESCRIPTION
CVT	4012	Controller Convert clock. Initiates a conversion cycle.
MARK	2932	Indicates receipt of a CVT command.
GETSET	2932	Pulse on leading edge of MARK. Duration adjustable via R8. May be used as a HOLD or data setup control.
GO	2932	Asserts on trailing edge of GETSET. Cleared by FINI. May be used to initiate data conversion and/or as internal BUSY status.
EOC1	User	End Of Conversion Channel 1 and Channel 2. Indicates data conversion complete and data ready for transfer into 2932 data latch.
FINI	2932	Pulse formed when EOC1 and EOC2 asserted and FULL condition NOT set. Used to reset GO and strobe data into latches.
FULL	2932	Indicates data latches have valid data. Set on FINI and reset when all data transfered to 4012.
DAV	2932	Data Available asserts when selected module has data available for transfer.
DACPT	4012	Indicates completion of a single channel data transfer from 2932 to 4012 controller.
DONE	4012	Indicates completion of all channel data transfers to 4012 for a single conversion cycle.
RESET	4012	System Reset command.
CH0 - CH7	4012	Channel Address. Selects channel to be accessed for next data transfer. Latched and decoded on leading edge of DACPT.
SEL0 - SEL7	2932	Decoded channel address to select internal data latches during readout.

SIGNAL	SOURCE	DESCRIPTION
U1D1-U1D16	USER	Channel 1 Data Latch input bus. D1=LSB D16=MSB.
U2D1-U2D16	USER	Channel 2 Data latch input bus.
LD1 - LD16	2932	Internal Data bus from Channel Latch to ADCBUS. Contains data from currently selected (SEL0-SEL7) latch.
D1 - D16	2932	TRAQ ADCBUS data. Contains data from currently selected module and channel.

DSP2932 FRONT PANEL DESCRIPTION

The DSP2932 front panel consists of a Module ID selection section and 5 general purpose connectors.

Module ID selection is described in Section x.y of the TRAQ System Manual.

Connector	Type	Use
J1	LEMO RA0.25	user defined
J2	LEMO RA0.25	user defined
J3	LEMO RA0.25	user defined
J4	LEMO RA0.25	user defined
J5	40PIN IDC	Option 1 - Channel 1&2 Data Input

OPTIONS

1. DIGITAL INPUT BUFFER INTERFACE

The digital input buffer option provides two (2) standard digital input channels at the front panel J5 connector. Handshake control lines are provided for synchronization with external devices.

Each channel consists of 16 Data lines, CHx-16 thru CHx-1, where x indicates the channel number (1 or 2). CHx-16 is the Most Significant Bit (MSB). All data lines are TTL compatible and each appear as one (1) TTL load to the external device.

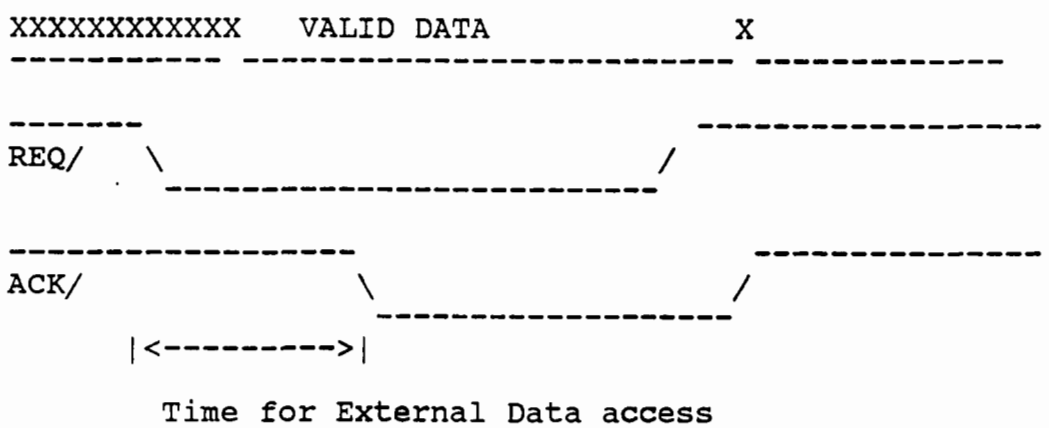
Handshake control is provided by CHx-REQ/ and CHx-ACK/ lines which are TTL LOW when asserted.

CHx-REQ/ indicates that the TRAQ system is requesting a "conversion cycle". This may be used as a data request to the external data source. It is generated by the DSP2932 on receipt of a CVT command from the DSP4012. Refer to the DSP2932 functional description for details.

CHx-ACK/ must be returned by the external data source when data is available on the channel's data lines CHx-[1..16]. It is used within the DSP2932 to form an End of Conversion (EOCx) signal. At that time CHx-REQ/ will be released. It is important to note that EOC is generated, and hence REQ/ released, only when BOTH channel's have asserted ACK/.

The data appearing on the lines CHx-[1..16] will be latched into the DSP2932 at the same time as REQ/ is released.

A typical timing sequence is shown below:



Time for External Data access

The time from assertion of REQ/ and receipt of ACK/ in most cases will be determined by the user's data source. The maximum time allowed is a function of the TRAQ CONVERSION Clock rate selected. An ACK/ must be received before the next CNVT clock to avoid data loss. For example, with a TRAQ sampling rate of 100KHz, a CNVT clock will be generated every 10 microseconds. Thus the maximum delay from REQ/ to ACK/ would be 10 uSec.

The minimum response time must be such to guarantee valid data at the DSP2932 J5 input when REQ/ is released. The cable length and drive capability of the data source must be taken into account.

If one of the 2 channels is not being used, the associated CHx-REQ/ line should be connected directly back to CHx-ACK/. For example, if Channel 2 is not required, tie CH2-REQ/ to CH2-ACK/, and set the TRAQ controller Number of Channels (NOC) parameter to one (1). Note that the Channel 2 REQ/ to ACK/ connection IS REQUIRED even though the controller NOC is set to 1 channel.

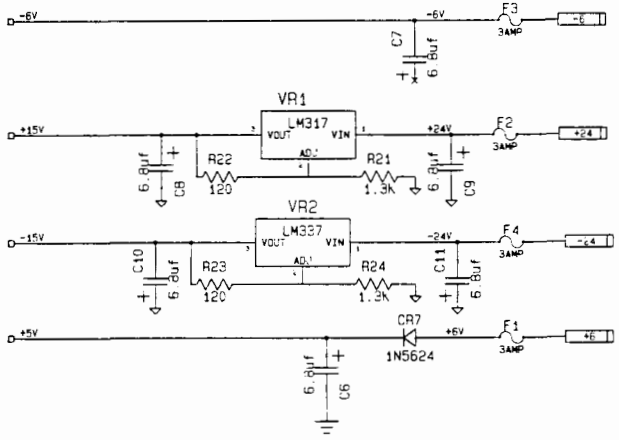
DIGITAL INPUT BUFFER OPTION

J5 PIN	SIGNAL		SOURCE
01	GROUND		
02	GROUND		
03	CH1-01	CHANNEL 1-DATA 01 (LSB)	EXTERNAL
04	CH1-02		EXTERNAL
05	CH1-03		EXTERNAL
06	CH1-04		
07	CH1-05		EXTERNAL
08	CH1-06		EXTERNAL
09	CH1-07		
10	CH1-08		
11	CH1-09		
12	CH1-10		
13	CH1-11		
14	CH1-12		
15	CH1-13		
16	CH1-14		
17	CH1-15		
18	CH1-16	CHANNEL 1-DATA 16 (MSB)	EXTERNAL
19	CH1-ACK/	CHANNEL 1 DATA ACKNOWLEDGE	EXTERNAL
20	CH1-REQ/	CHANNEL 1 DATA REQUEST	2932
21	GROUND		
22	GROUND		
23	CH2-01	CHANNEL 2-DATA 01 (LSB)	EXTERNAL
24	CH2-02		EXTERNAL
25	CH2-03		
26	CH2-04		
27	CH2-05		
28	CH2-06		
29	CH2-07		
30	CH2-08		
31	CH2-09		
32	CH2-10		
33	CH2-11		
34	CH2-12		
35	CH2-13		
36	CH2-14		
37	CH2-15		
38	CH2-16	CHANNEL 2-DATA 16 (MSB)	EXTERNAL
39	CH2-ACK/	CHANNEL 2 ACKNOWLEDGE	EXTERNAL
40	CH2-REQ/	CHANNEL 2 DATA REQUEST	2932

NOTE: J5 PIN IS LOWER-RIGHT AS VIEWED FROM FRONT OF DSP2932.

SYMBOLS

- CAMAC EDGE CONNECTOR
- EXTERNAL CONNECTOR
- CONTINUE ON SAME SHEET
- CONTINUE ON DIFFERENT SHEET
- UNUSED PIN
- JUMPERS
- OPTIONAL JUMPERS



NOTES (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE 1/4W 5%
2. ALL CAPACITORS ARE IN uf.
3. TIMING "T" AT 2E[13] IS ADJUSTED BY USING APPROPRIATE COMPONENTS FOR "C4" AND "R9". TIMING SHOULD BE GREATER THAN 2us OR GREATER THAN "ADC" CONVERSION TIME - WHICHEVER IS GREATER
4. ⏚ DENOTES ANALOG GROUND.
   ⏚ DENOTES DIGITAL GROUND.

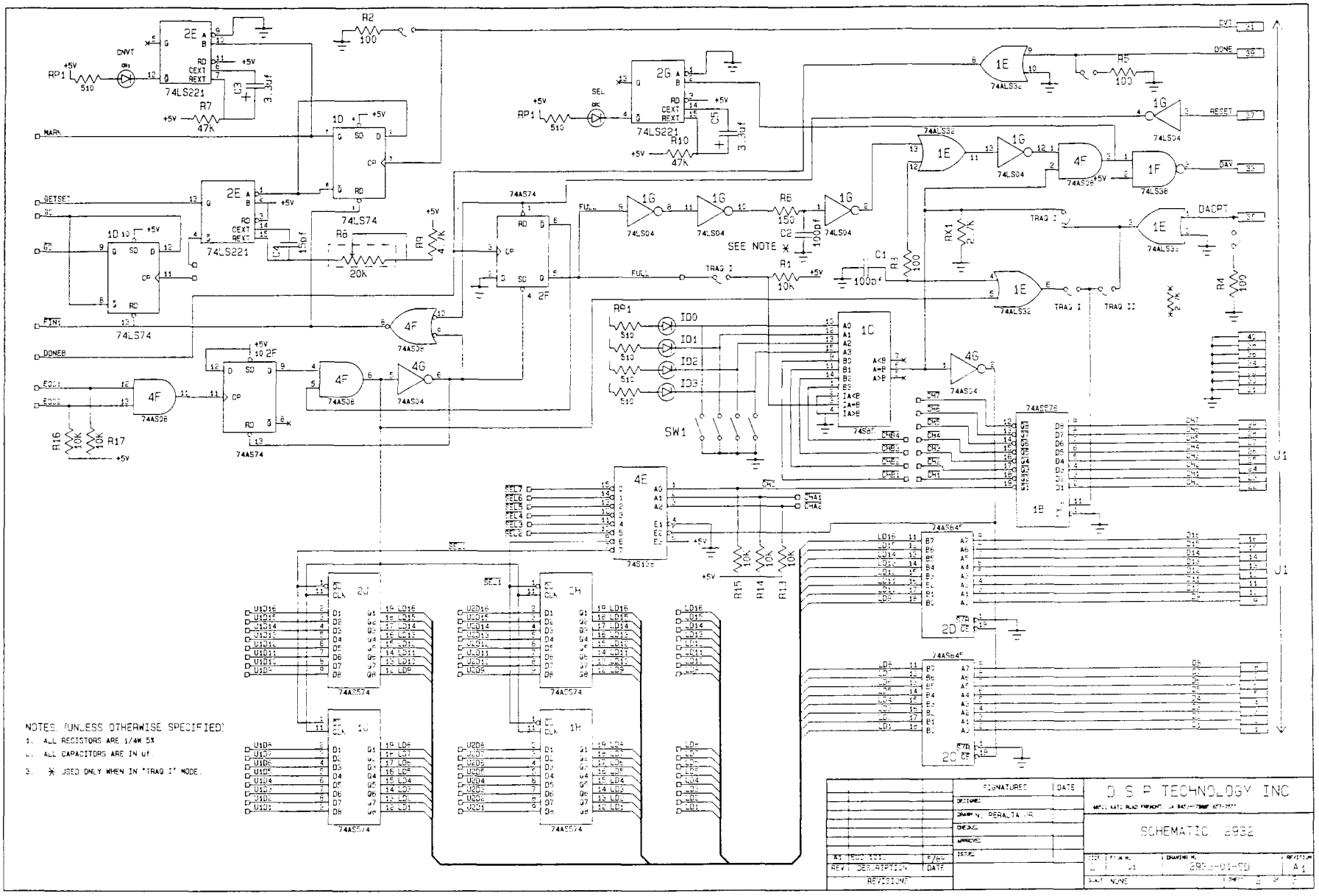
REV	DESCRIPTION	DATE
	REVISIONS	
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A	ECO 1044, 1059	6/87
	PROD RELEASE	

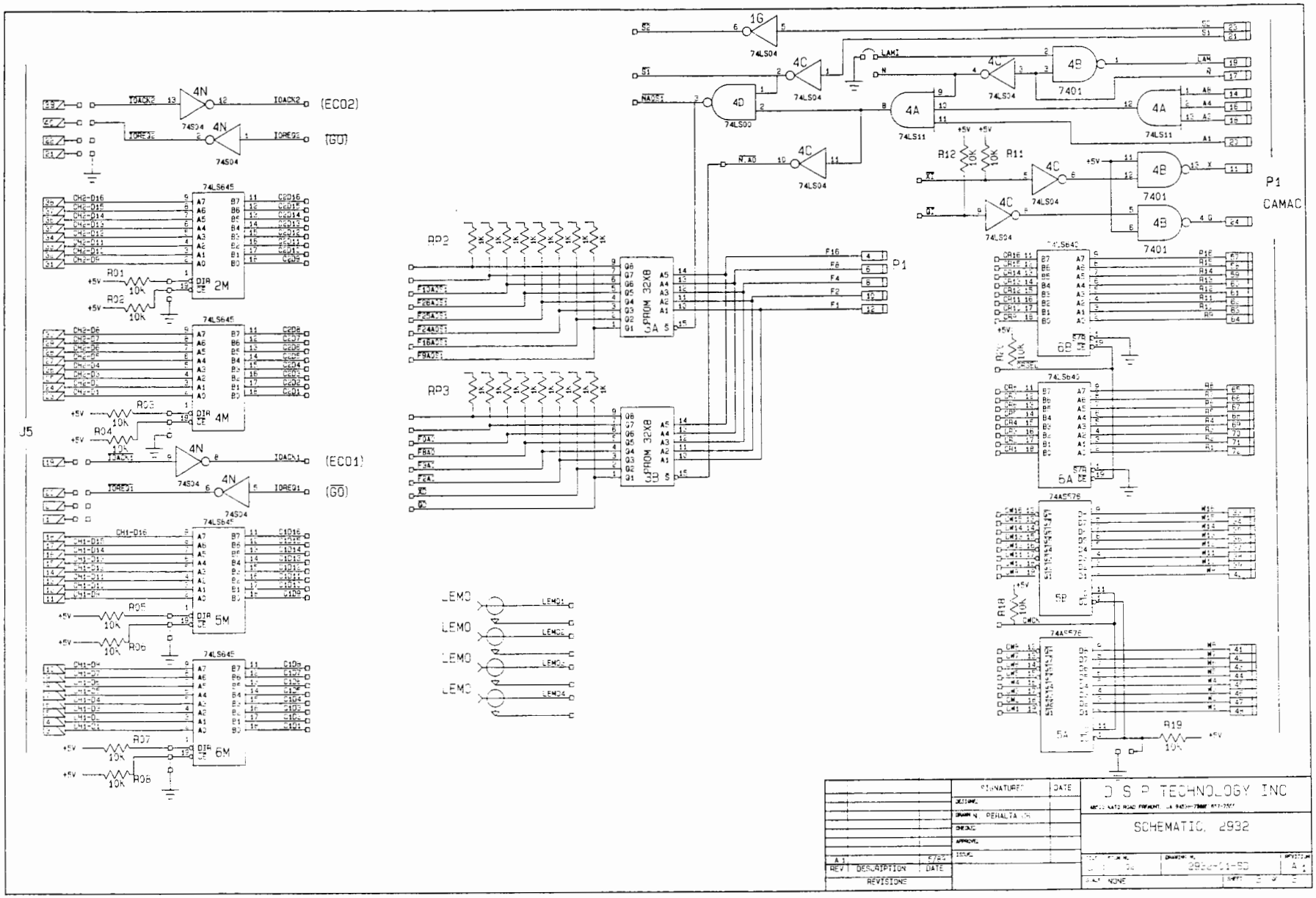
SIGNATURES	DATE
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ISSUED	

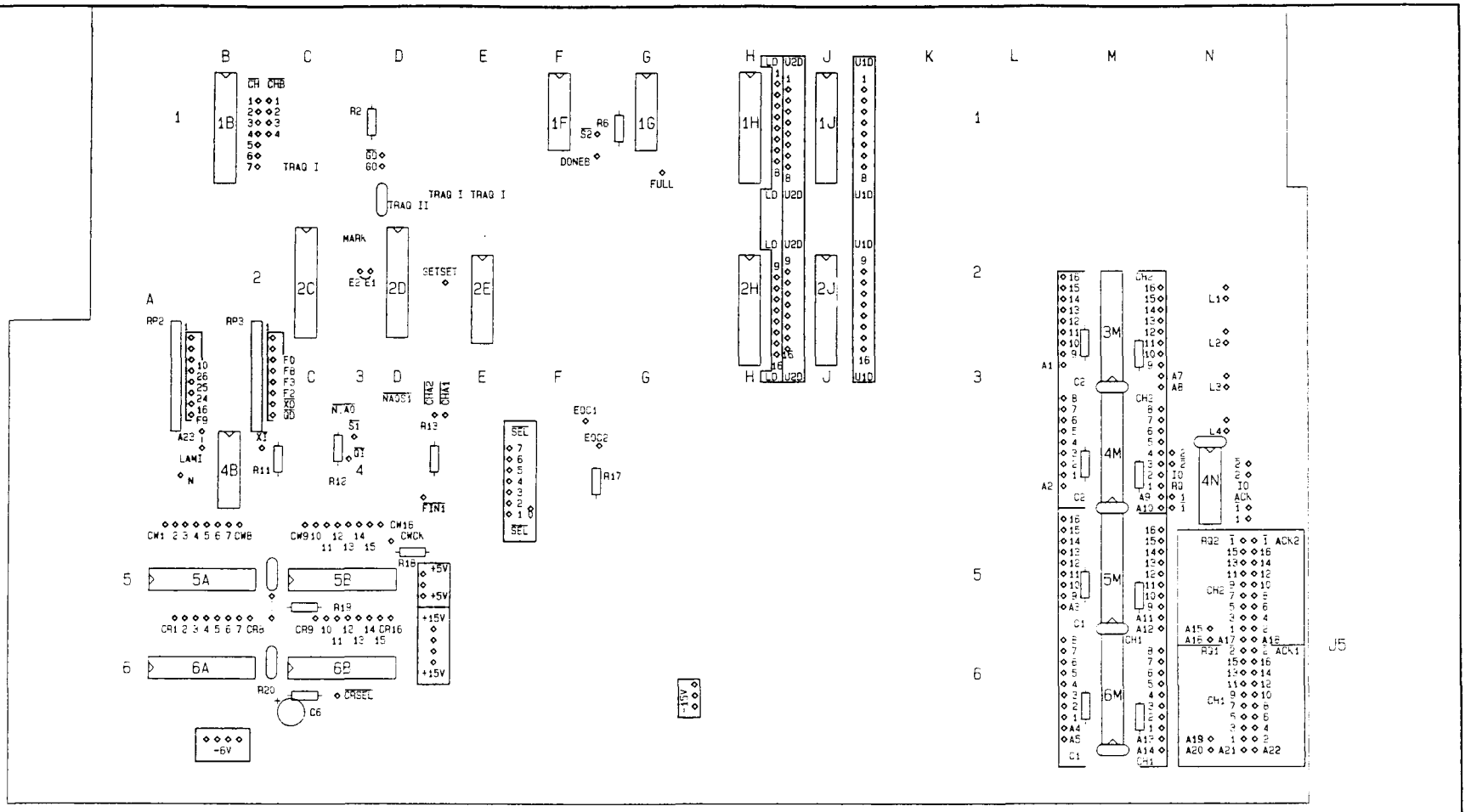
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SCHEMATIC, 2932

SIZE C | DRAWING NO. 2932-01-SD | REVISION A1 | SCALE NONE | SHEET 1 OF 2


NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTORS ARE 1/4W 5%
2. ALL CAPACITORS ARE IN uf.
3. * USED ONLY WHEN IN "TRAQ I" MODE.
SEE NOTE *
SW1
ID0
ID1
ID2
ID3
CNVT
GETSET
MARK
DONEB
FIN1
FULL
TRAQ I
TRAQ II
DACPT
CVT
DONE
RESET
DAV
D S P TECHNOLOGY INC
SCHEMATIC 2832
SIGNATURES
DATE
DRAWN
CHECKED
APPROVED
SIZE
SCALE NONE
REVISIONS
REV
DESCRIPTION


J5
P1
CAMAC
(EC02)
(GO)
(EC01)
(GO)
74LS645
74LS04
74LS00
74LS11
7401
74LS640
74AS676
32X8
PROM
LEMO
LEMO1
LEMO2
LEMO3
LEMO4
R01
R02
R03
R04
R05
R06
R07
R08
R09
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
10K
1K
2M
4M
5M
6M
5A
5B
6A
6B
DSP TECHNOLOGY INC
SCHEMATIC, 2932
2932-01-BD
SIGNATURE
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DESIGNED
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N. PERALTA
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APPROVED
ISSUED
REVISIONE
REVI
DESCRIPTION
DATE
NONE



ECO	REV	DESCRIPTION	DATE	APPROVED	
	A1	ECO 1008, 1014	5/18/94	MC	

REVISIONS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
2 PL DECIMALS +/-
3 PL DECIMALS +/-
ANGLES +/-
FRACTIONS +/-

SIGNATURES	DATE
DRAWN	
CHECKED	
APPROVED	
ISSUED	
NEXT ASSEMBLY	

D S P TECHNOLOGY INC
48500 KATO ROAD FREMONT, CA 94538-7338

WIRING LIST, 2932

SIZE	DRAWING NO.	REV
B	2932-01-WL	A1

SCALE FULL SHEET 1 OF 2

FROM				TO		
NO.	AWG	CONN	PIN	CONN	PIN	SIGNAL NAME
1	30	J5	CH1- 2	6M	2	CH1- 1 (LSB)
2	30	J5	CH1- 1	6M	3	CH1- 2
3	30	J5	CH1- 4	6M	4	CH1- 3
4	30	J5	CH1- 3	6M	5	CH1- 4
5	30	J5	CH1- 6	6M	6	CH1- 5
6	30	J5	CH1- 5	6M	7	CH1- 6
7	30	J5	CH1- 8	6M	8	CH1- 7
8	30	J5	CH1- 7	6M	9	CH1- 8
9	30	J5	CH1- 10	5M	2	CH1- 9
10	30	J5	CH1- 9	5M	3	CH1- 10
11	30	J5	CH1- 12	5M	4	CH1- 11
12	30	J5	CH1- 11	5M	5	CH1- 12
13	30	J5	CH1- 14	5M	6	CH1- 13
14	30	J5	CH1- 13	5M	7	CH1- 14
15	30	J5	CH1- 16	5M	8	CH1- 15
16	30	J5	CH1- 15	5M	9	CH1- 16 (MSB)
17	30	J5	A22		A20	GND
18	30	J5	RQ1	4N	6	REQ CH1
19	30	J5	ACK1	4N	9	ACK CH1
20	30	J5	A18		A16	GND
21	30	J5	RQ2	4N	3	REQ CH2
22	30	J5	ACK2	4N	13	ACK CH2
23	30	6M	19		A14	GND
24	30	6M	18	1N	9	U1D- 1
25	30	6M	17	1N	8	U1D- 2
26	30	6M	16	1N	7	U1D- 3
27	30	6M	15	1N	6	U1D- 4
28	30	6M	14	1N	5	U1D- 5
29	30	6M	13	1N	4	U1D- 6
30	30	6M	12	1N	3	U1D- 7
31	30	6M	11	1N	2	U1D- 8
32	30	5M	19		A16	GND
33	30	5M	18	2N	9	U1D- 9
34	30	5M	17	2N	8	U1D- 10
35	30	5M	16	2N	7	U1D- 11
36	30	5M	15	2N	6	U1D- 12
37	30	5M	14	2N	5	U1D- 13
38	30	5M	13	2N	4	U1D- 14
39	30	5M	12	2N	3	U1D- 15
40	30	5M	11	2N	2	U1D- 16
41	30	J5	CH2- 2	4M	6	CH2- 1 (LSB)
42	30	J5	CH2- 1	4M	2	CH2- 2
43	30	J5	CH2- 4	4M	4	CH2- 3
44	30	J5	CH2- 3	4M	5	CH2- 4
45	30	J5	CH2- 6	4M	6	CH2- 5
46	30	J5	CH2- 5	4M	7	CH2- 6
47	30	J5	CH2- 8	4M	8	CH2- 7
48	30	J5	CH2- 7	4M	9	CH2- 8
49	30	J5	CH2- 10	3M	2	CH2- 9
50	30	J5	CH2- 9	3M	3	CH2- 10

FROM				TO		
NO.	AWG	CONN	PIN	CONN	PIN	SIGNAL NAME
51	30	J5	CH2- 12	3M	4	CH2- 11
52	30	J5	CH2- 11	3M	5	CH2- 12
53	30	J5	CH2- 14	3M	6	CH2- 13
54	30	J5	CH2- 13	3M	7	CH2- 14
55	30	J5	CH2- 16	3M	8	CH2- 15
56	30	J5	CH2- 15	3M	9	CH2- 16 (MSB)
57	30	4M	19		A10	GND
58	30	3M	19		A8	GND
59	30	4M	18	1H	9	U2D- 1
60	30	4M	17	1H	8	U2D- 2
61	30	4M	16	1H	7	U2D- 3
62	30	4M	15	1H	6	U2D- 4
63	30	4M	14	1H	5	U2D- 5
64	30	4M	13	1H	4	U2D- 6
65	30	4M	12	1H	3	U2D- 7
66	30	4M	11	1H	2	U2D- 8
67	30	3M	18	2H	9	U2D- 9
68	30	3M	17	2H	8	U2D- 10
69	30	3M	16	2H	7	U2D- 11
70	30	3M	15	2H	6	U2D- 12
71	30	3M	14	2H	5	U2D- 13
72	30	3M	13	2H	4	U2D- 14
73	30	3M	12	2H	3	U2D- 15
74	30	3M	11	2H	2	U2D- 16
75	30	3M		4N	1	
76	30	4N	1	4N	5	
77	30	4N	8		EOC1	
78	30	4N	12		EOL2	
79	30	4B	LAMP		A23	
80	30	CH	1	CH B	1	
81	30	CH	2	CH B	2	
82	30	CH	3	CH B	3	
83	30	CH	4	CH B	4	
84	30	E1		E2		
85	30	J5	A 21		A19	GND
86	30	J5	A 17		A15	GND

ECO	REV	DESCRIPTION	DATE	APPROVED
	A	ECO 1006, 1014	5/89	

REVISIONS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
2 PL DECIMALS +/-
3 PL DECIMALS +/-
ANGLES +/-
FRACTIONS +/-

SIGNATURES	DATE
DRAWN	
CHECKED	
APPROVED	
ISSUED	

NEXT ASSEMBLY

D S P TECHNOLOGY INC
48500 KATO ROAD FREMONT, CA 94538-7338

WIRING LIST
2932

SIZE	DRAWING NO.	REV.
B	2932-01-WL	A 1

SCALE FULL | SHEET 2 OF 2

[redacted] Technology Inc. [redacted]

SINGLE LEVEL BILL OF MATERIAL REPORT

Assembly: A-2932-01 (ASY 2932: DIGITAL I/O PCB ASSY) Date: 01/29/90

Revision: A Page: 1

As of: 01/20/90

	Component	Description	Qty Per	As of	Until	Reference
1.	0100-0101	RES: RC07 100 OHM	4.00	03/13/86	12/31/99	R2-R5
2.	0100-0103	RES: RC07 10K OHM	19.00	05/20/87	12/31/99	R1, R11-R20, R01-R08
3.	0100-0121	RES 5% 1/4W CC RESISTOR R=120	2.00	03/13/86	12/31/99	R22 R23
4.	0100-0122	RES: 1/4W, 5%, R=1.2K	1.00	01/24/87	12/31/99	R9
5.	0100-0132	RES 5% 1/4W CC RESISTOR R=1.3K	2.00	03/13/86	12/31/99	R21 R24
6.	0100-0151	RES 5% 1/4W CC RESISTOR R=150	1.00	03/13/86	12/31/99	R6
7.	0100-0272	RES 5% 1/4W CC RESISTOR R=2.7K	1.00	01/24/87	12/31/99	RX1
8.	0100-0473	RES CF, 5% 1/4W R=47K	2.00	03/13/86	12/31/99	R7 R10
9.	0200-0511	RPK RES PK BNS 4308R-101-511	1.00	03/13/86	12/31/99	RP1
10.	0201-0102	RPK RES PK BNS 4310R-101-102	2.00	03/13/86	12/31/99	RP2 RP3
11.	0350-0203	RES:VAR. 1/4SQ BRNS RJ26FW203 R=20K	1.00	03/13/86	12/31/99	R8
12.	0500-0101	CSM C=100PF CDE # CD5FC101J03	1.00	03/13/86	12/31/99	C1
13.	0500-0102	CSM C=1000PF 5% AREO DM15-102J03	1.00	01/24/87	12/31/99	C4
14.	0520-0104	CMC 0.1UF CNTLB:CZ20A104M2 KEM:C322	22.00	05/20/87	12/31/99	
15.	0600-0335	CTE C=3.3UF TANT KEMET T362B335K03	2.00	03/13/86	12/31/99	C3 C5
16.	0600-0685	CTE C=6.8UF TANT 35WVDC KEMET T361B	6.00	03/13/86	12/31/99	C6-C11
17.	1030-5624	DSR: DIODE RECT 3A GE IN5624/BYM56	1.00	03/13/86	12/31/99	CR7
18.	111001	CONN: PIN, AUTOSW W228-025-400Q	291.00	07/03/86	12/31/99	
19.	1750-0001	ICS SN7401	1.00	08/19/87	12/31/99	4B
20.	1760-0000	ICS SN74LS00	1.00	08/19/87	12/31/99	4D
21.	1760-0004	ICS SN74LS04	2.00	08/19/87	12/31/99	4C, 1G
22.	1760-0011	ICS SN74LS11	1.00	08/19/87	12/31/99	4A
23.	1760-0038	ICS SN74LS38	1.00	03/13/86	12/31/99	1F
24.	1760-0074	ICS SN74LS74	1.00	03/13/86	12/31/99	1D
25.	1760-0221	ICS SN74LS221	2.00	03/13/86	12/31/99	2E 2G
26.	1760-0640	ICS SN74LS640	2.00	08/19/87	12/31/99	6A, 6B
27.	1760-0645	ICS SN74LS645	4.00	05/20/87	12/31/99	2M, 4M, 5M, 6M
28.	1762-0032	ICS 74ALS32 QUAD 2IN OR	1.00	03/13/86	12/31/99	1E
29.	1762-0574	ICS SN74ALS574	4.00	11/05/86	12/31/99	1H 2H 1J 2J
30.	1770-0004	ICS IC LSTTL HEX INV SN74S04	1.00	03/13/86	12/31/99	4N
31.	1770-0085	ICD 74S85 4BIT COMPARATOR	1.00	03/13/86	12/31/99	1C
32.	1770-0138	ICS SN74S138	1.00	03/13/86	12/31/99	4E
33.	1772-0004	ICD 74AS04	1.00	03/13/86	12/31/99	4G
34.	1772-0008	ICD 74AS08	1.00	03/13/86	12/31/99	4F
35.	1772-0074	ICD 74AS74	1.00	03/13/86	12/31/99	2F
36.	1772-0576	ICD 74AS576 OCTAL DFF INVERTING	3.00	08/19/87	12/31/99	1B, 5A, 5B
37.	1772-0645	ICD 74AS645 OCTAL XCVR 3-S	2.00	03/13/86	12/31/99	2C 2D
38.	1851-0044	PRM PROM M/F 1850-0001 2932-01 3A	1.00	08/19/87	12/31/99	3A
39.	1851-0045	PRM PROM M/F 1850-0001 2932-01 3B	1.00	08/19/87	12/31/99	3B
40.	2030-0317	ICS IC VOL REG NAT LM317T	1.00	03/13/86	12/31/99	VR1
41.	2030-0337	IC: VOLT REG, NEG ADJ, LM337T	1.00	03/13/86	12/31/99	VR2
42.	3100-0302	FUSE 3AMP LITTLEFUSE 251003	4.00	03/13/86	12/31/99	F1-F4
43.	5000-0014	SKT CAMBION 703-1314-01-04-10	12.00	03/13/86	12/31/99	1D-1G 2F 4A-4D 4F 4G 4N
44.	5000-0016	SKT CAMBION 703-1316-01-04-10	6.00	03/13/86	12/31/99	1C 2E 2G 3A 3B 4E
45.	5000-0020	SKT CAMBION 703-1320-01-04-10	15.00	05/20/87	12/31/99	1B, 1H, 1J, 2C, 2D, 2H, 2J 5A, 5B, 6A, 6B, 2M, 4M, 5M 6M
46.	5250-3703	JCK FUS CAMBION 450-3703-01-06-00	22.00	04/17/86	12/31/99	

Component	Description	Qty Per	As of	Until	Reference

Assembly: A-2932-01 (ASY 2932: DIGITAL I/O PCB ASSY)

SINGLE LEVEL BILL OF MATERIAL REPORT

Assembly: A-2932-01 (ASY 2932: DIGITAL I/O PCB ASSY)
Revision: A
As of: 01/20/90

	Component	Description	Qty Per	As of	Until	Reference
47.	5251-0001	JMP CAMBION 461-2251-01-03-10	1.00	05/20/87	12/31/99	TRAQ II
48.	5400-0023	CON 2 POS JUMPER APTRONICS 929955-0	5.00	04/17/86	12/31/99	
49.	5500-0004	HDR 40 PIN 3M 3432-1303	1.00	08/19/87	12/31/99	J5
50.	5500-0018	HDR 40 PIN R/A 4 WALL 3M#3595-5002	1.00	04/17/86	12/31/99	J1
51.	5510-0004	CON RT ANGLE LEMO RPL00.250TEF	4.00	03/13/86	12/31/99	P11-P14
52.	6000-0003	STC 4 POS DIP SWT AMP 435802-3	1.00	03/13/86	12/31/99	SW1
53.	6849-0002	INS BERGQUIST 3223-07 FR 54	2.00	04/17/86	12/31/99	VR1 VR2
54.	6850-0001	RAIL: GUIDE, MDL, 5 HOLE, C-BORE	2.00	03/13/86	12/31/99	
55.	7000-0052	PCB DWG# 2932-01-FD	1.00	03/13/86	12/31/99	
56.	7410-0003	HWD: SWAGE TYPE STANDOFF	6.00	05/20/87	12/31/99	
57.	DOCUMENTATION	PER ASSY DWG REFERENCE	2.00	04/20/87	12/31/99	2932-01 AD 2932-01 CD

dsp technology inc.

PRODUCT WARRANTY

(Excludes Software)

DSP TECHNOLOGY ("DSP") warrants its products to be free from defects in material and workmanship and to meet DSP's performance specifications. The warranty period is one year from the date of shipment to the buyer. The warranty is limited by the paragraphs below.

RETURN TO FACTORY

If a buyer discovers a defect in a DSP product covered by this agreement, buyer's exclusive remedy is to ship the product back to DSP's Fremont factory, where DSP will, at its option, either repair or replace the product. This remedy applies if DSP receives the returned product on or before the tenth day after the expiration of the warranty period and the buyer notifies DSP of the defect before returning the product.

COST TO BUYER OF REPAIRS OR REPLACEMENT

Buyer must prepay freight charges to DSP. DSP will pay standard return freight to buyer. Buyer will be charged for premium freight if that method of transport is requested by buyer. There is no other charge for repair or replacement during the warranty period.

TRANSFERRABLE WARRANTIES

In addition to the foregoing warranty, DSP also provides the buyer the transferrable warranty, if any, provided to DSP by the manufacturers of other products such as terminals and disk systems supplied by SEC as part of a total system.

LIMITATION OF WARRANTY AND LIABILITY

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