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PR-604

Dual 24-Bit Parallel Input Register

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Phone: 415-657-7555; Telex: 283608

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Diagram Connector Wiring 31-Pin Cannon Drawing No. 106281, Rev. D

Diagram Connector Wiring 52-Pin Cannon Drawing No. 106327

Assembly Wire Harness PR-604/K Drawing No. 105129, Rev. F

Assembly PCB PR-604 Drawing No. 105079, Rev. C5

PR-604 Manual Revision Record

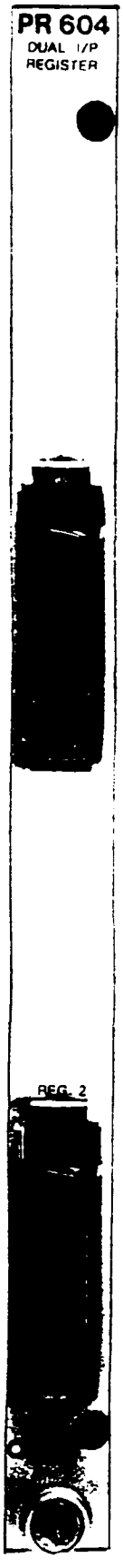
DSP Warranty

MODELS PR-604 & PR-604K

DUAL 24 BIT PARALLEL INPUT REGISTER

FEATURES

- Dual 24 Bit Parallel Input Register
- Latched, Strobed and Continuous Data Entry Operating Modes
- TTL Levels
- Choice of Front or Rear Connectors



ACTUAL SIZE

DESCRIPTION

This module contains the necessary input circuitry, bistable latches, and control logic for paralleling two sets of 24 bits of data onto the Dataway. All inputs accept standard TTL levels. Data inputs may be latched into registers or read directly onto the Dataway lines. Outputs from digital instruments such as DVMs, position encoders and counters are typical applications of the PR-604 registers.

These parallel input registers may be set to three modes of operation: Continuous (register follows inputs); Strobed (external strobe at "Load Data" inputs); and Single Strobe Data Entry (registers must be reset by CAMAC control). The operation mode is set for each of the two 24 bit registers by one of two toggle switches located in the module.

The PR-604 Parallel Input Register is a single-width CAMAC module with data entry through front (PR-604) or rear (PR-604K) mounted subminiature connectors.

APPLICATIONS

Holds and transfers up to 48 bits of data to the CAMAC Dataway.

OPERATION MODES

Single Strobe Data Entry (latched): The first positive "Load Data" input sets the "Data Ready" flag, and latches the parallel information into the register. Further strobes are then inhibited until after a proper CAMAC command. This mode is set by placing the toggle switch to the "L" position.

Strobed Data Entry (Strobe): Upon any positive level strobe to the "Load Data" input, the data applied at the data inputs at that instant will be locked into the appropriate register. This mode is set by placing the toggle switch to the "S" position.

Continuous Data Entry: By shunting the "Load Data" input with less than 100 Ohms to ground, the data applied at the inputs will be continually available to the Dataway gates. The toggle switch must be set to the "S" position for continuous mode.

The single Strobe Data Entry and the Strobe Data Entry Modes set "Data Ready" flag. "Data Ready" generates a LAM if the LAM has been enabled.

The "Data Ready" flag is available at the input connector to control external devices.

SPECIFICATIONS

INPUTS

TTL, 1 standard load
Strobe Width 50 nsec.

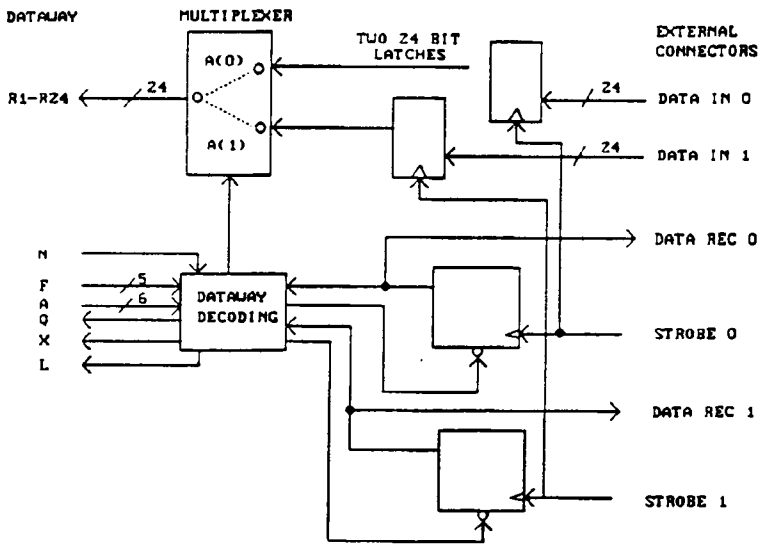
MATING CONNECTORS

Front panel connectors (model PR-604) are two double density 31 pin Cannon 2DA-31P. Mating connectors are not included. Order PN 70501/76006/70524. Two per module.

Rear panel connector (Model PR-604K) is one double density 52 pin Cannon 2DA-52P. Mating connector is not included. Order PN 70503/76005/70524.

COMPUTER COMMANDS

F(0)A(i): Read gate input, Reset LAM and Data Received Registers at S2, Q = 1
F(8)A(i): Test gate 1 or 2 LAM, Q = LAM
F(10)A(i): Reset gate 1 or 2 LAM Flip-Flop, Q = LAM
F(24)A(i): Disable gate 1 or 2 LAM, Q = 0
F(26)A(i): Enable gate 1 or 2 LAM, Q = 0, i = 0 or 1



PR-604 Block Diagram

PR-604 THEORY OF OPERATION

6/3/82

The PR-604 is designed for negative logic and all signals noted use this convention ("0" state > 3.5V; "1" state < .6V). All OR gates perform the logical AND function and all AND gates perform the logical OR function.

DATAWAY INPUTS

The F lines are inverted by U37 and decoded by U35 and U36 both of these decoders are enabled directly with the N line. The decoders are also selectively enabled by the state of the F16 line. U35 supplies function codes $F_{(0)}N...F_{(15)}N$.

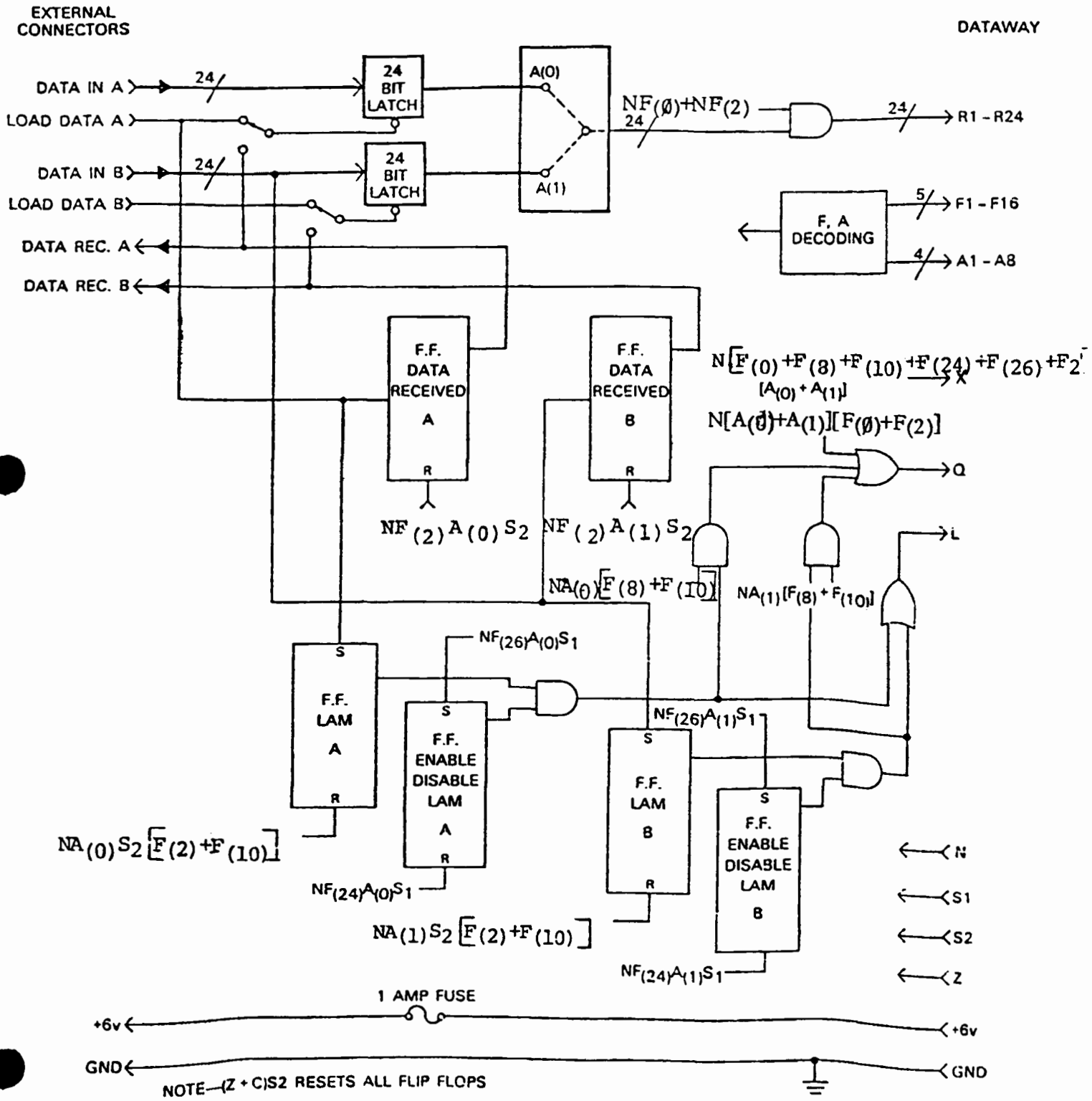
The A lines are decoded by U34. Signals A1, A2, and A4 enter U24 directly, while A8 is inverted by U37 pin 6 and acts as an enable line for U34.

The S1 line is bufferred by U7 pins 10 and 8 and the S2 line is bufferred by U11 pin 2. The C and Z lines are gated by U32 pin 11 to obtain C + Z.

DATA RECEIVED

The DATA RECEIVED FF(U8) is clocked from the enternal LOAD DATA input. This will indicate to external devices that the input data is latched into the holding registers. At time $NF_{(2)}S_2+S_2(C+Z)$, the FF is reset.

DUAL 24 BIT
PARALLEL INPUT REGISTER
PR-604
BLOCK DIAGRAM



DATA INPUT REGISTERS AND READ LINES

As the circuitry is similar for all inputs, only the first bit will be discussed.

The data input line has a 1K pull up resistor to V_{CC} and is fed to latch register U1. These registers are a dual 4 bit latch, with the latch mode control by one of three means:

1. SINGLE STROBE DATA ENTRY (LATCHED)

   A positive pulse through resistor R50 to inverter U7 triggers U8 data received flip flop. Resistor R50 and capacitor C1 is for integrating the input signal to remove spurious noise impulses. With S1 in the latched (L) position, the data received flip flop will latch the parallel information into registers U1 through U6. Further strobes are then inhibited until a proper CAMAC command $NF(2)A(0)A(1)S_2$ resets the data received flip flop.

2. STROBED DATA ENTRY (STROBE)

   With S1 in strobe (S) position, a strobe applied to U7 will latch the data present at that time into register U1 through U6. These registers will be updated whenever a strobe is present.

3. CONTINUOUS DATA ENTRY

   With S1 in the Strobe position and the LOAD DATA input shunted with less than 100 ohms to ground, the data applied to the inputs will be continuing available to the dataway multiplexers and gates. (In this mode the PR-604 will act as a parallel input gate).

The outputs of the latch registers U1 through U6 are fed to multiplexer U12 through U17. These multiplexers will select, via means of self-address A code, which set of 24 inputs are to be multiplexed onto the read lines. A low at pin 1 of U12 will select channel 1 ($A_{(0)}$) and a high selects channel 2 ($A_{(1)}$).

The outputs of the multiplexers, pins 4, 7, 9, and 12 drive the open collector gates U18 through U23 which are enabled by $NF_{(0)}$ or $NF_{(2)}$. The output of these gates drive the dataway read lines.

$F_{(0)}$ READ COMMAND

A read command results in a "Q" response and the gating of Data from the multiplexors U12 through U17 onto the Dataway via gates U18-U23.

$NF_{(0)}$ (U35 pin 1) is gated with $A_{(0)}A_{(1)}$ (U32 pin 8) to produce $(A_{(0)}A_{(1)})$ $NF_{(0)}$ at U31 pin 3. A low at this point results in a low at U32 pin 3 which is then buffered to the Q line by U11 pin 4. $NF_{(0)}$ $(A_{(0)}A_{(1)})$ at U31 pin 3 is also buffered by U11 pin 6 which enables gates U18-U23 thus driving the Dataway read lines.

$F_{(2)}$ READ & CLEAR COMMAND

A read & clear command results in a "Q" response, gates Data onto the Dataway and resets the LAM FF's. and the Data received FF's. $NF_{(2)}$ U35 pin 3 is gated with $A_{(0)}A_{(1)}$ U32 pin 8 to produce $A_{(0)}$ $A_{(1)}$ $NF_{(2)}$ at U31 pin 5. A low at this point results in a low at U32 pin 3 which is then buffered to the "Q" line by U11 pin 4. $A_{(0)}A_{(1)}$ $NF_{(2)}$ at U31 pin 5 is buffered by U11 pin 6 and enables gates U18-23 thus driving the Dataway read lines.

$NF_{(2)}$ is gated by $S_{(2)}$ to give $F_{(2)}S_{(2)}$ at U29 pin 3. This signal is in turn gated by $A_{(0)}$ to give $F_{(2)}A_{(0)}S_{(2)}$ at U28 pin 8. A low at this point will reset "Reg 1" LAM FF. Gating $F_{(2)}S_2$ U29 pin 3 with $A_{(1)}$ will give $F_{(2)}A_{(1)}S_2$ at U28 pin 11 this will reset "Reg 2" LAM FF.

$NF_{(2)}$ gated by S_2 at U30 pin 3 is in turn gated by $A_{(0)}$ at U10 pin 8. A low at this point resets "Reg 1" Data received FF. Gating $NF_{(2)}$ S_2 U30 pin 3 by $A_{(1)}$ at U10 pin 11 will reset "Reg 2" Data received FF.

$F_{(8)}$ TEST LAM AND $F_{(10)}$ TEST & RESET LAM, $F_{(2)}$ READ & CLEAR

A test LAM command results in a Q response from the module if LAM was set and enabled. $NF_{(8)}$ U35 pin 9 is gated with $NF_{(10)}$ U35 pin 11 and $NF_{(2)}$ U35 pin 3 to produce $NF_{(8)}+F_{(10)}+F_{(2)}$ at U33 pin 8. A low at this point enables a response on the Q line from the addressed channel. $NF_{(10)}$ is also ANDed with S2 U29 pin 6 and resets the addressed channels LAM flip flops through U9 pin 3 as described in a $F_{(0)}$ command. $F_{(2)}$ at U35 pin 3 is ANDed with S2 at U29 pin 3 and resets addressed LAM flip flop.

$F_{(24)}$ DISABLE LAM

This command disables the LAM signal of the addressed channel. $NF_{(24)}$ U36 pin 9 is gated with S1 to produce $NF_{(24)}$ S1 at U29 pin 8. This signal is then gated with $A_{(0)}$ U28 pin 6 and $A_{(1)}$ U28 pin 3. A low at either of these points will result in a low at either U27 pin 3 or U27 pin 6, respectively. A low at U27 pin 3 will result in a high at the output of the enable Flip Flop for channel 1, disabling the LAM signal for the channel. The same is true for U27 pin 6 and channel 2.

$F_{(26)}$ ENABLE LAM

An $F_{(26)}$ command enables the LAM signal of the addressed channel. $NF_{(26)}$ U36 pin 11 is gated with S1 producing the signal $NF_{(26)}$ S1. This signal is gated with $A_{(0)}$ U10 pin 6 and $A_{(1)}$ U10 pin 3. A low at U10 pin 6 will result in a low at the output of the Enable LAM flip flop U25 pin 11 for channel 1, thus enabling the LAM signal for channel 1. The same is true for U10 pin 3 and channel 2.

Q LINE

The module responds on the Q line when either of two conditions exits:

1. When $F_{(0)}$ command is accepted.
2. When a LAM is set and enabled and a $F_{(8)} + F_{(10)}$ command is accepted.

A low at U32 pin 1, $\overline{A_{(0)} + A_{(1)}}$ $NF_{(0)}$, produces a low at U32 pin 3. This signal is bufferred onto the dataway Q line by U11 pin 4. When gate 1's LAM FF. is set and enabled U26 pin 3 is low. If gate 1 is addressed, U29 pin 11 is low. The same logic is true for gate 2, U26 pin 8. A low at either of these points produces a low at U9 pin 6 where it is ANDed with $NF_{(8)} + NF_{(10)}$ by U30 pin 8. A low at this point produces a response on the Q line.

X LINE

$NF_{(8)}$ (U35 pin 9) and $NF_{(10)}$ (U35 pin 11) and $NF_{(2)}$ (U35 pin 3) are gated by U33 pin 8 to produce $NF_{(8)} + NF_{(10)}$. This signal along with $NF_{(0)}$ (U35 pin 1), $NF_{(24)}$ (U36 pin 9) and $NF_{(26)}$ (U36 pin 11) are gated by U33 pin 6 to obtain $N\overline{F_{(0)} + F_{(8)} + F_{(10)} + F_{(24)} + F_{(26)} + F_{(2)}}$ $A_{(0)}$ (U34 pin 9) and $A_{(1)}$ (U34 pin 7) are gated by U32 pin 8 to produce $A_{(0)} + A_{(1)}$. This signal is gated with the legal function codes $N\overline{F_{(0)} + F_{(8)} + F_{(10)} + F_{(24)} + F_{(26)} + F_{(2)}}$ (U33 pin 6) by U30 pin 11 and then bufferred by U11 pin 10 which drives the X line on the command $N\overline{A_{(0)} + A_{(1)}}$ $\overline{F_{(0)} + F_{(8)} + F_{(10)} + F_{(24)} + F_{(2)} + F_{(26)}}$. Hence, the module responds on the X line when a command is accepted.

L LINE

The module initiates the L line when a strobe is applied to the addressed external connector strobe input. Both channels are identical so only channel 1 will be discussed. The input contains a pull up and integrator circuit. After integration, the signal is inverted and applied to the clock inputs of the Data Received and LAM flip flops; the normally high outputs of both flip flops go low. If the enable LAM flip flop is enabled, a low appears at U26 pin 3. This signal produces a low at U32 pin 6 where it is ANDed with $\overline{X}$ by diodes CR1 and CR2. The signal is bufferred onto the dataway L line by U11 pin 12. A LAM signal is enabled only when a command is not accepted or when the module is not being addressed.

C + Z MASTER RESET

When a C + Z command is sent to the module the Data Received and LAM flip flop are reset and enable LAM flip flop are disabled for both channels. C + Z (U32 pin 11) is gated with S2 to produce S2 (C + Z) at U30 pin 6. A low at this point will result in a low at U9 pin 8 and U9 pin 11, resetting both data received flip flops. A low at U32 pin 12 also produces a low at U27 pin 11, 3, 8, 6, resetting the LAM flip flops and disabling the enable LAM flip flops for both channels.

APPLICATIONS NOTES:

PR604 K OR F

Several modes of operation are available to the user of the K and/or F models of the PR604.

a) Continuous data entry may be accomplished by grounding the "strobe" inputs (front panel Lemos) and placing the register toggle switch in the "S" position. This mode does not provide for Lam Flag operation; additionally, user must hold data at inputs until Dataway "read" operation is completed.

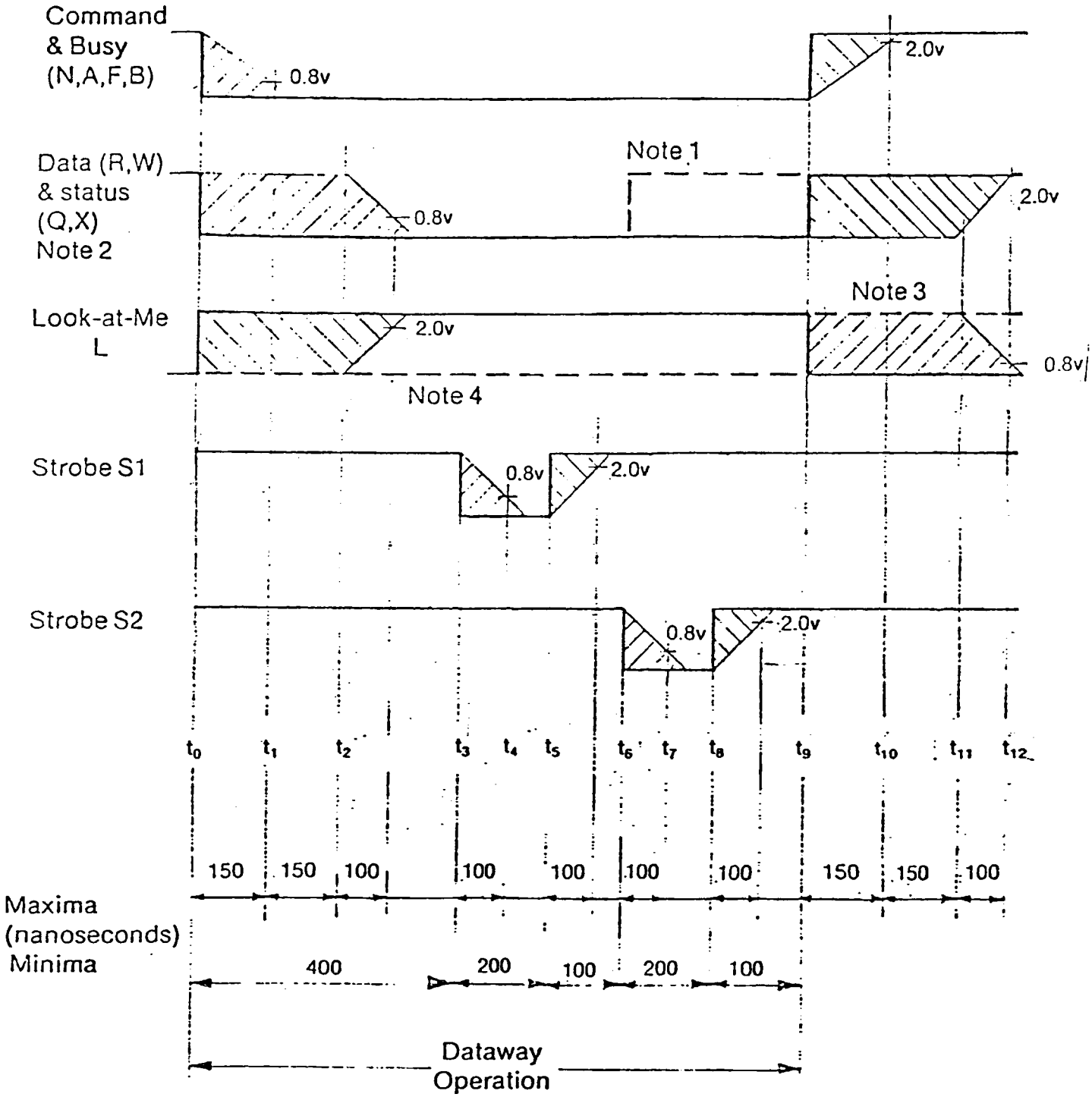
b) Data latch without Lam Flag operation may be accomplished by pulling the "Data Received" line (Pin 1 for Reg 1 or Pin 27 for Reg 2 of 52 pin connector) low. The data received line will latch itself low until a data read command using F(2) is issued. The high going transistion of "Data Received" can be monitored by users device to avoid overwriting. The register toggle switch(s) must be in the "L" position for this mode.

c) Data entry, strobed or latched, with Lam Flag operation. The front panel Lemos provide for data entry with Lam Flag operation. With the register toggle switch(s) in the "L" position, a high to low transistion at the "Strobe" input (Lemo(s)) will latch the incoming data and set the Lam Flag. The data latch and Lam Flag are reset automatically by an F(2) read command. In the latch mode, data cannot be over written. The "Data Received" line may be monitored by users device to indicate buffer empty.

With the register toggle switch(s) in the "S" position, operation is essentially the same as for the "L" position except that the data register(s) is(are) vulnerable and there is no CAMAC indication that data has been over written.

Appendixes

TIMING OF A DATAWAY COMMAND OPERATION



Note 1: Data & status may change in response to S2.
Note 2: During some operations Q may change at any time.
Note 3: LAM status may be reset during operation.
Note 4: L signal may be maintained during operation.

DATAWAY PIN ALLOCATION:

Contact Allocation at the Control Station (Viewed from Front of Crate):

		Pin No.			
Patch contact	P1	1	2	B	Busy
Patch contact	P2	3	4	F16	Function
Patch contact	P3	5	6	F8	Function
Patch contact	P4	7	8	F4	Function
Patch contact	P5	9	10	F2	Function
Command accepted	X	11	12	F1	Function
Inhibit	I	13	14	A8	Subaddress
Clear	C	15	16	A4	Subaddress
Patch contact	P6	17	18	A2	Subaddress
Patch contact	P7	19	20	A1	Subaddress
Strobe 1	S1	21	22	Z	Initialize
Strobe 2	S2	23	24	Q	Response
	L24	25	26	N24	
	L23	27	28	N23	
	L22	29	30	N22	
	L21	31	32	N21	
	L20	33	34	N20	
	L19	35	36	N19	
	L18	37	38	N18	
	L17	39	40	N17	
	L16	41	42	N16	
	L15	43	44	N15	
24 individual	L14	45	46	N14	24 individual
Look-at-me lines	L13	47	48	N13	Station number lines
L1 from Station 1,	L12	49	50	N12	N1 to Station 1,
etc.	L11	51	52	N11	etc.
	L10	53	54	N10	
	L9	55	56	N9	
	L8	57	58	N8	
	L7	59	60	N7	
	L6	61	62	N6	
	L5	63	64	N5	
	L4	65	66	N4	
	L3	67	68	N3	
	L2	69	70	N2	
	L1	71	72	N1	
-12 V dc	-12	73	74	-24	-24 V dc
+200 V dc	+200	75	76	-6	-6 V dc
117 V ac live	ACL	77	78	ACN	117 V ac neutral
Reserved	Y1	79	80	E	Clean earth
+12 V dc	+12	81	82	+24	+24 V dc
Reserved	Y2	83	84	+6	+6 V dc
0V (power return)	0	85	86	0	0V (power return)

FUNCTION CODES:

R/W:	Code F( ):	Function:
R	0	Read group 1 register.
R	1	Read group 2 register.
R	2	Read and clear group 1 register.
R	3	Read compement of group 1 register.
R	4	Nonstandard.
R	5	Reserved.
R	6	Nonstandard.
R	7	Reserved.
	8	Test look-at-me (LAM).
	9	Clear group 1 register.
	10	Clear look-at-me (LAM.
	11	Clear group 2 register.
	12	Nonstandard.
	13	Reserved.
	14	Nonstandard.
	15	Reserved.
W	16	Overwrite group 1 register.
W	17	Overwrite group 2 register.
W	18	Selective set group 1 register.
W	19	Selective set group 2 register.
W	20	Nonstandard.
W	21	Selective clear group 1 register.
W	22	Nonstandard.
W	23	Selective clear group 2 register.
	24	Disable.
	25	Execute.
	26	Enable.
	27	Test status.
	28	Nonstandard.
	29	Reserved.
	30	Nonstandard.
	31	Reserved.

7/11/88

DSP TECHNOLOGY INC.
SINGLE LEVEL BILL OF MATERIAL
AS OF 7/11/88

ASSEMBLY P/N 105097
DESCRIPTION ASSY: PCB, PR-604

PART NUMBER	DESCRIPTION
0100-0100	RES 5% 1/4W CC RESISTOR R=10
0100-0101	RES: RC07 100 OHM
0100-0102	RES: RC07 1K OHM
0100-0391	RES 5% 1/4W CC RESISTOR R=390
010113	CAP: CER, .01UF, 50V SPRAGUE 5GAT12
013330	CAP: AX TANT KEMET T110B336K010AS
020002	SWITCH: C&K 7101MDRB
0520-0103	CMC C=0.01UF MONO CENTRALAB CZ20A1
0525-0101	CDC C=100PF CERAMIC 1000WVDC SPRA
060414	DIO: 1N4148
061612	XSTR: NPN, 2N6121
062100	IC: 74100
064042	IC: 74LS42
067040	IC: MC4042
105098	PWB: PR-604
1705-0453	ICS: SN75453
1750-0004	ICS SN7404
1750-0007	ICS SN7407
1750-0074	ICS SN7474
1750-0154	ICS SN74154
1760-0000	ICS SN74LS00
1760-0004	ICS SN74LS04
1760-0008	ICS SN74LS08
1760-0021	ICS SN74LS21
1760-0032	ICS SN74LS32

PART NUMBER	DESCRIPTION

REV C5

QTY PER	AS OF	UNTIL	REFERENCE
1	5/11/86	12/31/99	R60
2	5/11/86	12/31/99	R50,R53
56	5/11/86	12/31/99	R54-R57,R59 R1-R49,R51,R52
1	5/11/86	12/31/99	R58
2	5/11/86	12/31/99	C4,C6
2	5/11/86	12/31/99	C3,C5
2	5/11/86	12/31/99	S1,S2
18	5/11/86	12/31/99	C7-C24
2	5/11/86	12/31/99	C1,C2
2	5/11/86	12/31/99	CR1,CR2
1	7/10/86	12/31/99	Q1
6	5/11/86	12/31/99	U1-U6
1	12/17/86	12/31/99	U34
6	5/11/86	12/31/99	U18-U23
1	5/11/86	12/31/99	
1	10/08/86	12/31/99	U31
1	3/17/87	12/31/99	U7
1	6/13/86	12/31/99	U11
1	3/17/87	12/31/99	U8
2	5/11/86	12/31/99	U35,U36
1	12/17/86	12/31/99	U25
1	3/17/87	12/31/99	U37
3	12/17/86	12/31/99	U9,U27,U32
1	12/17/86	12/31/99	U33
5	12/17/86	12/31/99	U10,U26,U28-U30

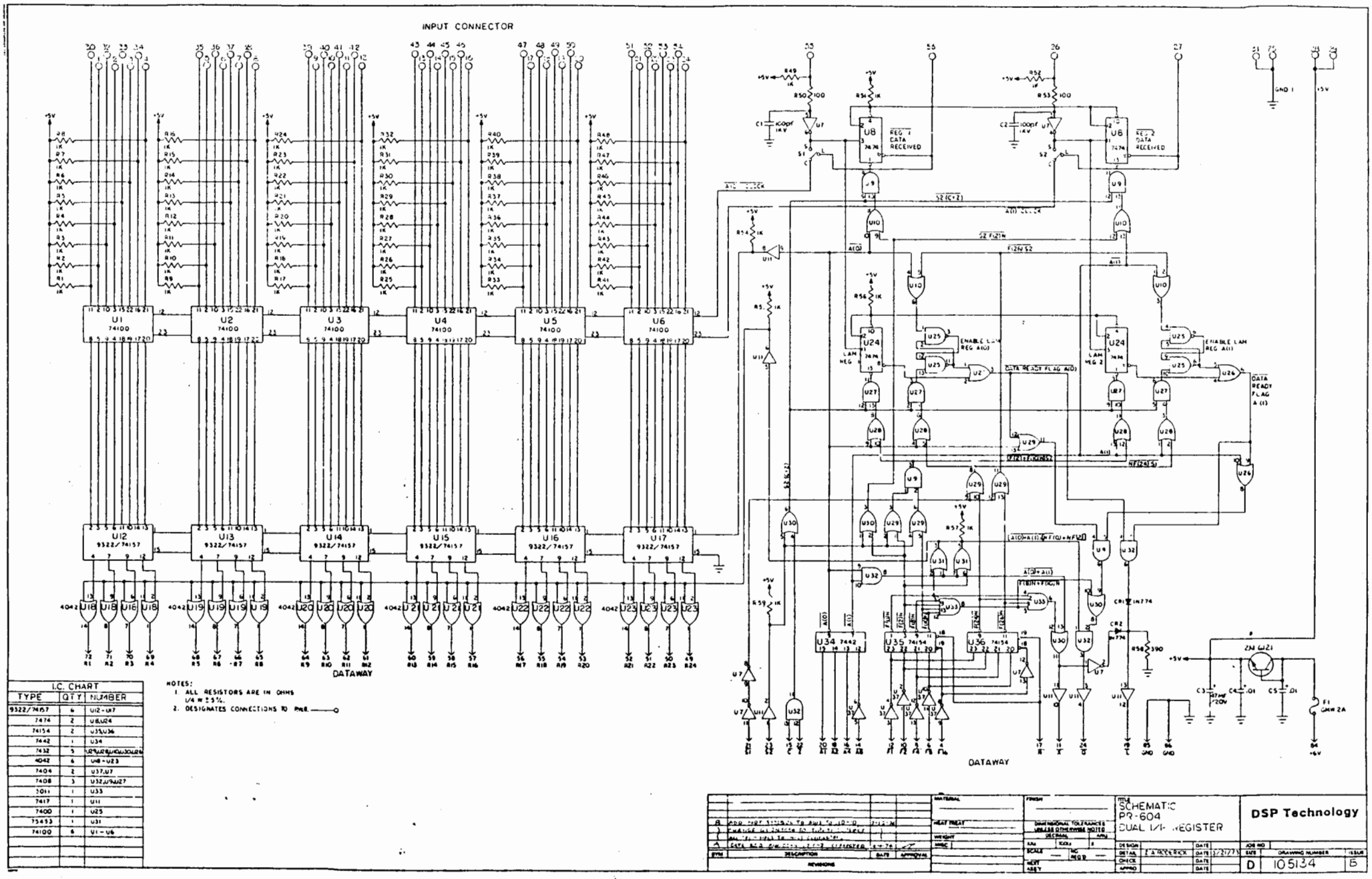
QTY PER AS OF UNTIL REFERENCE

ASSEMBLY P/N 105097 REV C5
DESCRIPTION ASSY: PCB, PR-604

PART NUMBER	DESCRIPTION	QTY PER	AS OF	UNTIL	REFERENCE
1760-0074	ICS SN74LS74	1	3/17/87	12/31/99	U24
1760-0157	ICS SN74LS157	6	5/11/86	12/31/99	U12-U17
3100-0202	FUS FUSE 2A LITTLEFUSE 251002	1	5/11/86	12/31/99	F1D
5000-0024	SKT CAMBION 703-1324-01-04-10	8	5/11/86	12/31/99	

SINGLE LEVEL BILL OF MATERIAL - by Part Number - for Assembly 105097

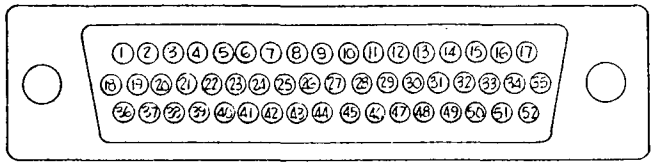
PART NUMBER	DESCRIPTION	QTY PER	AS OF	UNTIL	REFERENCE



I.C. CHART		
TYPE	QTY	NUMBER
9322/74157	6	U12-U17
7474	2	U8,U24
74154	2	U35,U36
7442	1	U34
7432	5	U29,U28,U10,U30,U26
4042	6	U18-U23
7404	2	U37,U7
7408	3	U32,U9,U27
3011	1	U33
7417	1	U11
7400	1	U25
75453	1	U31
74100	6	U1-U6

NOTES:
1. ALL RESISTORS ARE IN OHMS 1/4 W ±5%.
2. DESIGNATES CONNECTIONS TO PWB.

P.W. BOARD CONNECTIONS				CONNECTOR PIN NO'S
56	STROBE 1	VIO		1
30		BRN	BIT 1 (A0)	2
32		RED	BIT 2 (A0)	3
33		ORG	BIT 3 (A0)	4
34		YEL	BIT 4 (A0)	5
35		GRN	BIT 5 (A0)	6
36		BLU	BIT 6 (A0)	7
37		VIO	BIT 7 (A0)	8
38		GRY	BIT 8 (A0)	9
39		WHT/BLK	BIT 9 (A0)	10
40		WHT/BRN	BIT 10 (A0)	11
41		WHT/RED	BIT 11 (A0)	12
42		WHT/ORG	BIT 12 (A0)	13
43		WHT/YEL	BIT 13 (A0)	14
44		WHT/GRN	BIT 14 (A0)	15
45		WHT/BLU	BIT 15 (A0)	16
46		WHT/VIO	BIT 16 (A0)	17
47		WHT/GRY	BIT 17 (A0)	18
48		GRY	BIT 18 (A0)	19
49		BRN	BIT 19 (A0)	20
50		RED	BIT 20 (A0)	21
51		ORG	BIT 21 (A0)	22
52		YEL	BIT 22 (A0)	23
53		GRN	BIT 23 (A0)	24
54		BLU	BIT 24 (A0)	25
27	STROBE 2	VIO		26
1		GRY	BIT 1 (A1)	27
2		WHT/BLK	BIT 2 (A1)	28
3		WHT/BRN	BIT 3 (A1)	29
4		WHT/RED	BIT 4 (A1)	30
5		WHT/ORG	BIT 5 (A1)	31
6		WHT/YEL	BIT 6 (A1)	32
7		WHT/GRN	BIT 7 (A1)	33
8		WHT/BLU	BIT 8 (A1)	34
9		WHT/VIO	BIT 9 (A1)	35
10		WHT/GRY	BIT 10 (A1)	36
11		GRY	BIT 11 (A1)	37
12		BRN	BIT 12 (A1)	38
13		RED	BIT 13 (A1)	39
14		ORG	BIT 14 (A1)	40
15		YEL	BIT 15 (A1)	41
16		GRN	BIT 16 (A1)	42
17		BLU	BIT 17 (A1)	43
18		VIO	BIT 18 (A1)	44
19		GRY	BIT 19 (A1)	45
20		WHT/BLK	BIT 20 (A1)	46
21		WHT/BRN	BIT 21 (A1)	47
22		WHT/RED	BIT 22 (A1)	48
23		WHT/ORG	BIT 23 (A1)	49
24		WHT/YEL	BIT 24 (A1)	50
28	+5V	RED		51
GND		BLK		52



FRONT VIEW

NOTES:
1. ALL WIRES ARE 26 AWG. PER MIL-W-16878D
2. CONNECTOR: CANNON 2DB 52 P

REVISIONS				
SYM	DESCRIPTION	DATE	APPROVAL	

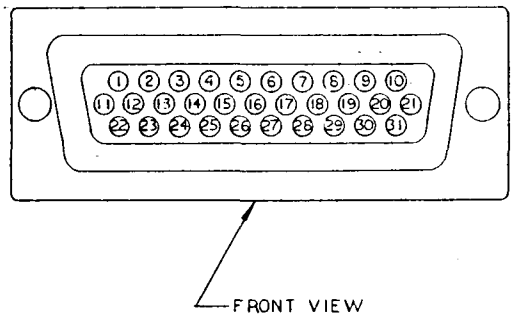
MATERIAL
HEAT TREAT
WEIGHT
MISC
FINISH
DIMENSIONAL TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ANG
XX± XXX± ±
SCALE NO REQ'D
NEXT ASS'Y

TITLE: DIAGRAM, CONNECTOR WIRING, 52-PIN CANNON

DSP Technology

DESIGN		DATE	
DETAIL	LOUDEN	DATE	7-19-73
CHECK		DATE	
APPRO		DATE	7-24-73

JOB NO.
SIZE C
DRAWING NUMBER 106307
ISS.



PC BOARD		CONNECTOR J1
30	BIT 1 BRN	1
32	BIT 2 RED	2
33	BIT 3 ORN	3
34	BIT 4 YEL	4
35	BIT 5 GRN	5
36	BIT 6 BLU	6
37	BIT 7 VIO	7
38	BIT 8 GRY	8
39	BIT 9 WHT/BLK	9
40	BIT 10 /BRN	10
41	BIT 11 /RED	11
42	BIT 12 /ORG	12
43	BIT 13 /YEL	13
44	BIT 14 /GRN	14
45	BIT 15 /BLU	15
46	BIT 16 /VIO	16
47	BIT 17 WHT/GRY	17
48	BIT 18 GRY	18
49	BIT 19 BRN	19
50	BIT 20 WHT/BLK	20
51	BIT 21 RED	21
52	BIT 22 ORG	22
53	BIT 23 YEL	23
54	BIT 24 BLU	24
	BLANK	25
56	GRN (NOTE 3)	26
55	VIO STROBE 1	27
	BLANK	28
28	RED VCC	29
	BLANK	30
25	BLK GND	31

PC BOARD		CONNECTOR J2
1	BIT 1 BRN	1
2	BIT 2 RED	2
3	BIT 3 ORN	3
4	BIT 4 YEL	4
5	BIT 5 GRN	5
6	BIT 6 BLU	6
7	BIT 7 VIO	7
8	BIT 8 GRY	8
9	BIT 9 WHT/BLK	9
10	BIT 10 /BRN	10
11	BIT 11 /RED	11
12	BIT 12 /ORG	12
13	BIT 13 /YEL	13
14	BIT 14 /GRN	14
15	BIT 15 /BLU	15
16	BIT 16 /VIO	16
17	BIT 17 WHT/GRY	17
18	BIT 18 GRY	18
19	BIT 19 BRN	19
20	BIT 20 WHT/BLK	20
21	BIT 21 RED	21
22	BIT 22 ORG	22
23	BIT 23 YEL	23
24	BIT 24 BLU	24
	BLANK	25
27	GRN (NOTE 3)	26
26	VIO STROBE 2	27
	BLANK	28
29	RED VCC	29
	BLANK	30
31	BLK GND	31

NOTES:

1. ALL WIRES ARE 26 AWG. PER MIL-W-16878D
2. CONNECTOR: CANNON 2DA 31P
3. CONNECTOR PINS J1, J2-26 ARE USED ONLY IN CERTAIN APPLICATIONS.

SYM	DESCRIPTION	DATE	APPROVAL
D	REVERSED 55,56 - 26,27 P.W.E. NO'S.		
C	CHANGED GND AND VCC CONNECTION	5-15-74	JAN

REVISIONS

MATERIAL: NOTE 1
HEAT TREAT:
WEIGHT:
MISC:

FINISH:
DIMENSIONAL TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL: XX ±.01, XXX ±.005 | ANG ±
SCALE: NO REQ'D
NEXT ASSY:

TITLE: DIAGRAM, CONNECTOR WIRING 31 PIN CANNON

DESIGN	CARRINGTON	DATE 6-27-75
DETAIL		DATE
CHECK		DATE
APPRO		DATE

DSP Technology

JOB NO:

SIZE	DRAWING NUMBER	ISSUE
C	106251	D

PR-604 MANUAL REVISION RECORD:

Revision:	Date Issued:	Description:	Reference:
A	11/10/81	Updated drawings list	None
B	6/3/82	Drawing No. 105129 raised from Rev E to Rev F; repaginated	None

dsp Technology Inc.

PRODUCT WARRANTY

(Excludes Software)

DSP TECHNOLOGY ("DSP") warrants its products to be free from defects in material and workmanship and to meet DSP's performance specifications. The warranty period is one year from the date of shipment to the buyer. The warranty is limited by the paragraphs below.

RETURN TO FACTORY

If a buyer discovers a defect in a DSP product covered by this agreement, buyer's exclusive remedy is to ship the product back to DSP's Fremont factory, where DSP will, at its option, either repair or replace the product. This remedy applies if DSP receives the returned product on or before the tenth day after the expiration of the warranty period and the buyer notifies DSP of the defect before returning the product.

COST TO BUYER OF REPAIRS OR REPLACEMENT

Buyer must prepay freight charges to DSP. DSP will pay standard return freight to buyer. Buyer will be charged for premium freight if that method of transport is requested by buyer. There is no other charge for repair or replacement during the warranty period.

TRANSFERRABLE WARRANTIES

In addition to the foregoing warranty, DSP also provides the buyer the transferrable warranty, if any, provided to DSP by the manufacturers of other products such as terminals and disk systems supplied by SEC as part of a total system.

LIMITATION OF WARRANTY AND LIABILITY

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