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E500A

STEPPER MOTOR CONTROLLER

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MODEL E500

INTELLIGENT STEPPER MOTOR CONTROLLER

FEATURES

- Eight Independent Channels
- Full Dataway Programming for Acceleration/Deceleration Time (0 Seconds to 2.55 Seconds), Slew Rate (5 pps to 20,000 pps), and Magnitude (24 bits).
- Automatic Correction for Missed Pulses
- Limit-switch Inputs
- Optional Remote Manual Control
- Advanced Control Algorithm Intel-8088 Microcomputer
- Single-width Module
- Maskable LAM Generation
- Software Abort Capability



ACTUAL SIZE

DESCRIPTION

The E500 is a high-density, extremely flexible module that controls incremental motors and other pulse-driven devices. Magnitude (number of steps), slew rate (steady-state pulse rate), and acceleration/deceleration time are programmable from the Dataway with a high degree of accuracy over wide limits. For each channel, the E500 supplies a direction bit and a pulse-train output in negative true logic at either a 24 V of a TTL level by using a jumper selection.

When the complementary pulse-train and direction bit inputs are connected to a compatible shaft encoder directly fixed to the motor being controlled, the E500 can be programmed to automatically correct for missed pulses caused by inertial overload or other factors.

Inputs for two normally-closed limit switches are provided. The presence of a limit immediately causes an interruption of pulses to the selected motor. The status of the limit switch state is readable by the computer.

Each channel of the E500 can be manually controlled by adding an E505 remote control unit. This unit is useful for the initial manual setup of stepper motor systems. Additional information on the E505 is contained on a separate data sheet.

Maskable LAM capability is provided for all channels and is available in each channel's CSR. A LAM is generated when an operation has been completed, when a limit has been reached, or when other special situations occur.

Smooth control of the motor is accomplished by using a stair step approximation to a linear acceleration/deceleration curve. A control algorithm determines the number and the character of the stair step pattern consistent with the programmed parameters. When a programmed operation is completed, the internal CPU compares the number of pulses returned with that requested and makes a single attemmpt to correct any deficiency up to a programmed maximum number of steps.

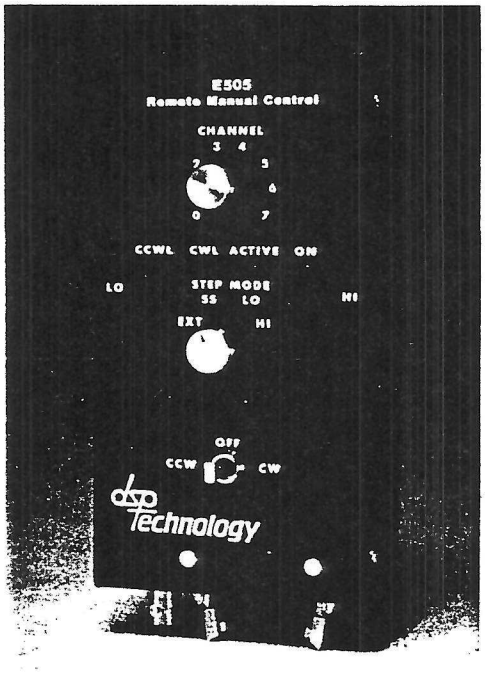
A move operation may be prematurely terminated by either a "hard" or "soft" abort. The hard abort immediately terminates pulses, while the soft abort immediately starts the deceleration portion of the cycle.

Once initialized, the absolute posiiton of each channel is maintained throughout all operations. An absolute accumulator that is nominally 24 bits in length can be extended using the overflow and the underflow bits available in each CSR.

Pulse and direction inputs, outputs, and limit switch inputs are directly compatible with the E450 and E455 termination panels. These panels are described in a separate data sheet.

MODEL E505

REMOTE CONTROL POD



FEATURES

- Channel selection switch
- Four clock sources: internal slow (adjustable), internal fast (adjustable), single step, and external clock (BNC)
- Limit indicators (LED)
- RS-422 interface

DESCRIPTION

The E505 is a compact, hand-held unit connected to the E500 module with a 20-conductor flat-ribbon cable. An operator can use the front-panel rotary switch on the E505 to manually adjust the position of any channel on the E500 module. A four-position mode switch designates high-speed stepping, low-stepping, single-step stepping, or external-clock-rate stepping. Action on the E505 is initiated with the CW/off/CCW toggle switch.

The low-range internal stepping rate is screwdriver adjustable over a range of approximately 5 pps to 200 pps. The high-range rate is adjustable likewise from 200 pps to 20,000 pps. Red LED's indicate the presence of limits on a selected channel. An amber "active" LED indicates that an operation is taking place. Unlike Dataway-programmed operations, E505 operations can go beyond the limit switch area, so caution should be exercised.

MODEL E500

APPLICATION

The E500 intelligent stepper motor controller controls any stepper motor by means of a user-supplied translator that accepts a direction bit and a pulse-train input (negative true logic). The E500 also accepts pulse and direction inputs from a remote shaft encoder and implements an automatic correction algorithm to provide additional precision in critical applications.

TECHNICAL SPECIFICATIONS

PACKAGING

#1 width CAMAC module

221 mm H, 18 mm W, 292 mm D* (8.7" x 0.7" x 11.5")

*Depth front to rear panel. Rear connector 13 mm (0.5"). In conformance with the CAMAC standard for RF shielded instrumentation modules (IEEE standard 583, European Esone Report #EUR4100e).

TEMPERATURE

0° to 40° C (32° F to 104° F) to operate within specifications when installed in crate with enough air flow to hold maximum air exit temperature to 55° C (131° F).

COMPUTER COMMANDS

F(0)A(i) Read remaining magnitude (2's complement) CSR or base rate for channel i (see F (25))

F(0)A(i+8) Read absolute accumulator (2's complement) or pulse parameters for channel i.

F(1) A(x) Read module identification code (500). Must be preceeded by A(2)F(25). X is any subaddress.

F(16)A(i) Write relative magnitude to channel i, two's complement.

F(16)A(i+8) Write absolute accumulator for channel i, two's complement.

F(17)A(i) Write SCR for channel i.

F(17)A(i+8) Write pulse parameters for channel i.

F(25)A(0) Load remaining magnitudes and current absolute accumulators for all channels into read registers.

F(25)A(1) Load CSR's and pulse parameters for all channels into read registers.

F(25)A(2) Load module identification (500) into read registers.

F(25)A(3) Start all motors simultaneously.

F(25)A(4) Load programmed and actual base rates into read registers.

F(25)A(i+8) Move channel i to "home" position, ie position 0.

MODEL E505

APPLICATION

The E505 remote control pod is used with the E500 intelligent stepper motor controller to manually position a channel from a remote location. A multiple-speed adjustable jogging feature of the unit allows quick and convenient system setup.

TECHNICAL SPECIFICATIONS

MECHANICAL

Hand-held enclosure

Size: 76 mm x 140 mm x 32 mm (3" x 5.5" x 1.25")

Weight: 0.6 kg (1.3 lb)

OPERATING TEMPERATURE

0° C to 50° C (32° F to 122° F) at less than 80% humidity

POWER REQUIREMENTS

24 V 350 mA

Interface: RS-422

PANEL CONTROLS

Channel select
Step mode
Actuate (CW/off/CCW)
High-range speed adjust
Low-range speed adjust

PANEL INDICATORS

On LED (green)
Active LED (amber)
CW limit LED (red)
CCW limit LED (red)

CONNECTORS

BNC (External clock)
20-pin Scotchflex (interface cable)

E500 MANUAL ADDENDUM, SECTION 3.3

3/23/89

The E500 has traditionally had a problem such that when a LAM is cleared by STARTing a new operation, the internal microprocessor may take a relatively long time to actually deassert the Dataway L line. This has serious consequences for event-driven multi-tasking operating environments because the still-asserted L line may be interpreted as another interrupt.

This problem has been fixed. However, because the fix is not software compatible with the existing protocol, the standard product has not been upgraded. Instead, the fix is available in the form of a Product Modification Notice which may be requested at no additional charge when the E500 is ordered. If there is any question as to whether or not your E500 has the upgrade, check the ID sticker on the right side panel for the indication "PMN 100".

The fix amounts to implementing Dataway command F(10) A(0) to immediately clear Dataway L. This command should be issued from within your interrupt service routine as one of its first actions. This is in addition to STARTing a new operation or setting the channel's LAM mask bit.

Note however that the E500 cannot assert L again until <u>all</u> pending LAMs in the module are cleared. This means that the interrupt service routine should service and clear all LAM sources before exiting.

1. PRODUCT DESCRIPTION

1.1 INTRODUCTION AND SCOPE

The purpose of this manual is to acquaint the user with the various features of the Standard Engineering E500A Intelligent Stepper Motor controller. The intelligence contained on card provides extended functionality and a greatly decreased burden on the host controller, but the user must first master the comprehensive instruction set in order to realize the full power of the module.

Section 1 contains a functional description of the module without the detail which follows later. A discussion of the control algorithm follows giving the user an idea of how the module functions in outputting the programmed parameters.

Section 2 is a restatement of the module data sheet, listing the mechanical, electrical, and command set parameters.

Section 3 is a detailed discussion of the programming the E500A including a map of all appropriate control, status and data registers.

Section 4 describes the E450/E455 termination panel specifically designed for interfacing the E500A to the external world.

Section 5 discusses the optional E505 remote control pod, its uses and limitations.

Section 6 is reserved for a discussion of applications of the E500A including the framework for a self optimizing motion control system.

1.2 FUNCTIONAL DESCRIPTION

1.2.1 General

Although the E500A is called a stepper motor controller, it can be used in other applications where a controlled parameter pulse train is desired such as with a step mode analog controller used in process control. The E500A offers very high channel density (8 channels in a single width module), unprecedented programmability, and a very wide range of operating parameters. The E500A permits completely automatic control of a stepper motor cycle including the correction of

lost steps if so programmed. In addition to pulse train outputs, the E500A features inputs for clockwise and counter clockwise limit switches permitting failsafe operation.

1.2.2 Output Functions

The E500A features both a pulse train output and a direction output for each of the eight channels. The pulse train is normally compatible with SEC termination panels which require 24 volt logic. The board can be strapped however to be TTL compatible. When an operation has been programmed into the E500A and executed, the pulse train begins at some lower frequency, increases according to the programmed parameters to a steady state value, and then decreases finally to a stop condition. The direction bit output specifies what direction the stepper motor is to go.

Both of these outputs in turn feed the translator associated with the stepper motor either directly or through an appropriate termination panel. The pulse train and direction bit outputs for all eight channels are located on connector J1. Except for the "handshake" signals used on the remote control pod, these are the only outputs on the E500A.

All signals associated with the front panel connectors except for the remote control connector, are low true signals which nominally are set for 24 volt logic, but which may be altered for TTL compatibility by changing a single jumper. The location of this jumper is shown on figure 1.

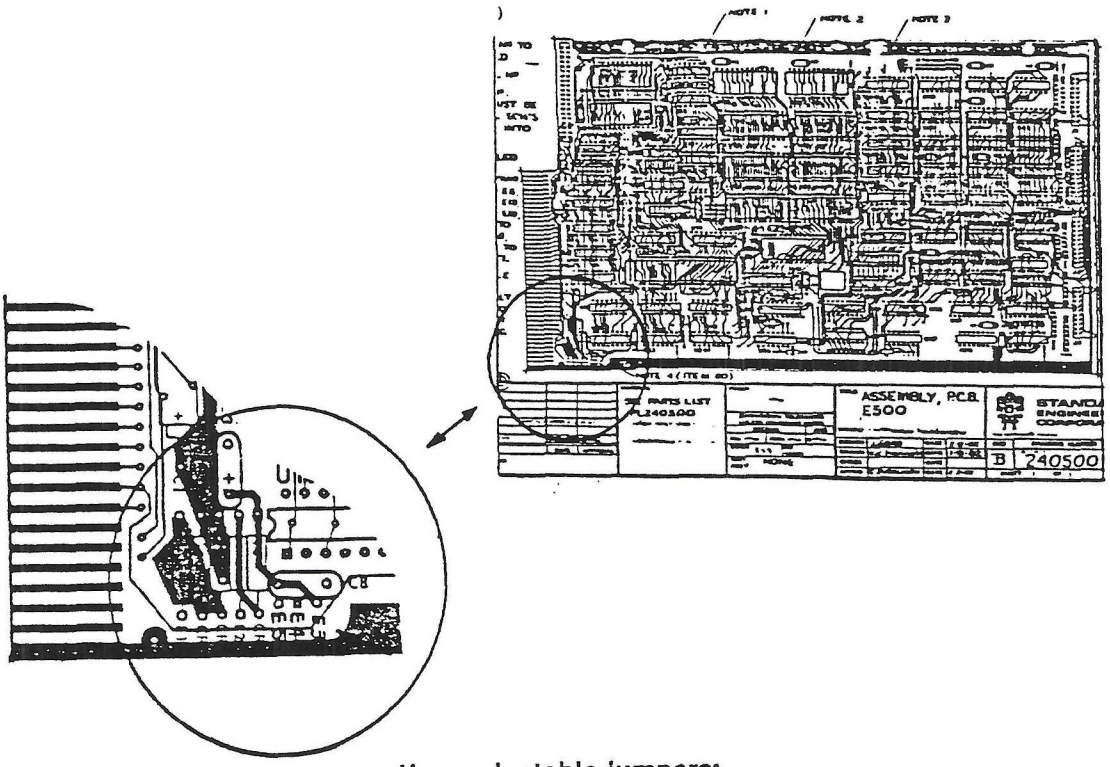
1.2.3 Feedback Inputs

Two kinds of information can be fed back into the E500A from the front panel connectors. A returning pulse train and direction information is mandatory. Ideally these signals should come from a shaft encoder tied directly to the stepper motor being controlled. This shaft encoder must have the same resolution as the motor i.e. must return one pulse back for every one pulse output. A direction bit must be returned as well indicating the sense of rotation in the same polarity as the outgoing bit.

If a shaft encoder is not available, the outgoing pulse train and direction bit can simply be looped back to the input connector. The module will then operate correctly although it will not be able to correct for missed steps due to inertial overload.

The pulse train output and direction bits for all eight channels are located on connector J1 and the corresponding input information appears on connector J2 on the same pins. A cable

Figure 1
Jumper Connection for +5V Logic



User-selectable jumpers:
- **E3 to E4 for 24V logic**
- **E4 to E5 for 5V logic**

for accomplishing the loopback is avaialable as SEC part number 150555, although any standard 20 insulation displacement connector of the "SCOTCHFLEX" type can be fitted to the output cable and plugged in to J2. Section 2.2.2 shows a detailed layout of the pins for all front panel connectors.

The second set of feedback signals involve the use of switches which indicate that a rotational limit has been reached. Each channel has an input for a CW and CCW limit switch. The use of these inputs is optional. When used, these signals trigger a hardware interlock which immediately prevents pulses from being output in the disallowed direction. Furthermore, the limit status information is made available to the host controller through the status register.

1.2.4 Dataway Programmability

The E500A features enormous flexibility in programming the parameters of the individual channels. Each of the eight channels is completely independent and can be operated asynchronously. Despite the flexibility, certain precautions must be noted with respect to programming the module.

The E500A represents the first in a new series of highly intelligent CAMAC modules. These devices can substantially reduce the burden on the host controller. Most of the functions of the module are conducted by a microprocessor, in this case the Intel iAPX 88. These microprocessors are not fast enough in many cases to service the dataway directly, so an indirect method of control is necessary. The E500A uses two methods to "throttle" the speed of input commands.

In all cases the Q bit on the dataway indicates whether or not a command was accepted and acted upon. Since each command is decoded and acted upon by the iAPX 88, the host controller may have to wait before issuing a subsequent command. If the module is still busy, as indicated by Q=0, the controller will have to repeat the operation until Q=1. Typically this limitation will be most noticable when issuing rapid WRITE or EXECUTE commands, and less so with READ commands, but the Q status must always be checked.

In addition to Q, a set of EXECUTE commands has been implemented which tell the iAPX 88 to load a group of values into a dual ported RAM accessible from the dataway. In effect one EXECUTE command replaces many potential handshaking commands.

1.2.5 Status Reporting

The E500A features extensive status reporting on the condition of each channel. In addition to implementing eight channels of control, the E500A also has eight channels of up/down accumulation which keeps track of the absolute position of the device connected to each channel. While nominally 24 bits long, this accummulator can be extended in the host controller through the overflow/underflow bits available in the status registers. As mentioned above, the limit status of each channel is also reported. The module implements a LAM capability and the status of LAMs and their associated mask bits is also available.

1.3 THE CONTROL ALGOROTHM

In order to effectively use the E500A, it is necessary to understand part of how the control algorithm functions. Since it is possible to program the E500A with mutually

incompatible parameters, surprises can be avoided by understanding the process of building a parameter file.

1.3.1 Magnitude

The key parameter in the E500A is the magnitude, or the number of steps the motor is expected to go. This number is represented by a 24 bit binary value whose MSB is the direction (1 for CW, 0 for CCW) and whose lower 23 bits indicate the scalar number of pulses. The magnitude represents a vector displacement from wherever the motor (or other device) currently rests and is therefore a relative write operation. As will be seen presently, the module keeps track of ABSOLUTE position and generally reports this quantity. The magnitude is the highest priority parameter and the module will do whatever is required to correctly output the specified number of pulses.

1.3.2 Slew Rate

The slew rate is the nominal velocity desired in pulses per second. Since most operations will involve a finite acceleration and deceleration period, the slew rate represents the steady state portion of the cycle. The minimum value for slew rate is 5 pulses per second (pps). The maximum value permitted is 20,000 pps. Values outside of this range will be adjusted to the nearest limit.

The slew rate is programmed as a 16 bit scalar integer. Slew rate and accel/decel time interact heavily. Care should be taken when deciding on values for these two quantities. For example, if a high slew rate and a long accel/decel period is selected, the desired magnitude may not permit the motor to come up to final speed before exhausting the avaialable pulses. Slew rate has the lowest priority of the three major parameters. This means that the slew rate will be achieved only if the other two parameters permit it.

While the slew rate is programmable in integer values, the true steady state slew rate achieved may differ due to round off errors. Generally at rates below 5,000 pps, the maximum error will be less than 2% steadily improving as the rate falls. The maximum error of about 7% occurs in the region of 20,000 pps. Stated a different way, several different slew rates programmed into the E500A may result in the same steady state slew rate being output within the error limits above.

Although all channels are nominally identical, the lower numbered channels are serviced at a higher priority level than the higher numbered channels. This means that the lower numbered channels can statistically support a higher interrupt

load and in turn higher slew rates without overstepping (see section 1.3.5). Therefore, those motors requiring higher stepping speeds should be assigned to the lower numbered channels. At rates below 3,000 pps, ordering according to speed will probably have no beneficial effect.

1.3.3 Acceleration and Deceleration Time

The acceleration and deceleration parameter is programmable in terms of the time required to go from minimum speed to the desired slew rate rather than the actual acceleration rate in pulses per second per second. The "ramp up/down" process is symmetrical i.e. the acceleration time equals the deceleration time in all cases.

This parameter is programmable in tens of milliseconds using an eight bit binary number. This means the minimum time is 10 ms and the max time is 2,550 ms.

The algorithm attempts the best approximation to a linear accel/decel curve and makes its best effort to preserve the rate desired (not the time) if limits are imposed by the choice of parameters. This point is worth restating. The accel/decel parameter is programmed in terms of time, but the resulting rate is the preserved quantity.

The time programmed corresponds to one ramp period, therefore the total time spent in acceleration and deceleration is twice that programmed. The accuracy for actual accel/decel time (provided other parameters permit) is typically better than 1%.

If the value programmed for accel/decel time is 0, this means that whatever pulses are called for will be output at the chosen slew rate.

1.3.4 Base Rate

The rate at which acceleration begins and deceleration ends is called the "base rate". This can be programmed in increments of 10 pps over the range of 10 pps to 2550 pps using an 8-bit binary scaler. A value of zero indicates that the profiling algorithm is to select an appropriate base rate.

The programmed value is not an absolute priority. If the profiling algorithm requires a base rate higher than the programmed value, the algoritm takes precedence. This is necessary to preserve the priority of the other parameters.

1.3.5 Correction Limit

The E500A uniquely provides the capability for correcting for "missed steps" if an external shaft encoder is provided. Missed steps can mean either over stepping or under stepping. Steps can be missed due to a motor with a high inertial load, insufficient torque, or an inappropriate accel/decel value. The correction algorithm calls for the module to make one effort to correct for any difference between that magnitude programmed and what actually happened according to the shaft encoder.

It is prudent to limit the size of the correction since major adjustments indicate basic errors which should be noted without repeating a large stepping operation. This limit is set via the correction limit parameter. This is an eight bit number allowing a correction of up to 255 steps. The direction of the correction is handled automatically.

A correction operation which is unsuccessful, or missed pulses in excess of the programmed limit will cause a correction failure bit to be set in the appropriate CSR. Note that correction will not be attempted if the correction limit is too small for the observed error.

Under certain circumstances, the E500A outputs fewer pulses than are required to achieve the final destination, depending on the correction cycle to compensate. This occurs because of the statistical nature of servicing interrupts for several motors moving simultaneously. The actual undercount is a function of the programmed slew rate and the channel number with the worst case error being about 40 steps. This means that if the correction limit is set for at least 40 steps, no output errors should be seen.

A special case exists when short, high speed moves are requested with little or no accel/decel time. These are known as "single segment" moves and overstepping cannot be prevented without reducing the stepping rate. Furthermore this effect is more pronounced for higher channel numbers. This is because the interrupt priority in the 8088 is higher for the lower numbered channels. The reduced stepping rate selected by the profiling algorithm is readable as the actual base rate as described in section 3.1.1.

Figure 2 shows a family of curves illustrating, for each channel, the region where a reduction of the requested rate is effected. Areas below and to the right of the line are so affected.

1.3.6 The Absolute Accumulator

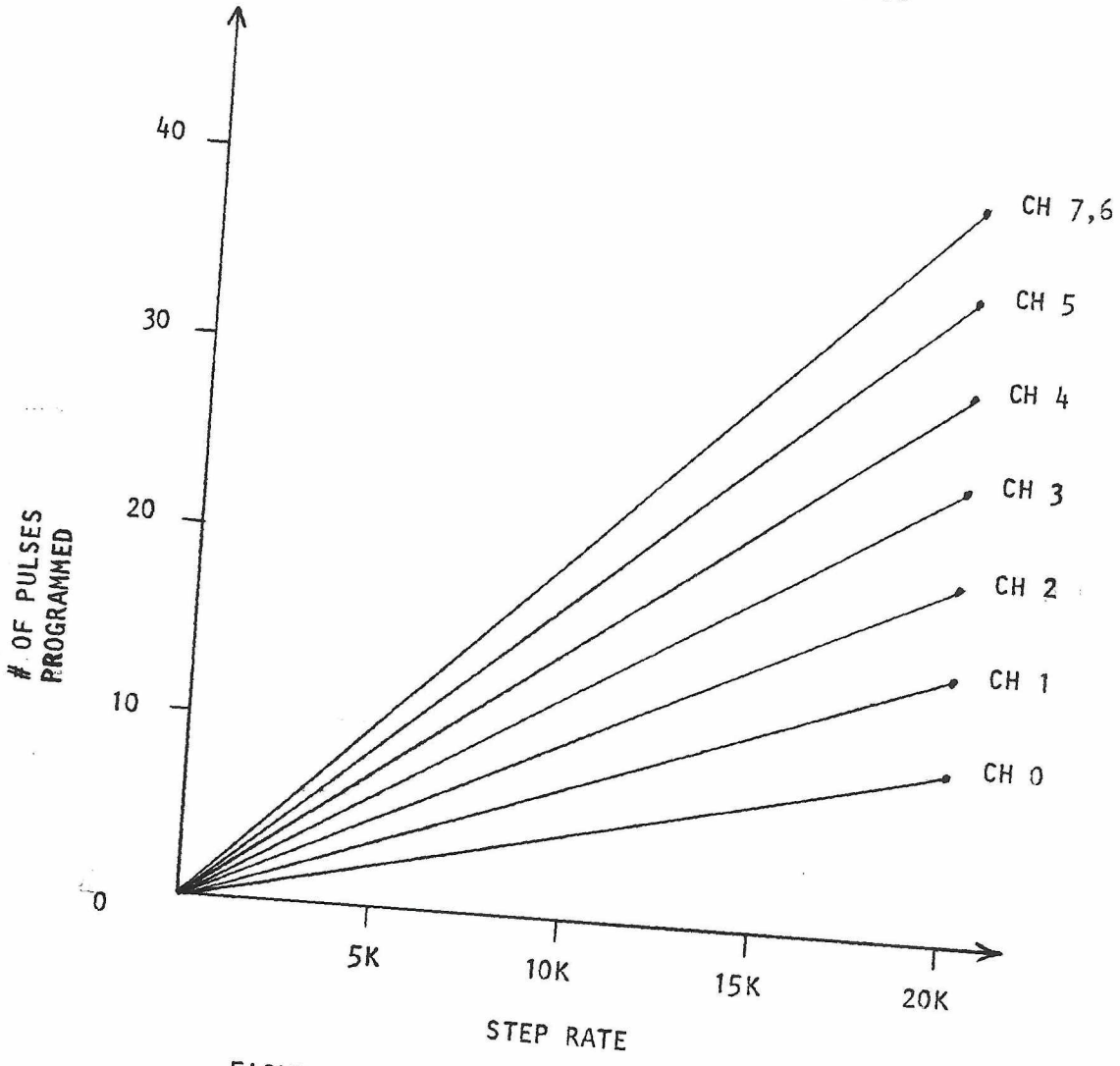


FIGURE 2: BASE RATE ALTERATION CURVE

While the magnitude is programmable as a relative quantity, the position of the motor is reportable as an absolute quantity. The internal register dedicated to maintaining a picture of the motor"s position is the absolute accumulator. The initial value of this register (one for each channel) is programmable via the dataway. In fact the value can be changed at any time but this is probably not desirable. The accumulator is a 24 bit sign plus magnitude number. The accumulator is updated after every operation to reflect the true position of the motor. An exception occurs when an EXECUTE command is issued before an operation is complete. See section 3.1.2 for further details.

1.3.7 Segmenting the Velocity Profile

The E500A implements the ramp up and ramp down process as a series of discrete pulse rates each faster or slower than the

preceding one. In the limit, this approaches the ideal "analog" ramp function characteristic of previous controllers. Before an operation can begin, the module firmware must build a file of data from which to execute this segmented velocity profile. The number of segments used, the length of each, the rate in pulses per second of each segment, are all variables which depend entirely on the programmed parameters.

The mathematical algorithm which converts the programmed parameters into the data file is complex and is beyond the scope of this manual. However it is useful to become familiar with some of its characteristics. The larger the number of segments, the better the approximation to the ideal accel/decel curve. The number of segments (max 48) depends in a complex way upon the product of the accel time and the slew rate. The larger these two quantities, the more segments, and the lower the beginning frequency for the cycle. Each segment is of a nearly equal duration. The segmentation algorithm always provides for a symmetrical ramp even if there is insufficient magnitude to achieve the programmed steady state slew rate. Each segment must contain at least two complete cycles, therefore rapid accel times at low slew rates are a fundamental problem coped with by the algorithm.

2. SPECIFICATIONS

This section contains the general specifications of the E500A module. Additional information on the command set can be found in Chapter 3.

2.1 MECHANICAL

The E500A conforms to all mechanical specifications for a single width CAMAC card. The front panel shown in figure 3 contains only four connectors and the jack screw. The module weighs 1.5lbs.

2.2 ELECTRICAL

The E500A is fully compatible with the IEEE 583 (CAMAC) buss standard. All mandatory functions are implemented.

2.2.1 Power Consumption

The E500A uses both +6 volt and +24 volt power. The average drain at +6 volts with all counters operating, logic level selected at +5 and with TTL loads applied is 3 amperes. The main module (E500A) does not use +24 volts unless this logic level is selected or unless the remote control pod is connected. The average drain from +24 volts with all counters running and nominal termination panel loads applied is 0.16 amperes. The remote pod draws an additional average of 0.35 amperes.

2.2.2 Connectors

All four connectors on the E500A utilize 20-pin flat ribbon cable connectors of the insulation displacement variety. The module uses male connectors, as do the SEC termination panels. Table 1 shows the pinouts for each connector.

CONNECTOR PINOUT TABLE

J1	1	GROUND
	2	GROUND
	3	CHANNEL 0 MOTOR DIRECTION
	4	CHANNEL 0 PULSE TRAIN OUTPUT
	5	CHANNEL 1 MOTOR DIRECTION
	6	CHANNEL 1 PULSE TRAIN OUTPUT
	7	CHANNEL 2 MOTOR DIRECTION
	8	CHANNEL 2 PULSE TRAIN
	9	CHANNEL 3 MOTOR DIRECTION
	10	CHANNEL 3 PULSE TRAIN
	11	CHANNEL 4 MOTOR DIRECTION
	12	CHANNEL 4 PULSE TRAIN
	13	CHANNEL 5 MOTOR DIRECTION
	14	CHANNEL 5 PULSE TRAIN
	15	CHANNEL 6 MOTOR DIRECTION
	16	CHANNEL 6 PULSE TRAIN
	17	CHANNEL 7 MOTOR DIRECTION
	18	CHANNEL 7 PULSE TRAIN
	19	+24 VOLTS
	20	+24 VOLTS

J2 Connector J2 has the same pinouts as J1, but corresponding to the signals returning from the remote shaft encoder. +24 volts does not appear on the connector.

J3	1	GROUND
	2	GROUND
	3	CHANNEL 0 CCW LIMIT
	4	CHANNEL 0 CW LIMIT
	5	CHANNEL 1 CCW LIMIT
	6	CHANNEL 1 CW LIMIT
	7	CHANNEL 2 CCW LIMIT
	8	CHANNEL 2 CW LIMIT
	9	CHANNEL 3 CCW LIMIT
	10	CHANNEL 3 CW LIMIT
	11	CHANNEL 4 CCW LIMIT
	12	CHANNEL 4 CW LIMIT
	13	CHANNEL 5 CCW LIMIT
	14	CHANNEL 5 CW LIMIT
	15	CHANNEL 6 CCW LIMIT
	16	CHANNEL 6 CW LIMIT
	17	CHANNEL 7 CCW LIMIT
	18	CHANNEL 7 CW LIMIT
	19	N.C.
	20	N.C.

J4	1	GROUND	
	2	GROUND	
	3	CW LIMIT LED INDICATOR	
	4	CCW LIMIT LED INDICATOR	
	5	REMOTE CONTROL DIRECTION (+)	
	6	REMOTE CONTROL DIRECTION (-)	
	7	REMOTE CONTROL REQUEST (+)	
	8	REMOTE CONTROL REQUEST (-)	
	9	MUX ADDRESS A (+)	
	10	MUX ADDRESS A (-)	
	11	MUX ADDRESS B (+)	
	12	MUX ADDRESS B (-)	
	13	MUX ADDRESS C (+)	
	14	MUX ADDRESS C (-)	
	15	REMOTE CONTROL ENABLE (+)	OUTPUT
	16	REMOTE CONTROL ENABLE (-)	OUTPUT
	17	REMOTE CONTROL PULSE (+)	
	18	REMOTE CONTROL PULSE (-)	
	19	+24 VOLTS	
	20	+24 VOLTS	

TABLE 1

2.2.3 Logic Levels

In general logic levels are set by a jumper option as explained in section 1.2.2. Connector J4, however, always is set to RS-422 logic levels. When the +5 volt option is enabled, (TTL) outputs are capable of driving 1 normal TTL load (4.7K resistor pull up on open collector gate). Inputs at either logic level exhibit 4.7 kohm input impedance.

2.2.4 Data Rates

Although the E500A is compatible with CAMAC systems, sequential commands cannot be issued to the module at the full Dataway rate (1Mhz). This is because the commands are interpreted and executed by an internal microcomputor which runs at a slower rate than the Dataway. The rate at which commands can be accepted by the module depends upon the particular command, previous commands and the number of channels operating and the parameters entered into each channel. For this reason, the Q bit must be monitored to insure that the issued command has been accepted and is being acted upon.

2.3 ACCURACY

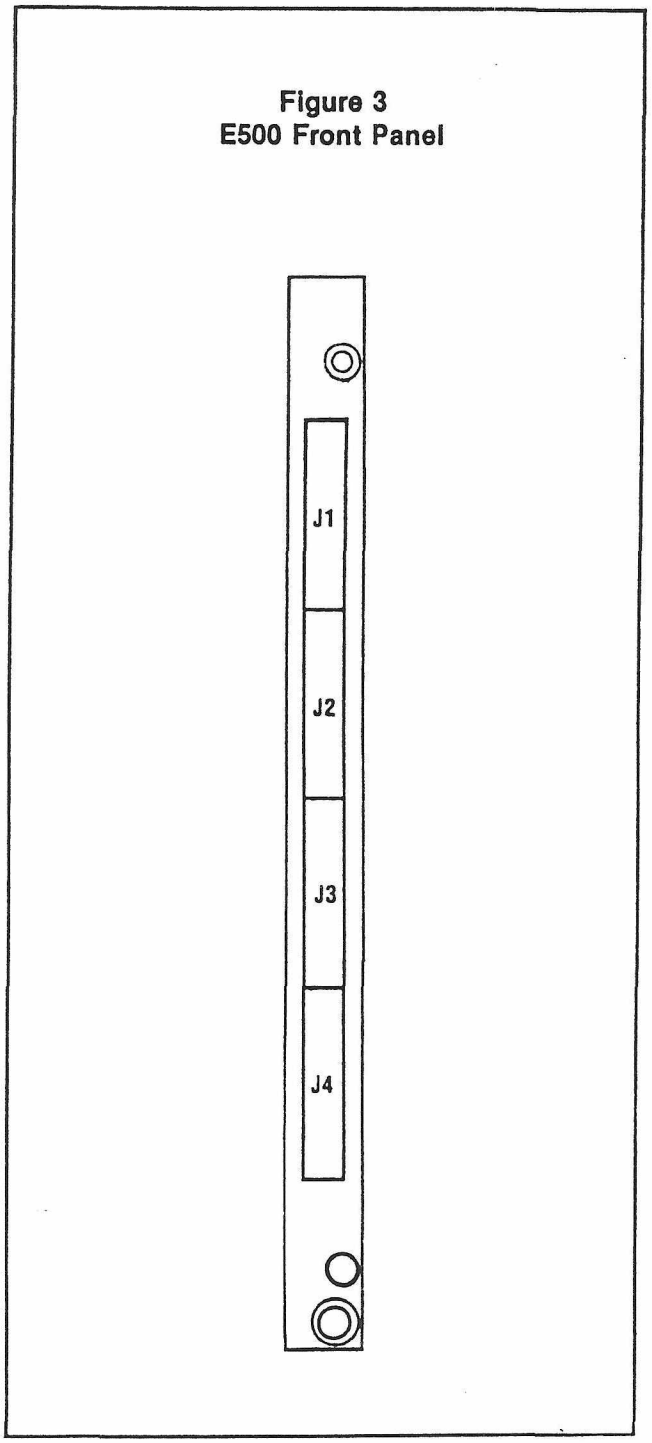


Figure 3
E500 Front Panel

In the E500A accuracy can be described in relation to the three programmable parameters of MAGNITUDE, SLEW RATE, AND ACCEL/DECEL TIME. The magnitude is the highest priority parameter and every effort is made to output exactly the correct number of pulses. In the absence of a correction cycle (correction limit = 0), the module normally provides the correct

pulse count except for the "undercount" phenomenen described in section 1.3.5. The correction cycle will correct for such errors.

The accuracy of the programmed slew rate depends upon the actual values. At the highest slew rate (20,000 pps), the maximum error is less than 7%, decreasing roughly in proportion to frequency. At rates around 2,000 pps the error is less than 1%. At yet lower rates, accuracy is limited by the internal crystal. If the programmed parameters do not permit reaching steady state velocity, accuracy has no meaning.

Accuracy of acceleration/deceleration is complex, being dependent upon the actual values of magnitude, slew rate and time. If the magnitude is insufficient for the entire accel/decel period, accuracy suffers. In general, the higher the slew rate and the larger the accel/decel time, the more accurate the ramp function. These are the same conditions that create a larger number of finitely small steps and a smooth ramp. Under most normal conditions, the accel/decel time accuracy is 2% or better.

3. PROGRAMMING

3.1 COMMAND SET

The following sections describe in detail the function of each command implemented by the E500A. Recall that due to response time of the internal microprocessor, the controller must monitor the Q line to be certain that the module was able to accept and act upon the command.

3.1.1 F(0)A(i): READ MAGNITUDE REGISTER i or CSR i or BASERATE i

The exact function of this command depends on a preceeding execute command. If an F(25)A(0) had been issued, this command will read the number of pulses yet to be taken on channel i based on the previously programmed relative magnitude. If the operation is complete, this number will be zero. This command is used to get a "progress report" on slow stepping operations. Be aware that the information may be old depending on the length of time elapsed between the execute and read commands.

If the previous execute command was an F(25)A(1), this command will read the CSR for channel i. Section 3.2 describes the makeup of the CSR in detail.

If the previous execute command was an F(25)A(4), this command will read the programmed and actual base rates for channel i. The programmed rate appears in the high byte and the actual rate appears in the low word.

Q=1 implies valid data was received

3.1.2 F(0)A(i+8): READ ABSOLUTE ACCUMULATOR i or PULSE PARAMETER REGISTER i

As before, the meaning of the command depends on the previous execute command. If F(25)A(0) had been issued, this command will read the absolute accumulator for channel i in sign plus magnitude format. In the case of a previous F(25)A(1), the pulse parameter register would be read. The pulse parameter register contains both the slew rate and accel/decel time last programmed for channel i. The format is as follows:

Bits 1 to 16: Slew rate in PPS, 5 to 20,000.
Bits 17 to 24: Accel/Decel time in 10's of msec.

3.1.3 F(1)A(x): READ MODULE ID CODE (500)

This command will read the decimal value 500 in the lower 16 bits and the firmware revision level in the upper 8 bits provided an F(25)A(2) command has been issued immediately prior. A(x) indicates that any subaddress will yield the same result. The ID code may also be read immediately following initialization, either power on or dataway Z.

3.1.4 F(16)A(i): WRITE RELATIVE MAGNITUDE i

This command is used to write the 24 bit sign plus magnitude value for magnitude corresponding to channel i. Recall that this is a relative write operation where a positive value represents clockwise rotation and a negative value represents counterclockwise rotation. As with all commands, the Q bit must be monitored to assure the controller that the command was processed.

3.1.5 F(16)A(i+8): WRITE ABSOLUTE ACCUMULATOR i

This command permits the controller to set the current value of the absolute accumulator for channel i. Typically this is done once after power up in conjunction with a known positioning of the stepper motor. If the position of the motor is to be remembered through a power outage, the absolute accumulator should be stored in non-volatile memory and reloaded after power up.

3.1.6 F(17)A(i): WRITE CSR i

This command writes data into the CSR for channel i. Only some of the bits in the CSR are writable. The remainder will be ignored. The makeup of the CSR is detailed in section 3.2

3.1.7 F(17)A(i+8): WRITE PULSE PARAMETER REGISTER i

This command simultaneously writes the accel/decel time and the slew rate into the pulse parameter register. Section 3.1.2 outlines the makeup of the pulse parameter register.

3.1.8 F(25)A(0): LOAD MAGNITUDE COUNTS AND ABSOLUTE ACCUMULATORS

This command loads 16 locations of dual ported memory which can be read from the dataway using the appropriate F(0) commands. The first eight locations contain the remaining magnitude counts as described in section 3.1 above. The second eight locations contain the absolute accumulator values for the eight channels. Keep in mind that the data

read via the F(0) commands is only as recent as the last corresponding F(25) EXECUTE command.

3.1.9 F(25)A(1): LOAD CSR AND PULSE PARAMETER REGISTERS

This command loads the lower eight locations of the dual ported memory with the current CSRs for all channels, and the upper eight locations with the current values of the pulse parameter registers for all channels.

3.1.10 F(25)A(2): LOAD MODULE ID

This command loads all locations of the dual port memory with the module ID number (500 decimal) and firmware version (currently 20 representing version 2.0).

3.1.11 F(25)A(3): SIMULTANEOUS START

This command causes all channels not currently moving to start moving.

3.1.12 F(25)A(4): LOAD BASE RATE

This command causes the lower eight locations of the dual port memory to be loaded with the base rate as described in section 3.1.1.

3.1.13 F(25)A(i+8): GO TO HOME

This command causes channel i to return to its "home" position, that is the location where the Absolute Accumulator is zero. The current values for Accel/Decel time, Stepping Rate, Base Rate and Correction Limit are used to build a file with sufficient magnitude and direction to move the motor to the zero position.

The HOME command causes a new file to be built thus destroying the previous file. If a START command is issued following a HOME, the file created for the HOME command will be executed causing the motor to move off zero in the opposite direction.

A HOME command issued while the Absolute Accumulator is zero will issue no pulses but will build a zero magnitude file.

3.2 CONTROL AND STATUS REGISTER MAKEUP

The CSR for each channel consists of 24 bits broken down into three 8-bit fields. Two of the three fields implement different functions for writing and reading.

3.2.1 High Byte: Bits 17 to 24

READ - LAM Status

The upper eight bits of the CSR report the status of LAM on each channel. This enables you to quickly determine which channel generated the LAM. This LAM status is NOT conditioned by the LAM mask bits.

WRITE - Base Rate

The base rate is specified in units of 10 pps with a range of 10 to 2550 pps. A value of 0 means that the control algorithm should determine the base rate.

3.2.2 Middle Byte: Bits 9 to 16

This byte is the same for both reading and writing and implements the correction limit, the maximum number of steps the module will correct during the correction cycle. The minimum is 0 and the maximum is 255.

3.2.3 Low Byte: Bits 1 to 8

This byte implements miscellaneous control and status functions as follows:

BIT	CONTROL (WRITE)	STATUS (READ)
8	IMMEDIATE ABORT	CCW LIMIT
7	SOFT ABORT	CW LIMIT
6	ABS. ACCUM UNDERFLOW RESET	ABS. ACCUM. UNDERFLOW
5	ABS. ACCUM. OVERFLOW RESET	ABS. ACCUM. OVERFLOW
4	RESERVED	CORRECTION FAILURE
3	BUILD FILE	BUSY
2	START	ILLEGAL INSTRUCTION
1	LAM MASK	LAM MASK

WRITE

IMMEDIATE ABORT: A 1 causes the module to execute an immediate abort on the channel addressed. Output pulses will be immediately terminated (within the latency time of the Dataway polling cycle), the operation aborted, and the absolute accumulator updated. All of the programmed parameters will be left intact.

SOFT ABORT: A 1 causes the module to execute a soft abort (within the latency time of the Dataway polling cycle). The module will immediately begin a deceler-

ation cycle unless already in this portion of the operation, in which case the deceleration continues. The absolute accumulator is updated, and the LAM set if not masked.

ABSOLUTE ACCUMMULATOR UNDERFLOW RESET: A 1 clears a preexisting underflow condition. This has no effect on the contents of the absolute accumulator. This is used for extending the range of the accumulator to beyond 24 bits.

ABSOLUTE ACCUMULATOR OVERFLOW RESET: This is the complement of the above.

BUILD DATA FILE: A 1 causes the module to build a data file based on the parameters previously programmed. This operation is defined separately from the start function since it is a lengthy process and will increase the latency time to actual motor movement.

Note: It is not necessary to BUILD DATA FILE again unless the parameters are changed.

START: A 1 begins the process of executing the current data file which in turn initiates motor movement. This operation will always execute the last data file built, not the last parameters entered.

LAM MASK: A 1 sets the LAM mask preventing this channel from asserting the module's L line. A 0 clears the mask.

READ

CCW LIMIT: A 1 indicates the current presence of a counterclockwise limit (within the latency time of the polling cycle).

CW LIMIT: Same as above for the clockwise direction.

ABSOLUTE ACCUMULATOR UNDERFLOW: A 1 indicates that the absolute accumulator has decremented beyond negative 2**23-1 or 7FFFFF hexidecimal.

ABSOLUTE ACCUMULATOR OVERFLOW: A 1 indicates that the absolute accumulator has incremented beyond 2**23-1 or FFFFFF hexidecimal.

CORRECTION FAILURE: A 1 indicates that the number of pulses returned to the input counter was different from the number of pulses output by an amount larger than the correction limit, or that the correction cycle was attempted and failed to completely correct.

BUSY: A 1 indicates that the internal microcomputor is engaged in executing an operation on the addressed channel.

ILLEGAL INSTRUCTION: A 1 indicates that the module has received a valid instruction which it cannot execute at this time. For example, if a channel is engaged in an operation (busy bit set) and the Dataway requests another operation to that channel, the illegal instruction bit will be set. This bit is reset when an acceptable command is issued.

LAM MASK: A 1 indicates that the LAM mask is set, 0 means it is cleared.

3.3 LAM GENERATION AND HANDLING

The E500A provides a comprehensive LAM generating facility. Knowledge of how these LAMs are generated and controlled is necessary for the efficient use of the module.

Each channel has associated with it a LAM mask bit in the CSR. Setting this bit will prevent LAMs from being generated by the associated channel reguardless of the originating condition. This is an immediate function and preexisting LAMs can be disabled by setting the mask bit. The LAM status shown in the CSR is gated by the LAM mask such that only enabled LAMs are read in the CSR.

LAM status is set by a variety of conditions and is not cleared until a new operation is STARTed. Therefore, channels not busy must have their LAMs masked to avoid spurious interupts. After STARTing an operation, the mask bit should be cleared to enable the proper LAM. It is possible that the controller may reenable LAMs (clear mask bit) before the E500A CPU can reset LAM status. For this reason, the controller should always check the busy bit and LAM status register to insure that the LAM was genuine.

LAMs can result from any of the following conditions on any channel. The controller must determine the true source of the LAM by examining the appropriate CSRs.

1. Completion of the operation, whether or not correction was attempted, regardless of success.

2. On termination of an abort sequence.

3. If a limit is encountered. In this case, the limit fault must be resolved before the LAM status can be reset.

NOTE: Absolute accumulator overflow or underflow does NOT generate a LAM and thus the controller should scan for this information in the CSRs.

3.4 INITIALIZATION

Dataway Z causes the internal processor to issue a hardware RESET to all of its peripherals and then set up all peripherals as required.

WARNING

The "Z" must be a single CAMAC cycle. If the "Z" is manually originated, or is extended beyond one Dataway cycle by the crate controller, the dataway decode circuitry will be held disabled through the processor's RESET. Consequently the processor will be unable to respond to subsequent dataway cycles. This has the appearance from the dataway of a completely unresponsive module that does not return Q. The only escape from this condition is to power down the module and repower it.

4. E450 TERMINATION PANEL

4.1 FUNCTIONAL DESCRIPTION

The E450 and E455 Termination Panels interface the E500A to the wide variety of available motor translators and shaft encoders with a minimum of difficulty. The E450 provides the following seven functions:

1) Optical isolation and level shifting
2) Output format conversion if required
3) Input format conversion if required
4) Limit switch simulation if required
5) Output/input loop back (no shaft encoder available)
6) Channel selection
7) Field wiring support

Optical isolation is important in the industrial environment where heavy inductive loads can induce large common mode transients in field wiring. Optical isolation on all inputs and outputs provide a large measure of protection from these faults.

While the E500A was designed to interface to translators using the Pulse/Direction input format, a significant number of translators require the CW pulse/CCW pulse format. The E450 provides either format, switch selectable.

Shaft encoders are available in an even wider variety of interfaces. The three most common are CW pulse/CCW pulse, pulse/direction, and the direct quadrature output format. Each of these is supported directly, again by switch selection. Choice of format as well as all operating parameters are selectable on a channel by channel basis.

The E500A supports a comprehensive limit switch capability, but if these switches are not used (or if only one direction has limits), unused inputs must be grounded to allow the module to operate properly. Switches are provided on the E450 for this purpose.

If shaft encoders are either not available or not desired, it is necessary to loop the E500A outputs back to the inputs provided for the shaft encoders. This too can be easily done on a channel by channel basis using switches. Very inexpensive non-direction sensing incremental encoders can be handled by looping back only the direction information.

The E450 is set up as a four channel device, supporting all input and output functions for one half of an E500A module. Support of all channels requires one E450 and one E455 panel. The E450 is factory set to interface channels 0 through 3 of the E500A, while the E455 is set for channels 4 through 7. While this addressing arangement should be satisfactory for most applications, any E500A channel can be assigned to any E450 channel by altering a series of jumpers.

Finally, the E450, in common with all of SEC's termination panels supports large gauge field wiring using universally accepted 6-32 screw barrier strips. This provides ruggedness as well as convenience and flexibility.

4.2 CONFIGURATION

A number of operating parameters may be altered on a channel by channel basis by means of DIP switches. Each channel has two groups of switches; a set of four double throw switches labelled SW1 and a set of eight single throw switches labelled SW2. For quick reference the function of each switch is labelled on the PC board.

4.2.1 Addressing

The E450 is factory set to interface channels 0 through 3 of the E500A, while the E455 is set for channels 4 through 7. The address selection is accomplished through a set of 24 jumpers located adjacent to the three flat cable connectors. See assembly drawing 240450. Any of the four ports can be changed from its E450 channel address to the equivalent E455 address or vice-versa by restoring the cut trace with a jumper and cutting the opposite trace as shown on the assembly drawing.

4.2.2 E500A Logic Levels

The E500A supports two logic levels: TTL (5 volt) and high level (24 volt). The E450 has been designed to accept either level interchangably. The logic level of the host E500A need not be changed, however the current drain from the +24 volt supply can be drastically reduced if the TTL level is used.

4.2.3 Output Formatting

The E500A module is designed to output pulse and direction information to the user supplied translator. While many translators accept this format, others require CW pulses on one line and CCW pulses on another. Switches 5 and 6 on switch pak SW2 control this format. Setting both switches ON

selects pulse/pulse format while setting both switches OFF selects pulse/direction mode.

In pulse/direction mode, the pulses appear at the A output and the direction appears at the B output. In pulse/pulse mode, A is the CCW output and B is CW.

4.2.4 Input Formatting

The E450 supports three different formats for shaft encoder input:

pulse/direction
pulse/pulse
quadrature

The first two are as described in the previous section. Quadrature input consists of two square waves phase shifted by 90 degrees with respect to each other. The relative phase shift, that is which signal "leads" and which "lags", determines the direction of rotation.

Input format is selected by SW1, a 4-pole, double throw DIP switch, according to the following table:

Mode	SW1-1	SW1-2	SW1-3	SW1-4
Pulse/pulse	C	P	C	C
Pulse/Dir.	C	C	P	C
Quadrature	P	C	C	P

C means the switch is detented towards the rear connectors,
P means it is detented towards the front panel.

In pulse/pulse mode, input A accepts the CCW pulse and input B accepts the CW pulse. In pulse/direction mode, input A is pulse and input B is direction. In quadrature mode, the phase which lags during CW rotation is connected to input A and the other phase is connected to B.

In order for the E500A to respond properly to quadrature encoders, the phase which lags during CW rotation must supply current to its input LED while at rest. This may require some adjustment of the encoder-to-motor coupling. This will insure that the pulse input to the E500A rests in a logic high state. The input logic in the pulse/pulse and pulse/direction format is such that normally current should not be flowing through the input LED until a pulse is activated. The direction channel (pulse/direction) does not matter in this regard.

4.2.5 LoopBack

If a shaft encoder is not available or not required, the E450 provides a convenient method for looping back the pulse and direction output signals to the corresponding inputs as required by the E500A. Direction and pulse information can be looped back separately. This is useful if the shaft encoder provides movement pulses but no direction information. The direction bit would then be looped back with the pulse train supplied by the encoder.

Loopback is controlled by switches 3 and 4 of SW2. Setting switch 3 ON loops back the pulse output and setting switch 4 ON loops back direction.

A word of caution about loopback. The input and output formats must agree i.e. both must be pulse/pulse or pulse/direction. Quadrature input must not be selected with loopback. Furthermore, if loopback is enabled, do not apply any signals to the shaft encoder inputs.

4.2.6 Limit Switch Simulation

The E500A requires that limit switch inputs be pulled to a logic low state for normal operation. Open inputs float high thus inhibiting operation if a wire breaks. If limit switches are not used or if only one is used, the remaining inputs must be handled. Setting switches 1 and 2 of SW2 to ON disables respectively the CCW and CW limit switch inputs.

4.3 INSTALLATION

4.3.1 Cabling

Like all Quantrol modules and panels, the E450 and E455 connect to the E500A through 20 conductor flat ribbon cables. J1, J2 and J3 on the E450 and E455 correspond directly to J1, J2 and J3 on the E500A.

Support of all eight channels of an E500A requires both an E450 and an E454. The two panels are wired in parallel to the E500A. The E450 is shipped with three "daisy-chain" cables (SEC part number 150555) to implement this connection. These are 8 foot cables with a third connector mounted approximately 2 feet from one end. This 2 foot section is installed between the panels and the 6 foot section goes from the panels to the module.

Note that the E455 is normally shipped without cables.

4.3.2 External Connections

The E450 panel is divided into four "ports" labelled A to D. As shipped from the factory, these ports correspond to E500A channels as follows:

	Channel	
Port	E450	E455
A	0	4
B	1	5
C	2	6
D	3	7

Translator outputs are standard optical isolators. Both the emitter and collector outputs are available on the front panel. The LED exciters for these devices are driven such that the output will sink or source up to 3ma or two standard TTL loads. When used in a common emitter circuit, the output will be normally high (CCW direction or no pulse) and be active low. This polarity can be inverted by connecting the output in a common collector configuration.

The IN (shaft encoder) and LIMIT inputs are each the LED of an optical isolator in series with a 180 ohm resistor and shunted by 1.5 kohms. The LEDs must be driven with about 6 to 8 ma of current. As the unit comes from the factory, this requirement is met when interfacing the limits and shaft encoder inputs to a TTL source. When voltage excitation at higher levels is used, additional series resistance MUST be provided. For each additional volt over 5 that is applied, an additional 120 ohms of resistance must be provided. For example, if 12 volt excitation is used, the extenal resistor should be (12-5)*120 = 840 ohms. 820 ohms is the nearest standard value and is acceptable.

Limit switch inputs will support either normally open or normally closed switches using either a shunt or series arrangement respectively. If solid state devices are used, an open collector arrangement will provide the most flexibility.

5. OPTIONAL REMOTE CONTROL POD

An optional remote control pod is available for the E500A which will allow the operator to manually adjust the position of any motor from a remote location. This option is not required for normal operation of the module in conjunction with the Dataway.

5.1 FUNCTIONAL DESCRIPTION

The E505 provides the capability to manually initiate the following functions on any of the eight channels:

Select a channel 0-7
Single step the channel
Step at a low-range speed, potentiometer adjustable
Step at a high range speed, potentiometer adjustable
Observe the presence of a CW or CCW limit via LEDs

The E505 is connected to the E500A via a 20-pin flat ribbon cable with female connectors on both ends. A 20 foot mating cable is supplied with the E505 which may be located up to 100 feet from the main module.

5.2 OPERATOR CONTROLS

The E505 has three switches and two potentiometers.

5.2.1 Channel Select

This 8-position rotary switch selects one of the eight E500A stepper motor channels to be controlled by the E505.

5.2.2 Step Mode

This 4-position rotary switch selects the operation that will be performed when the direction switch is activated. The choices are:

HI	Step at the rate set by the HI range pot
LO	Step at the rate set by the LO range pot
SS	Execute one step each time the direction switch is activated.
EXT	Step rate is controlled by an external source feeding the BNC connector next to the flat cable connector.

5.2.3 Direction

This is a 3-position center return toggle switch. When moved in either direction from center, the selected channel will move either clockwise or counterclockwise as selected by the Step Mode.

5.2.4 Velocity Pots

A screwdriver adjustable potentiometer is located on each side of the E505 pod for setting the velocities for the LO and HI step modes. The ranges are approximately as follows:

LO	1.5 to 150 steps/sec
HI	125 to 13000 steps/sec

5.3 INDICATORS

The E505 has four LED indicators as follows:

CCWL	Red	Indicates that counterclockwise limit is activated.
CWL	Red	Indicates that clockwise limit is activated.
ACTIVE	Yellow	Indicates that the E505 has control of the selected channel.
ON	Green	Indicates that the E505 is powered.

5.4 OPERATION

The E505 and the E500A execute a "handshake" protocol to insure that the Dataway cannot interfere with manual stepping and vice-versa. Pressing the direction switch left or right does not immediately begin an operation, but rather requests service from the microprocessor on the E500A module. The request is honored only after all pending Dataway operations initiated before the request are complete.

While a manual operation is in progress, the local microprocessor continues to track the position of the selected channel.

For example, if an operation has been requested and granted, the channel number may not be changed without the CPU negating the grant. The grant status (whether the channel is actually stepping) is shown by the LED shown at indicator 3. The channel to be stepped is determined by the setting of the channel switch shown at indicator 4. Select the channel before requesting an operation.

In general it is a good practice to suspend dataway operations before using the E505.

5.5 INTERFACE CONSIDERATIONS

The E505 and the E500A are connected via a 20 conductor cable using RS-422 drivers and receivers. The receivers are not normally terminated, but the artwork provides for terminations if required. The terminations may permit operation over very long distances if required. The voltage loss in the power conductors of the cable may well limit distance first.

6.0 APPLICATIONS INFORMATION

This section offers hints on the use of the E500A in the hope of avoiding surprises for the user. As field experience with this module increases, we expect to add material in this section.

6.1 OPERATION NEAR THE LIMIT AREA

The limit switch inputs are provided as a safety measure to prevent physical damage to the stepper motor, associated equipment or personnel. When a limit is encountered during an operation, the output pulse train immediately terminates and the CPU initiates a "hard abort" sequence. This sequence is triggered by a poll of the limit register which in turn has a latency associated with it. The abort will generate a LAM and the fact that a limit has occurred can be observed in the CRRs. If the limit switch subsequently deasserted itself (mechanical creep etc.) the CSR, after a polling interval, would no longer show the limit although the operation had halted and a LAM had been generated. Examination of the absolute accumulator can give useful information in this case. If a shaft encoder is not used, the absolute accumulator can only derive its information from the outgoing pulse train and may introduce significant errors in case a limit is encountered at high slew rates. Clearly this is not a normal mode of operation and should be avoided.

6.2 SHAFT ENCODER JITTER

The E500A determines absolute postion by monitoring the state of an input counter and a direction bit. The input counter is unidirectional and its count must be interpreted in light of the direction bit. If the bit exhibits jitter at a rate faster than the polling time of the CPU, information will be lost. Generally this is not a problem during normal stepping operations except perhaps at the end of cycle should the motor have a damped oscilation.

DSP Technology Inc.

SINGLE LEVEL BILL OF MATERIAL REPORT

Assembly: E500 (8 CH MICRO P STEPPER MOTOR CONTROL)
Revision: A6
As of: 12/09/89

Date: 12/12/89
Page: 1

	Component	Description	Qty Per	As of	Until	Reference
1.	0100-0472	RES 5% 1/4W CC RESISTOR R=4.7K	1.00	05/20/86	12/31/99	R2
2.	0100-0474	RES RC07 470K OHM 1/4W 5%	1.00	10/24/88	12/31/99	R1
3.	0100-0681	RES 5% 1/4W CC RESISTOR R=680	3.00	05/20/86	12/31/99	R3, R6. R7
4.	010015	CAP: CER 15PF 1KV CRL DD-150	1.00	05/20/86	12/31/99	C17
5.	010503	CAP: CER, .05UF, 12V CRL UK12-503	29.00	05/20/86	12/31/99	C4-C7, C9, C11-16, C19-C36
6.	010821	CAP: CER 820PF 1KV 20% ARCO CCD821	2.00	05/20/86	12/31/99	C10, C8
7.	013330	CAP: AX TANT KEMET T110B336K010AS	2.00	05/20/86	12/31/99	C1, C2
8.	0200-0472	RPK RES PK BNS 4308R-101-472	9.00	01/01/88	12/31/99	RA6-RA13, RA17
9.	056510	RES: 8PIN BNS 4308R-101-681	4.00	05/20/86	12/31/99	RA1-RA3, RA5
10.	056523	RES: SIP 8 PIN BNS 4308R-102-473	8.00	05/20/86	12/31/99	RA4, RA18-RA24
11.	056526	RES: SIP 8PIN BNS 4308R-102-121	3.00	05/20/86	12/31/99	RA14, RA16, RA25
12.	0600-0475	C TANT 4.7MF 10% 35V	2.00	05/20/86	12/31/99	C3, C18
13.	060400	DIO: 1N4003	3.00	05/20/86	12/31/99	CR1, CR2, CR3
14.	060414	DIO: 1N4148	1.00	05/20/86	12/31/99	CR4
15.	062045	IC: SN7445	2.00	05/20/86	12/31/99	U66, U67
16.	064033	IC: 74LS33	1.00	05/20/86	12/31/99	U14
17.	066022	IC: MC3487	1.00	05/20/86	12/31/99	U70
18.	066024	IC: MC3486	2.00	05/20/86	12/31/99	U71, U72
19.	067138	IC: INTEL P8259A	1.00	05/20/86	12/31/99	U31
20.	067139	IC: INTEL P8284A	1.00	05/20/86	12/31/99	U29
21.	067140	IC: 8304	1.00	05/20/86	12/31/99	U30
22.	067144	IC: D8088 16 BIT	1.00	05/20/86	12/31/99	U20
23.	067254	ICS: 8254	8.00	05/20/86	12/31/99	U25-U28, U32-U35
24.	068040	CRYSTAL 15MHZ FOX #150	1.00	05/20/86	12/31/99	Y1
25.	069584	IC: 40106BE	8.00	05/20/86	12/31/99	U13, U17, U54-U56, U68 U69, U73
26.	078005	CONN: JUMPER, BUSSCO B5153-100-240T	2.00	04/13/87	12/31/99	
27.	106278	RAIL: GUIDE, MDL, 11 HOLE	2.00	05/20/86	12/31/99	
28.	111001	CONN: PIN, AUTOSW W228-025-400Q	3.00	05/20/86	12/31/99	E3, E4, E5
29.	120421	HDW:SCRW 4.40X3/8 ALN SKT BLK	2.00	05/20/86	12/31/99	
30.	120432	HDW: 4-40 X 3/8 PH 100 FLAT S.S	6.00	05/20/86	12/31/99	
31.	120440	HDW: SCREW 4-40 X 3/16 BHMS ZINC	4.00	05/20/86	12/31/99	
32.	122045	HDW: 4-40 KEP NUT ZINC	6.00	05/20/86	12/31/99	
33.	1750-0006	ICS SN7406	3.00	05/20/86	12/31/99	U60, U62, U64
34.	1760-0014	ICS SN74LS14	1.00	05/20/86	12/31/99	U12
35.	1760-0038	ICS SN74LS38	1.00	05/20/86	12/31/99	U4
36.	1760-0074	ICS SN74LS74	1.00	07/01/88	12/31/99	U11
37.	1760-0138	ICS SN74LS138	2.00	05/20/86	12/31/99	U44, U46
38.	1760-0151	ICS SN74LS151	10.00	05/20/86	12/31/99	U48-U53, U59, U61, U63 U65
39.	1760-0244	ICS SN74LS244	6.00	05/20/86	12/31/99	U15, U16, U37, U45, U58 U57
40.	1760-0259	ICS SN74LS259	1.00	05/20/86	12/31/99	U38
41.	1760-0373	ICS SN74LS373	10.00	05/20/86	12/31/99	U5-U8, U18, U19, U40 U41, U42, U43
42.	1760-0393	ICS SN74LS393	1.00	10/08/86	12/31/99	U47
43.	1770-0289	ICS SN74S289	6.00	05/20/86	12/31/99	U9, U10, U21-U24
44.	1910-0001	ICS HITACHI#HM6116P-3 200 NS	1.00	05/20/86	12/31/99	U2
45.	240022	PRM: M/F 1850-0003 E500 U3	1.00	05/20/86	12/31/99	U3
46.	240023	PRM: M/F 1850-0003 E500 U36	1.00	05/20/86	12/31/99	U36

| | Component | Description | Qty Per | As of | Until | Reference |

Assembly: E500 (8 CH MICRO P STEPPER MOTOR CONTROL)
Revision: A6
As of: 12/09/89

	Component	Description	Qty Per	As of	Until	Reference
47.	240024	PRM: M/F 1850-0003 E500 U39	1.00	05/20/86	12/31/99	U39
48.	240025	PRM: M/F 1852-2732, E500, UI, REV 2	1.00	05/20/86	12/31/99	U1
49.	240501	PCB: E500	1.00	05/20/86	12/31/99	
50.	240502	PNL: FT, E500	1.00	05/20/86	12/31/99	
51.	3100-0102	FUSE: PICO, 1AMP LITTLEFUSE 255001	1.00	08/11/86	12/31/99	F2
52.	3100-0402	FUS FUSE 4AMP LITTLEFUSE 251004	1.00	08/08/88	12/31/99	F1
53.	5000-0016	SKT CAMBION 703-1316-01-04-10	3.00	07/19/86	12/31/99	U3,36,39
54.	5000-0018	SKT CAMBION 703-1318-01-04-10	1.00	05/20/86	12/31/99	U29
55.	5000-0020	SKT CAMBION 703-1320-01-04-10	17.00	05/20/86	12/31/99	U5-U8,U15,U16,U18 U19,U30,U37,U40-U43 U45,U57,U58
56.	5000-0024	SKT CAMBION 703-1324-01-04-10	10.00	05/20/86	12/31/99	U2,U25-U28,U32-U35 U1
57.	5000-0040	SKT CAMBION 703-1340-01-04-10	1.00	05/20/86	12/31/99	U20
58.	5001-0028	SKT CAMBION 703-1328-01-04-10	1.00	05/20/86	12/31/99	U31
59.	5500-0020	CONN: HEADER 20PIN RA	4.00	05/20/86	12/31/99	
60.	6852-0001	SCR:FT PNL JCK DEUTCH D7500M4B4	1.00	05/20/86	12/31/99	
61.	6852-0002	PNL: CAMAC SIDE STD	1.00	10/02/86	12/31/99	

ASSEMBLY P/N E450 REV B
DESCRIPTION ISOLATED E500 INTERFACE PANEL

PART NUMBER	DESCRIPTION	QTY PER	AS OF	UNTIL	REFERENCE
0100-0121	RES 5% 1/4W CC RESISTOR R=120	16	10/10/86	12/31/99	R2-R5 4 PLACES
0100-0152	RES 5% 1/4W CC RESISTOR R=1.5K	8	10/10/86	12/31/99	R8,R9
0100-0471	RES 5% 1/4W RES R=470	9	10/10/86	12/31/99	R1(1PLACE)R6,R7(4P)
0100-0472	RES 5% 1/4W CC RESISTOR R=4.7K	4	10/10/86	12/31/99	R10
026409	SW: DIP 6 POSN C&K BD06	4	10/10/86	12/31/99	SW2
026410	SW: ROCKER DIP 4POS GRYHL 76SC04	4	10/10/86	12/31/99	SW1
040001	DIO: LED, RED STANLEY SAR 3931	24	10/10/86	12/31/99	DS1-DS6
056521	RES: DIP NTWK BNS 4116R-001-102	4	9/24/86	12/31/99	3C
0600-0475	C TANT 4.7MF 10% 35V	3	10/06/86	12/31/99	C3-C5
060400	DIO: 1N4003	16	10/10/86	12/31/99	CR1-CR4
060414	DIO: 1N4148	16	10/10/86	12/31/99	CR5-CR8
065111	IC: CNY17-4	24	9/24/86	12/31/99	1A-6A
069013	IC: 4013B	4	9/24/86	12/31/99	2C
069093	IC: 4093B	8	9/24/86	12/31/99	2B,5B
069107	IC: 40107B	8	9/24/86	12/31/99	5C,6B
071026	CONN: 20PIN HDR LOCKING	3	9/24/86	12/31/99	J1-J3
074020	CONN: 16POS TERMINAL BLOCK	1	9/24/86	12/31/99	
074021	CONN: 34POS TERMINAL BLOCK	1	9/24/86	12/31/99	
076550	CONN: MALE QUIK DISCONNECT	1	9/24/86	12/31/99	J4
1020-0751	DSZ DIODE SIL ZNR V=5.1 MOT IN751	1	10/10/86	12/31/99	CR9
120645	HDW: SCREW 6.32 X 3/4	6	9/24/86	12/31/99	
120652	HDW: SCREW 6.32 X 9/16	3	9/24/86	12/31/99	
122066	HDW: NUT #6 KEP	7	9/24/86	12/31/99	
150555	ASSY: CBL, FLAT	3	9/24/86	12/31/99	
2030-3412	ICA 12V POS REG NATIONAL LM340T-12	1	9/24/86	12/31/99	Q1

| PART NUMBER | DESCRIPTION | QTY PER | AS OF | UNTIL | REFERENCE |

ASSEMBLY P/N E450 REV B
DESCRIPTION ISOLATED E500 INTERFACE PANEL

PART NUMBER	DESCRIPTION	QTY PER	AS OF	UNTIL	REFERENCE
240043	BLK: MTG, E400	2	9/24/86	12/31/99	
240451	PCB: FAB, E450/E455	1	9/24/86	12/31/99	
240452	PNL: FT, E450	1	9/24/86	12/31/99	
DOCUMENTATION	PER ASSY DWG REFERENCE	2	9/24/86	12/31/99	240450-AD 240041-AD

SINGLE LEVEL BILL OF MATERIAL - by Part Number - for Assembly E450

PART NUMBER	DESCRIPTION	QTY PER	AS OF	UNTIL	REFERENCE

DSP Technology Inc.

SINGLE LEVEL BILL OF MATERIAL REPORT

Assembly: 240506 (ASSY: PWB, E505)
Revision: A
As of: 07/15/89

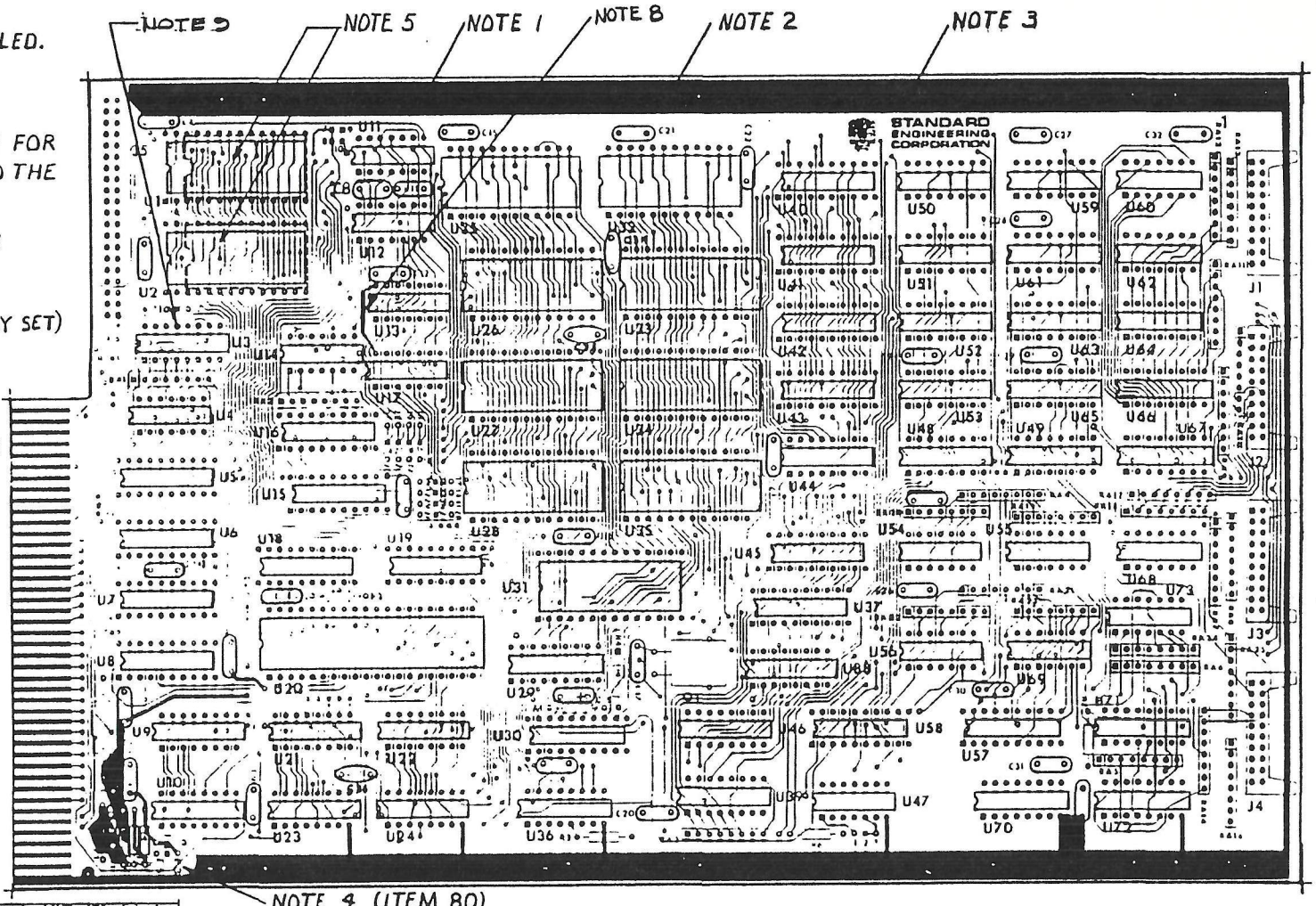
Date: 07/19/89
Page: 1

	Component	Description	Qty Per	As of	Until	Reference
1.	0100-0121	RES 5% 1/4W CC RESISTOR R=120	3.00	07/18/86	12/31/99	R1,R2,R6
2.	0100-0331	RES 5% 1/4W CC RESISTOR R=330	5.00	07/18/86	12/31/99	R3,R4,R7,R9,R13
3.	0100-0472	RES 5% 1/4W CC RESISTOR R=4.7K	5.00	05/21/86	12/31/99	R8,R10,R14,R15,R20
4.	0100-0681	RES 5% 1/4W CC RESISTOR R=680	6.00	05/21/86	12/31/99	R5,R16-R19,R23
5.	010503	CAP: CER, .05UF, 12V CRL UK12-503	4.00	05/21/86	12/31/99	C3,C8-C10
6.	040001	DIO: LED, RED STANLEY SAR 3931	2.00	05/21/86	12/31/99	DS3,DS4
7.	040003	DIO: LED, YEL HP HLMP1401	1.00	05/21/86	12/31/99	DS2
8.	040004	DIO: LED, GRN HP HLMP1501	1.00	05/21/86	12/31/99	DS1
9.	0525-0101	CDC C=100PF CERAMIC 1000WVDC SPRA	1.00	07/18/86	12/31/99	C7
10.	056046	RES VAR BNS 3006P-1-104	2.00	05/21/86	12/31/99	R11,R12
11.	057007	RES: 5W WW CLAROSTAT VC5E-12	2.00	05/21/86	12/31/99	R21,R22
12.	0600-0475	C-TANT 4.7MF 10% 35V	6.00	05/21/86	12/31/99	C1,C2,C4-C6,C11
13.	060414	DIO: 1N4148	3.00	05/21/86	12/31/99	CR1-CR3
14.	064148	IC: 74LS148	1.00	05/21/86	12/31/99	U1
15.	066022	IC: MC3487	2.00	07/18/86	12/31/99	U8,U9
16.	066024	IC: MC3486	1.00	05/21/86	12/31/99	U7
17.	067555	IC: M7555	2.00	05/21/86	08/01/88	U5,U6
18.	071026	CONN: 20PIN 3M 3428-1302	1.00	05/21/86	12/31/99	J1
19.	1760-0074	ICS SN74LS74	1.00	05/21/86	12/31/99	U3
20.	1760-0132	ICS SN74LS132	1.00	05/21/86	12/31/99	U2
21.	240507	PCB: E505	1.00	05/21/86	12/31/99	
22.	2080-7555	IC:ICM7555IPA	2.00	08/01/88	12/31/99	U5,U6
23.	0200-0472	RPK RES PK BNS 4308R-101-472	1.00	01/01/89	12/31/99	RA1

Component	Description	Qty Per	As of	Until	Reference
Assembly: 240506 (ASSY: PWB, E505)					

NOTES:

1. ENGRAVE Nº TO WHICH ASSEMBLED.
2. ENGRAVE SERIAL Nº.
3. ENGRAVE ECN Nº.
   ECN HISTORY MUST BE SHOWN FOR ALL ECNS INCORPORATED INTO THE ASSEMBLY.
4. USER SELECTABLE JUMPERS:
   E3 TO E4 : 24 VOLT LOGIC
   E4 TO E5 : 5 VOLT (FACTORY SET) LOGIC
5. INSTALL 24 PIN SOCKETS (ITEM 71) IN U1 & U2 TO THE FAR RIGHT. E500 (240500) U2 ONLY.
6. CUT E41 TRACE BETWEEN U4-12 AND U4-13 ON E500 (240500) ONLY. DO NOT CUT TRACE ON E503 (240503) SOLDER SIDE.
7. ON E503 (240503), THE SQUARE PADS OF CR1, CR2 & CR3 BECOME E38, E39 & E40.
8. INSTALL 30 AWG JUMPER FROM U13 PIN 14 TO U17 PIN 14 ON SOLDER SIDE.
9. DRILL & SLEEVE U3 [13]



A1	ECO 1007 (NOTE 9)	12/5/83	
A1	ECO # 610		
A1	ECO # 516	4/16/83	K.K
A1	ECO 481 ADDED CAP DESIGNATIONS	10/19/82	RG
A1	ECO 480 ADDED C8	10/7/82	RG
A1	SEE ECO 0269	5-28-82	
A	RELEASE	10-22-82	
11	RELEASE	1-8-82	
	DESCRIPTION		

REVISIONS

MATERIAL: SEE PARTS LIST PL 240500

FINISH:

DIMENSIONAL TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ANG
XX: ~ XXX: ~

SCALE 1:1 NO REQ ~

NEXT ASS'Y 400100 E 503 ONLY

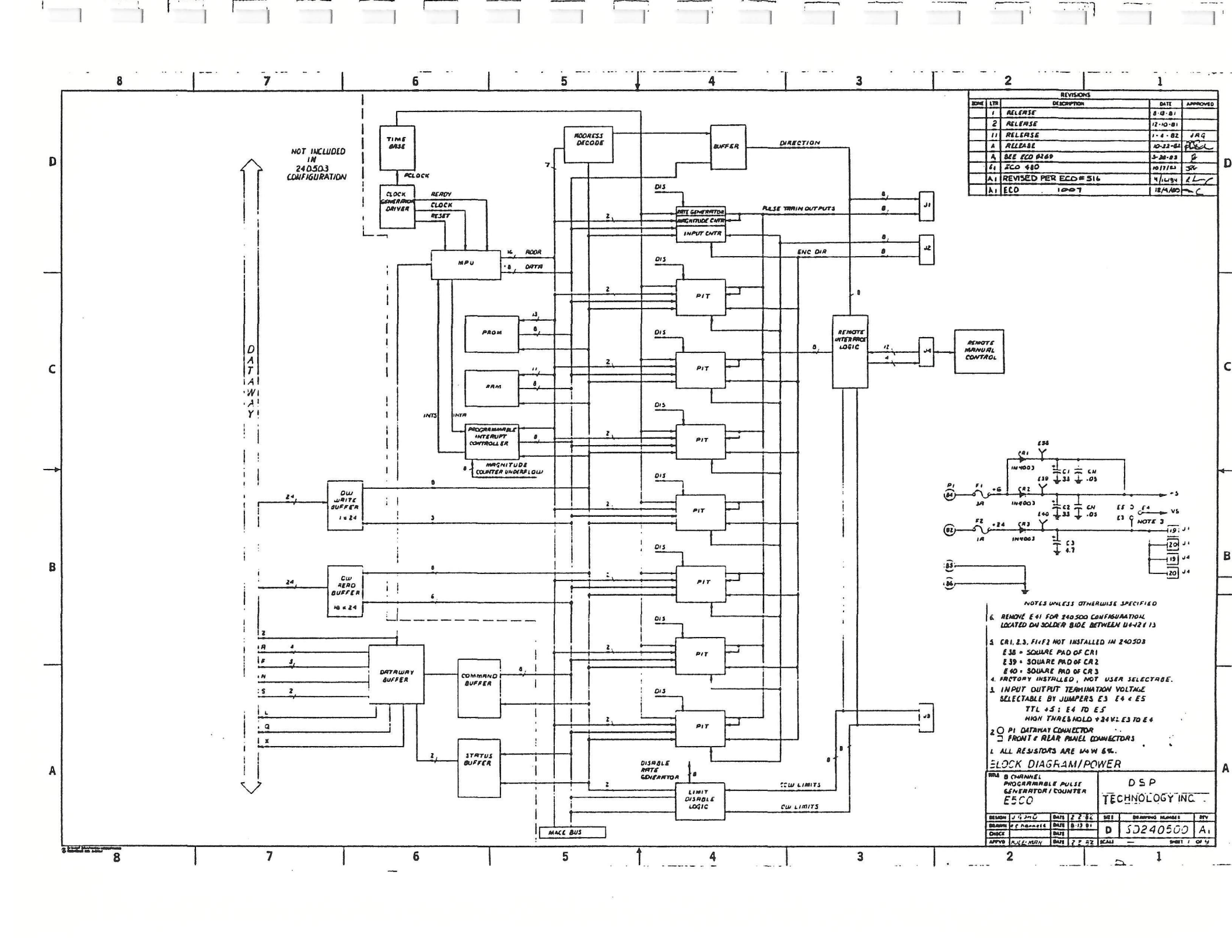
TITLE: ASSEMBLY P.C.B. E500 / E503

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DRAWN	C. Rugomez	DATE	10-22-82
CHECK		DATE	
APPR		DATE	5 NOV 82

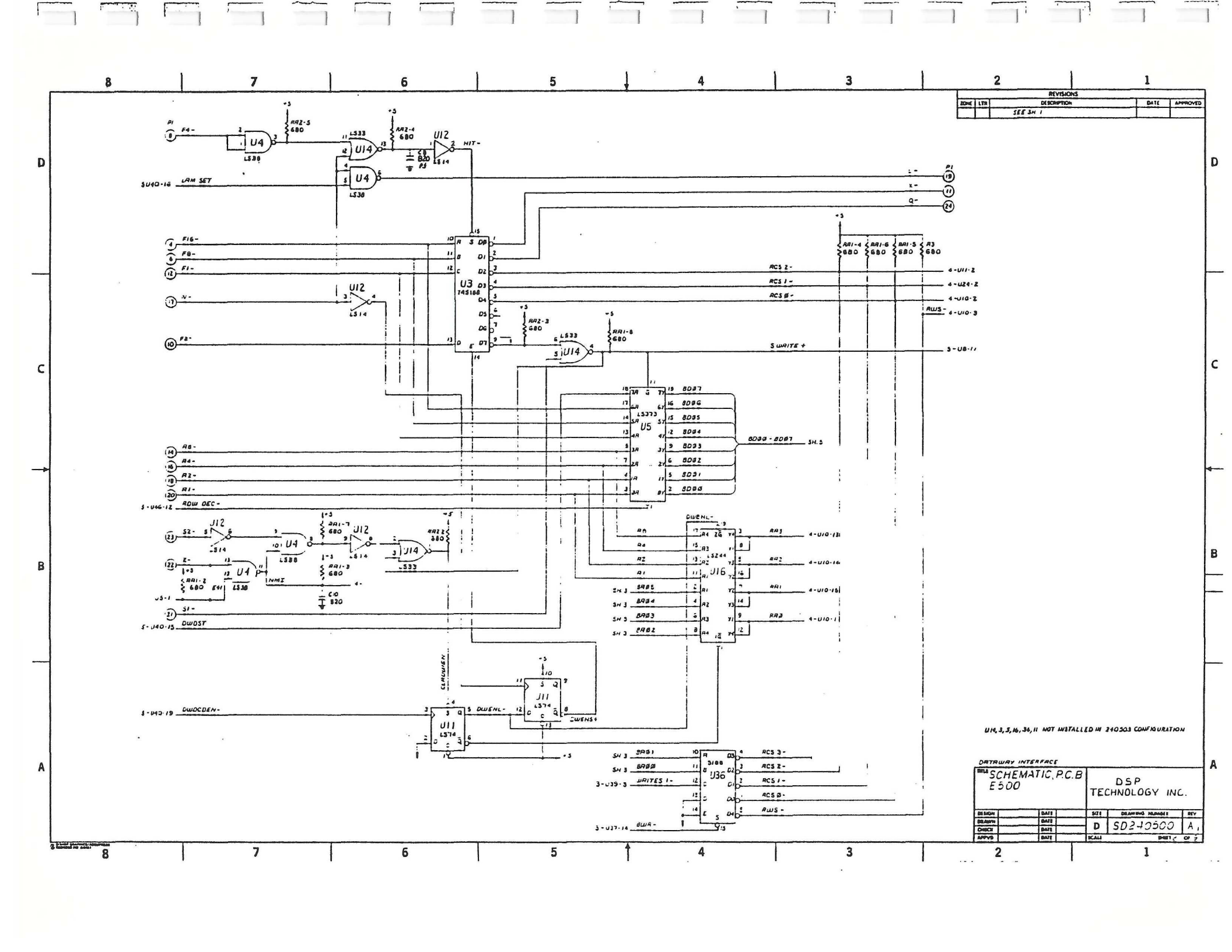
STANDARD ENGINEERING CORPORATION

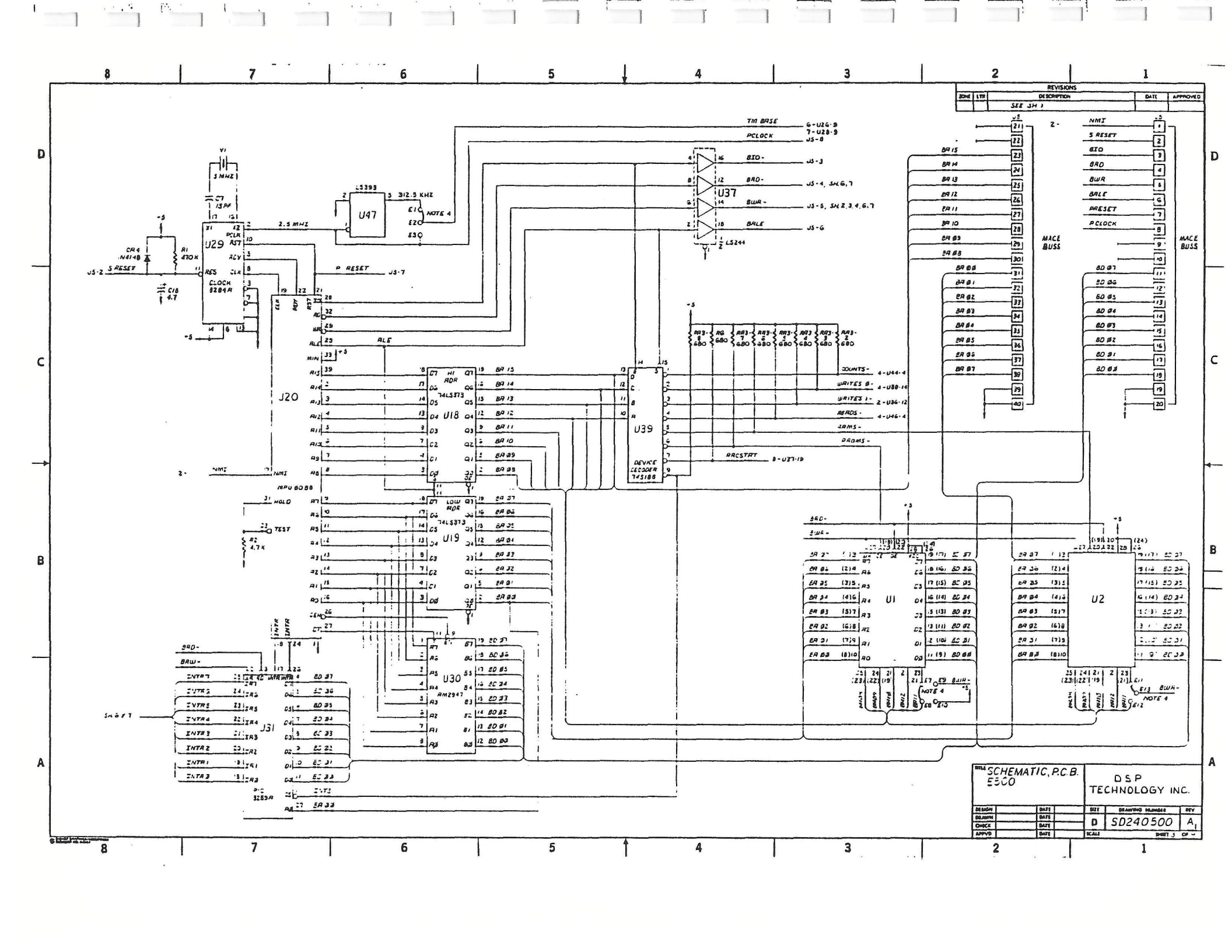
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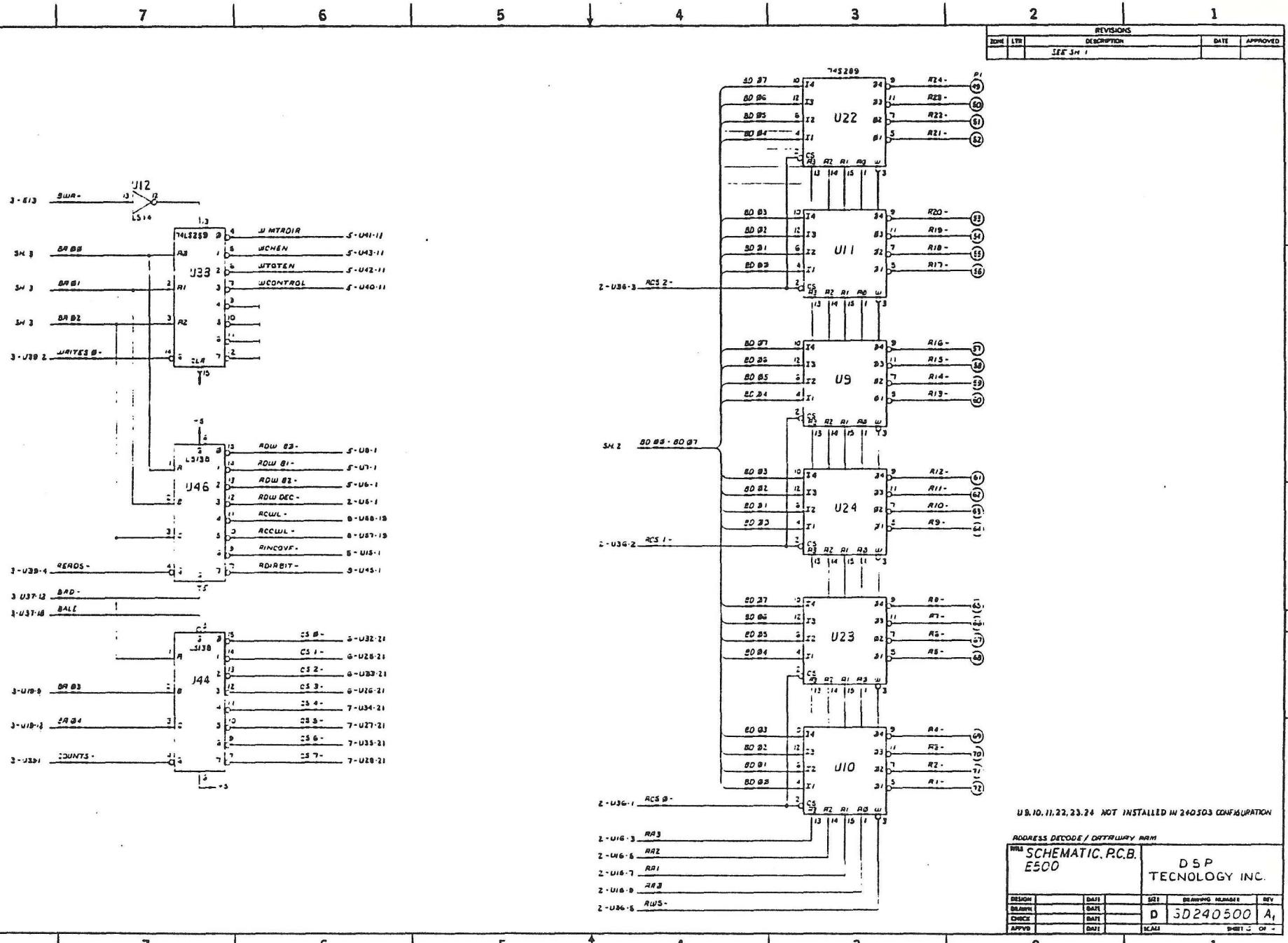
SHEET 1 OF 1

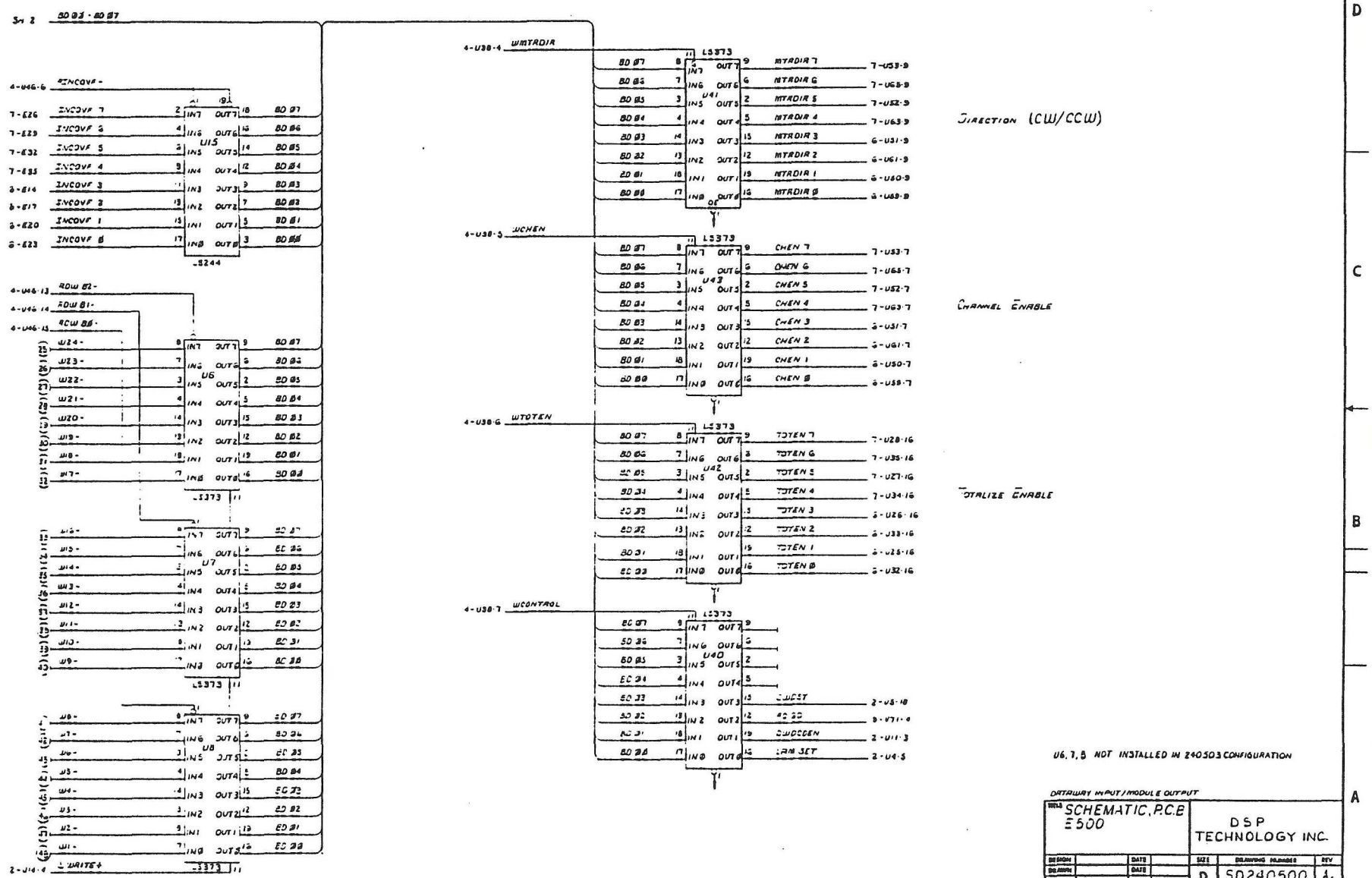


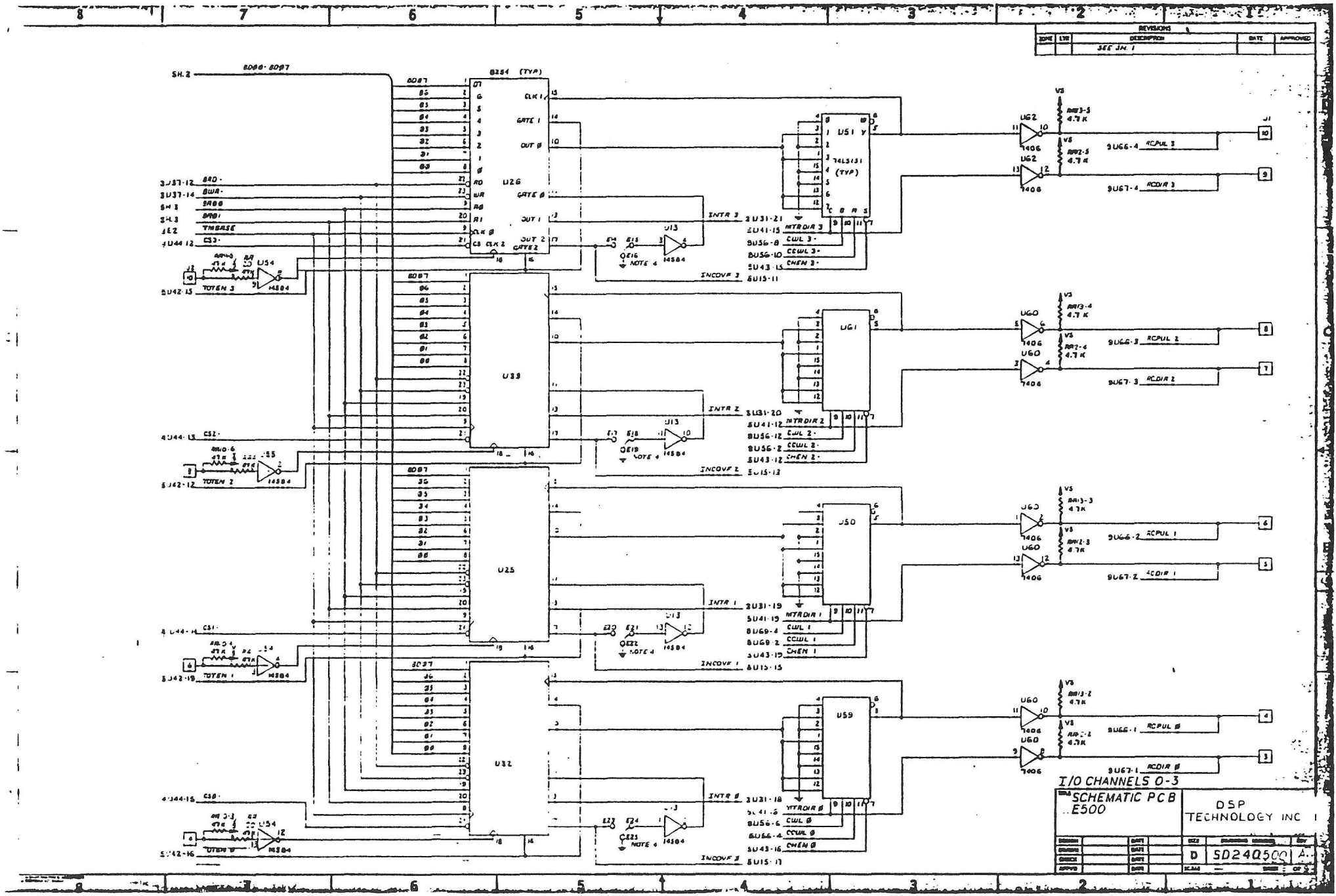
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	2	RELEASE	12-10-81	
	11	RELEASE	1-4-82	JAG
	A	RELEASE	10-22-82	
	A	BEE ECO 0269	3-28-83	
	A1	ECO 480	10/17/83	
	A1	REVISED PER ECO # 516	4/14/84	
	A1	ECO 1207	18/4/180	

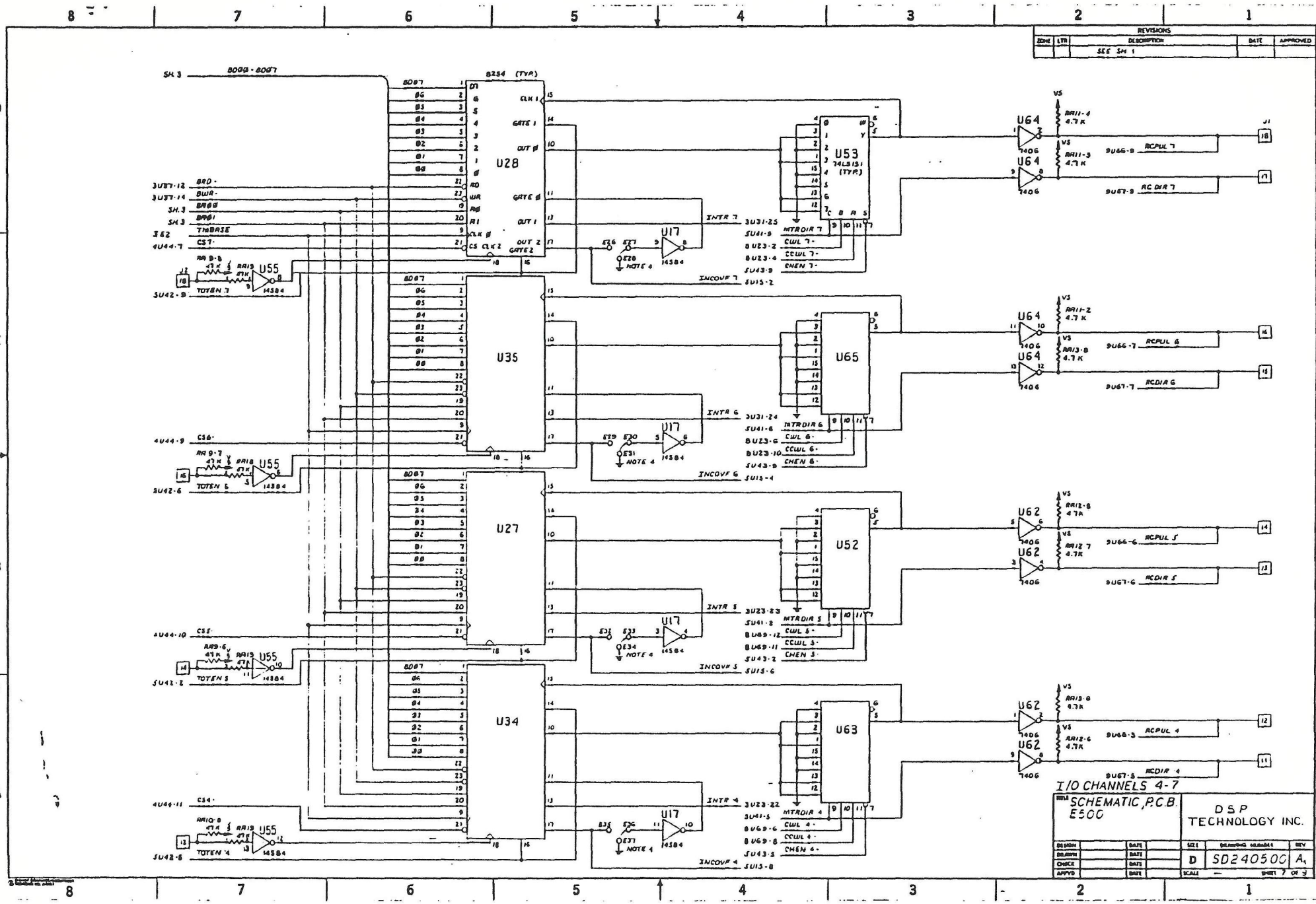

REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
SEE SH 1
U4
LS38
U14
LS33
U12
LS14
U3
74S188
U5
LS373
U16
LS244
U11
LS374
U36
3188
U10
J11
LS74
HIT-
LAM SET
RAM OEC-
DWOST
DWOCDEN-
DWENL-
DWENS+
INMI
BWR-
WRITES 1-
RCS 3-
RCS 2-
RCS 1-
RCS 0-
RWS-
S WRITE +
BD00 - BD07
U14, 3, 5, 16, 36, 11 NOT INSTALLED IN 240503 CONFIGURATION
DATAWAY INTERFACE
SCHEMATIC, P.C.B
E500
DSP
TECHNOLOGY INC.
SIZE
D
SD240500
REV
A1

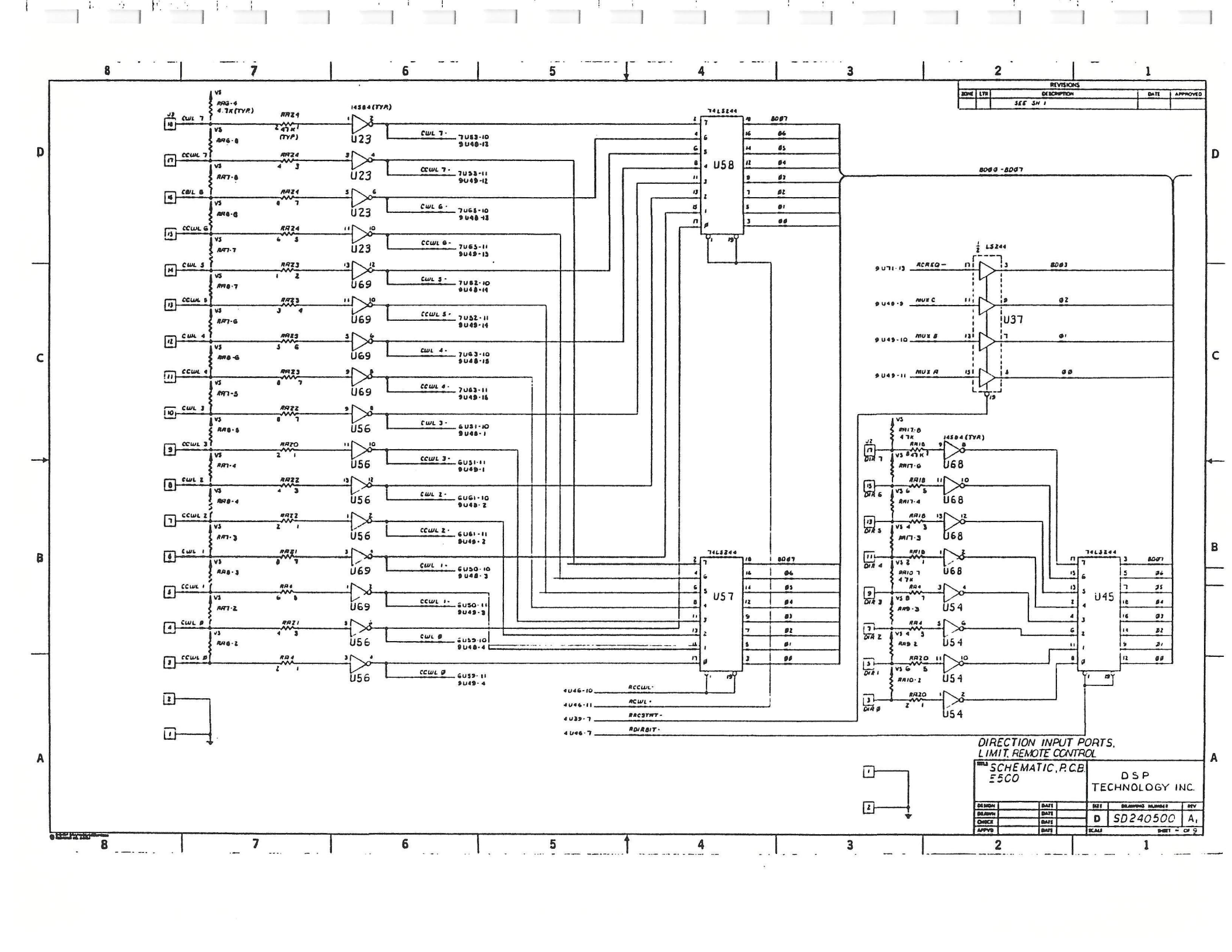

REVISIONS
DESCRIPTION
DATE
APPROVED
SEE SH 1
TIM BASE
PCLOCK
BIO-
BRD-
BWR-
BALE
U37
LS244
U47
U29
CLOCK 8284A
U18
U19
U30
AM2947
U39
DEVICE DECODER 74S188
U20
J20
J31
U1
U2
MACE BUSS
P RESET
S RESET
ALE
NMI
HOLD
TEST
BRCSTRT
SCHEMATIC, P.C.B.
E3CO
DSP TECHNOLOGY INC.
SD240500
A1

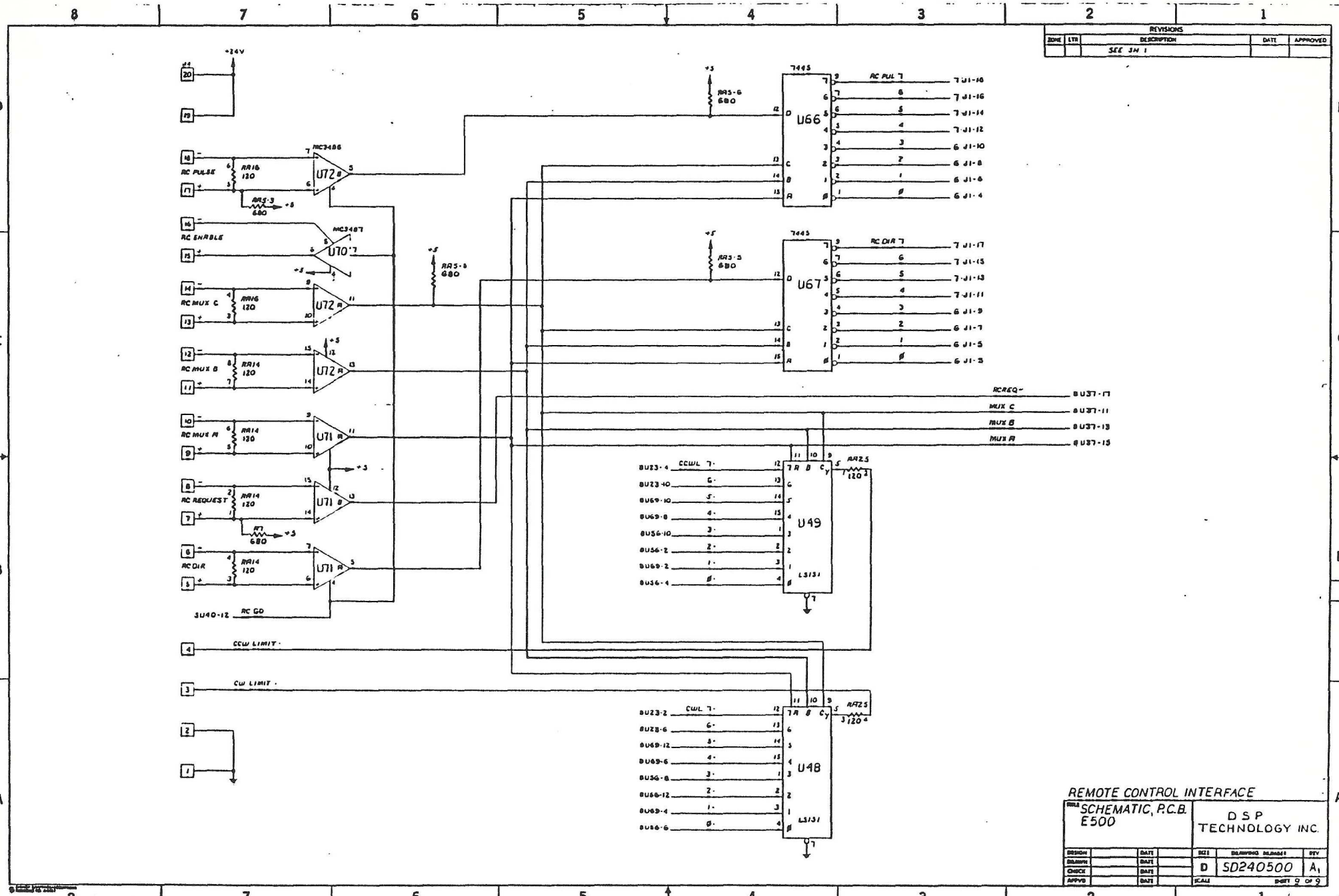

REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
SEE SH 1
U12
LS14
U33
74LS259
U46
LS138
U44
LS138
U22
U11
U9
U24
U23
U10
74S289
SCHEMATIC, P.C.B. E500
DSP TECNOLOGY INC.
D
3D240500
A1
U8,10,11,22,23,24 NOT INSTALLED IN 240303 CONFIGURATION
ADDRESS DECODE / DATAWAY RAM

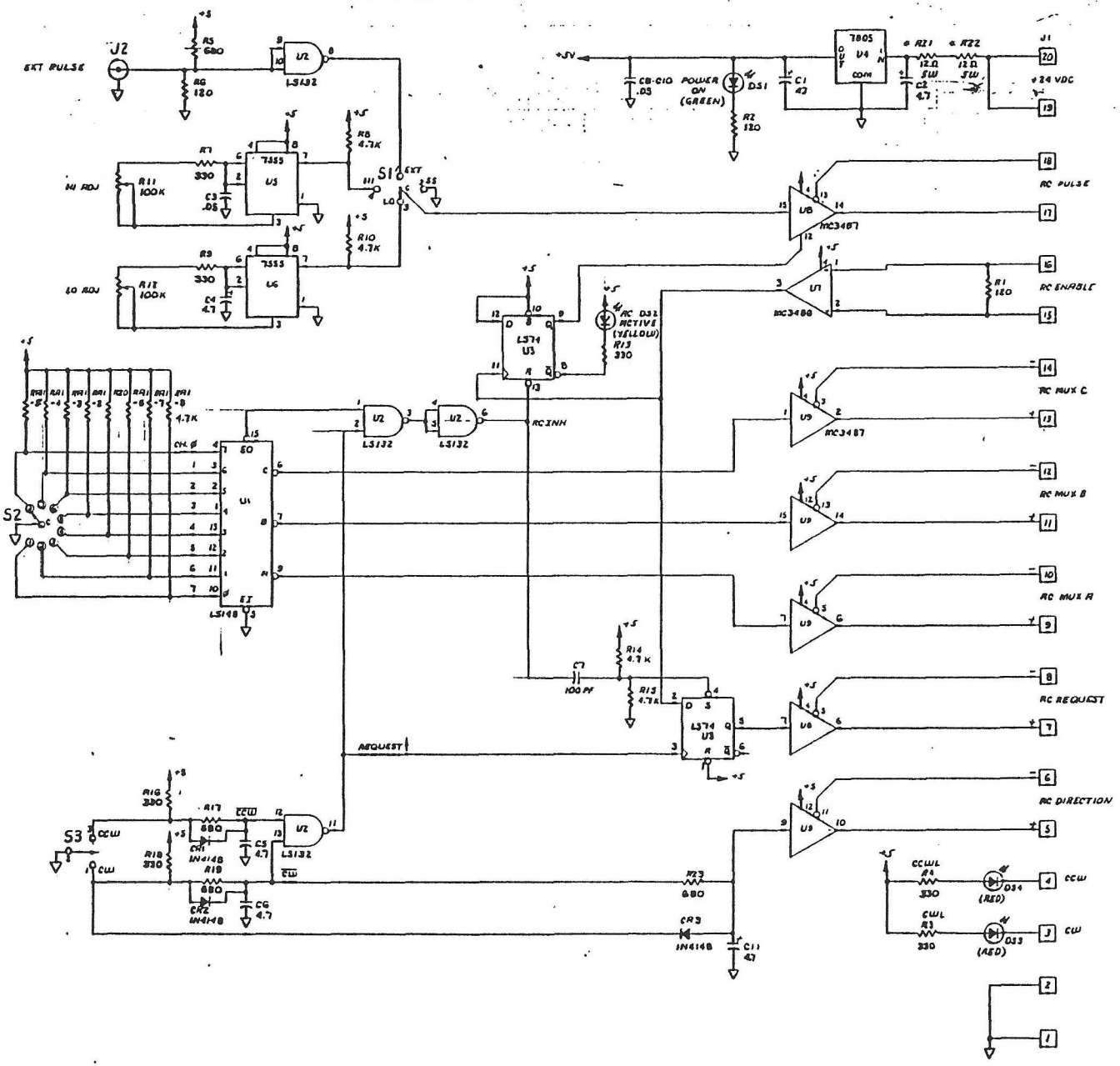

REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
SEE SH 1
SH 2 BD Ø3 - BD Ø7
4-U46-6 *ENCOVF-
7-E26 ENCOVF 7
7-E29 ENCOVF 6
7-E32 ENCOVF 5
7-E35 ENCOVF 4
8-E14 ENCOVF 3
8-E17 ENCOVF 2
8-E20 ENCOVF 1
8-E23 ENCOVF Ø
U15
LS244
4-U46-13 RDW Ø2-
4-U46-14 RDW Ø1-
4-U46-15 RDW Ø0-
U24- U23- U22- U21- U20- U19- U18- U17-
U6
LS373
U16- U15- U14- U13- U12- U11- U10- U9-
U7
LS373
U8- U7- U6- U5- U4- U3- U2- U1-
U8
LS373
2-U14-4 L DRITE+
4-U38-4 WMTRDIR
U41
LS373
BD Ø7 BD Ø6 BD Ø5 BD Ø4 BD Ø3 BD Ø2 BD Ø1 BD Ø0
MTRDIR 7 MTRDIR 6 MTRDIR 5 MTRDIR 4 MTRDIR 3 MTRDIR 2 MTRDIR 1 MTRDIR Ø
7-U53-9 7-U68-9 7-U52-9 7-U63-9 6-U31-9 6-U61-9 6-U60-9 6-U69-9
DIRECTION (CW/CCW)
4-U38-5 WCHEN
U43
LS373
CHEN 7 CHEN 6 CHEN 5 CHEN 4 CHEN 3 CHEN 2 CHEN 1 CHEN Ø
7-U53-7 7-U68-7 7-U52-7 7-U63-7 6-U31-7 6-U61-7 6-U60-7 6-U69-7
CHANNEL ENABLE
4-U38-6 WTOTEN
U42
LS373
TOTEN 7 TOTEN 6 TOTEN 5 TOTEN 4 TOTEN 3 TOTEN 2 TOTEN 1 TOTEN Ø
7-U28-16 7-U35-16 7-U27-16 7-U34-16 6-U26-16 6-U33-16 6-U25-16 6-U32-16
TOTALIZE ENABLE
4-U38-7 WCONTROL
U40
LS373
CWDST 4Ø 3Ø CWDCDEN LRM SET
2-U8-18 9-U71-4 2-U11-3 2-U4-5
U6,7,8 NOT INSTALLED IN 240503 CONFIGURATION
DATAWAY INPUT/MODULE OUTPUT
SCHEMATIC, P.C.B
E500
DSP
TECHNOLOGY INC.
DESIGN DRAWN CHECK APPVD DATE
SIZE D
DRAWING NUMBER SD240500
REV A
SCALE —
SHEET 3 OF 5


REVISIONS
SEE SH. 1
I/O CHANNELS 0-3
SCHEMATIC PCB
E500
DSP
TECHNOLOGY INC
D
SD240500
A


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
SEE SH 1
SH 3
8088 - 8087
8254 (TYP)
U28
U35
U27
U34
U53
74LS151 (TYP)
U65
U52
U63
U64
U62
U55
U17
14584
1406
INTR 7
INTR 6
INTR 5
INTR 4
INCOVF 7
INCOVF 6
INCOVF 5
INCOVF 4
MTRDIR 7
MTRDIR 6
MTRDIR 5
MTRDIR 4
CWL 7-
CCWL 7-
CHEN 7-
CWL 6-
CCWL 6-
CHEN 6-
CWL 5-
CCWL 5-
CHEN 5-
CWL 4-
CCWL 4-
CHEN 4-
BRD-
BWR-
BA00
BA01
TMBASE
CS7-
CS6-
CS5-
CS4-
TOTEN 7
TOTEN 6
TOTEN 5
TOTEN 4
RCPUL 7
RCDIR 7
RCPUL 6
RCDIR 6
RCPUL 5
RCDIR 5
RCPUL 4
RCDIR 4
I/O CHANNELS 4-7
SCHEMATIC, P.C.B.
E500
DSP TECHNOLOGY INC.
SIZE
D
SD240500
REV
A


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
SEE SH 1
74LS244
U58
U57
U37
U45
14584(TYP)
U23
U69
U56
U68
U54
LS244
BD00 - BD07
DIRECTION INPUT PORTS,
LIMIT, REMOTE CONTROL
SCHEMATIC, P.C.B.
ESCO
DSP
TECHNOLOGY INC.
SD240500
A1


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
SEE SH 1
+24V
RC PULSE
RC ENABLE
RC MUX C
RC MUX B
RC MUX A
RC REQUEST
RC DIR
RC GO
3U40-12
CCW LIMIT
CW LIMIT
MC3486
MC3487
U72 B
U72 A
U71 A
U71 B
U10 7
RA16 120
RA14 120
RA5-3 680
RA5-5 680
RA5-6 680
RA5-7 680
RA5-8 680
7445
U66
U67
RC PUL 7
RC DIR 7
7 J1-16
7 J1-15
7 J1-14
7 J1-12
7 J1-17
7 J1-15
7 J1-13
7 J1-11
6 J1-10
6 J1-8
6 J1-6
6 J1-4
6 J1-9
6 J1-7
6 J1-5
6 J1-3
RCREQ~
MUX C
MUX B
MUX A
8U37-17
8U37-11
8U37-13
8U37-15
U49
U48
LS151
RA25 120
CCWL 7
CWL 7
8U23-4
8U23-10
8U69-10
8U69-8
8U56-10
8U56-2
8U69-2
8U56-4
8U23-2
8U23-6
8U69-12
8U69-6
8U56-8
8U56-12
8U69-4
8U56-6
REMOTE CONTROL INTERFACE
SCHEMATIC, P.C.B. E500
D S P TECHNOLOGY INC.
SIZE D
SD240500
REV A1
SHEET 9 OF 9



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	1	RELEASE	8-19-81	
	2	RELEASE	1-18-82	
	2*	J1-3 WAS TO DS4, J1-4 WAS TO DS3	5-6-82	
	A	RELEASE	6-10-82	

NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTORS ARE 1/4 W, 5% . VALUES ARE IN OHMS.
2. ALL CAPACITOR VALUES ARE IN MICRO FARADS.
3. @ R21 / R22 INSTALLED FOR 240506-5 VERSION 24VDC. FOR 240506-8 VERSION, 12VDC. INSTALL (2) JUMPERS

TITLE	MODULE, REMOTE MANUAL CONTROL E505 & E508		
DESIGN	J R GORD	DATE	
DRAWN	PC NAMES	DATE	8-19-81
CHECK		DATE	
APPVD		DATE	

OSP TECHNOLOGY INC.

SIZE	DRAWING NUMBER	REV
D	SD240506	A

SCALE — SHEET 1 OF 1

REVISION HISTORY

Rev.	Date	Description
A	03/12/82	Initial release
B	09/04/84	Revised and word processed
C	02/01/85	ECO 573

dsp Technology Inc.

PRODUCT WARRANTY

(Excludes Software)

DSP (TECHNOLOGY ("DSP") warrants its products to be free from defects in material and workmanship and to meet DSP's performance specifications. The warranty period is one year from the date of shipment to the buyer. The warranty is limited by the paragraphs below.

RETURN TO FACTORY

If a buyer discovers a defect in a DSP product covered by this agreement, buyer's exclusive remedy is to ship the product back to DSP's Fremont factory, where DSP will, at its option, either repair or replace the product. This remedy applies if DSP receives the returned product on or before the tenth day after the expiration of the warranty period and the buyer notifies DSP of the defect before returning the product.

COST TO BUYER OF REPAIRS OR REPLACEMENT

Buyer must prepay freight charges to DSP. DSP will pay standard return freight to buyer. Buyer will be charged for premium freight if that method of transport is requested by buyer. There is no other charge for repair or replacement during the warranty period.

TRANSFERRABLE WARRANTIES

In addition to the foregoing warranty, DSP also provides the buyer the transferrable warranty, if any, provided to DSP by the manufacturers of other products such as terminals and disk systems supplied by SEC as part of a total system.

LIMITATION OF WARRANTY AND LIMITATION OF WARRANTY AND LIABILITY

The foregoing constitutes DSP's entire warranty, expressed, implied, and/or statutory (except as to title), and to any other party for any breach of such warranty and for damages, whether direct, special, incidental, or consequential. Other than as expressly provided in this document, no warranties expressed or implied, including any warranty of merchantability of fitness for a particular purpose are made. No employee, representative or agent or seller has any authority expressed or implied to alter or supplement the terms of this warranty.

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