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ADC-HX, ADC-HZ Series

12-Bit, 8 and 20µsec Analog-to-Digital Converters

INNOVATION and EXCELLENCE

FEATURES

- **12-bit resolution**
- **8 or 20 microsecond conversion times**
- **5 input voltage ranges**
- **Internal high Z input buffer**
- **Short-cycle operation**
- **MIL-STD-883 models available**



GENERAL DESCRIPTION

The ADC-HX and ADC-HZ Series are self-contained, high-performance, 12-bit A/D converters manufactured with thick and thin-film hybrid technology. They use the successive approximation conversion technique to achieve a 12-bit conversion in 20 and 8 microseconds, respectively. Five input voltage ranges are programmable by external pin connection. An internal buffer amplifier is also provided for applications in which 50 megohm input impedance is required.

These converters utilize a fast 12-bit monolithic DAC which includes a precision zener reference source. The circuit also contains a fast monolithic comparator, a monolithic 12-bit successive approximation register, a clock and a monolithic buffer amplifier. Nonlinearity is specified at ±1/2LSB maximum.

Both models have identical operation except for conversion speed. They can be short-cycled to give faster conversions in lower-resolution applications. Use of the internal buffer amplifier increases conversion time by 3 microseconds, the settling time of the amplifier. Output coding is complementary binary, complementary offset binary, or complementary two's complement. Serial data is also brought out. The package is a 32-pin ceramic TDIP. Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges. MIL-STD-883 and DESC Standard Military Drawing models are also available.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 (LSB)	32	SERIAL DATA OUTPUT
2	BIT 11	31	–15V POWER
3	BIT 10	30	BUFFER INPUT
4	BIT 9	29	BUFFER OUTPUT
5	BIT 8	28	+15V POWER
6	BIT 7	27	GAIN ADJUST
7	BIT 6	26	ANALOG COMMON
8	BIT 5	25	20V INPUT RANGE
9	BIT 4	24	10V INPUT RANGE
10	BIT 3	23	BIPOLAR OFFSET
11	BIT 2	22	COMPARATOR INPUT
12	BIT 1 (MSB)	21	START CONVERT
13	BIT 1 ($\overline{\text{MSB}}$)	20	E.O.C. (STATUS)
14	SHORT CYCLE	19	CLOCK OUT
15	DIGITAL COMMON	18	REFERENCE OUT
16	+5V POWER	17	CLOCK RATE

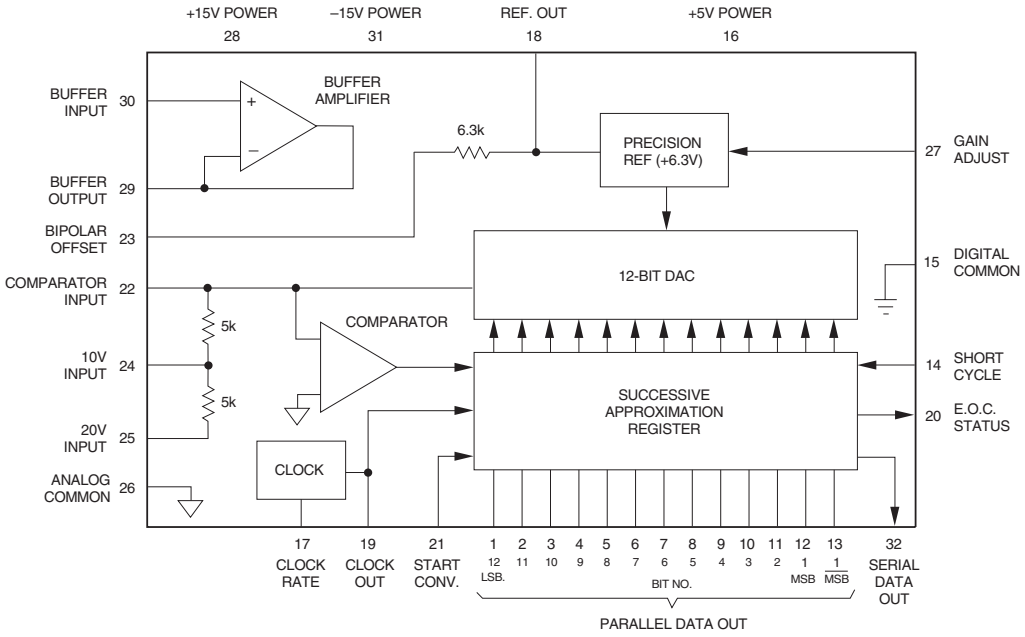


Figure 1. Functional Block Diagram

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ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply, Pin 28	+18	Volts
–15V Supply, Pin 31	–18	Volts
+5V Supply, Pin 16	+7	Volts
Digital Inputs, Pins 14, 21	±5.5	Volts
Analog Inputs, Pins 24, 25	±25	Volts
Buffer Input, Pin 30	±15	Volts
Lead Temperature (10 seconds)	300	°C

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C and ±15V and +5V supplies unless otherwise noted)

INPUTS	ADC-HX12B	ADC-HZ12B
Analog Input Ranges		
Unipolar	0 to +5V, 0 to +10V	
Bipolar	±2.5V, ±5V, ±10V	
Input Impedance	2.5k (0 to +5V, ±2.5V) 5k (0 to +10V, ±5V) 10k (±10V)	
Input Impedance with Buffer	50 megohms	
Input Bias Current of Buffer	125nA typical, 250nA max.	
Start Conversion	+2V min. to +5.5V max. positive pulse with duration of 100ns min. Rise and fall times <30ns. Logic "1" to "0" transition resets converter and initiates next conversion. Loading: 2 TTL loads.	
PERFORMANCE		
Resolution	12 bits	
Nonlinearity	±1/2LSB max.	
Differential Nonlinearity	±3/4LSB max.	
Accuracy Error ①		
Gain (before adjustment)	±0.2%	
Zero, Unipolar (before adj.)	±0.1% of FSR ②	
Offset, Bipolar (before adj.)	±0.2% of FSR ②	
Temperature Coefficient		
Gain	±20ppm/°C max.	
Zero, Unipolar	±5ppm/°C of FSR max. ②	
Offset, Bipolar	±10ppm/°C of FSR max. ②	
Diff. Nonlinearity Tempco	±2ppm/°C of FSR max. ②	
No Missing Codes	Over opererating temperature range	
Conversion Time ③		
12 Bits	20µs max.	8µs max.
10 Bits ④	15µs max.	6µs max.
8 Bits ④	10µs max.	4µs max.
Buffer Settling Time (10V step)	3µs to ±0.01%	
Power Supply Rejection	±0.004%/% supply max.	
OUTPUTS ⑤		
Parallel Output Data	12 parallel lines of data held until next conversion command. V_{OUT} ("0") ≤ +0.4V V_{OUT} ("1") ≥ +2.4V	
Unipolar Coding	Complementary binary	
Bipolar Coding	Complementary offset binary Complementary two's complement	
Serial Output Data	NRZ successive decision pulses out, MSB first. Compl. binary or compl. offset binary coding.	
End of Conversion (Status)	Conversion status signal. Output is logic "1" during reset and conversion and logic "0" when conversion complete.	
Clock Output	Train of positive going +5V 100ns pulses. 600kHz for ADC-HX and 1.5MHz for ADC-HZ (pin 17 grounded).	
Internal Reference	+6.3V	
Reference Tempco	±20ppm/°C max.	
External Reference Current	2.5mA max.	

POWER REQUIREMENTS	
Power Supply Voltages	+15V ±0.5V at +20mA –15V ±0.5V at –25mA +5V ±0.25V at +85mA
PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range, Case	0 to +70°C or –55 to +125°C
Storage Temperature Range	–65 to +150°C
Package Type	32-pin ceramic TDIP
Weight	0.5 ounces (14 grams)
Thermal Impedance	
θ_{JC}	6°C/W
θ_{JA}	30°C/W

Footnotes:

① Adjustable to zero.

② FSR is full scale range and is 10V for 0 to +10V or ±5V inputs and 20V for ±10V input, etc.

③ Without buffer amplifier used. ADC-HZ may require external adjustment of clock rate.

④ Short cycled operation.

⑤ All digital outputs can drive 2 TTL loads.

TECHNICAL NOTES

1. It is recommended that the ±15V power input pins both be bypassed to ground with a 0.01µF ceramic capacitor in parallel with a 1µF electrolytic capacitor and the +5V power input pin be bypassed to ground with a 10µF electrolytic capacitor as shown in the connection diagrams. In addition, GAIN ADJUST (pin 27) should be bypassed to ground with a 0.01µF ceramic capacitor. These precautions will assure noise free operation of the converter.

2. DIGITAL COMMON (pin 15) and ANALOG COMMON (pin 26) are not connected together internally, and therefore must be connected as directly as possible externally. It is recommended that a ground plane be run underneath the case between the two commons. Analog ground and ±15V power ground should be run to pin 26 whereas digital ground and +5V ground should be run to pin 15.

3. External adjustment of zero or offset and gain are made by using trimming potentiometers connected as shown in the connection diagrams. The potentiometer values can be between 10k and 100k Ohms and should be 100ppm/°C cermet types. The trimming pots should be located as close as possible to the converter to avoid noise pickup. In some cases, for example 8-bit short-cycled operation, external adjustment may not be necessary.

4. Short-cycled operation results in shorter conversion times when the conversion is truncated to less than 12 bits. This is done by connecting SHORT CYCLE (pin 14) to the output bit following the last bit desired. For example, for an 8-bit conversion, pin 14 is connected to the bit 9 output. Maximum conversion times are given for short-cycled conversions of 8 or 10 bits. In these two cases, the clock rate is accelerated by connecting the CLOCK RATE adjust (pin 17) to +5V (10 bits) or +15V (8 bits). The clock rate should not be arbitrarily speeded up to exceed the maximum conversion rate at a given resolution, as missing codes will result.

5. Note that output coding is complementary coding. For unipolar operation it is complementary binary, and for bipolar operation it is complementary offset binary or complementary two's complement. In cases in which bipolar coding of offset binary or two's complement is required, this can be achieved by inverting the analog input to the converter (using an op amp connected for gain of –1). The converter is then calibrated so that –FS analog input gives an output code of 0000 0000 0000, and +FS – 1LSB gives 1111 1111 1111.

6. These converters can be operated with an external clock. To accomplish this, a negative pulse train is applied to START CONVERT (pin 21). The rate of the external clock must be lower than the rate of the internal clock as adjusted (see Short Cycle Operation tables) for the converter resolution selected. The pulse width of the external clock should be between 100 and 300 nanoseconds. Each N-bit conversion cycle requires a pulse train of N + 1 clock pulses for completion, e.g., an 8-bit conversion requires 9 clock pulses for completion. A continuous pulse train may be used for consecutive conversions, resulting in an N-bit conversion every N + 1 pulses, or the E.O.C. output may be used to gate a continuous pulse train for single conversions.

7. When the input buffer amplifier is used, a delay equal to its settling time must be allowed between the input level change, such as a multiplexer channel change, and the negative-going edge of the START CONVERT pulse. If the buffer is not required, BUFFER INPUT (pin 30) should be tied to ANALOG COMMON (pin 26). This prevents the unused amplifier from introducing noise into the converter. For applications not using the buffer, the converter must be driven from a source with an extremely low output impedance.

CODING TABLE
UNIPOLAR OPERATION

INPUT RANGE		COMP. BINARY CODING
0 to +10V	0 to +5V	MSB LSB
+9.9976V	+4.9988V	0000 0000 0000
+8.7500	+4.3750	0001 1111 1111
+7.5000	+3.7500	0011 1111 1111
+5.0000	+2.5000	0111 1111 1111
+2.5000	+1.2500	1011 1111 1111
+1.2500	+0.6250	1101 1111 1111
+0.0024	+0.0012	1111 1111 1110
0.0000	0.0000	1111 1111 1111

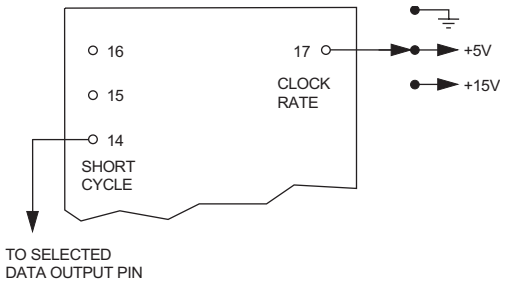
CODING TABLE
BIPOLAR OPERATION

INPUT VOLTAGE RANGE			COMP. OFFSET BINARY	COMP. TWO'S COMPLEMENT
±10V	±5V	±2.5V	MSB LSB	MSB LSB
+9.9951V	+4.9976V	+2.4988V	0000 0000 0000	1000 0000 0000
+7.5000	+3.7500	+1.8750	0001 1111 1111	1001 1111 1111
+5.0000	+2.5000	+1.2500	0011 1111 1111	1011 1111 1111
0.0000	0.0000	0.0000	0111 1111 1111	1111 1111 1111
–5.0000	–2.5000	–1.2500	1011 1111 1111	0011 1111 1111
–7.5000	–3.7500	–1.8750	1101 1111 1111	0101 1111 1111
–9.9951	–4.9976	–2.4988	1111 1111 1110	0111 1111 1110
–10.0000	–5.0000	–2.5000	1111 1111 1111	0111 1111 1111

SHORT CYCLE OPERATION

Refer to Technical Note 4 for methods of reducing the ADC-HX or ADC-HZ conversion times.

CONNECTIONS



CLOCK RATE VS. VOLTAGE

PIN 17 VOLTAGE	CLOCK RATE	
	ADC-HX	ADC-HZ
0V	600kHZ	1.5MHZ
+5V	720kHZ	1.8MHz
+15V	880kHz	2.2MHz

8, 10 & 12-BIT CONVERSION TIMES

RESOLUTION	12 BITS	10 BITS	8 BITS
ADC-HX Conversion Time	20µs	15µs	10µs
ADC-HZ Conversion Time	8µs	6µs	4µs
Connect These Pins Together	17 & 15 14 & 16	17 & 16 14 & 2	17 & 28 14 & 4

PIN 14 CONNECTION

RES. (BITS)	PIN 14 TO	RES. (BITS)	PIN 14 TO
1	PIN 11	7	PIN 5
2	PIN 10	8	PIN 4
3	PIN 9	9	PIN 3
4	PIN 8	10	PIN 2
5	PIN 7	11	PIN 1
6	PIN 6	12	PIN 16

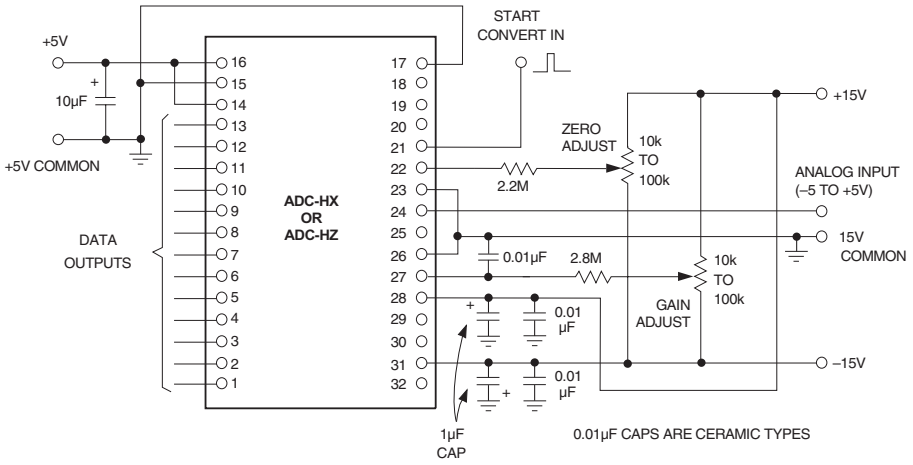


Figure 2. Bipolar Operation, –5 to +5V

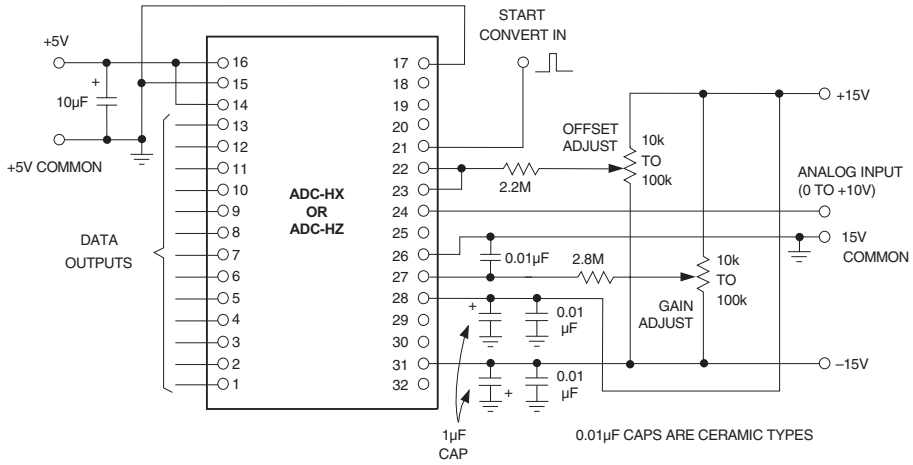


Figure 3. Unipolar Operation, 0 to +10V

CONNECTIONS AND CALIBRATION

INPUT CONNECTIONS

INPUT VOLTAGE RANGE	WITHOUT BUFFER			WITH BUFFER			
	INPUT PIN	CONNECT THESE PINS TOGETHER		INPUT PIN	CONNECT THESE PINS TOGETHER		
0 to +5V	24	22 & 25	23 & 26	30	22 & 25	23 & 26	29 & 24
0 to +10V	24	—	23 & 26	30	—	23 & 26	29 & 24
±2.5V	24	22& 25	23 & 22	30	22 & 25	23 & 22	29 & 24
±5V	24	—	23 & 22	30	—	23 & 22	29 & 24
±10V	25	—	23 & 22	30	—	23 & 22	29 & 25

CALIBRATION PROCEDURE

1. Connect the converter for bipolar or unipolar operation. Use the input connection table for the desired input voltage range and input impedance. Apply START CONVERT pulses of 100 nanoseconds minimum duration to pin 21. The spacing of the pulses should be no less than the maximum conversion time.

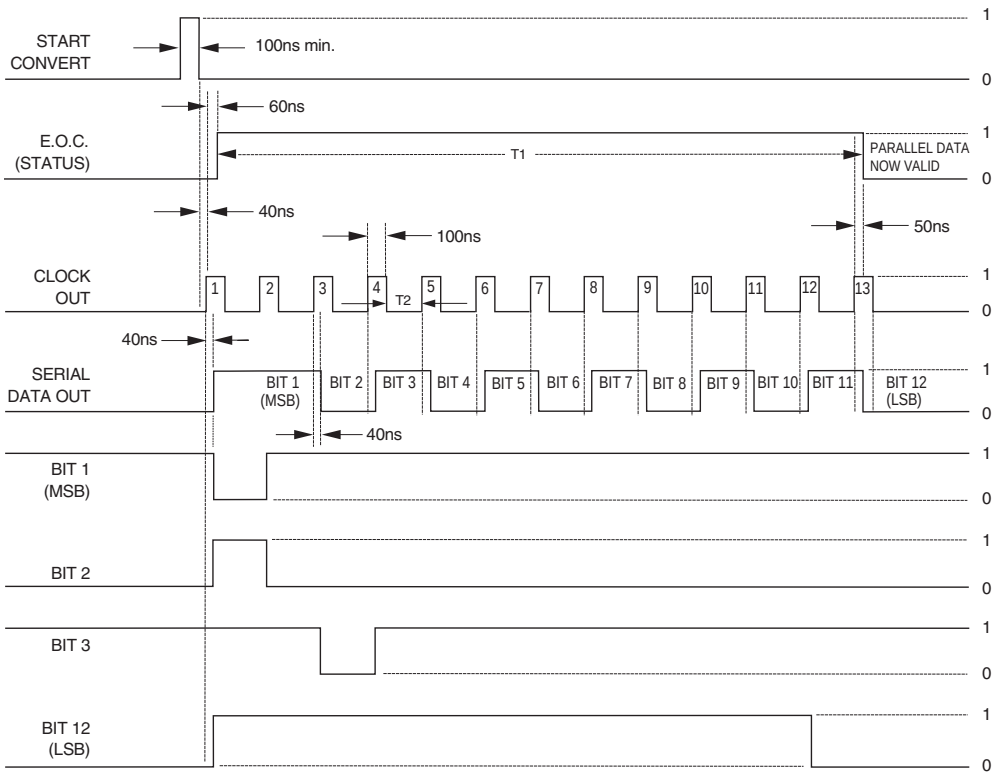
2. **Zero and Offset Adjustments**
   Apply a precision voltage reference source between the selected analog input and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (zero + 1/2LSB) or the bipolar offset adjustment (–FS + 1/2LSB). Adjust the trimming potentiometer so that the output code flickers equally between 1111 1111 1111 and 1111 1111 1110.

3. **Full Scale Adjustment**
   Change the output of the precision voltage reference source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS – 1.5LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 0000 0000 0001 and 0000 0000 0000.

CALIBRATION TABLE

	RANGE	ADJUST.	INPUT VOLTAGE
UNIPOLAR	0 to +5V	Zero Gain	+0.6mV +4.9982V
	0 to +10V	Zero Gain	+1.2mV +9.9963V
BIPOLAR	±2.5V	Offset Gain	–2.4994V +2.4982V
	±5V	Offset Gain	–4.9988V +4.9963V
	±10V	Offset Gain	–9.9976V +9.9927V

TIMING DIAGRAM FOR
ADC-HX, ADC-HZ OUTPUT: 101010101010

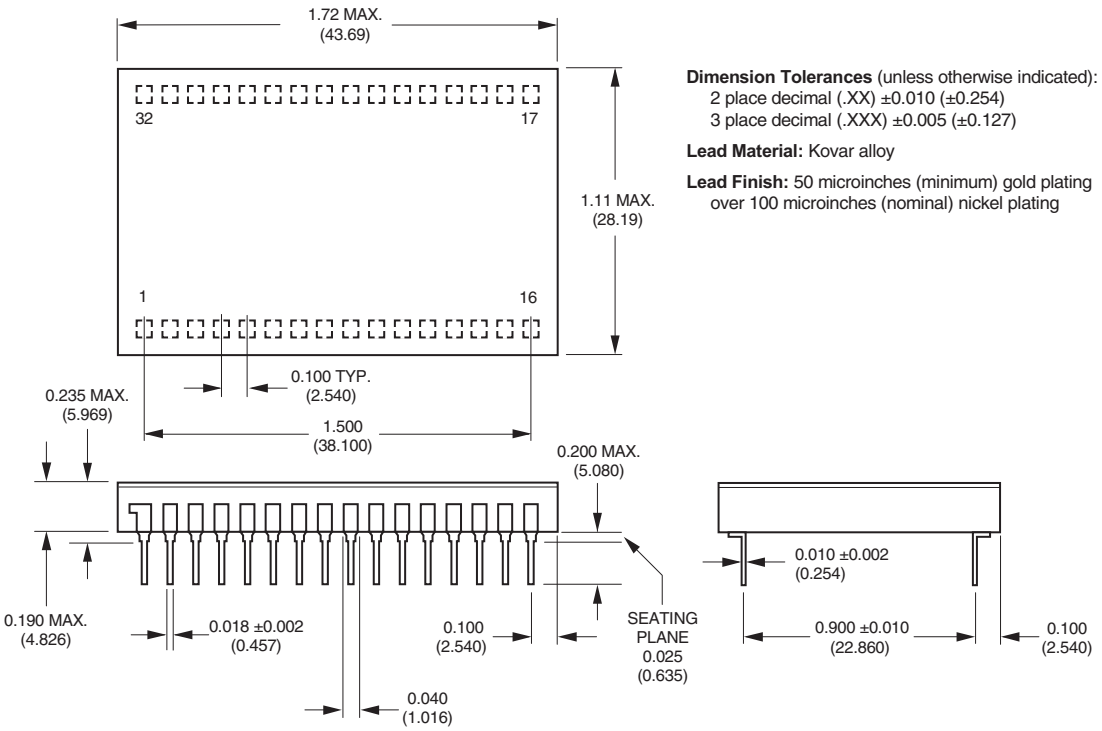


TIMING DIAGRAM
OPERATING PERIODS

	ADC-HX	ADC-HZ
T_1	20µs	8µs
T_2	1.56µs	0.56µs

MECHANICAL DIMENSIONS

INCHES (mm)



Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL	TEMP. RANGE
ADC-HX12BGC	0 to +70°C
ADC-HX12BMC	0 to +70°C
ADC-HX12BMM	–55 to +125°C
ADC-HX12BMM-QL	–55 to +125°C
ADC-HX/883	–55 to +125°C
ADC-HZ12BGC	0 to +70°C
ADC-HZ12BMC	0 to +70°C
ADC-HZ12BMM	–55 to +125°C
ADC-HZ12BMM-QL	–55 to +125°C
ADC-HZ/883	–55 to +125°C

MIL-STD-883B units are available under DESC Drawing Number 5962-88508. Contact DATEL for 883 product specification.

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