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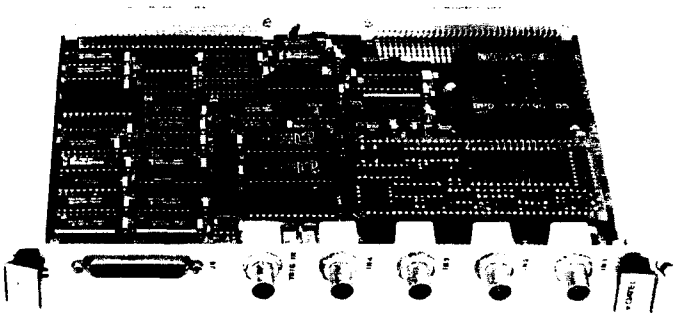
# DVME-614

## High Speed Analog Input Board for VMEbus Computers

*PRODUCT DATA*

### FEATURES

- **Up to 4 MHz A/D sample rate**
- **Choice of 12- or 14-bit A/D resolution**
- **Optional 4 simultaneous sample/hold's**
- **On-board FIFO memory for up to 4096 samples**
- **Very low harmonic distortion**
- **Ideal for FFT's, DSP or array processor "front ends"**
- **Non-Bus burst parallel port for seamless non-stop recording.**
- **Analog input comparator trigger**



### GENERAL DESCRIPTION

Offering very high system speed, the DVME-614 is a multi-channel analog input board for VMEbus computers. Single channel full power input bandwidth is available up to 2.5 MHz and may be sampled up to 4 MHz.

The single-ended analog input ranges of the A/D converter are selectable as unipolar 0 to +10 Volts, or bipolar ±5 Volts, or ±10 Volts depending on model. The gain on the DVME-614A may be user-selected times one or times ten on two channels. The DVME-614E offers 16 single-ended or 8 differential inputs and programmable gain up to times 100.

Model DVME-614A uses a Simultaneous Sample/Hold section (SSH). The SSH acquires signals on parallel channels at the same time then the A/D converter rapidly digitizes each held signal sequentially. This provides phase correction and deskewing of multichannel correlated signals.

A/D data passes to an on-board First-In, First-Out (FIFO) data memory. The design can continuously collect analog data with non-stop converter triggering while data is simultaneously read from the FIFO. Functions such as FFT sampling cannot tolerate lost samples without increases in "arithmetic" noise during computation processing. The FIFO decouples the precise timing of the A/D section to conform with the block-oriented data transfers to the bus. Data may be transferred to mass storage peripherals such as disk or magnetic tape via the host computer bus interface under host software control.

The FIFO data output may also be routed under host software control to an on-board parallel digital data port. The parallel outport uses a universal ready/acknowledge transfer handshake adaptable to any remote parallel port. Typically, a FIFO half-full interrupt from the DVME-614 triggers an external processor to burst a fixed length block of samples.

The analog section of the DVME-614 is optimized for high signal quality and very low dynamic noise. The board is de-

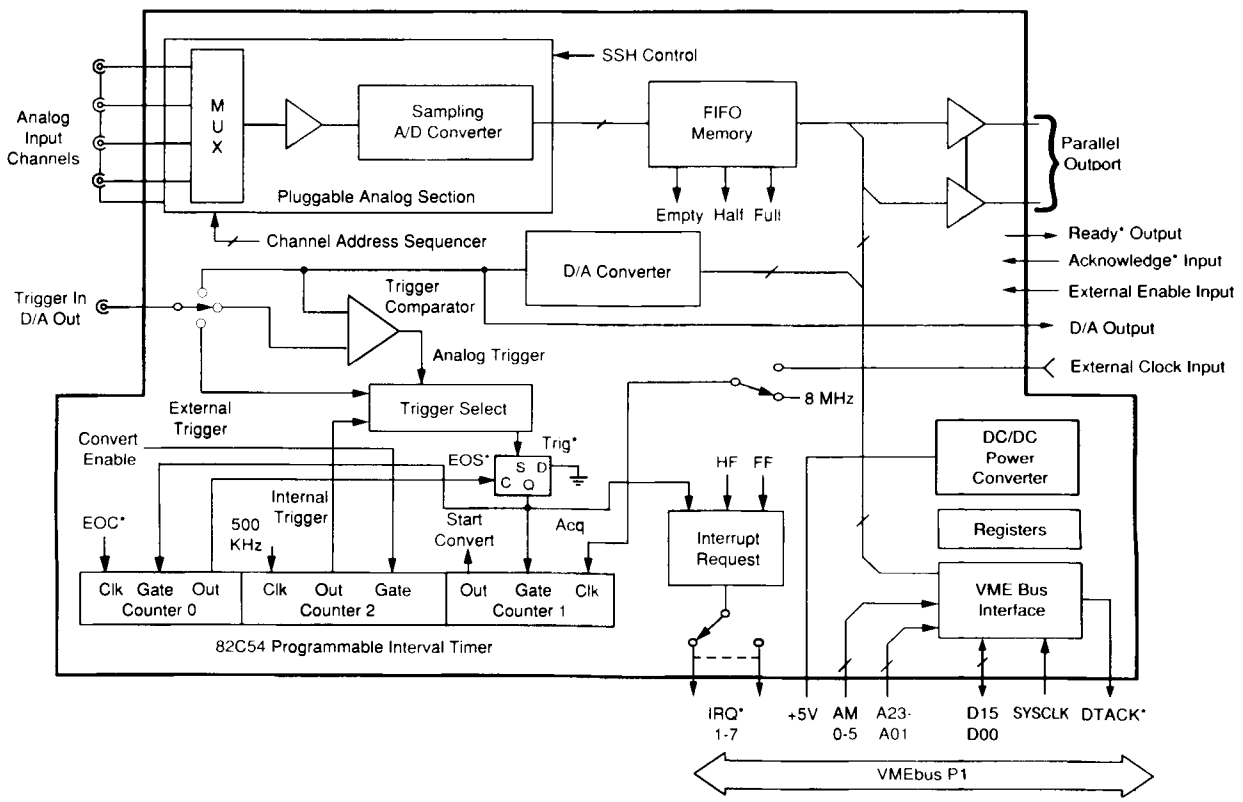



**Figure 1. DVME-614 Block Diagram**

signed and qualified with low Total Harmonic Distortion (THD) characteristics. The DVME-614 is ideal as an FFT "front end" or DSP quantizer.

The A/D conversion timing section is designed for accurate multi-scan data acquisition. Software programmable timers control the interval between each conversion and each multi-channel scan. A programmable sample counter allows sample blocks of specified length independent of FIFO length. The timer/counter section uses a precision on-board VMEbus clock and may be replaced by an external timebase. Timeout and sample count activities may be monitored from the computer bus using I/O status registers and/or programmable interrupts.

S/H-A/D triggering may use several sources under software control. The internal timebase is the normal trigger source although single conversions or scans may be directly commanded by host I/O register writes. An external trigger clock may also be used to precisely synchronize sampling with external events. This external trigger may start a single sample, a single multichannel scan, or "N" multiple scans separated by programmable delays.

Analog sampling may also be level-triggered using an on-board analog comparator. The reference trigger level to the comparator is derived from an on-board 12-bit D/A converter. If preferred, the D/A converter may also be used as an analog output channel for any purpose.

The DVME-614 A-D have five front panel signal connectors. Four connectors are for the sampled analog channels. The fifth connector is for a choice of the external timebase clock input, the external analog trigger level or for the D/A output. The DVME-614E uses a 25-pin connector. The computer interface for control and status uses 24-bit addressing. Board control and A/D data uses 16-bit VMEbus transfers. A single interrupt is generated for a variety of conditions under host software control. These include A/D data ready, sample count reached, FIFO half-full or FIFO full.

A/D output data coding is right-justified two's complement with sign extension. This format is excellent for integer data typing with high level computer languages such as "C", FORTRAN, Pascal or Ada. It is also directly compatible with very fast arithmetic instructions for all microprocessor assembly languages and math coprocessors. Straight binary coding may also be selected.

A high-efficiency, low noise DC/DC converter provides quiet power to linear sections. The burst channel parallel port uses a 25-pin "D" front panel connector.

The DVME-614 is supplied with a set of low level device driver examples in assembly language and "C". These are supplied on universal 5.25" MS-DOS disks. The drivers may be adapted to most host Operating Systems. The user manual has register and timing information for programmers to write their own software for any CPU or operating system. The drivers may operate in either interrupt or status mode.

## DVME-614 FEATURE/BENEFIT SUMMARY

| DESIGN FEATURE | BENEFIT | APPLICATIONS |
|---|---|---|
| Common motherboard with small, pluggable analog input modules. | Various S/H and A/D speed and resolution options available. | High-speed, wide bandwidth sampling of different input signals with minimal physical changes. |
| User-selectable input gains of X1 and X10; input impedance of 10 MΩ. | Makes one volt input ranges available; reduced errors due to high input loading. | Analyzing wide band communications signals from receiver outputs. |
| Simultaneous Sample-and-Hold (SSH) | Allows scanning up to four input channels at once. | High-speed cross-channel computation, beam-former coherency for sonar or acoustics, telemetry, multiple-carrier demodulation, and highly concurrent system testing. |
| FIFO data memory configuration. | Allows collection of 'seamless' wide-bandwidth samples of millions of samples or better. | Long baseline studies in astrophysics, stress life testing, and anomalous pattern searches. |
| Parallel digital data 'outport' | Lets external processors read data at high rates, eliminating bus delays. | Array processors, host mainframe I/O ports. |
| Software-programmable timers. | Allows precise control over conversions and multi-channel scans. | Software-programmable user-supplied Direct Memory Access (DMA) data transfers to host memory. |
| I/O status register and programmable interrupts. | Allows monitoring events from the host bus. | |
| Optional external trigger interrupt. | Allows precise synchronization with external events. | |

## FUNCTIONAL SPECIFICATIONS

Typical at +25 °C, gain = 1, dynamic conditions unless noted.

### ANALOG INPUTS

| | 614A | 614B, E | 614C | 614D |
|---|---|---|---|---|
| **Full Scale Input Ranges** | | | | |
| **Gain = 1, 0 to +5V** | – | – | ✓ | – |
| 0 to +10V | ✓ | ✓ | ✓ | – |
| ±10V | ✓ | ✓ | ✓ | – |
| ±5V | – | ✓ | ✓ | – |
| ±1.25V | – | – | – | ✓ |
| **Gain = 10 (Note 7)** | | | | |
| 0 to ±1V | ✓ | – | – | – |
| ±1V | ✓ | – | – | – |

| | |
|---|---|
| **Number of Channels** | 4 Channels (Models A, B, C)<br>1 Channel (DVME-614D)<br>16S/8D Channels (DVME-614E) |
| **Input Configuration** | Single-ended, non-isolated (614A - D)<br>Single-ended or differential (614E) |
| **Input Impedance** | 10 Megohms (min.), power on<br>*(See Tech. Note 1)* 50Ω in, 614D<br>1.5 Kilohms power off |
| **Input Bias Current** | ±1 nA |
| **Input Capacitance** | 10 pF per channel |
| **Input Overvoltage** | ±15V max. (no damage) |
| **Common Mode Volt. Range** | ±10V max. (614E) |
| **Common Mode Rejection (Gain = 100)** | 80 dB (614E) |
| **Overvoltage Recovery** | 2 Microseconds Maximum |
| **Addressing Modes** | a. Single channel<br>b. Simultaneous Sample/Hold (614A )<br>c. Sequential with autosequenced addressing<br>d. Random addressing by host software |

### SAMPLE/HOLD CHARACTERISTICS

| | 614A | 614B, E | 614C | 614D |
|---|---|---|---|---|
| **Acquisition Time (max.)** | | | | |
| **(10V step) to 0.01% of FSR** | 750 nS | 750 nS | 200 nS | 50nS |
| **Aperture Delay** | 6 nS | 30 nS | 30 nS | 10nS |
| **Aperture Delay Uncertainty SSH Channel-to-channel** | ±1 nS | ±5 nS | ±5 nS | ±10pS |
| **Linearity Tracking** | ±0.03% | – | – | – |
| **Droop Rate, µV/µS** | 1 | 1 | 1 | 1 |

### A/D CONVERTER

| | 614A | 614B | 614C, E | 614D |
|---|---|---|---|---|
| **Resolution** | 12 bits | 14 bits | 12 bits | 12 bits |
| **Conversion Period** | 500 nS | 1 µS | 1 µS | 200nS |

| | |
|---|---|
| **Output Coding** | Positive-true right-justified straight binary (unipolar) or right-justified two's complement (bipolar) with sign extension through bit 15. |
| **Trigger Sources (Software selectable)** | a. Local Pacer sample clock<br>b. External TTL sample clock<br>c. Analog threshold comparator<br>d. Host write to channel address register. |

### TOTAL SYSTEM DYNAMIC PERFORMANCE

| | 614A | 614B | 614C | 614D, E |
|---|---|---|---|---|
| **Full Scale Temp. Coef. LSB per °C** | ±0.1 | ±0.3 | ±0.1 | ±0.1 |
| **Zero or Offset Temp. Coef. LSB per °C** | ±0.1 | ±0.3 | ±0.1 | ±0.1 |
| **Integral Non-linearity, LSB** | ±1 | ±1.5 | ±1 | ±1 |
| **Diff. Non-linearity, LSB** | ±0.75 | ±1 | ±0.75 | ±1 |
| **Power Supply Rejection, (% of bus +5V)** | ±0.004 | ±0.004 | ±0.004 | ±0.004 |

### A/D MEMORY

| | |
|---|---|
| **Architecture** | First-In, First-Out (FIFO) |
| **Memory Capacity** | 1024 A/D samples, standard. Up to 4096 A/D samples (optional) |

### TOTAL SYSTEM DYNAMIC PERFORMANCE

| *See Tech. Note 2* | 614A | 614B [614E] | 614C | 614D |
|---|---|---|---|---|
| **System Bandwidth** (single channel, half-scale input) | 1 MHz | 200 KHz | 1 MHz | 2.5 MHz |
| **Total Throughput to FIFO** (single channel, gain=1) | 700 nS | 2 µS | 1µS | 250 nS |
| **Throughput to FIFO** (sequential channels, gain = 1) (See Tech. Note 3) | 1 µS | 3 µS [4 µS] | 2 µS | – |
| **Throughput to FIFO** (sequential channels, gain = 10) | 10 µS | – | – | – |
| **Total Harmonic Distortion,** min. with half-scale input (See Tech. Note 4) | -72 dB | -75 dB [-72 dB] | -72 dB | -68dB |
| **System Noise (referred to input)** | 200 microvolts. dc to 100 KHz | | | |

### TRIGGER CONTROL

| | |
|---|---|
| **Timer/Counter** | 82C54. (programmable) |
| **Functions** | a) A/D EOC sample count<br>b) A/D start rate (16 bit divisor)<br>c) Scan or frame rate (16 bit divisor) |
| **Pacer Sample Counter** | 1 to 65,536 samples. Drives the Acquire flag/interrupt. |
| **82C54 Clock Source** (User-selectable) | a) Internal 8 MHz clock derived from VMEbus SYSCLK.<br>b) External BNC TTL input, 10 MHz max. |
| **Scan Clock Source** | 125, 250, or 500 KHz |
| **Analog Trigger Input Range** *(See Tech. Note 5)* | ±10 Volts |
| **Analog Trigger Response** | 2 microseconds to set status flag |
| **Analog Trigger Hysteresis** | 40 millivolts |

### ANALOG OUTPUT

| | |
|---|---|
| **Number of Channels** | One channel |
| **Function** | a) General purpose analog output |
| **(user-selectable)** | b) Threshold comparator for A/D trigger. |
| **Resolution** | 12 bits |
| **Output Voltage Range (User-selectable)** | 0 to +10V, ±5V, ±10V |
| **Linearity** | ±0.05% of FSR |
| **Settling time (10V step)** | 5 microseconds to 0.05% |
| **Input Coding** | Straight binary |

### VMEbus INTERFACE

| | |
|---|---|
| **Standards Compliance** | IEEE P1014/D1.0 |
| **Data Bus Width** | 16 bits using P1 connector. |
| **Address Bus** | 24 address lines (A23-A01) plus 6 Address Modifiers. |
| **Address Modifier Codes** | 39 hex or 3D hex. selectable. |
| **VMEbus Interrupt** | 1 line. selectable IRQ 1-7*. Asserts maskable programmable 8-bit vector ID code. |
| **Architecture** | SAD24:SD16 slave consisting of 16 contiguous word registers. |
| **Bus Interrupt Sources** | Scan acquire flag (sample count). FIFO full or half full. |
| **Control/Status Functions** | FIFO reset. FIFO flags, interrupt select and status, trigger source, timer control and period, sample count load, parallel outport transfer status, A/D enable, MUX autosequence. |
| **Data Transfer** | Uses 16 MHz VMEbus SYSCLK signal to generate DTACK* with selectable |

| PARALLEL PORT | |
|---|---|
| Parallel Outport | 16 lines, TTL levels from FIFO. Includes ready out, acknowledge in and transfer enable in handshakes. Outport steering is software enabled. |
| Function | Asynchronous slave to remote master. Does not provide addressing. All data is sequential. The transfer enable input from a remote master is displayed as a status bit. |
| Parallel Port Loading | 24 mA out, 1.6 mA in |
| Parallel Port Data Rate | 4 MHz max. to external processor |
| **CONNECTORS** | |
| VMEbus, P1 | 96-pin male DIN connector. The P2 connector is not used. |
| Analog Input Connectors | Four BNC bayonet coaxial, mounted on front panel. DB-25 used for 614E |
| Multipurpose Connector | 5th BNC user-selectable for: a) Pacer trigger input b) Analog threshold comparator input c) D/A output |
| Parallel Port | Front panel 25-pin DB-25S female. Provides external clock in. |
| **MISCELLANEOUS** | |
| Power Required | +5V dc ±5% at 3.0 Amps max. from VMEbus. |
| Operating Temp. Range | 0 to +60 °C. Forced cooling is recommended. |
| Storage Temp. Range | -20 to +80 °C |
| Relative Humidity | 10% to 90%, non-condensing. |
| Altitude | 0 to 10,000 feet. |
| Outline Dimensions | Double height VME, 6U outline. 9.19"W x 6.3"D x 0.6"H (233.5 x 160 x 15.24 mm). |
| Weight | 17 ounces (482 grams) |
| Analog Section Modularity | The MUX-S/H-A/D module is socketed for function interchange. |
| Analog Adjustments | Offset and gain per channel for SSH on DVME-614A. A single offset and gain pot is provided on DVME-614B,C, D, E. |

1. (Programmable gain is selectable on 2 channels on the DVME-614A only)

## TECHNICAL NOTES:

1. The input impedance of 10 Megohms minimum avoids attenuation errors from external input source resistance. For many applications, an external inline 50 ohm shunt, inserted adjacent to the front connectors, is recommended to reduce coaxial line reflections and standing wave errors.

2. Total throughput includes MUX settling time after changing the channel address, S/H acquisition time to rated specifications, A/D conversion and FIFO transfer. Total throughput is not delayed by host software whenever the FIFO is not full.

3. The rates shown for sequential sampling are the maximum A/D converter start rates and include MUX sequencing and settling. For example, if four channels were scanned, the maximum sample rate on any one channel of the DVME-614C would be 2 µSec. x 4 chan. = 8 microseconds (125 KHz per channel).

## TECHNICAL NOTES (Cont.)

4. THD test conditions are:

   1. Input frequency — 500 KHz (DVME-614A); 200 KHz (DVME-614B, E); 300 KHz (DVME-614C); 1 MHz (DVME-614D)
   2. Generator/filter THD is assumed to be -90 dB min.
   3. THD computed by FFT to 5th harmonic.

$$THD = 20 \times \log10 \frac{(V2^2 + V3^2 + V4^2 + V5^2)^{0.5}}{Vin}$$

   4. Inputs are half-scale. No channel advance.
   5. A/D trigger rate 1.5 MHz (DVME-614A), 500 KHz (DVME-614B,C,E), 4 MHz (DVME-614D).

5. For fastest response on the analog comparator trigger, keep the reference voltage near the trip input voltage. To avoid overload recovery delays, do not let the trip input (or any other analog input) exceed ±10 Volts.

6. Allow 20 minutes warmup time to rated specifications for model DVME-614B.

7. The DVME-614E offers programmable gain from X1 to X100 selected by a precision gain resistor. Higher gains will have increased settling delay.

### Simultaneous Sample/Hold

Four input signals are sampled at the same time using the DVME-614A's Simultaneous Sample/Hold (SSH) option. Once the signals are acquired, they are rapidly digitized sequentially by the A/D converter. For correlation of phase-related signals, SSH removes skew delay errors from conventional mux scanning.

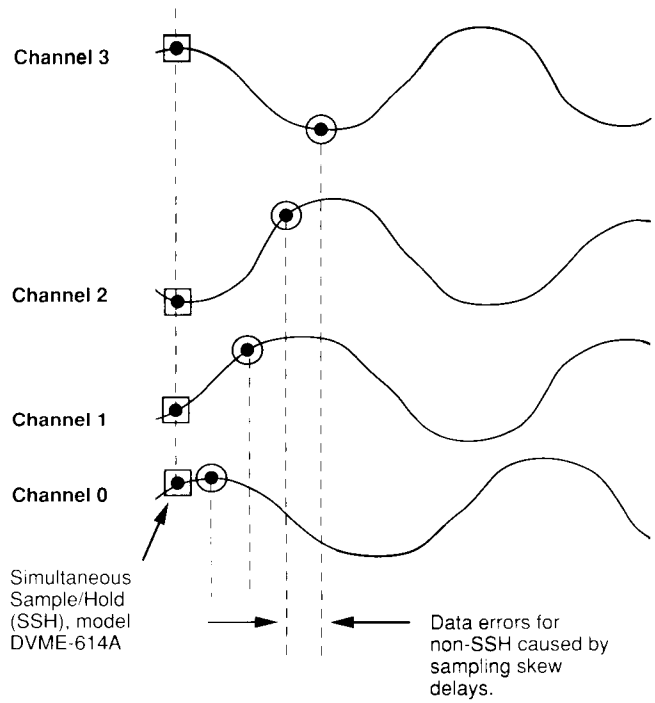



**Figure 2. Advantage of DATEL's SSH Design**

## Register Memory Mapping

The Base address may be selected anywhere up to $FFFF00h on 32-byte boundaries.

| Address (hex) | Direction | Description |
|---|---|---|
| Base + 0 | Write | Command Register |
| Base + 0 | Read | Status Register |
| Base + 2 | Write | Channel Address Register |
| Base + 4 | Write | D/A Data Register |
| Base + 6 | Write | FIFO Reset Register |
| Base + 8 | Not used | |
| Base + 0Ah | Not used | |
| Base + 0Ch | Read/Write | Interrupt Vector ID |
| Base + 0Eh | Read | FIFO A/D Data Register |
| Base + 10h | Read/Write | Counter #0 (82C54) |
| Base + 12h | Read/Write | Counter #1 (82C54) |
| Base + 14h | Read/Write | Counter #2 (82C54) |
| Base + 16h | Read/Write | Control Register (82C54) |

At power-up or VMEbus reset, all registers contain zeroes except the FIFO HF and FF bits. The registers may be programmed in any sequence as long as the command register is last.

## Command Register (Write BASE + 0)

| 15-8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| x-x | Interrupt Source | | | Port/ Bus* | Trig Pol | Cnvrt Enbl | Trigger Source | |
| | FF | HF | ACQ | | | | | |

"x" bits are not used or don't care.

Trigger Source [Bits 1,0]
- 00 =Scan by a write to the channel address register (normally not used).
- 01 =Scan by internal trigger.
- 10 =Scan by external TTL trigger.
- 11 =Scan by external analog threshold trigger.

Convert Enable [Bit 2]
- 0 =Disable A/D conversion (default)
- 1 =Enable A/D conversion

Trigger Polarity [Bit 3]
- 0 =Trigger on falling edge (default)
- 1 =Trigger on rising edge

Select FIFO Output Data Steering [Bit 4]
- 0 =Select VMEbus data register (Inhibit parallel port)
- 1 =Enable FIFO transfers to parallel port (Inhibit VMEbus data access)

Interrupt Source [Bits 7,6,5) These bits are OR'd.
- Bit 5 =Acquisition done flag (Counter 0 done)
- Bit 6 =FIFO half full flag
- Bit 7 =FIFO full flag
  - 0 =Disable interrupt (default)
  - 1 =Enable interrupt

(Only one interrupt source should be enabled at any one time.)

## Status Register (Read BASE + 0)

| 15-8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| x-x | FIFO Status | | | Ovr Smp Err | Xfr in Pro | Ana Trg Lvl | EOC Sts | ACQ Sts |
| | FF | HF | EF | | | | | |

Acquisition Status [Bit 0]
- 0 = A/D scan not in progress or scan done (Counter 0 sample count was reached).
- 1 = A/D scan in progress (Counter 0 sample count not reached)

End of A/D Conversion Status (EOC) [Bit 1]
- 0 = A/D conversion in progress, data invalid
- 1 = A/D conversion done, data valid

Analog Trigger Comparator Output [Bit 2]
- 0 = Analog trigger input is below reference
- 1 = Analog trigger input is above reference

Transfer in Progress [Bit 3]
- 0 = Remote device not ready for transfer
- 1 = Remote device is ready for transfer

Bit 3 displays parallel inport pin 2 (external Transfer Enable In) AND'd with command bit 4.

Oversample Error [Bit 4]
- 0 = No error
- 1 = A/D triggered before EOC is done.

Bit 4 is cleared by disabling A/D conversions (write command 2=0).

FIFO Status Flags [Bits 7,6,5]
- Bit 5: 0=FIFO is empty, 1= FIFO not empty
- Bit 6: 0=FIFO is half full, 1=less than half full
- Bit 7: 0=FIFO is full, 1=FIFO is not full

Note the negative true coding on these bits.

### Channel Address Register (Write BASE + 2)

| 15-8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| x-x | Auto Incr | SSH Ctrl | Not Used | | Channel Addr | | | |
| | | | | | 3 | 2 | 1 | 0 |

Channel Address [Bits 3 -0]
Only bits 1 and 0 are used for the 4-channel analog modules. 4 bits are used for DVME-614E.

Simultaneous Sample/Hold Control [Bit 6]
- 0 = Sequential or single channel mode
- 1 = Simultaneous sample/hold mode (see timing diagram)

In SSH mode, counter 0 must be programmed with the number of SSH channels (max = 4). One trigger is required per scan.

Channel Address Autoincrement [Bit 7]
- 0 =Single channel (no increment)
- 1 =Sequence channel address at start or end of A/D conversion

### D/A Data Register (Write BASE + 4)

| 15-12 | 11 | 10 | ... | 1 | 0 |
|---|---|---|---|---|---|
| x-x | DA1 MSB | DA2 | | DA11 | DA12 LSB |

### FIFO Reset Register (Write BASE + 6)

| 15 | ... | 00 |
|---|---|---|
| x | | x |

Any write to this register will clear the FIFO and set the empty flag true. If A/D conversion is still running, the FIFO will be not empty when the next A/D sample EOC occurs.

### Interrupt Vector Register (Read/Write BASE + 0Ch)

| 15-8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| x-x | V7 | V6 | V5 | V4 | V3 | V2 | V1 | V0 |

This register may also be used to verify proper board addressing before interrupts are enabled. Write and read back a range of values into the bits 7 - 0.

### FIFO Data Register (Read BASE + 0Eh)

| 15 | 14 | 13 | 12 | 11 | ... | 00 |
|---|---|---|---|---|---|---|
| S | S | S | S | MSB | | LSB |

12-bit A/D data

| 15 | 14 | 13 | ... | 00 |
|---|---|---|---|---|
| S | S | MSB | | LSB |

14-bit A/D data

"S" bits are sign-extended from either bit 11 (12 bit A/D's) or bit 13 (14-bit A/D's) in bipolar input range. For unipolar ranges, S = 0.

### 82C54 Programmable Interval Timer

The DVME-614 User Manual, shipped with the board, contains detailed programming information.

### Counter Register (Read/Write BASE + 10h-Counter #0) (Read/Write BASE + 12h - Counter #1) (Read/Write BASE + 14h - Counter #2)

| 15-8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| x-x | C07 | C06 | C05 | C04 | C03 | C02 | C01 | C00 |

### Control Word Register (Read/Write BASE + 16h)

| 15-8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| x-x | SC1 | SC0 | RL1 | RL0 | M2 | M1 | M0 | BCD |

| | | | |
|---|---|---|---|
| Select Counter | SC1 | SC0 | |
| | 0 | 0 | Select counter #0 |
| | 0 | 1 | Select counter #1 |
| | 1 | 0 | Select counter #2 |
| | 1 | 1 | Read back command |
| Read/Load | RL1 | RL0 | |
| | 0 | 0 | Counter latch operation |
| | 0 | 1 | Read/Load LSB only |
| | 1 | 0 | Read/Load MSB only |
| | 1 | 1 | Read/Load LSB then MSB |
| Mode | M2 | M1 | M0 |
| | x | 1 | 0 Rate generation |
| | 1 | 0 | 0 S/W trigger |
| | 1 | 0 | 1 H/W trigger |
| BCD | BCD | | |
| | 0 | | 16-bit binary count |
| | 1 | | 4-decade binary coded decimal count |

### Array Preprocessing

Figure 3 shows the DVME-614 installed in a typical VME application. The DVME-614 may be connected to an array processor board via a parallel port or the VMEbus. The parallel port offers higher speed by offloading block data transfers from the VMEbus. A separate cable is required for the parallel port.

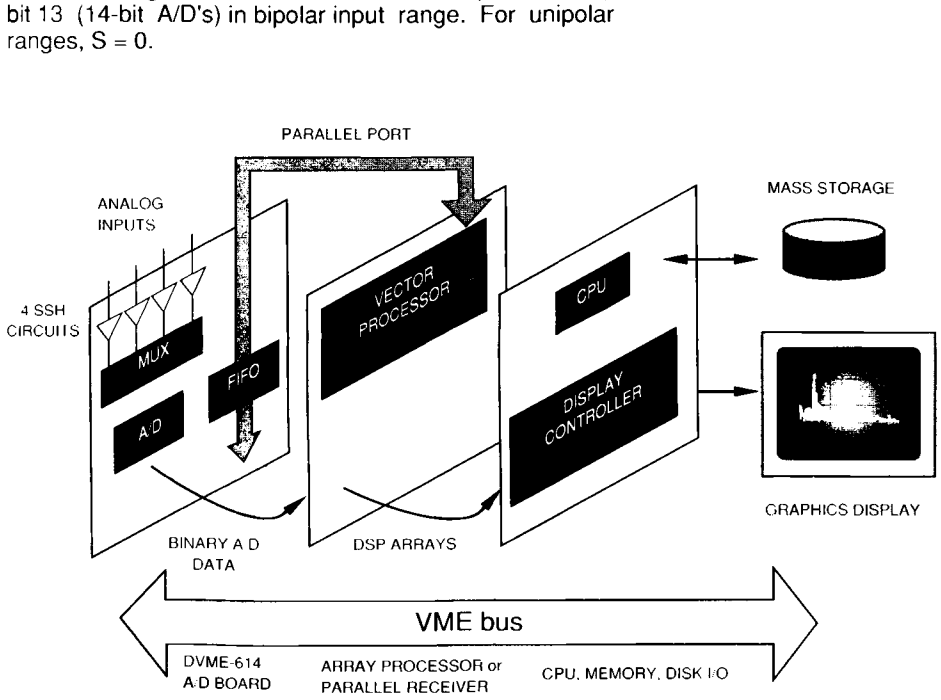



**Figure 3. Array Pre-processing with the DVME-614**

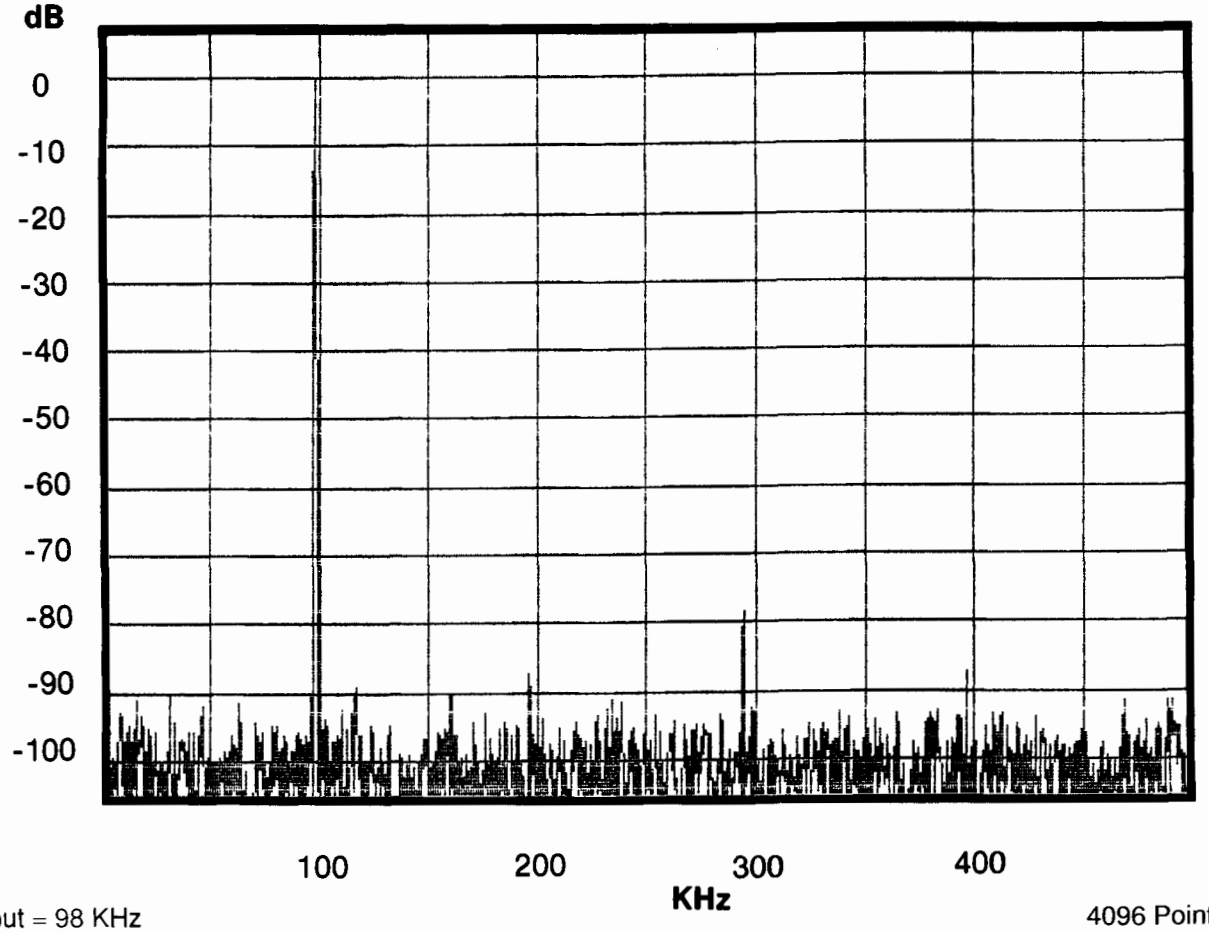



**Figure 4. DVME-614C Fast Fourier Transform**

## ANALOG TRIGGER

The analog threshold trigger is ideal for monitoring noisy inputs such as a telemetry receiver or RF/IF channel. As soon as the trigger threshold is transitioned, the FIFO immediately starts filling with A/D samples. The raw comparator output may be polled from the VMEbus in the status register, bit 2.

Since random noise may start this sampling process, the strategy is to collect a stream of A/D samples and quickly analyze if most of the samples contain valid data. If not, discard the sample array and start over.

The analog trigger input also accepts a purely digital input instead. By polling status bit 2, the analog trigger may be used as a general-purpose external control input. For example, this would terminate a high speed A/D file recording on disk from an external event

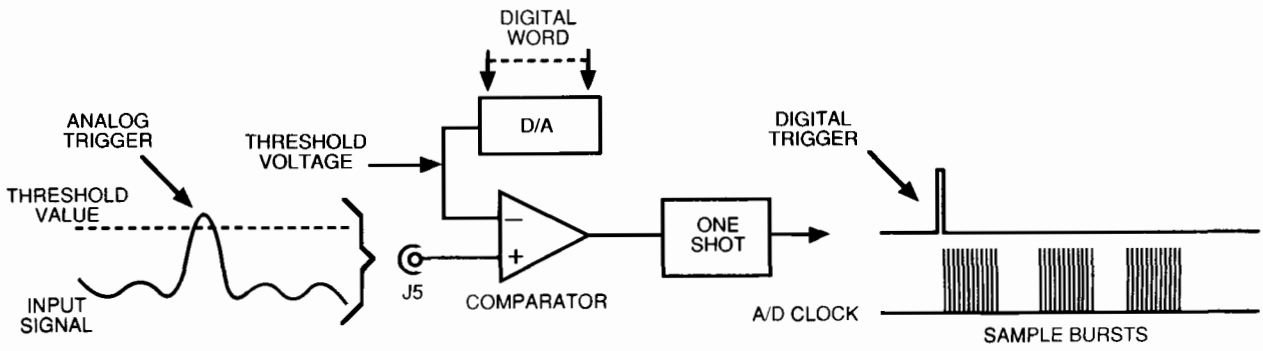



**Figure 5. Analog Threshold Trigger**

## System Timing Diagram

Because of the flexibility of the local timing and trigger systems, the DVME-614 operates in many modes. Figure 6 shows multiple trigger configurations with the Acquire flag as an A/D converter clock gate. Triggering may be from internal or external clocks or from the analog comparator. For precise phase tracking, use both an external trigger and an external A/D start clock.

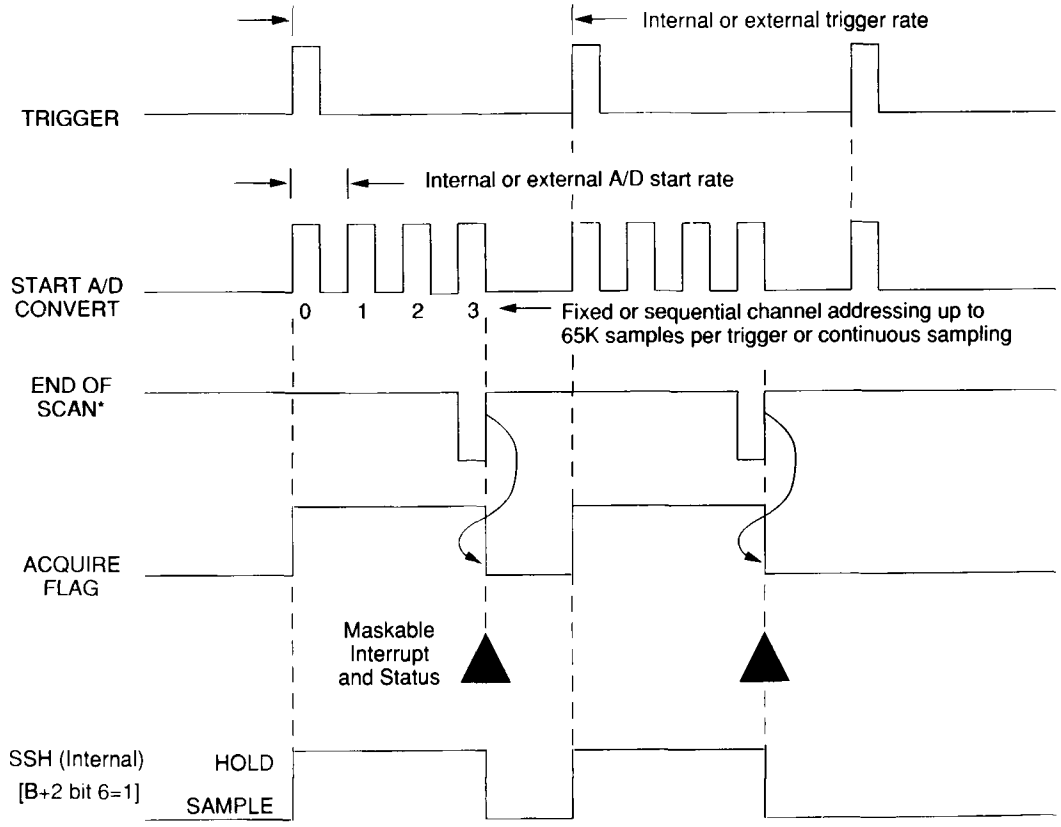



**Figure 6. Trigger per Scan Mode**

**ORDERING GUIDE**

| Model | A/D Bits | No. of Channels | Single Channel Sample rate | FIFO size (A/D samples) | Simul. S/H | PGA |
|---|---|---|---|---|---|---|
| **DVME-614A1** | 12 | 4 | 1.5 MHz | 1024 | 4 channels | x1,x10 |
| **DVME-614A2** | 12 | 4 | 1.5 MHz | 4096 | 4 channels | x1,x10 |
| **DVME-614B1** | 14 | 4 | 500 KHz | 1024 | none | none |
| **DVME-614B2** | 14 | 4 | 500 KHz | 4096 | none | none |
| **DVME-614C1** | 12 | 4 | 1 MHz | 1024 | none | none |
| **DVME-614C2** | 12 | 4 | 1 MHz | 4096 | none | none |
| **DVME-614D1** | 12 | 1 | 4 MHz | 1024 | none | none |
| **DVME-614D2** | 12 | 1 | 4 MHz | 4096 | none | none |
| **DVME-614E1** | 12 | 16S/8D | 250 KHz | 1024 | none | 1-100 |
| **DVME-614E2** | 12 | 16S/8D | (scan) | 4096 | none | 1-100 |

A software disk and user manual are included.
Boards are power-cycle burn-in tested.

**DVME-691** Screw terminal signal conditioning panel, pin-compatible to DVME-614E

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