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μTech

M-Vision 1500 Installation and User's Guide

MuTech Corporation

When Your Image Counts

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1 Introduction

1.1 Description

The M-Vision 1500 is a PCI bus frame grabber supporting up to 16-bit RS422 digital camera. On the camera side, it captures the image and stores the image in the on board VRAM. It features a maximum camera data clock of 40 MHz and all the features for camera control, timing and grabbing are software programmable (no jumper setting needed). On the PCI bus interface side, it can be programmed as either a bus master or a bus target. The on board VRAM sizes are 1MB, 2MB or 4MB (optional only at the time of order). And the maximum transfer rate for the PCI bus interface when programmed in the bus master mode is 55MB per second.

The MV-1500 board can interface to line scan, field scan (progressive) or frame scan (interlace) cameras from DALSA, EG&G, KODAK, PULNiX, etc. Contact MuTech for a complete list of supported cameras.

The MV-1500 is a three-quarter sized PCI board. It employs a 68-pin industrial standard connector. This makes cable assembling simple. The connections of the 68 pin connector is compatible with the AIA standard. Please refer to Appendix A for signal conections.

MuTech provides several digital cables for popular camera models from PULNiX, KODAK, DALSA, and EG&G. For digital cables of other cameras and other companies, please contact the Customer Support Group.

1.2 Distribution Software

Several utility programs are delivered with the MV-1500 board. They can be used for testing the installation, simple debugging, and demonstration purposes. Or they can be used as utilities for capturing video and saving to files. The operating environments supported by the distribution software are:

- DOS with a 32-bit extender
- Microsoft Windows 3.1 or 3.11, 16 bit DLL
- Windows 95, 32 bit DLL
- Windows NT 3.5 or later, 32 bit DLL
- IBM OS/2 Warp 3, 32 bit DLL

Also distributed with MV-1500 board is a group of camera configuration files which have been tested using corresponding cameras. If the camera you are using is not in this group, you can do one of the followings:

- Select a configuration file for a similar camera from the distributed group, then copy and edit it for your camera with any text editor;
- If you haved used the target camera with MV-1000/1100 and have a working camera configuration file for that board set. You should start from that configuration file, since most entries of the MV-1500 configuration file are backward compatible with the MV-1000 file.
- Contact the customer support group of MuTech corporation. The supporting staff might be able to help you generate and test the configuration file.

For detailed description of the MV-1500 configuration file format, please refer to Appendix C of this document.

1.3 Software Development Kits

The MV-1500 Software Development Kit enables developers and OEMs to program the MV-1500 board and create various applications using C and C++ languages. The MV-1500 SDKs have currently been designed and implemented for the following operating environments:

- MS-DOS, 32 bit object LIB using a DOS extender
- Microsoft Window 3.1 or 3.11, 16 bit DLL
- Windows 95, 32 bit DLL
- Windows NT 3.5 or later, 32 bit DLL
- IBM OS/2 Warp 3, 32 bit DLL

Sample source codes to demonstrate various features of the MV-1500 are also included with the SDK.

Please contact the customer support group at MuTech for any updated information regarding the products.

Camera Configuration File

The MV-1500 SDK helps programmers and OEMS to easily set up the frame grabber to work with various types of camera. A group of camera configuration files for various cameras is distributed with the MV-1500 boards.

A camera configuration file is a text file which contains parameter settings for one particular camera. Application developers and end-users can use any text editor to modify the camera configuration file. Please see the ***readme.txt*** file provided on the diskette(s) for a list of camera configuration files.

File Utility Routines

The MV-1500 SDK includes a group of file utility routines. Applications can use these routines to save grabbed images in various file formats, such as TIFF, TARGA, JPEG, BMP, and/or to display image files.

Sample Program

The MV-1500 SDK comes with sample programs and makefiles (where applicable) for each of the supported operating environments. These programs use many of the routines mentioned above and demonstrate the rich functionality and the ease of programming of the MV-1500 products.

No Register Level Access

The MV-1500 SDK does not provide the APIs for register level access to the MV-1500 board. MuTech believes that most applications do not need the register level access, since the equivalent functional level APIs have been provided through the SDK. The application programs developed with the current version of hardware/software will have much better compatibility with future revisions of MV-1500 products.

Please refer to the MV-1500 Software Development Guide for more details of the SDK.

2 Installation

2.1 System Requirements

Before installing the MV-1500 board, make sure that the following requirements are satisfied.

- The system must have at least one PCI slot available
- You must have a digital camera with either standard RS422 or low voltage differential interface to capture an image
- You must have the cable for the specific model/maker of your camera

2.2 Package Information

The standard shipping package of MV-1500 includes the following:

- MV-1500 board (1/2/4MB VRAM, specified at the time of order)
- MV-1500 User's Guide (this document)
- MV-1500 distribution diskette(s) for the operating environment of your choice

The following options should be ordered separately:

- MV-1500 Cable, which provides custom connection to the camera of your choice.
- SDK, which includes the diskette(s) and the MV-1500 Software Development Guide for the selected operating environment.

Please check your packing contents carefully; always check the readme file on the Distribution Diskette for the latest change of the package contents. If something is missing or damaged, you should immediately contact the MuTech Customer Support Deportment. The telephone number and email address are listed on the cover page.

2.3 Hardware Installation

MuTech strongly recommend that the users read the readme file in the MV-1500 Distribution Disk first. It contains the latest information regarding hardware/software installation procedures.

As a PCI bus frame grabber, MV-1500 is a Plug and Play device. It features automatic system configuration and ease of use. There is no need to set either I/O or memory addresses. All controls are software programmable.

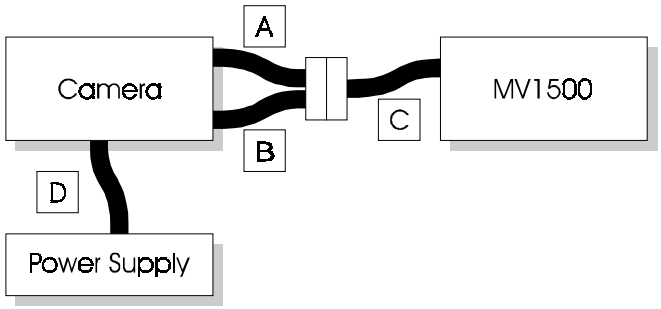
OEM Jumpers

There are three jumpers on the MV-1500 board for OEMs or integrators to configure them to provide an ID for particular application. For details on user settable jumpers, please see Appendix A.

2.4 Cable Connections

For a user who purchased the cable for the specific camera from MuTech, Figure 2.1 shows a typical case of how to connect the cable, the MV-1500, the camera and the camera power supply.

If the user needs to make his own cable, an AIA standard 68-pin male connector must be used. Consult Appendix B for the pin assignments of the connector.



A: Camera Data
B: Camera Control (many camera combine A and B in one)
C: MV-1500 68-Pin male AIA connector
D: Power plug (depending on camera)

Fig. 2.1 Cable Connection between Camera and MV-1500

2.5 Software Installation

Using the DOS Install Utility

Follow the steps below to install the MV 1500 software which includes the DOS and Windows demonstrations.

1) Insert the supplied DOS Distribution Disk and type:

   a:install or b:install

   for whichever floppy drive you are using. Press ENTER.

2) The install program will request the base directory name. The default directory is C:\MV-1500. You may enter a new directory name, or press ENTER to accept the default.

3) The install program makes four sub directories named "diag", "win", “camcfg", and "doc" under the main directory.

   - The base directory contains the initialization file mv-1500.ini for the MV 1500.
   - The "diag" directory contains the "dos4gw.exe" file (the DOS extender) and the demonstration/diagnostic program, m15diag.exe and a testing program,

camtest.exe, that can be used to verify the camera connection and newly created camera configuration files.

- The "win" directory contains a Windows Demo "w15demo.exe", a DLL and a bitmap files for the demo program.
- The "camcfg" directory contains a group of camera specific initialization (.ini) files.
- The "doc" directory contains a text file, readme.dst, which contains the most up-to-date information regarding the MV-1500 hardware and software.

4) Change the directory to "doc" from the base directory and print the "readme.dst" file. The readme.dst file also provides a description of functionality of the demonstration program.

Windows 3.1 Install Utility

Follow the steps below to install the MV 1500 software.

1) If you are already in Microsoft Windows, you can skip this step. If not, type:

   win

2) Insert the Windows Distribution Disk..

3) In the Windows Program Manager, select “File” and then “Run”, Type:

   "a:setup" or "b:setup"

4) In the Run dialog box for whichever floppy driver you are using. Press ENTER or click OK.

5) The install program requests a base directory name. The default directory name is C:\MV-1500. You may enter a new directory name, or press ENTER or click OK to accept the default.

6) The install program makes four subdirectories named "diag", "win", "camcfg", and "doc" under the main directory.

   - The main directory contains the initialization file MV-1500.ini for the MV-1500.
   - The "diag" directory contains the "dos4gw.exe" file (the DOS extender) and the demonstration/diagnostic program, m15diag.exe and a testing program,

camtest.exe, that can be used to verify the camera connection and newly created camera configuration files.

- The "win" directory contains a Windows Demo "w15demo.exe", a DLL and a bitmap file for the demo program.
- The "camcfg" directory contains a group of camera specific initialization (.ini) files.
- The "doc" directory contains a text file, readme.dst, which contains the most up-to-date information regarding the MV-1500 hardware and software.

7) The install program will request permission to create the MuTech Program Group. Click YES to create the Program Group or NO to abandon this procedure.

8) Change the directory to "doc" under the main directory and print the "readme.dst" file. The readme.dst file provides a description of functionality of the demonstration program.

Windows 95 and Windows NT Install Utilities

The procedures for the MV-1500 software installations under Windows 95 and Windows NT are similar to that for Windows 3.1, except that the demo program is named “cm15demo.exe” or “nm15demo.exe”, and stored under “win95” or “winnt” subdirectories, respectively.

Because a different installation tool is used for these 32-bit software installation, the user interface is slightly different during the installation comparing to that for Windows 3.1.

OS/2 Install Utilities

The procedure for the MV-1500 software installation under OS/2 is similar to that for Windows 3.1, except that the demo program is named “om15demo.exe” and stored under “os2” subdirectory.

2.6 Distribution Software

This section gives simple descriptions of the software distributed with MV-1500 board. These include a DOS demonstration utilities named m15diag.exe and camtest.exe, a Windows demonstration utility named either wm15demo.exe, cm15demo.exe or nm15demo.exe and an OS/2 demonstration program om15demo.exe.. Before you start the demo program, you must have a correct camera configuration file for you specific camera. Refer to Appendix C for detailed information on how to create a camera configuration file.

DOS

At the DOS prompt, type *camtest camera_configuration_file*, then press enter. You will see live video on screen. Here "camera_configuration_file" is a camera configuration file that is either created on-site or distributed with the MV-1500 software. This file contains parameters that MV-1500 will use to interface with a particular camera. The file is normally with an ".ini" extension. Please refer to Appendix C for the detailed description of the MV-1500 camera configuration file format and definitions.

Another program, "m15diag.exe", is provided for on-site diagnosis of the MV-1500 board. At the DOS prompt, type *m15diag* to start the program. Among other things, there is a list of menu selections. Type "4" to select diagnosis. A submenu will then show. Select "4" to start the diagnosis procedure and watch for each step of the diagnosis report. A camera is required during the diagnosis. The camera configuration file can be specified either when the program is first executed or by modifing the "Default Camera" entry under "[CAMERA]" section of the "mv-1500.ini" file, which can be located under the MV-1500 installation base directory.

Windows and OS/2

From the program manager, double click the icon. You will see a window pop up with the following menus.

- File: Load/Save an image from/to file.
- Video: Set camera and video capturing size.
- Display: Set VGA display mode.
- Snap: Using this menu to capture single frame.
- LUT: Under this menu, you can set the look up table.
- Help: Use this to get information about the demo program.

3 Architecture

3.1 Block Diagram

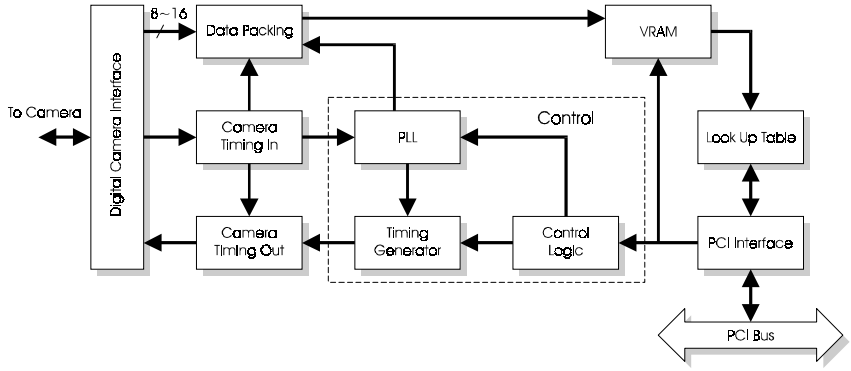


Figure 3.1 Block Diagram of MV-1500

Figure 3.1 shows the major components of the MV-1500 board. These Components are:

- Digital Camera Interface
- Data Packing
- VRAM Buffer
- Look Up Table
- Camera Timing Input
- Camera Control Output
- Control Logic
- PCI Bus Interface
- Phase-Locked Loop (PLL)
- Timing Generator

3.2 Overview of the Block Diagram

Digital Camera Interface This block provides necessary conversion between RS422 differential signals and TTL signals. It also provides necessary buffers for all the control sigals in TTL level out of and into the MV-1500 board.

Data Packing This block consists of a group of registers. Its purpose is to pack pixel data into 32-bit double word. The maximum input data width is 16-bit. A programmable shift operation can be done on the incoming data with a down shift value of 0, 2, 4, 6, and 8. The MSBs after shift-down is padded with 0 if no corresponding valid pixel data bit is available. The shift down capability results in flexibility of cable connections and in convenience of displaying to VGA with data depth greater or equal to 10 bits.

VRAM The size of the on board VRAM may be ordered as 1MB, 2MB or 4MB. The VRAM on the MV-1500 board is organized as a one-dimensional array. During video capture, the video data are always packed into doublewords and stored in VRAM linearly. There is no gap in storage between the last pixel of line n and the first pixel of line n+1. The memory is shared between the capturing and the PCI interface.

Look Up Table The host accesses the VRAM data through the on board Look Up Table. The LUTs are organized as four 8-bit physical lanes. Each lane of LUTs is a 2kx8 SRAM and can be used either as 8 banks of 256x8 LUTs or as 2 banks of 1024x8 LUTs. The selection is software controllable.

Camera Timing In There are four basic timing signals: Line Data Valid (LDV), Frame Data Valid (FDV), Pixel Clock (PCLK) and Field (FLD). They provide important timing information of the camera. They are used to control the video capture process on the board.

Camera Control Output The most important signals in this block are the EXternal SYNC (EXSYNC) and Master CLocK OUT (MCLKOUT). They provide the camera a the sync signal and the timing clock. Other signals in this group provide integration/exposure control, etc. over the camera.

Control Logic The control is set by software. A camera configuration file can be easily used to set the operation of the control logic. The control logic generates camera control signals and coordinates the operation between data packing block and VRAM. It also takes one of several possible trigger sources to start video capture.

Phase-Locked Loop (PLL)

The PLL is used to generate either pixel clock or master clock. It can be operated in one of three modes: (1) locking to LDV and generating board pixel clock; (2) locking to PCLK and generating board pixel clock; and (3) synthesizing to a specified master clock from the on-board crystal oscillator reference.

Timing Generator

This block generators several signals used to drive/control the camera unders software control. It takes a pixel/master clock, and generates H.Drive, V.Drive and H.Gate (may be used to control the exposure tme).

PCI Bus Interface

The PCI interface of the MV-1500 is designed to use configuration space and memory space only. The MV-1500 requires an 8MB memory slot within the 4GB PCI memory space. The registers and LUTs are all located in the first 4MB starting at the Memory Base Address (assigned by the system at bootup). The VRAM buffer is located at the Memory Base Address + 4MB and occupies 1, 2 or 4MB of space. The MV-1500 PCI interface can be configured as either a PCI bus master or a PCI bus target.

Appendix A: Jumper Settings

All the six jumpers on the MV-1500 board correspond to a status register. When the jumper is in, the corresponding bit is read as a 0. Otherwise, it is a 1. Table A.1 lists MV-1500 jumpers, their functions and their factory default setting. Fugure A.1 shows the position of the jumpers on the MV-1500 board.

Jumper	Function	Factory Default
JP6, 5, 4	For OEM Use	All out
JP3, 2, 1,	Reserved, Don't Use	All out

Table A.1 MV-1500 Jumpers

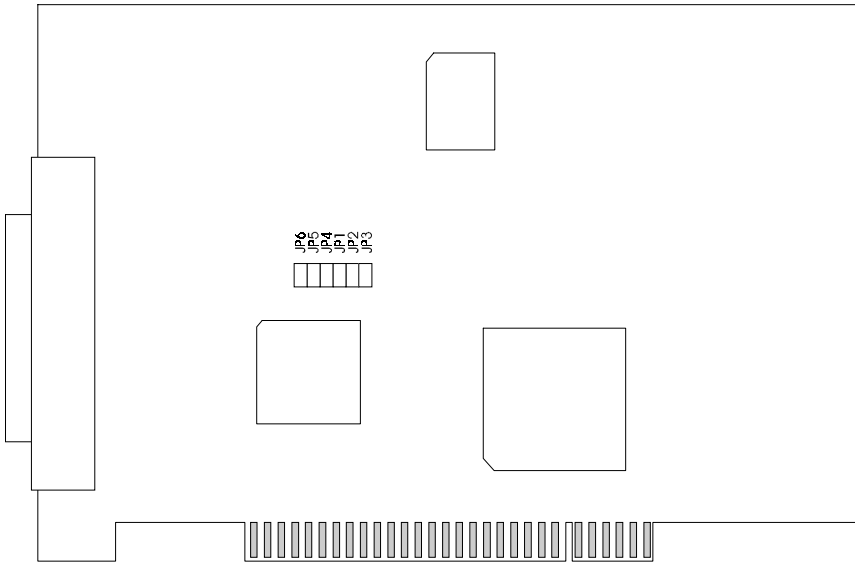


Figure A.1 Jumper Positions on MV-1500 Board

Appendix B: Specification of Connector

There is only one connector P1 on the MV1500 board. This is an AIA standard 68-pin female connector. The connector pin assignment is listed in table B. 1.

Signal Name	MV-1500 68 Pin Female
D0+	20
D0-	54
D1+	19
D1-	53
D2+	16
D2-	50
D3+	15
D3-	49
D4+	14
D4-	48
D5+	13
D5-	47
D6+	11
D6-	45
D7+	10
D7-	44
D8+	9
D8-	43
D9+	8
D9-	42
D10+	7
D10-	41
D11+	6
D11-	40
D12+	5
D12-	39

D13+	4
D13-	38
D14+	3
D14-	37
D15+	2
D15-	36
LDV+	26
LDV-	60
FDV+	25
FDV-	59
PIXCLK+	29
PIXCLK-	63
MCLKIN/FIELD+	24
MCLKIN/FIELD-	58
EXSYNC/SHTR+	30
EXSYNC/SHTR-	64
PRIN/FST+	22
PRIN/FST-	56
MCLKOUT+	23
MCLKOUT-	57
VINIT/FST&EXP	21
VD_OUT	65
HD_OUT	66
INTEG/MC1	32
INT_ENA/MC0	31
GP#1/MC2	33
GP#0	28
CONT_SIG_TRIG	67
GRAB_TRIG	55
SIGNAL GND	1,12,34,35,46,68
RESERVED	27,61,62
NO CONNECTION	17,18,51,52

Table B.1 Connector pin assignment

Figure B.1 shows the pin positions of the P1 connector when facing the pins.

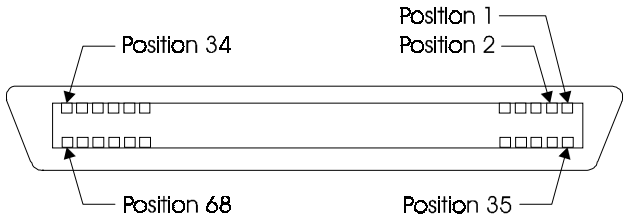


Figure B.1 68-Pin male connector

Appendix C: Camera Configuration File Format

Figures C.1 and C.2 are camera configuration control roadmaps of the MV-1500 board. They are included here to help the user to understand the meaning and the usage of the connector signals, the configuration file parameters and some of the key internal signals. The shaded parameters correspond to an entry in the camera configuration file. The all uppercase names at the connectors are the input/output connections of the P1 connector. Please refer to Appendix B for pin assignments. This appendix gives information on what these parameters do to interface a camera.

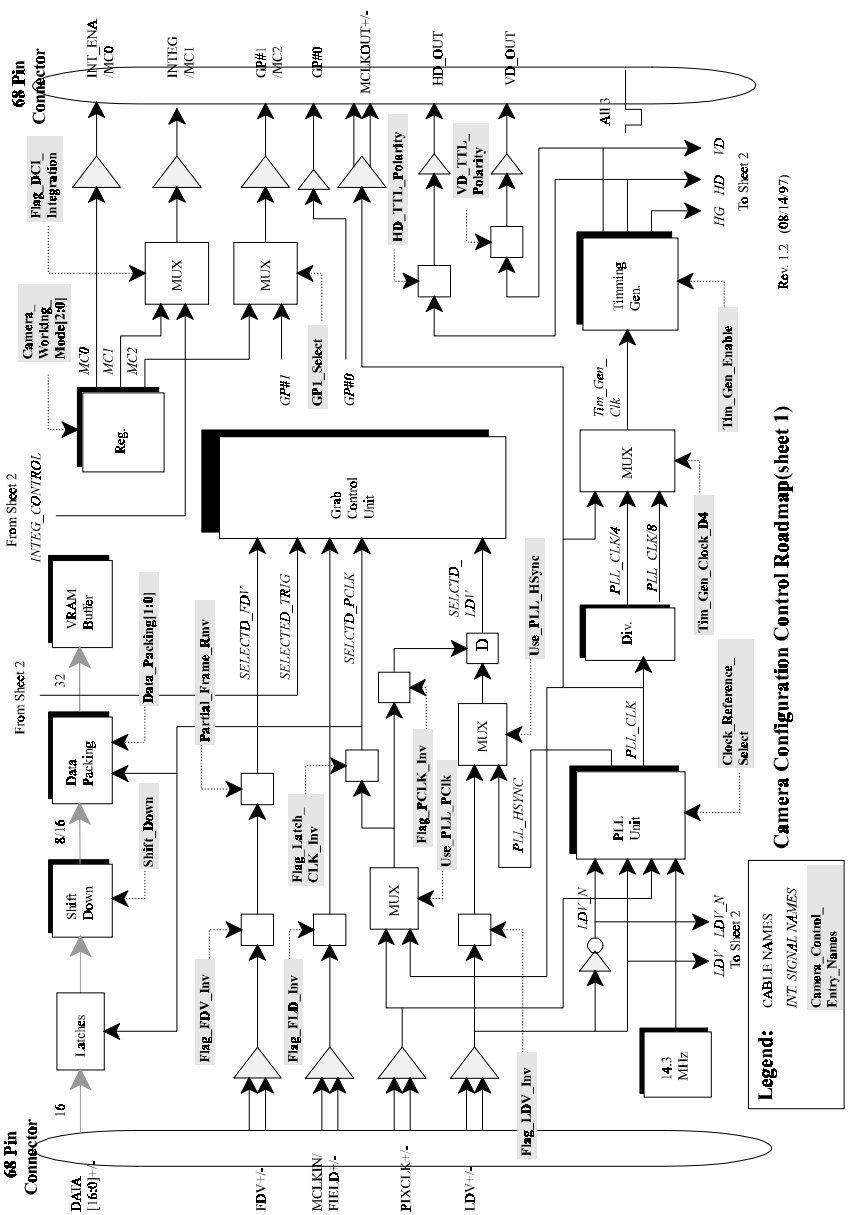


Figure C.1 Camera Configuration Control Roadmap 1

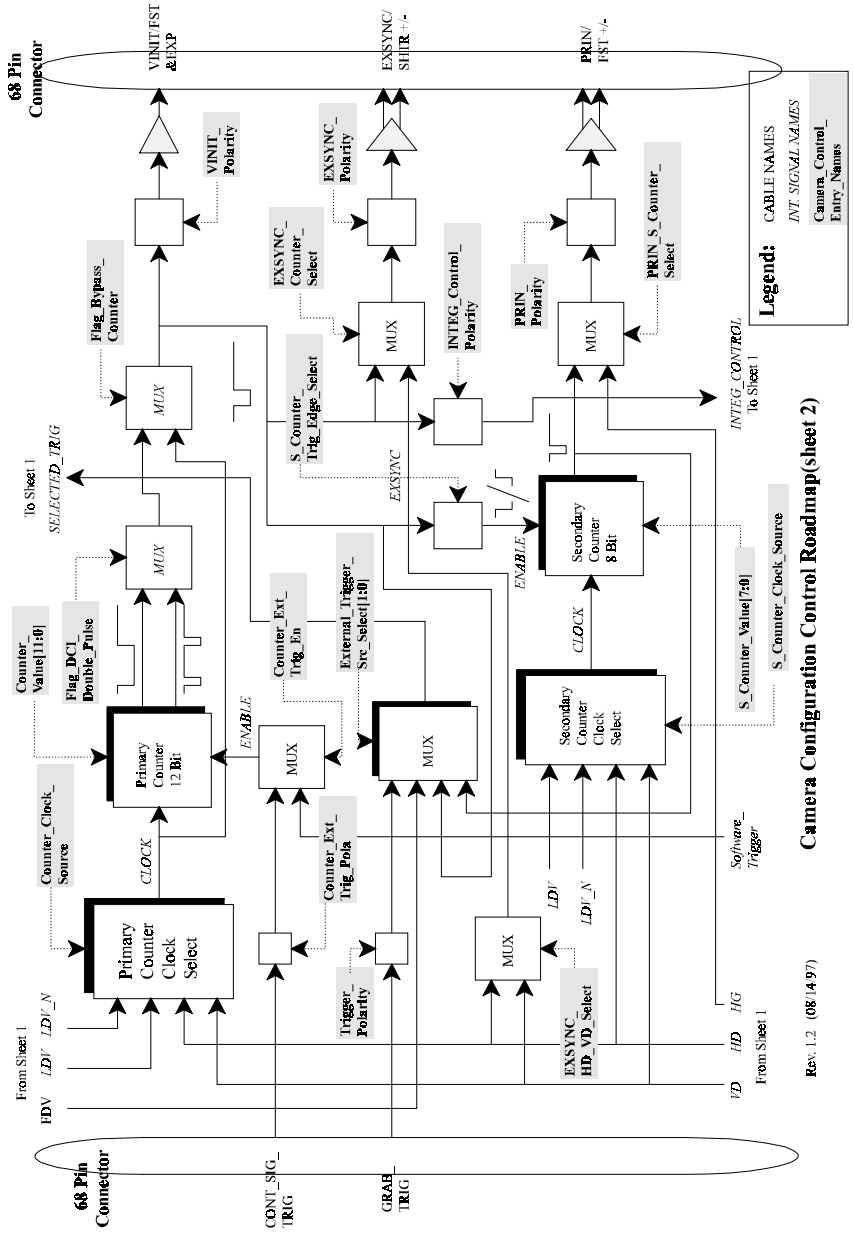


Figure C.2 Camera Configuration Control Roadmap 2

A camera configuration file consists of one or more sections with each section containing names and values; each pair of a name and a value is used too accomplish a specific task. Some sections are only used for particular cameras and some parameters are only used for some special features of a camera. Each section in this file has the following format.

```
[Section Name]
Name1=Value1
Name2=Value2
...
```

The old Camera Configuration File Format 1.0 uses single section orgnization: A section name to identify the camera, followed by all the names specified. The advantage of this approach is that a single file can contain configurations for multiple cameras.

Camera Configuration File Formats 2.0 and later use multiple sections to define a camera setting. This approach makes the camera configuration file better organized. Because all the section names are predefined, one file can specifiy only one camera. Also added in the new format are the new names defined for some special camera features.

Format 2.0 and later allow integers to be given in either decimal or hexadecimal format. The hexadecimal format requires a “0x” prefix.

While the MV-1500 still recognizes camera configuration files in format 1.0 and 2.x, which are originally designed for the MV-1000, Camera Configuration File Format 3.0 is designed specifically for the MV-1500. This is necessary because the MV-1500 offers many new software controllable features that are not available in the MV-1100 module and hence cannot be specified in either format 1.0 or 2.x.

Since this format is similar to the Microsoft Windows format for program initialization, **GetPrivateProfileString()**, and **GetPrivateProfileInt()**, which are available from the Windows API and the WIN32 API, can be used to access a camera configuration file.

If a name is not specified in the camera configuration file, the MV-1500 software internal default value for that name is used.

A camera configuration file of format 3.0 contains the following sections.

```
[Miscellaneous]
[General Control]
[Sync/Trigger Selection]
[PLL Control]
[Grab Window Control]
[Digital Camera Control]
[Digital Grab Control]
```

The next few sections explain all the names defined in a camera configuration file in version 3.0 format.

C.1 Miscellaneous Section

This section is dedicated to providing information about the camera and the configuration file.

```
Version=3.0
CameraID=Name of the camera
```

Version indicates the camera configuration file format in use. The MV-1500 SDK handles versions 1.0, 2.0, 2.1 and 3.0.

CameraID is a free form text string to identify the camera. This field is defined mainly for the application program and is not used by the SDK internally.

C.2 General Control Section

This section provides the high level setup to control different kinds of cameras and data arrangements. In this section the MV-1500 can be programmed to work with: (1) interlaced or non-interlaced cameras, (2) field scan or line scan cameras, and (3) cameras that need an external clock or cameras that have their own clocks

```
Flag_Digital_Cam=1
Flag_Line_Scan=0
Tim_Gen_Enable=0
Flag_Interlace=1
Pixel_Mode=0
Shift_Down=0
```

Flag_Digital_Cam indicates that this is for a digital camera. This is a reserved field and should always be set to 1.

Flag_Line_Scan specifies the option for a line scan or an area scan camera.

```
0: Use area scan camera
1: Use line scan camera
```

Tim_Gen_Enable enables or disables the MV-1500 timing generator. This generates timing signals for a given camera (eg. when performing camera integration) or generate synchronization signals to drive a camera. This parameter works in conjunction with the *PLL Control* and *Timing Generator Control* sections.

```
0: Disable timing generator
1: Enable timing generator
```

Flag_Interlace indicates the use of an interlaced or non-interlaced camera.

```
0: Use a non-interlaced camera
1: Use an interlaced camera
```

Pixel_Mode specifies how digital data is to be packed into 32 bit double words before being stored in the MV-1500s memory buffer.

```
0: 8 bits per pixel. (4 pixels packed in each
   double word )
1: 10 bits per pixel (2 pixels packed in each
   double word )
2: reserved value and should not be used
3: 12 bits per pixel (2 pixel packed in each
   double word )
4: 16 bits per pixel (2 pixel packed in each
   double word )
```

Shift_Down determines whether and how to perform a pixel data shift by the MV-1500. The highest bits of the shifted down data are filled with zeroes if no corresponding valid pixel bits are available.

```
0: No shift
1: 2 bits shift down
2: 4 bits shift down
3: 6 bits shift down
4: 8 bits shift down
```

C.3 Sync/Trigger Selection Section

Entries in this section are used to select Sync and Triggering signals. Selections include the channel where the Sync. signal originates, the source of the Sync signal, the type of Sync signal, whether an external signal should be used for triggering, the Sync signal polarity, and the triggering signal polarity.

```
External_Trigger=0
External_Trigger_Src_Select=0
Trigger_Polarity=0
Use_PLL_HSync=0
Use_PLL_PClk=0
```

External_Trigger is used to control the external trigger mode. When set to 1, it also sets the signal GRAB_TRIG on pin 55 as the external trigger signal.

```
0: External Trigger disable.
1: External Trigger enable.
```

External_Trigger_Src_Select determines the trigger source among the 4 possible candidates. This field is ignored if External_Trigger is set to 0.

```
0: Use the signal from GRAB_TRIG at Pin 55.
1: Use FDV input as the trigger signal.
2: Use the output from the primary counter
   as the trigger signal..
3: Use the output from the secondary counter
   as the trigger signal.
```

Trigger_Polarity determines the polarity of the external trigger. This field is not used when **External_Trigger** is set to 0.

```
0: Trigger at falling edge (active low).
1: Trigger at raising edge (active high).
```

Use_PLL_HSync determines whether to use the external LDV signal (after the polarity control) or to use the internal PLL generated H. Sync signal as the MV-1500 internal horizontal timing reference clock.

```
0: Use external LVAL
1: Use internal PLL generated H. Sync
```

Use_PLL_PClk determines whether to use the external pixel clock or to use the internally generated PLL pixel clock as the clock reference for data latching and data packing.

```
0: Use the external pixel clock
1: Use the internally generated PLL pixel
   clock.
```

C.4 PLL Control Section

Entries in this section are used to program the Phase Lock Loop (PLL) to lock on the Reference PLL signal (externally or internally) in order to generate the pixel clock.

```
H_Period=63.556
Pixel_Per_Line=0x4f8
Clock_Reference_Select=3
Pixel_Clock_Freq=14.318180
```

H_Period specifies the camera line period (not just the active part of it) in micro-seconds. This timing is also used internally to determine the PLL reference. This value can be obtained from the camera vendor or from the camera's specification. This name is used if the name **Clock_Reference_Select** is set to 0 or 1.

Pixel_Per_Line specifies the number of pixels in each line. This is the total pixel clock in the full line, not just the active pixel in a line. This name is used if the name **Clock_Reference_Select** is set to 0 or 1.

Clock_Reference_Select selects one of the four references from the PLL Reference Multiplexer for the PLL circuit.

```
0: Select inversed Line Valid (LVAL inv)
1: Select Line Valid (LVAL)
2: Select External pixel clock from the cam-
   era
3: Select 14.31818 MHz clock generated by
   the MV-1500 on-board crystal
```

Pixel_Clock_Freq specifies the frequency (in MHz) of the pixel clock which the PLL needs to generate. This clock may be provided externally or may be generated (5 - 40 MHz) by the MV-1500 internally. This name is used if the name **Clock_Reference_Select** is set to 2 or 3.

C.5 Grab Window Control Section

Entries in this section are used to define the size and the starting position of the captured video.

```
H_Offset=0x10
V_Offset=0x0
H_Max_Capture_Size=0x2f4
```

```
V_Max_Capture_Size=0x1e4
```

H_Offset specifies the horizontal starting point in pixels of the active video from the front edge of the Horizontal Sync Signal.

```
Range:0 - 0xFFFF (Hex)
```

V_Offset specifies the vertical starting point in lines of the active video from the front edge of the Vertical Sync Signal. This parameter is in Hex format.

```
Range:0 - 0xFFFF (Hex)
```

H_Max_Capture_Size specifies the maximum number of pixels to be captured per line of active video. The sum of the **H_Offset** and the **H_Max_Capture_Size** must be smaller that the total number of clock cycles in a full line.

V_Max_Capture_Size specifies the maximum number of lines to be captured per frame of active video. In the case of an interlaced camera, this is the number of lines in a frame, not in a field.

C.6 Timing Generator Control Section

Entries in this section are used to control special cameras which require Sync or timing signal inputs. By specifying the parameters, a camera can be driven with different kinds of Sync signals and/or different pixel clocks generated by the MV-1500. H + V Sync signals with different polarities can be provided. Different resolutions of the camera being driven can be defined.

This section will be ignored if **Tim_Gen_Enable** in [*General Control*] equals to 0.

```
Camera_Master_Clock=0
Camera_Pixel_Per_Line=0x38e
Camera_Drive_Width=0x67
Camera_Drive_Height=0x3
Camera_Line_Per_Frame=0x20d
Camera_Interlace=1
Tim_Gen_Clock_D4=0
```

Camera_Master_Clock specifies whether the pixel clock frequency from the PLL is the so-called MASTER CLOCK. A MASTER CLOCK (2 x pixel clock) is required by some cameras as the input clock. This flag tells the timing generator that the received clock is twice the pixel clock frequency.

```
0: Use PLL pixel clock
1: Use 2 x PLL pixel clock
```

Camera_Pixel_Per_Line specifies the number of pixels per full line period for the camera being driven.

Camera_Drive_Width specifies the width (in pixels) of the Horizontal Sync signal to drive the camera.

Camera_Drive_Height specifies the height (in lines) of the Vertical Sync signal to drive the camera.

Camera_Line_Per_Frame specifies the number of lines per frame, not just active video, for the camera being driven.

Camera_Interlace specifies the type of camera being driven by the MV-1500.

```
0: Interlaced camera
1: Non-Interlaced camera
```

Tim_Gen_Clock_D4 generates a special clock for the MV-1500. Notice that this name, Tim_Gen_Clock_D4, is inherited from the MV-1000. The MV-1500 can support “divide by 8” while the MV-1000 supports “divide by 4” only.

```
0: Use the clock generated by the PLL.
1: Use a clock derived from the PLL clock.
   This clock is 4 times slower than the PLL
   clock.
2: Use a clock derived from the PLL clock.
   This clock is 8 times slower than the PLL
   clock.
```

C.7 Digital Camera Control Section

Entries in this section are used to control a digital camera. Some of these parameters are used to control special cameras. All digital camera control signals are connected to a 68 pin high density connector. Please refer to *Appendix B* for more details on the connection. Please refer to the block diagrams (Figure C.1 and Figure C.2) for the names discussed in this section and the next section.

```
Flag_DCI_Integration=0
Flag_DCI_Double_Pulse=0
Camera_Working_Mode=0x3
GP1_Select=1
```

```
Counter_Clock_Source=0
Counter_Value=0x10
Counter_Ext_Trig_En=0
Counter_Ext_Trig_Pola=0
Flag_LS_Exp_En=0
LS_Exp_Start=0x0
LS_Exp_End=0x0
Flag_Bypass_Counter=0
Flag_ExSync_Auto=0
S_Counter_Clock_Source=0
S_Counter_Value=0
S_Counter_Trig_Edge_Select=0
VINIT_Polarity=0
PRIN_S_Counter_Select=0
PRIN_Polarity=0
HD_TTL_Polarity=0
VD_TTL_Polarity=0
Flag_Latch_CLK_Inv=0
Flag_FLD_Inv=0
INTEG_Control_Polarity=0
EXSYNC_HD_VD_Select=0
EXSYNC_Counter_Select=0
EXSYNC_Polarity=0
```

Flag_DCI_Integration enables and disables the integration control for a digital camera. When it is enabled, Pin 32 of the digital camera cable carries the integration control signal. When it is disabled, Pin 32 carries a static MC1 signal.

```
0: Disable
1: Enable
```

Flag_DCI_Double_Pulse generates double pulses for reset of a digital camera.

```
0: No double pulses
1: Generate double pulses
```

Camera_Working_Mode controls outputs (MC0 - MC2) for a digital camera. These outputs are usually used for Kodak and Pulnix cameras through a DB37 female connector.

The default value is 0, which means:

```
MC0 = OFF, MC1 = OFF, MC2 = OFF
```

If the value is ON, the corresponding signal will be set to a static HIGH and vice versa.

GP1_Select determines whether the shared pin (Pin 33) carries a general purpose control signal or an MC2 signal.

```
0: MC2 signal on Pin 33
1: GP signal on Pin 33
```

Counter_Clock_Source selects one of four clock sources to drive the 12 bits down counter which generates the signal for digital camera control.

```
0: Line data valid (LDV) signal
1: Inverted line data valid signal
2: Horizontal Drive (H.D.) signal generated
   by the Timing Generator
3: Vertical Drive (V.D.) signal generated by
   the Timing Generator
```

Counter_Value specifies the value for the 12 bit down counter. This counter is used to adjust the pulse width of the generating digital control signal. Several control signals which are sent out as PRIN, EXSYNC or INTEG are programmed through this counter. The output of this counter is active low.

```
Range:0 - 0x0FFF
```

Counter_Ext_Trig_En selects the hardware signal (CONT_SIG_TRIG, pin 67) or the software signal to trigger the 12 bits down counter.

```
0: Use the External Trigger signal
1: Use the Software Trigger signal
```

Counter_Ext_Trig_Pola selects the polarity of the CONT_SIG_TRIG signal which triggers the 12 bits down counter.

```
0: the falling edge
1: the raising edge
```

This parameter has effect only when the Counter_Ext_Trig_En is used.

Flag_LS_Exp_En enables and disables PRIN control output for a linescan camera. When it is enabled, LS_Exp_Start and LS_Exp_End define the position and duration of the linescan exposure reduction control signal.

```
0: Disable
1: Enable
```

LS_Exp_Start specifies the beginning of the exposure control signal in terms of pixel clocks for a line scan camera. This parameter only has effect on line scan cameras.

LS_Exp_End specifies the end of the exposure control signal in terms of pixel clocks for a line scan camera. This parameter only has effect on line scan cameras.

Flag_ExSync_Auto selects the frame rate control for the Dalsa CA camera. The control signal will go out to the EXSYNC control output (pins 27 and 28 of the 68 Pin female connector).

```
0: Frame rate controlled by the signal from
   the EXSYNC control output.
1: Run at the maximum frame rate mode of the
   Dalsa CA camera, refer to the camera man-
   ual for details.
```

This entry is only used with the Dalsa CA camera.

Flag_Bypass_Counter enables or disables a special feature which re-routes the clock source (specified by Counter_Clock_Source) as if it is the 12-bit Primary Counter output, instead of using it to drive the 12 bit counter. This feature is specifically used for EG&G cameras.

```
0: Disable
1: Enable
```

S_Counter_Clock_Source selects one of the four (4) possible signals as the clock for the secondary camera control counter. This is an 8-bit counter which is automatically triggered by the output of the Primary Counter.

```
0: Use the raising edges of the Line Data
   Valid signal clock
1: Use the falling edges of the Line Data
   Valid signal clock
2: Use the MV-1500 generated horizontal
   drive signal generated by the Timing Gen-
   erator
3: Use the MV-1500 generated vertical drive
   signal generated by the Timing Generator
```

S_Counter_Value takes an 8-bit value as the secondary counter

Range:0 - 255

S_Counter_Trig_Edge_Select determines at which edge of the Primary Counter output to start the Secondary Counter.

```
0: The falling edge
1: The raising edge
```

VINIT_Polarity determines the polarity of the signal VINIT/ FST&EXP (pin 21). The result of the setting also depends on the selection of **Flag_Bypass_Counter**. **If Flag_Bypass_Counter** is set to 0, then

```
0: No change
1: Inverted
```

If Flag_Bypass_Counter is set to 1

```
0: Active low
1: Active high
```

PRIN_S_Counter_Select determines whether to use the output of the secondary counter or to use the on-board Timing Generator H. Gate signal as the differential output of PRIN/FST on Pin 22 and 56. The polarity of the output is further determined by PRIN_Polarity setting.

```
0: Select H. Gate
1: Select secondary counter output
```

PRIN_Polarity determines the polarity of PRIN/FST output on Pin 22 and 56.

```
0: Active low
1: Active high
```

HD_TTL_Polarity determins the polarity of the TTL horizontal drive signal.

```
0: Active low
1: Active high
```

VD_TTL_Polarity determins the polarity of the TTL vertical drive signal.

```
0: Active low
1: Active high
```

Flag_Latch_CLK_Inv determines the polarity of the clock used on the first stage of data latching. This is based on the PIXCLK input (pin 29 and 63).

```
0: No change
1: Inverted
```

Flag_FLD_Inv determines the polarity of the field signal before it is passed further to other MV-1500 control logics. The resulting signal is used to determine the field order for interlaced cameras. This is based on the MCLKIN/FIELD input (pin 24 and 58).

```
0: No change
1: Inverted
```

INTEG_Control_Polarity determines the polarity of the INTEG_CONTROL before it is passed further as the INTEG/MC1 output on pin 32. Notice that the final output on pin 32 is determined by **Flag_DCI_Integration**.

```
0: Active low
1: Active high
```

EXSYNC_HD_VD_Select determines whether to use the H. Drive or V. Drive as the EXSYNC output. Notice that the final EXSYNC/SHTR output is determined by EXSYNC_Counter_Select.

```
0: Use H. Drive
1: Use V. Drive
```

EXSYNC_Counter_Select Determines whether to use EXSYNC or the counter output as the EXSYNC/SHTR output (pin 30 and 4). Notice that the polarity of the final output if further determined by EXSYNC_Polarity.

```
0: Select EXSYNC
1: Select counter
```

EXSYNC_Polarity determines the polarity of the EXSYNC/SHTR output.

```
0: Active low
1: Active high
```

C.8 Digital Grab Control Section

Entries in this section are used to program the size of the video (if a digital area scan camera is used) or the length of the scan line (if a digital line scan camera is used).

```
Flag_LDV_Inv=0
Flag_FDV_Inv=0
Flag_PCLK_Inv=1
Flag_Partial_Frame_Rmv=0
```

Flag_LDV_Inv enables and disables inversion of the input LDV signal (pin 26 and 60) before it is passed to the grab and packing controller.

```
0: LDV not inverted
1: LDV inverted
```

Flag_FDV_Inv enables and disables inversion of the input FDV signal (pin 25 and 59) before it is passed to the grab and packing controller.

```
0: FDV not inverted
1: FDV inverted
```

Flag_PCLK_Inv enables and disables inversion of the input pixel clock signal (pin 29 and 63) before it is passed to the grab and packing controller.

```
0: PCLK not inverted
1: PCLK inverted
```

Flag_Partial_Frame_Rmv enables and disables the partial frame removal feature when using the asynchronous reset mode of some digital camera.

```
0: Not remove partial frame on Async. reset.
1: Remove partial frame on Async. reset.
```

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