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NALLATECH

# BenADDA™

## 14-Bit, ADC and DAC DIME-II™ Module

### Overview

The BenADDA provides high-speed digital-to-analogue and analogue-to-digital conversion. As part of the scalable DIME-II family, the BenADDA can be easily integrated into systems, through the range of available DIME-II motherboards and associated software/firmware.

### DIME-II

Building upon the global success of the award-winning DIME standard, the DIME-II modular systems platform with TeraOPS performance enables users to harness the full capability of advanced FPGAs. DIME-II brings together unparalleled off-module I/O, flexible FPGA device support and exceptional bandwidth capabilities for next-generation systems design. The scaleable DIME-II family of products includes DIME-II motherboards, modules, firmware and software, providing a complete systems solution. The firmware and software associated with the DIME-II hardware products are designed to make FPGA and Software application design easy and integration into existing systems straightforward – reducing risk, costs and time to market.

### FUSE Software

The BenADDA is fully compatible with Nallatech FUSE (Field Upgradeable Systems Environment) Software, supplied with Nallatech motherboards. The plug'n'play FUSE Software facilitates flexible and scaleable functionality for the control and configuration of FPGAs on modules and motherboards and allows data to be transferred between the motherboard and Host PC, hence allowing data transfer to and from designs running in on-board FPGAs. FUSE provides a number of interfaces, including the scripting language DIMEscript, a GUI application and the FUSE development APIs for C/C++, with optional APIs also available for Java and MATLAB.

### Key Features

At the heart of the BenADDA is the on-board Xilinx® Virtex™-II FPGA, which provides a powerful data processing resource. Various FPGA devices, ranging from XC2V250 up-to XC2V6000, with a choice of speed grades are available. The BenADDA also offers the option of on-board ZBT SRAM memory, using 1MByte devices.

### Digital to Analogue Conversion

The BenADDA offers flexible, high-speed, high-resolution data conversion for both baseband and direct IF applications. Two Analog Devices AD9772A DACs are directly controlled by the on-board FPGA, allowing users maximum operating flexibility.

### Analogue to Digital Conversion

To complement the on-board DACs the BenADDA has two Analog Devices AD6644(5) ADCs. The sampled data can be processed directly by the on-board FPGA. The AD6644(5) is a high-speed, high-performance, monolithic 14-Bit analogue-to-digital converter.

### BenADDA




### BenADDA Product Highlights

- ✓ **On-board Xilinx Virtex-II FPGA**
- ✓ **Various FPGA device packages, sizes and speed grade options available**
- ✓ **Two independent analogue capture channels**
- ✓ **2x 14-Bit ADC Resolution, up to 105MSPS per channel sampling rate**
- ✓ **Two independent channels to extract analogue data**
- ✓ **2x 14-Bit DAC Resolution, 160MSPS per channel sampling rate**
- ✓ **Up-to 8MB of ZBT SRAM memory, in two independent banks.**
- ✓ **Nallatech ZBT SRAM interfacing IP Core available**
- ✓ **Multiple Clocking Options: Internal & External**
- ✓ **Example designs and source code included**

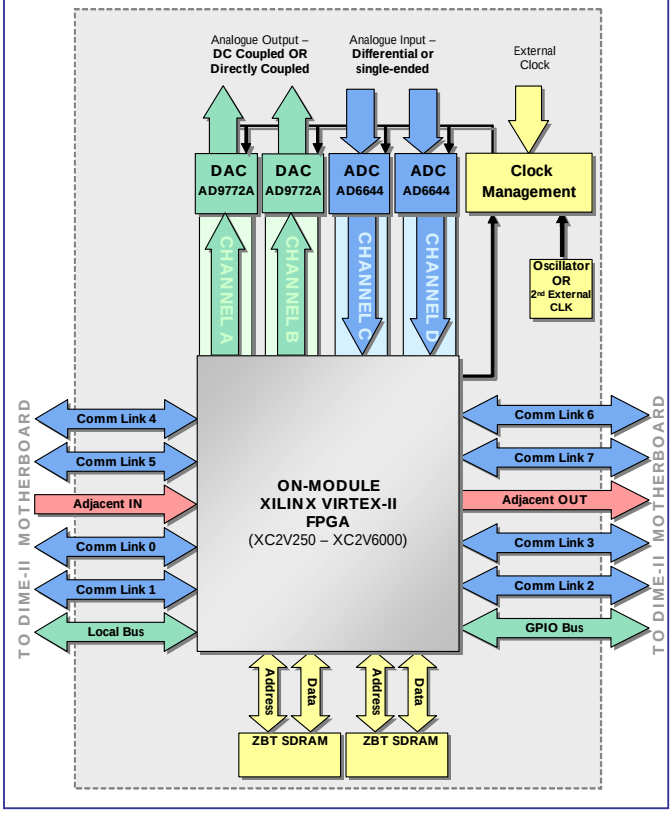
### Applications

Some examples of applications for the BenADDA are:

- **Mobile communications systems**
- **Infrared Imaging**
- **Wideband Cable Systems**
- **Multi-Channel, Multi-Mode Receivers**

# BenADDA™

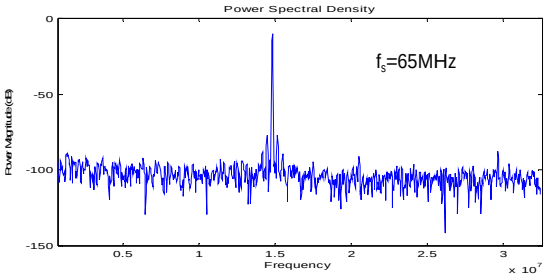
## BenADDA Functional Diagram




## BenADDA Signal and Noise Analysis

### ADC Performance

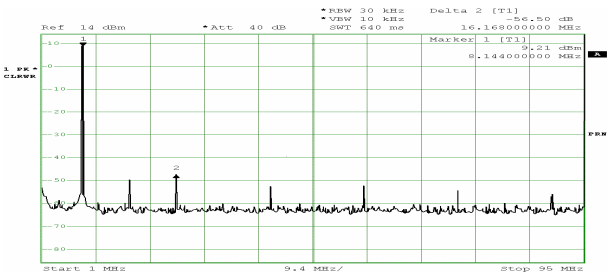
The Power Spectral Density for a $2V_{pp}$ sine wave at 14.8MHz.




ENOB: 11-12; SFDR=80dBc; SNR=71.3dB.

### DAC Performance

Image of an 8.1MHz signal with 10dBm amplitude sampled at 65MHz.



SFDR=56.5dBc; THD=-56dBc.

## BenADDA Specification

| Features | 2V250 | 2V1000 | 2V3000 | 2V6000 |
|---|---|---|---|---|
| ADC Up to 105MSPS (x2) | 14-Bit | 14-Bit | 14-Bit | 14-Bit |
| DAC 160MSPS (x2) | 14-Bit | 14-Bit | 14-Bit | 14-Bit |
| Total ZBT SRAM* | n/a | n/a | 4MB | 8MB |
| ZBT Memory Banks | n/a | n/a | 2 Banks | 2 Banks |
| On Board Programmable Clock s in User FPGA | 3 | 3 | 3 | 3 |
| No. of methods for Clocking ADCs/ DACs** | 7 | 7 | 7 | 7 |
| User FPGA Status LEDs | 2 | 2 | 2 | 2 |

*Figures quoted are in MBytes and is the total size of memory on-board.

**External Clock source available through front panel, 4 user programmable clocks from User FPGA (can be used as single-ended or differential), either use of on-board Oscillator OR 2nd external clock source (this is a special build option). A total of 6 clocking methods will be available on the module at any one time

## Order Codes

| Product | Order Code |
|---|---|
| BenADDA with XC2V250-4 FPGA | BenADDA-2V250-4-**xx** |
| BenADDA with XC2V1000-4 FPGA | BenADDA-2V1000-4-**xx** |
| BenADDA with XC2V3000-4 FPGA | BenADDA-2V3000-4-**xx** |
| BenADDA with XC2V6000-4 FPGA | BenADDA-2V6000-4-**xx** |

***xx: Select appropriate code for the following build options:***

| | |
|---|---|
| **01** | Op_Amp (DC) Coupled Outputs + Single-ended Analogue Inputs |
| **02** | Op_Amp (DC) Coupled Outputs + Differential Analogue Inputs |
| **03** | Directly Coupled Outputs + Single-ended ADC Inputs |
| **04** | Directly Coupled Outputs + Differential Analogue Inputs |

## DIME-II User I/O Bus Support

| Bus | 2V250 | 2V1000 | 2V3000 | 2V6000 |
|---|---|---|---|---|
| Adjacent Bus In | 16 bits | 26 bits | 64 bits | 64 bits |
| Adjacent Bus Out | 16 bits | 26 bits | 64 bits | 64 bits |
| Local Bus | 32 bits | 54 bits | 64 bits | 64 bits |
| Comm Links 0 & 2 | 12 bits | 12 bits | 12 bits | 12 bits |
| Comm Links 1 & 3 | n/a | n/a | 12 bits | 12 bits |
| Comm Links 4 & 6 | n/a | n/a | 12 bits | 12 bits |
| Comm Links 5 & 7 | n/a | n/a | 12 bits | 12 bits |
| GPIO Bus (21 bit) | n/a | n/a | 21 bits | 21 bits |

## Further Information

Contact Nallatech for further product information:


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