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Find the *Nallatech BenDATA-DD* at our website: *Click HERE*

NALLATECH

BenDATA-DD™

BenDATA-DD - Virtex-II™ DIME-II™ Module

BenDATA-DD - local deep memory takes the burden out of the PCI.

Overview

The BenDATA-DD is one of a range of memory modules available from Nallatech. The BenDATA-DD provides 1GByte of local memory storage on a single width DIME-II module. As part of the scalable DIME-II family, the BenDATA-DD can be easily integrated into systems, through the range of available DIME-II motherboards and associated software/firmware.

DIME-II

Building upon the global success of the award-winning DIME standard, the DIME-II modular systems platform with TeraOPS performance enables users to harness the full capability of advanced FPGAs. DIME-II brings together unparalleled off-module I/O, flexible FPGA device support and exceptional bandwidth capabilities for next-generation systems design.

The scaleable DIME-II family of products includes DIME-II motherboards, modules, firmware and software, providing a complete systems solution. The firmware and software associated with the DIME-II hardware products are designed to make FPGA and Software application design easy and integration into existing systems straightforward – reducing risk, costs and time to market.

FUSE Software

The BenDATA-DD is fully compatible with Nallatech FUSE (Field Upgradeable Systems Environment) Software, supplied with Nallatech motherboards. The plug'n'play FUSE Software facilitates flexible and scaleable functionality for the control and configuration of FPGAs on modules and motherboards and allows data to be transferred between the motherboard and Host PC, hence allowing data transfer to and from designs running in on-board FPGAs. FUSE provides a number of interfaces, including the scripting language DIMEscript, a GUI application and the FUSE development APIs for C/C++, with optional APIs also available for Java and Matlab.

Key Features

The BenDATA-DD module is offered with a range of Virtex-II devices. On board data storage is achieved in the form of 4 banks of high-speed memory utilising DDR SDRAM technology. The module also comes with user definable LEDs.

Main Feature

The four banks of independently selectable DDR memory allow large amounts of real-time data to be stored quickly in a local environment that is independent of the PCI bus. Once stored, the data can be read out through the PCI bus to the user host. For example, DIME-II enables users to couple tightly 4 BenDATA-DD modules on a CPCI card such as the BenERA, which would provide 4GBytes of memory on a single card. With FUSE™ this can be expanded to multiple memory cards.

BenDATA-DD



BenDATA-DD Product Highlights

- ✓ **On-board Xilinx Virtex-II FPGA**
- ✓ **Can be ordered with Xilinx device 2V3000, 2V6000 or 2V8000 populated**
- ✓ **Single Width DIME-II Module (56.5 x 98mm)**
- ✓ **1GByte of DDR-SDRAM, in four independent banks**
- ✓ **DDR Data Rate:**
  - o **Either 200MHz or 266MHz**
- ✓ **Tricolour LEDs for FPGA Design Status**
- ✓ **On-board Temperature Sensor**
- ✓ **Optimum Bandwidth of 4.2Gbytes/sec.**
- ✓ **Nallatech DDR SDRAM interfacing IP Core**

Applications

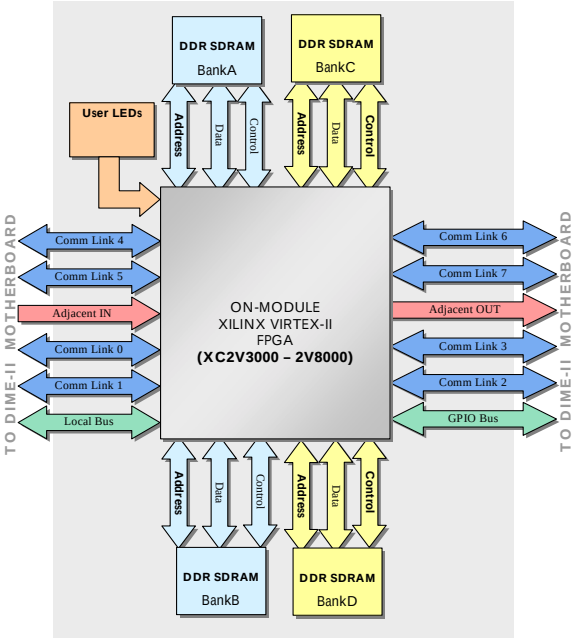
Some examples of applications for the BenDATA-DD are:

- **Fast local memory storage**
- **Data Capture**
- **Computationally intensive algorithms**
  - o **Image processing**
  - o **CFD**

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BenDATA-DD™

BenDATA-DD Functional Diagram



BenDATA-DD Specification

Features	2V3000	2V6000	2V8000
No. of Independent banks of DDR SDRAM	4	4	4
Data Bus width per Bank	32-Bit	32-Bit	32-Bit
Total DDR SDRAM	1GB	1GB	1GB
DDR Clock Speed[1]	133MHz	133MHz	133MHz
DDR Data Rate	266MHz	266MHz	266MHz
On Board Programmable Clock s in User FPGA	3	3	3
User FPGA Status LEDs	2	4	4

[1] Customers who wish to operate the DDR memory at a clock rate of 133MHz must order the Virtex-II FPGA with a -5 or greater speed grade. *See Order Codes for details.*

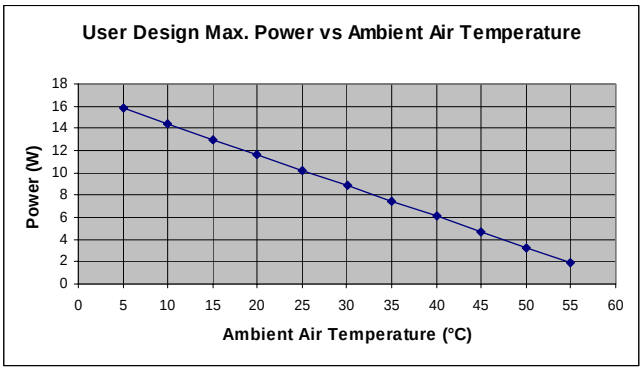
NOTE: MB = Mega-Bytes, GB = Giga-Bytes and Mb = Mega-bits.

DIME-II User I/O Bus Support

Bus	2V3000 (FF1152)	2V6000 (FF1152)	2V8000 (FF1152)
Adjacent Bus In	64 bits	64 bits	64 bits
Adjacent Bus Out	64 bits	64 bits	64 bits
Local Bus	64 bits	64 bits	64 bits
Comm Links 0 & 2	✓	✓	✓
Comm Links 1 & 3	✓	✓	✓
Comm Links 4 & 6	✓	✓	✓
Comm Links 5 & 7	✓	✓	✓
GPIO Bus (21 bit)	✓	✓	✓

BenDATA-DD – Thermal Information

The BenDATA-DD is supplied with a heatsink that exceeds PCI specification R2.2 by 12.5mm. This is designed to improve the thermal characteristics of the BenDATA-DD so that reasonable-sized user designs can be implemented. A BenDATA-DD mounted on a Nallatech PCI motherboard, such as the BenERA compactPCI, infringes into the adjacent PCI slots. The BenERA is intended to be a double width (8HP) card, however the BenDATA-DD heatsink exceeds the height limit for a double width card by 11mm, which means a BenERA loaded with one or more BenDATA-DD modules becomes a 12HP wide card taking up 3 slots of the cPCI backplane (1 behind and 2 in front of the card).



Each bank of DDR memory on the BenDATA-DD requires a DDR IP core (supplied) to function correctly. If the user implements all 4 banks of DDR memory this uses 30% of a 2V3000 FPGA resource and the power required to run all 4 cores at 133MHz (266MHz data rate) is 6.42 Watts. The above graph shows the amount of power remaining for the user designs at a given ambient air temperature before the maximum junction temperature of the FPGA is exceeded. Tools such as the power estimator from Xilinx can be used to calculate the power required for a design. If your solution requires high density designs, the infringement of either PCI or cPCI specification is a concern or you wish to use the BenDATA-DD in a PC/104*plus* system solution please contact Nallatech, as customer-specific heatsink alternatives can be offered.

Order Codes

Product Description	Order Code
BenDATA-DD with 4x Banks of DDR memory running at 100MHz (FPGA set to -4 speed grade or higher)	BenDATA-DD-2V####-*-03
BenDATA-DD with 4x Banks of DDR memory running at 133MHz (FPGA set to -5 or higher speed grade)	BenDATA-DD-2V####-*-04

Where #### represents the FPGA size. i.e. 3000, 6000 or 8000 and * represents the speed grade.

E.g. To order a DDR Core operating at CLK speed of 133MHz, with a XC2V6000 Virtex-II and speed grade -5, the code would be:

Example Code: BenDATA-DD-2V6000-5-02

Further Information

Contact Nallatech for further product information:

Email contact@nallatech.com

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