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BenDATA-DD
Reference Guide

NT107-0169 - Issue 5

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24/10/2003	4	Update to oscillator clock frequency notice
30/01/2004	5	Update to section 1.4.1 "Fitting to a BenNUEY-PCI motherboard". New picture added to show correct jumper configuration.

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About this Reference Guide

This Reference Guide provides detailed information on using the BenDATA-DD DIME-II module. It is designed to provide information that allows you to become acquainted with the module and the functionality it provides.

Symbols Used

Throughout this Guide there are symbols to draw attention to important information:

▼ **The red arrow symbol indicates a set of procedures to follow, such as installing software or setting up hardware.**



The blue 'i' symbol indicates useful or important information.



The red '!' symbol indicates a warning, which requires special attention.

Reference Guide Format

The Reference Guide is divided into **Sections**, which are grouped into **Parts**. The parts divide the document as follows:

- Introduction: Provides a brief introduction to the Reference Guide and the BenDATA-DD module.
- Reference Information: Provides information on all aspects of the module.

Related Documentation

- Infineon — DDR SDRAM Datasheet (512 Mb)
- Nallatech — DIMEscript User Guide
- Nallatech — DIME-II Installation Guide
- Nallatech — DDR SDRAM Controller Core Datasheet
- Nallatech — FUSE C-C++ API Developers Guide

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- Nallatech FUSE System Software User Guide

Abbreviations

- **API:** Application Programming Interface
- **DDR:** Double Data Rate
- **DIME:** DSP and Image Processing Modules for Enhanced FPGAs
- **FPGA:** Field Programmable Gate Array
- **GUI:** Graphical User Interface
- **MDF:** Module Definition File
- **PCI:** Peripheral Component Interconnect
- **PnP:** Plug and Play
- **RAM:** Random Access Memory
- **SRAM:** Synchronous Random Access Memory

FUSE Naming Conventions

Please note that the DIME-II clocks are named differently in the FUSE System Software compared to this Reference Guide. The clock naming conventions are shown in Table 1 on page viii.

Clock Names in FUSE	Clock Names in Documentation
System Clock (SYSCLK)	Clock A (CLK A)
DSP Clock (DSPCLK)	Clock B (CLK B)
Pixel Clock (PIXCLK)	Clock C (CLK C)

Table 1: FUSE naming conventions

For more information please see “DIME-II System Clocks” on page 35.

Comments and Suggestions

At the back of this Reference Guide, you will find a remarks form. We welcome any comments you may have on our product or its documentation. Your remarks will be examined thoroughly and taken into account for future versions of Nallatech products.

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Part I:Introduction

This part of the Reference Guide provides an introduction to the BenDATA-DD and outlines its key features and functionality.

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Section 1

BenDATA-DD Overview

In this section:

- BenDATA-DD key features
- BenDATA-DD specification
- BenDATA-DD SDRAM Controller Core
- Clock frequency notice
- BenDATA-DD functional diagram
- FUSE overview



For BenDATA-DD installation instructions please refer to your copy of the **DIME-II Installation Guide** supplied with the module. It is also available on the BenDATA-DD CD in the following directory: '<CDROM Drive>:\Documentation\Product\. This manual covers all installation procedures for the BenDATA-DD including hardware installation, FUSE software installation and an introduction to the key components of Nallatech systems and solutions.



This Reference Guide refers to the 1 GByte DDR SDRAM version of the BenDATA-DD. This is populated with 512 Mbit DDR SDRAM chips. A 0.5 GByte DDR SDRAM version of the BenDATA-DD was shipped on limited release prior to September 2003. This version is populated with 256 Mbit DDR SDRAM chips. Some of the information in this Reference Guide does not apply to the 0.5 Gbyte version of the BenDATA-DD - users of this version should refer to the Errata Sheet available from Nallatech. Please contact Nallatech support (support@nallatech.com) if you have any queries regarding this matter.

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1.1 BenDATA-DD Key Features

The BenDATA-DD provides 1GByte of local memory storage on a single width DIME-II module. The module is designed for storing large amounts of data which can be rapidly accessed by other DIME-II modules on the carrier motherboard. Example application areas for the BenDATA-DD include fast local memory storage, data capture and computationally intensive algorithms.

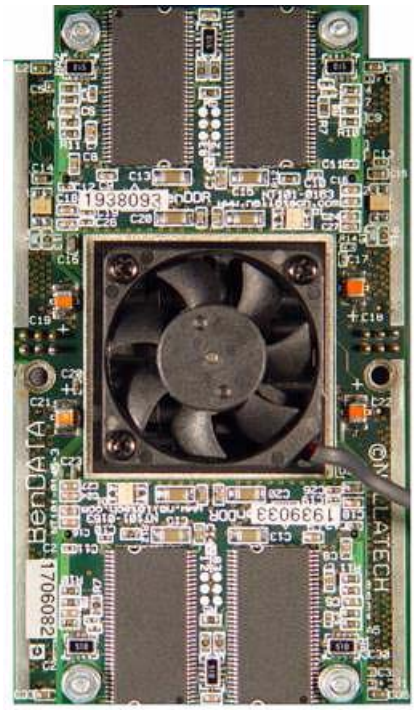


Figure 1: BenDATA-DD

The key features of the BenDATA-DD include:

- On-board Xilinx Virtex-II FPGA
- Single width DIME-II module
- 1GByte of DDR-SDRAM in four independent banks
- Tricolor LEDs for FPGA design status
- Optimum bandwidth of 4GBytes/sec
- On-board temperature sensor
- Nallatech DDR SDRAM interfacing IP Core

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1.2 BenDATA-DD Specification

The BenDATA-DD is available in the following specification:

Features	2V3000 FF1152	2V6000 FF1152	2V8000 FF1152
Total DDR SDRAM*	1GByte	1GByte	1GByte
DDR Memory Banks	4	4	4
DDR data bus per bank	32	32	32
On Board Programmable Clocks in User FPGA	3	3	3
User FPGA status LEDs	2	4	4

Table 2: BenDATA-DD specification

*Based on populating 512 Mbit DDR chips.

1.3 DDR SDRAM Controller Core

The BenDATA-DD is supplied with a DDR SDRAM Controller Core to simplify FPGA application design for system developers. This abstracts the complexities of interfacing from the developer and provides a simple user interface. The core is designed specifically for use with the BenDATA-DD and is available in two versions - one for DDR200 and the other for DDR266. A datasheet for the core is provided on the BenDATA-DD CD in the following directory: '<CDROM Drive>:\Documentation\Product\.

1.4 Oscillator Clock Frequency Notice

The BenDATA-DD is supplied with either a 100MHz (DDR200) **OR** 133MHz (DDR266) oscillator depending on the speed grade of the Virtex-II FPGA. The DDR SDRAM Controller Core supplied with the BenDATA-DD uses CLKC from the carrying DIME-II motherboard, and requires this oscillator to be fitted to the motherboard. There are three options for this oscillator:

1. If you order the BenDATA-DD with a DIME-II motherboard, the oscillator is pre-fitted to the motherboard with appropriate jumpers pre-set.

2. If you order the BenDATA-DD independent of a DIME-II motherboard (with the exception of the BenERA), the oscillator is sent unfitted with the BenDATA-DD. See “Fitting the Oscillator” on page 6 for details of populating the oscillator on a DIME-II motherboard.

3. If you order the BenDATA-DD independent of a DIME-II motherboard and wish to use it on a **BenERA** purchased prior to September 2003, please contact support@nallatech.com for further information. Please include your existing BenERA serial number(s) in your E-mail and reference this page of the BenDATA-DD manual.

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1.4.1 Fitting the Oscillator

When installing your BenDATA-DD on a DIME-II motherboard you will also need to populate the supplied oscillator. Please refer to your motherboard type within this section for details of fitting the oscillator.

When fitting the oscillator special attention must be paid to the orientation of the pins. Figure 2 on page 6 shows the marking to indicate Pin1 of the oscillator.

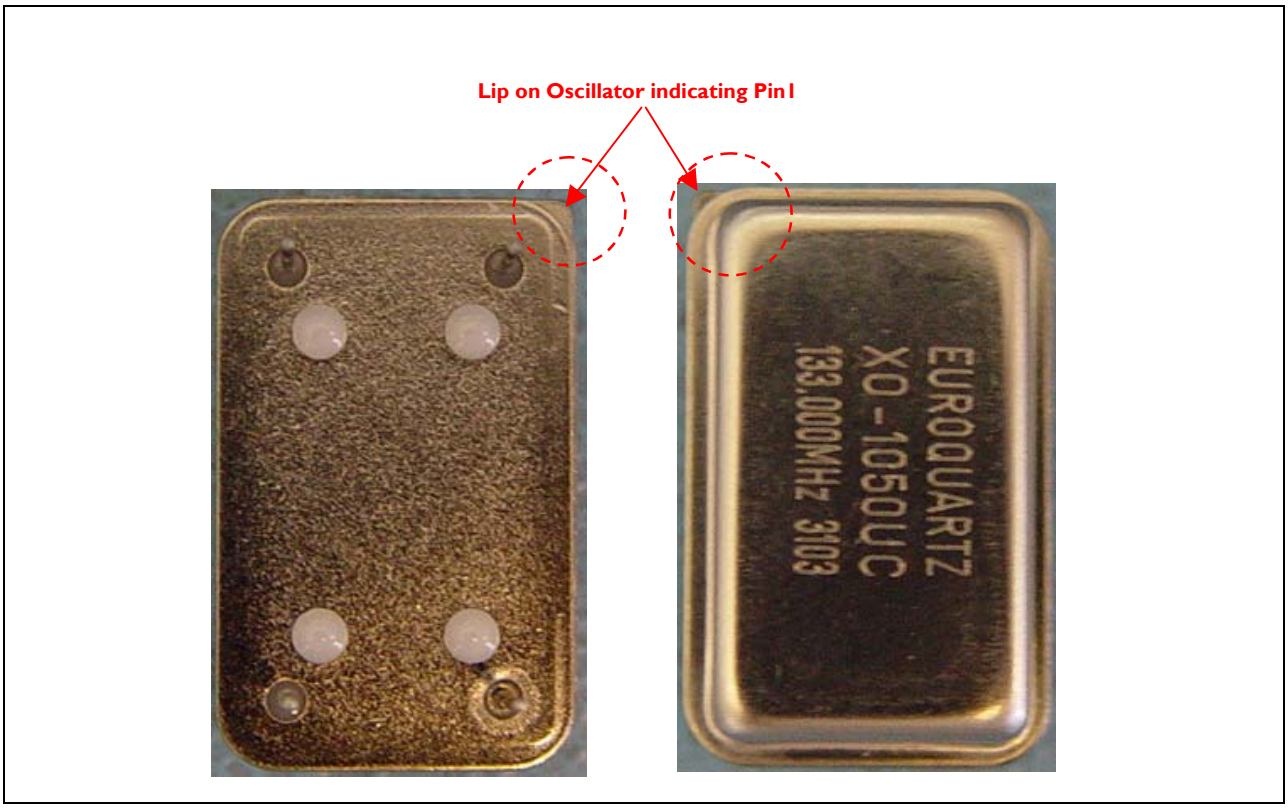


Figure 2: Pin 1 Location

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Fitting to a BenONE-PCI motherboard

Fit the oscillator into the oscillator sockets on the BenONE-PCI motherboard as shown in Figure 3 on page 7.

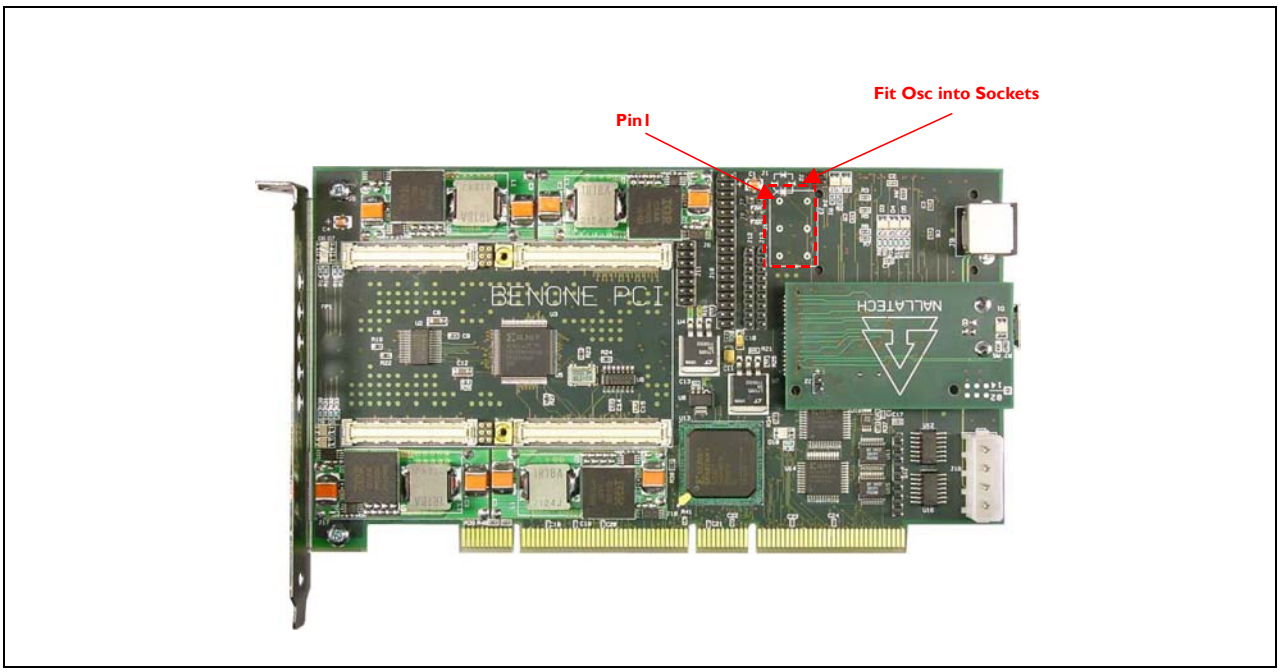


Figure 3: Fitting Oscillator to BenONE-PCI

Fitting to a BenNUEY-PCI motherboard

On the BenNUEY-PCI motherboard the oscillator should be fitted to the socket on the PCB AND the jumper settings must be modified so that CLKC is driven by the fixed oscillator. The jumpers should be set to:

- J13 - Jumper pins 2-to-4
- J12 - Jumper pins 1-to-2

Figure 4 on page 7 shows the location of the jumpers and the space for the oscillator on the BenNUEY. Note that the jumpers shown in Figure 4 are standard settings and should be changed as outlined above.

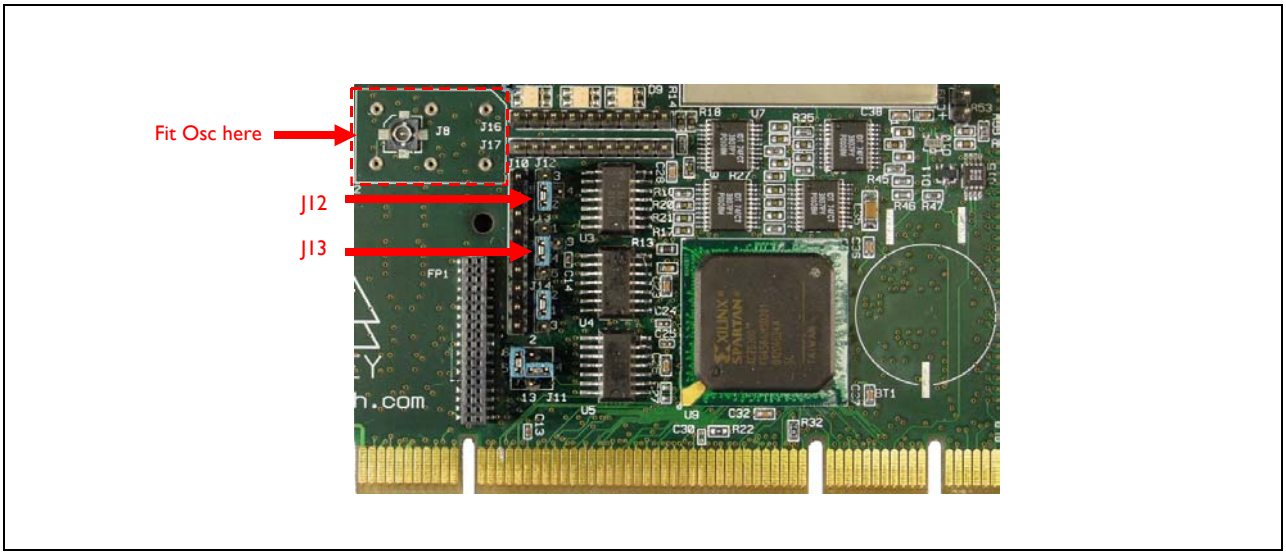


Figure 4: Fitting Oscillator to BenNUEY-PCI

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Fitting to a BenNUEY-PC/104-*Plus* motherboard

On the BenNUEY-PC/104-*Plus* motherboard the Oscillator should be fitted to the sockets on the PCB AND the jumper settings must be modified so that CLKC is driven by the fixed oscillator. The jumpers should be set to:

- J3 - Jumper pins 2-to-4
- J2 - Jumper pins 1-to-2

Figure 5 on page 8 shows the location of the jumpers and the space for the oscillator on the BenNUEY-PC/104-*Plus*. Note that the jumpers shown in Figure 5 are standard settings and should be changed as outlined above.

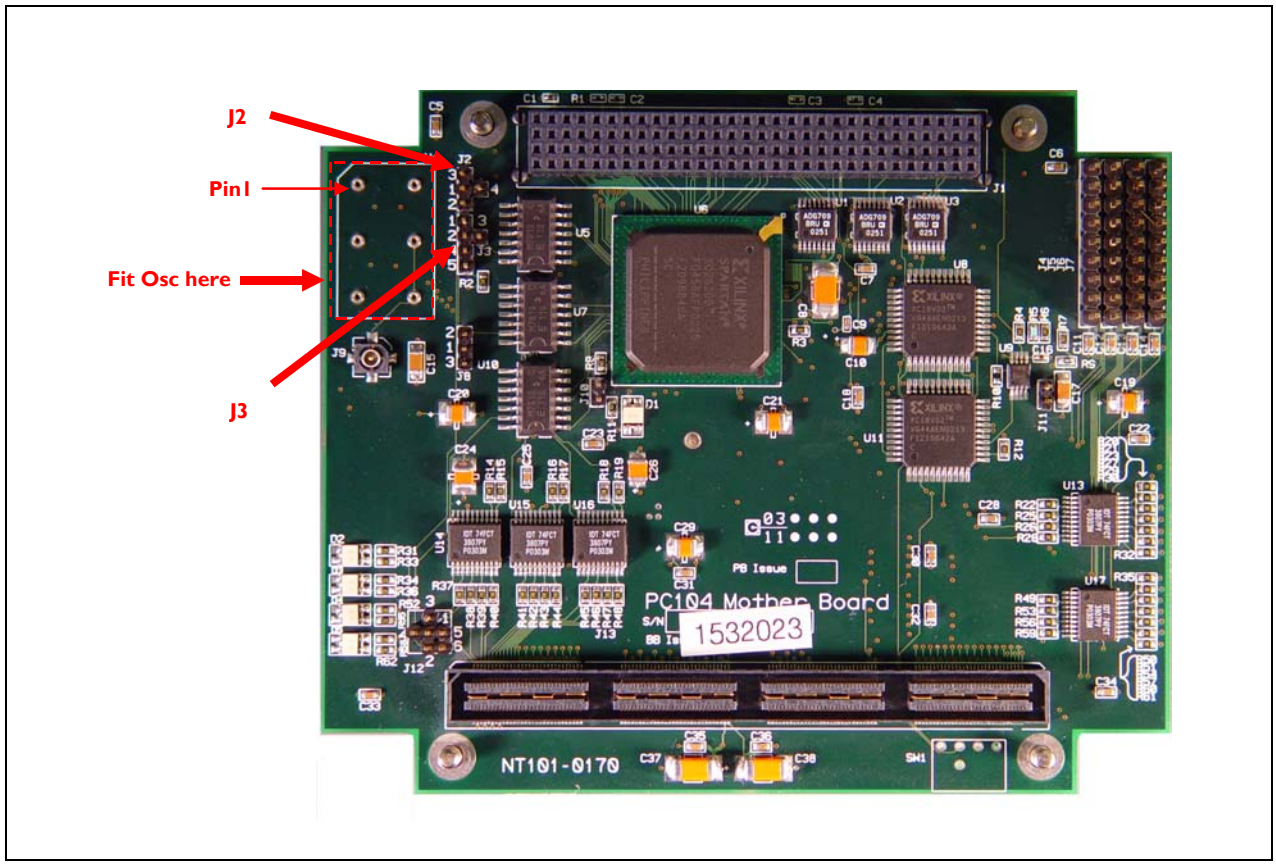


Figure 5: Fitting Oscillator to BenNUEY-PC/104-*Plus*

If your DIME-II motherboard is not shown here, please consult your Motherboard Reference Guide for details of fitting an oscillator and setting any jumpers for CLKC.

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1.4.2 Jumper Settings for the BenERA

Prior to using the BenDATA-DD on a BenERA purchased before September 2003, please read "Oscillator Clock Frequency Notice" on page 5 and contact Nallatech support as described.

When using the BenDATA-DD on a BenERA the jumper to drive CLKC from the fixed oscillator must be set. The jumpers should be set to:

- JR2 - Jumper pins 1 - 3

Figure 6 on page 9 shows the location of this jumper on the BenERA.

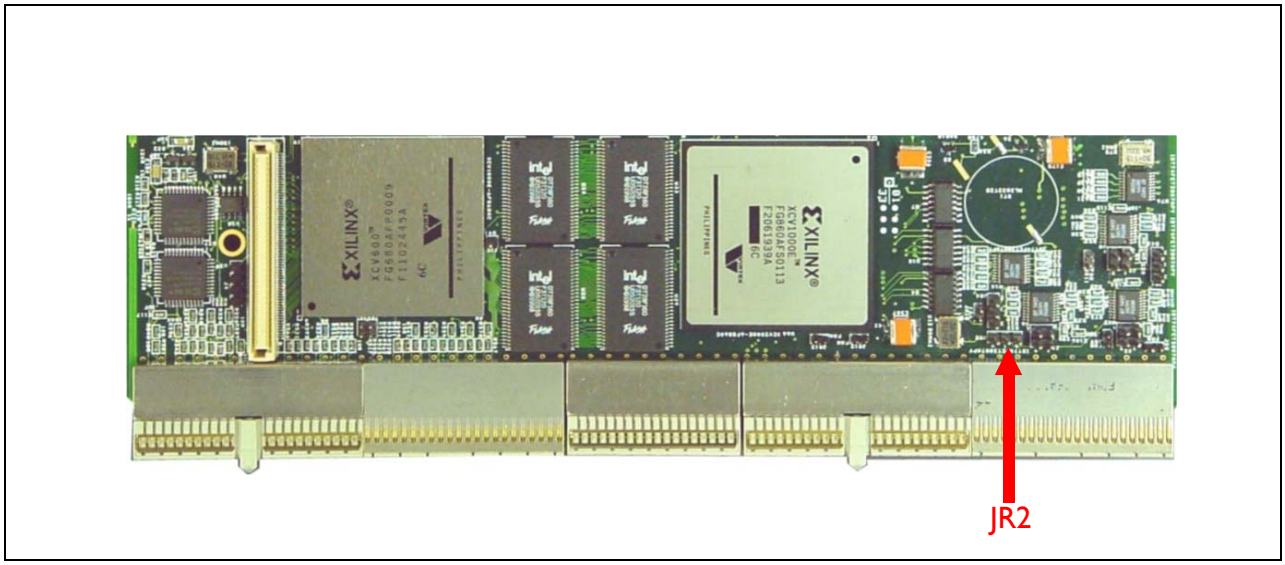


Figure 6: Jumper JR2, set 1-3, on BenERA.

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1.5 BenDATA-DD Functional Diagram

Figure 7 on page 10 shows the key functional features of the BenDATA-DD and the available user interconnections. The signals internal to the BenDATA-DD do not cross the boundary of the grey shaded region that represents the BenDATA-DD domain.

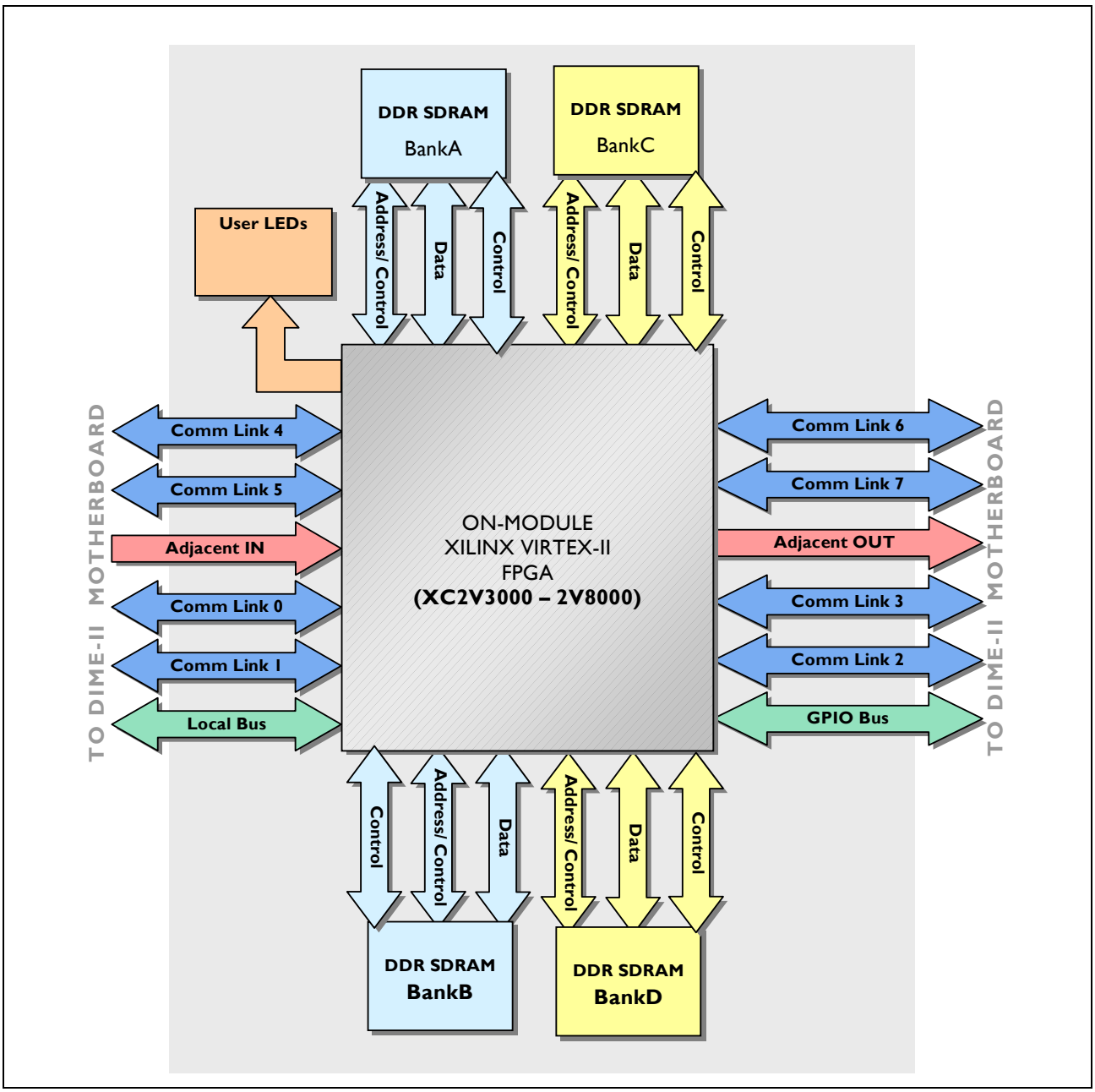


Figure 7: BenDATA-DD functional diagram

For more information on:

- the on-board Xilinx Virtex-II FPGA, please see “User FPGA” on page 34.
- the Adjacent IN and OUT, Local and GPIO busses see “DIME-II Communication Busses” on page 35.
- LEDs, see “User LEDs” on page 38.
- DDR SDRAM memory banks, see “DDR SDRAM Memory” on page 32.

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- Comm Links 0-7, see "DIME-II Communication Busses" on page 35.

1.6 FUSE Overview

This section provides an overview of the FUSE system software and how it relates to the BenDATA-DD.

1.6.1 DIME and DIME-II

DIME is a modular standard developed specifically for Field Programmable Gate Arrays (FPGAs) which allows design engineers to develop re-programmable systems with the opportunity to alter or experiment with the partitioning of their designs at any stage of the design cycle. DIME-II has been introduced in response to increasing bandwidth and performance requirements.

1.6.2 FUSE

FUSE Reconfigurable Computer Operating System provides a high level interface to Nallatech products - in this case the BenDATA-DD. The FUSE interface, common across tools and underlying host operating systems, allows designers to configure the BenDATA-DD FPGA, and provides data transfer to and from designs running on this FPGA.

FUSE provides several interfaces for working with the BenDATA-DD, including the FUSE Probe Tool, the scripting language DIMEscript and Nallatech's reconfigurable computing network system, DIMEtalk. Also available are the FUSE development APIs for C/C++, with optional APIs available for Java and MATLAB.

- For more information on using the FUSE software and the FUSE APIs please see the **FUSE System Software User Guide** and the **FUSE C-C++ API Developer's Guide** respectively. Both are supplied on the FUSE CD in the following directory '<CDROM Drive>:\Documentation\FUSE\'.

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1.7 Confidence Tests

1.7.1 BenDATA-DD Confidence Test 1

Once the BenDATA-DD module has been installed (see **DIME-II Installation Guide** on the BenDATA-DD CD for full installation instructions) you should carry out the following confidence tests to ensure the on-board FPGA and memory devices on the BenDATA-DD are functioning correctly.

This confidence test shows the BenDATA-DD populated on a BenONE-PCI DIME-II motherboard, however the tests can be carried out on most BenDATA-DD - DIME-II motherboard combinations.

To configure the LED Confidence Test use the following procedures:

1. On the Windows task bar, click:

   Start -> Programs -> FUSE -> Software -> FUSE Probe

2. In the FUSE Probe Tool window shown in Figure 8 on page 12, select **Card Control\Open card** from the menu at the top of the window.

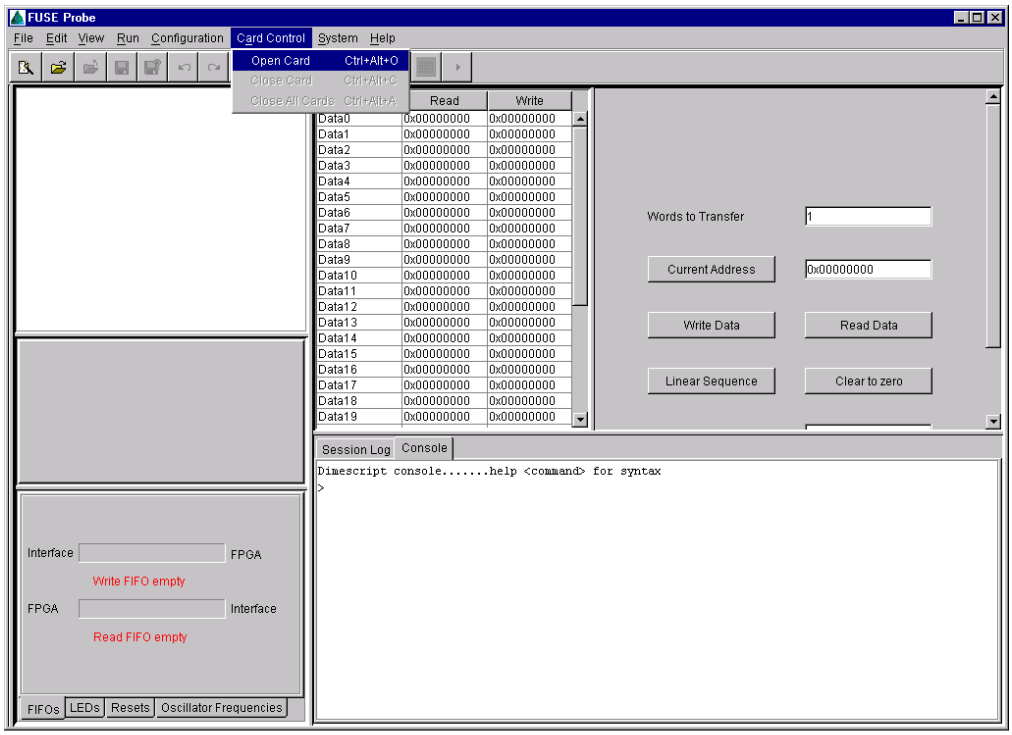


Figure 8: FUSE Probe Tool

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3. The Locate Card window is then displayed as shown in Figure 9 on page 13. Select **PCI** in the Interface box, and **All Card Types** in the Card Type box. Then click on **Locate Cards.**

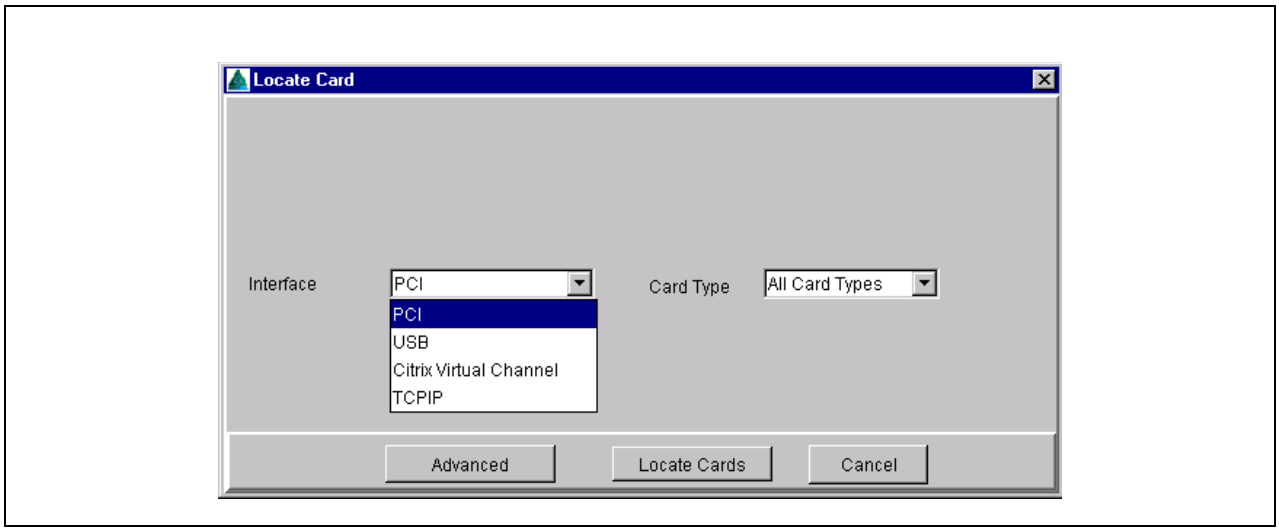


Figure 9: Dialogue box to locate cards

4. In the Selected Cards window shown in Figure 10 on page 13, check the card box and click on **Open Cards.**

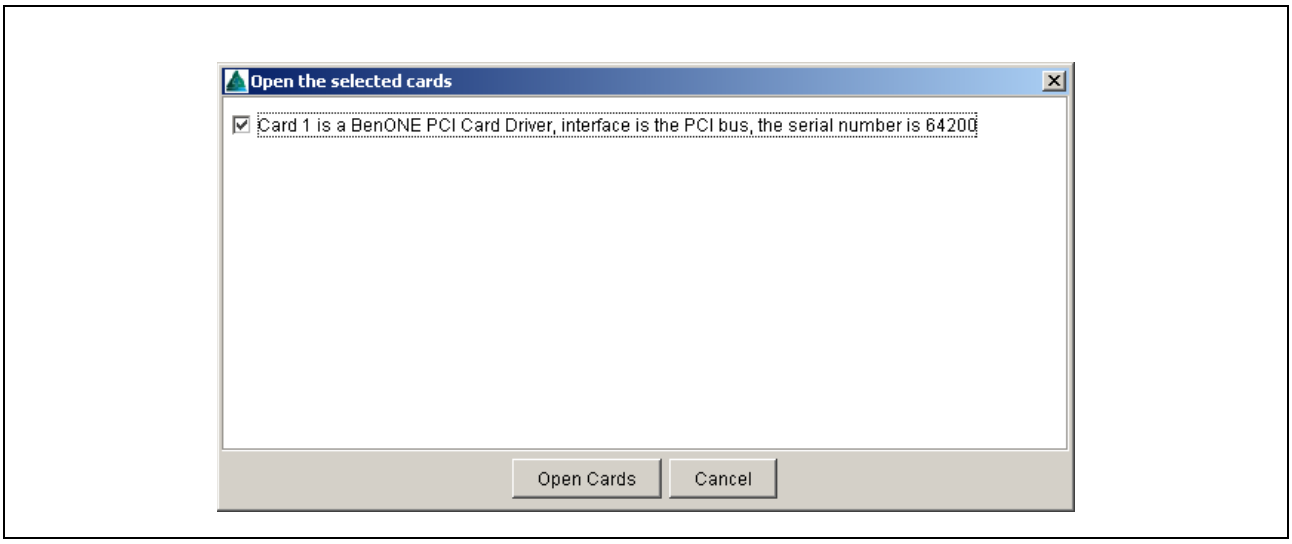


Figure 10: Dialogue box to open cards

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5. Under the 'BenONE' node, open the 'Nallatech BenDATA' node in the device tree, right-click 'Virtex2 2V#####', where ##### refers to the type of Virtex populated on the BenDATA-DD. From the menu which appears, select '**Assign and Configure**'.

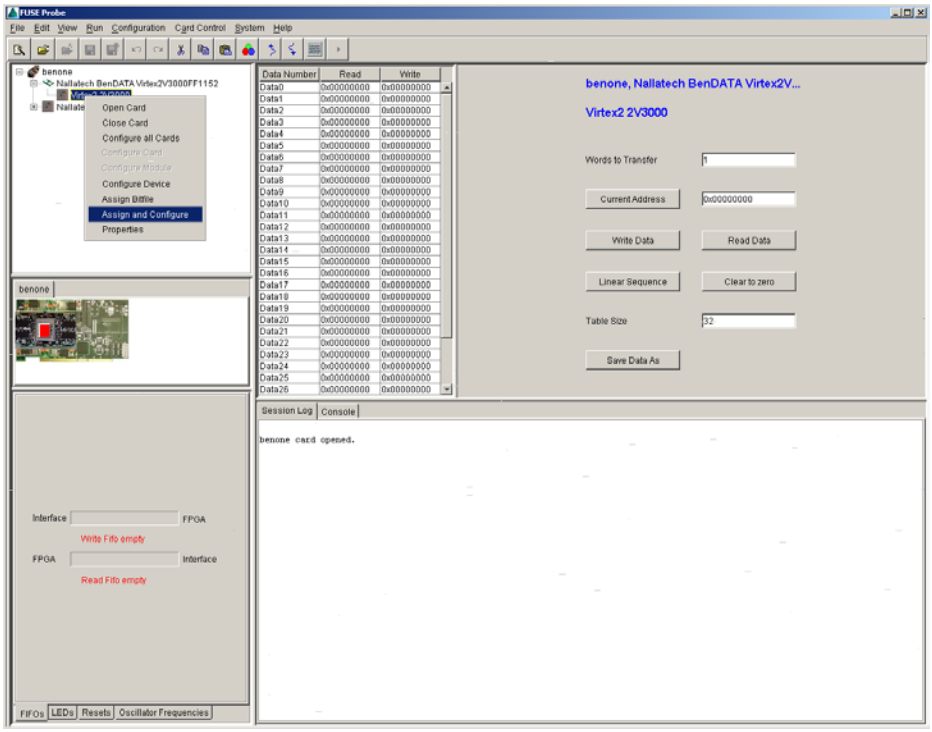


Figure 11: FUSE Probe Tool showing open card

6. A dialogue box is displayed which allows you to browse and select the correct bitfile for the device, as shown in Figure 12 on page 14. The bitfile for this device is named 'led_flash_benDATA_2V#####.bit' where ##### refers to the type of Virtex populated on the BenDATA-DD. The bitfile is located at the path '<CDROM Drive>:\Examples\LED FLASH\Bitfiles\' on the BenDATA-DD CD.

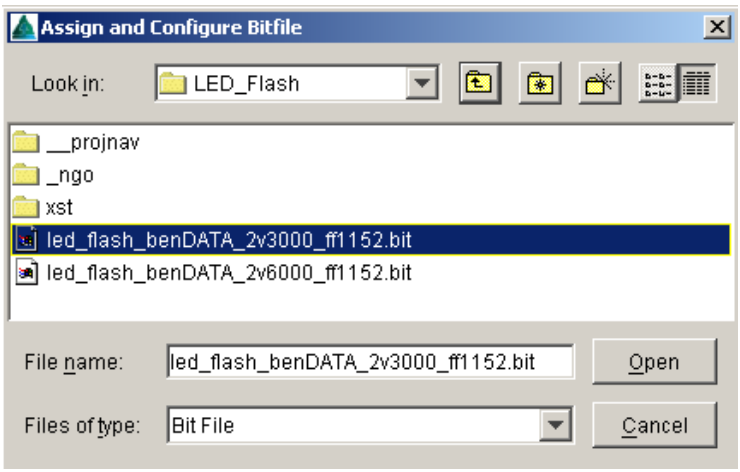


Figure 12: Assign Bitfile

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7. The LEDs highlighted in Figure 13 on page 15 should now go through a flashing sequence to indicate successful configuration.

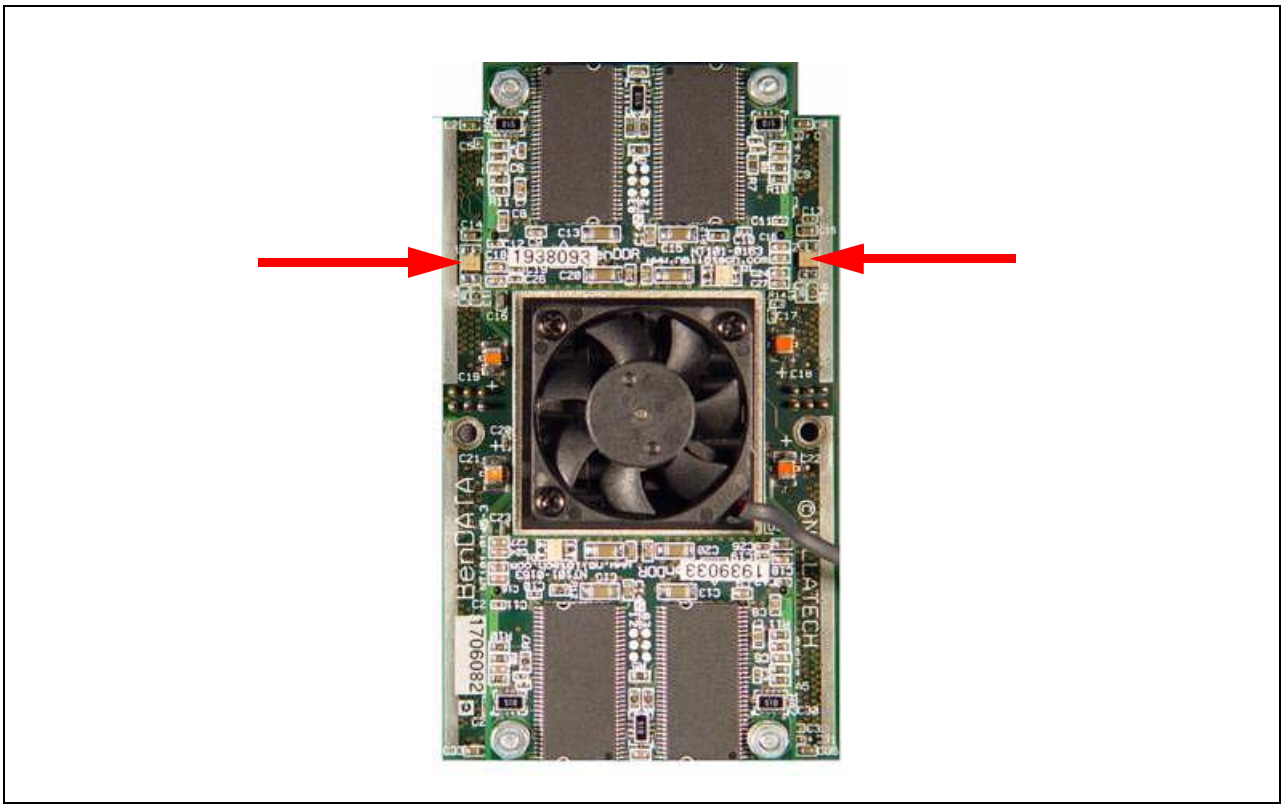


Figure 13: Confidence Test 1 LEDs

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8. The on-board FPGA has now been configured as shown in Figure 14 on page 16.

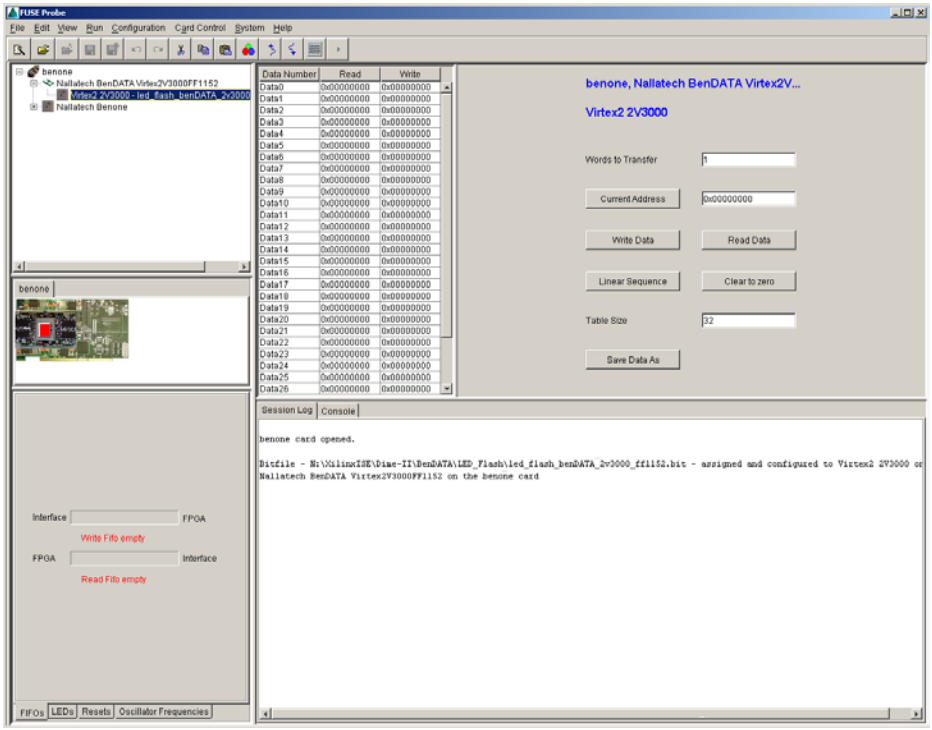


Figure 14: Device Configuration

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1.7.2 BenDATA-DD Confidence Test 2

This second Confidence Test is used to show that the BenDATA-DD's on-board memory devices are functioning correctly. The test is configured in the same way as the LED Confidence Test - if you have already opened the card for Confidence Test 1 please advance to step 5 to reconfigure the FPGA for Confidence Test 2, otherwise begin at step 1.

▼ **To configure the On-board Memory Test use the following procedures:**

1. On the Windows task bar, click:

   Start -> Programs -> FUSE -> Software -> FUSE Probe

2. In the FUSE Probe Tool window shown in Figure 8 on page 12, select **Card Control\Open card** from the menu at the top of the window.

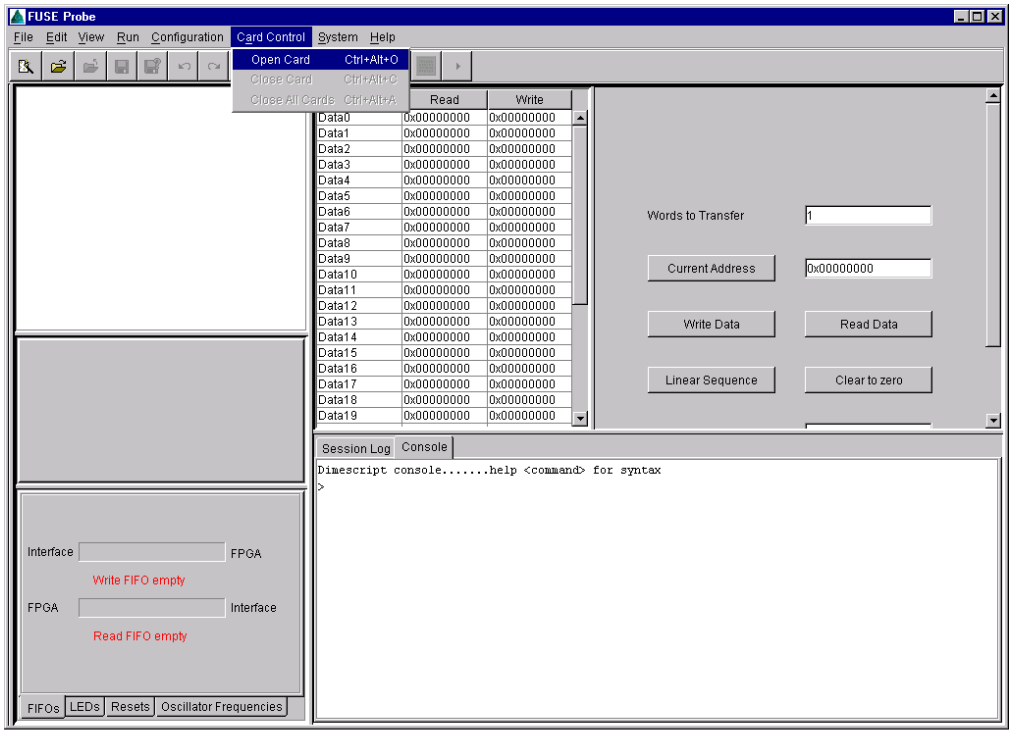


Figure 15: FUSE Probe Tool

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3. The Locate Card window is then displayed as shown in Figure 9 on page 13. Select **PCI** in the Interface box, and **All Card Types** in the Card Type box. Then click on **Locate Cards**.

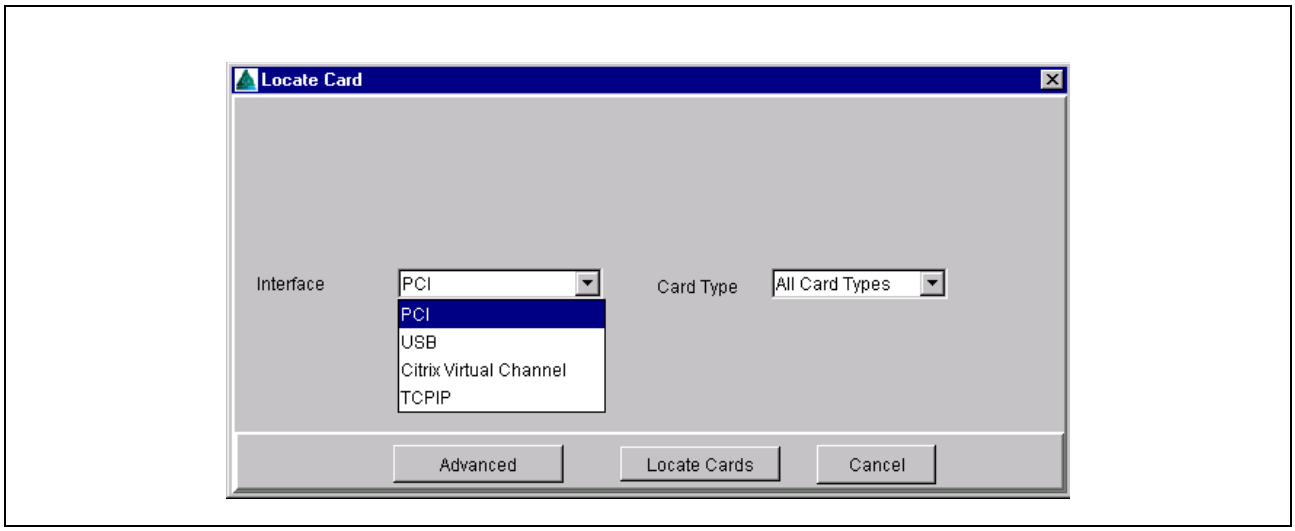


Figure 16: Dialogue box to locate cards

4. In the Selected Cards window shown in Figure 10 on page 13, check the card box and click on **Open Cards**.

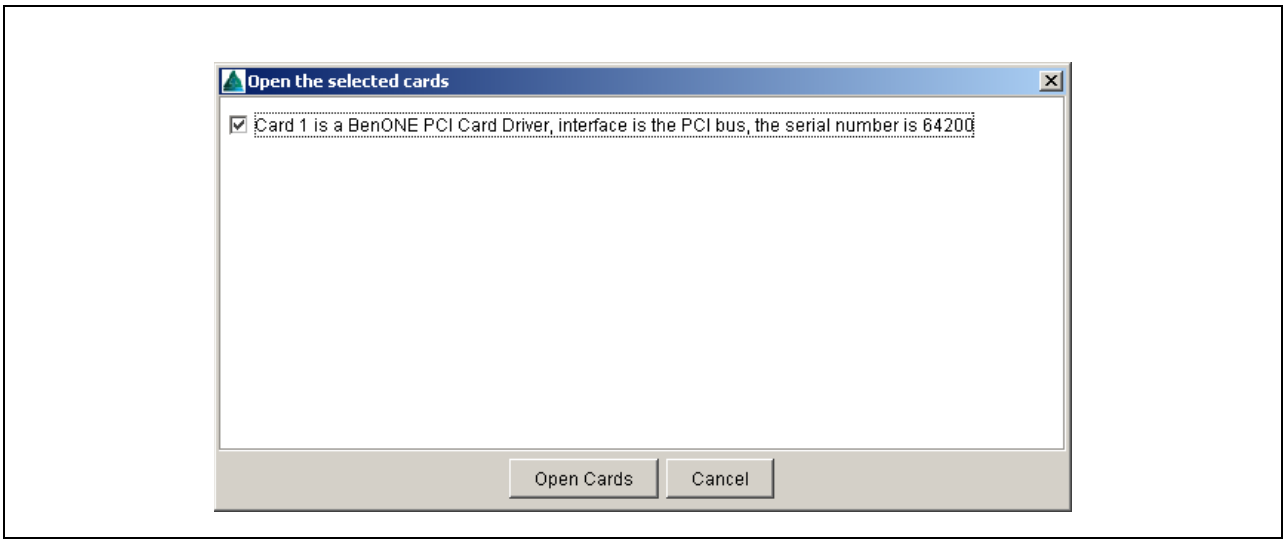


Figure 17: Dialogue box to open cards

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5. Under the 'BenONE' node, open the 'Nallatech BenDATA' node in the device tree, right-click 'Virtex2 2V#####', where ##### refers to the type of Virtex populated on the BenDATA-DD. From the menu which appears, select '**Assign and Configure**'.

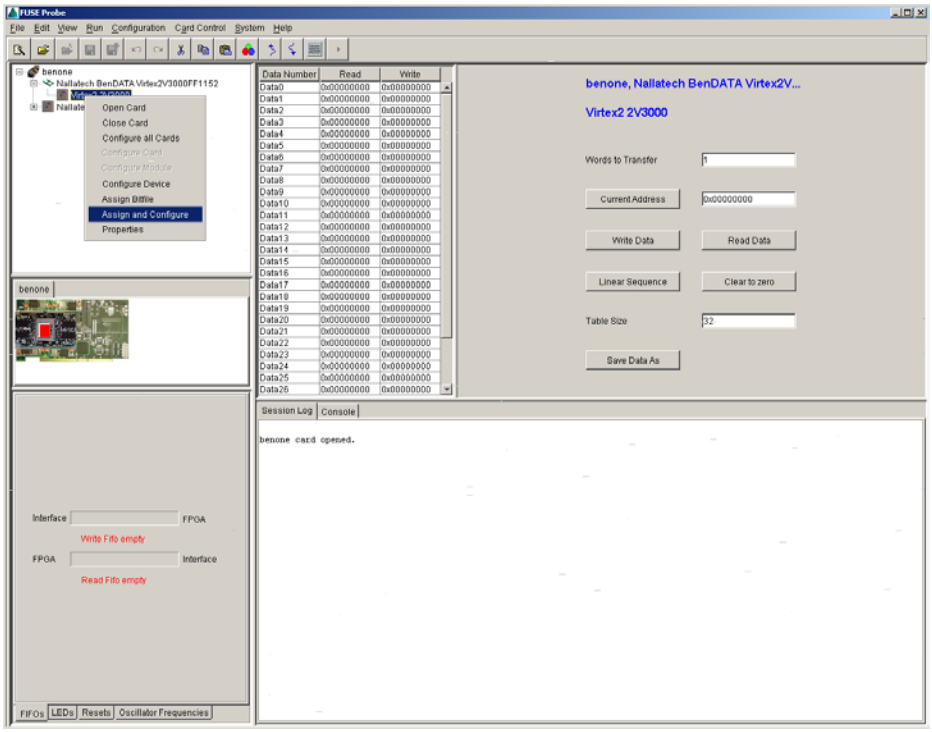


Figure 18: FUSE Probe Tool showing open card

6. A dialogue box is displayed which allows you to browse and select the correct bitfile for the device. The bitfile for this device is named 'memory_test_***MHz_benDATA_2V#####.bit', where *** refers to the speed of the populated oscillator on the carrier board and ##### refers to the type of Virtex populated on the BenDATA-DD. The bitfile is located at the path '<CDROM Drive>:\Examples\MEMORY TEST\Bitfiles\' on the BenDATA-DD CD.

7. In the bottom left hand pane of the FUSE Probe Tool window there are several tabs. On the 'Oscillator Frequencies' tab enter value '80000' in the DSPCLK field and hit 'return'.

8. Click on the 'Resets' tab, then check and uncheck the 'System Reset' box.

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Each LED on the BenDATA-DD represents a bank of memory - the 2 green LEDs represent the 2 on-board banks and the 2 red LEDs represent the 2 daughter boards, if present. After carrying out a reset the green LEDs flash to represent correct operation of the on-board banks, whilst the 2 red LEDs flash to indicate the correct operation of the daughter boards, if present. As the LEDs are tricolor, both the green and red diodes will flash simultaneously, combining to appear yellow. The location of the LEDs which flash to indicate a successful confidence test are shown in Figure 19 on page 20.

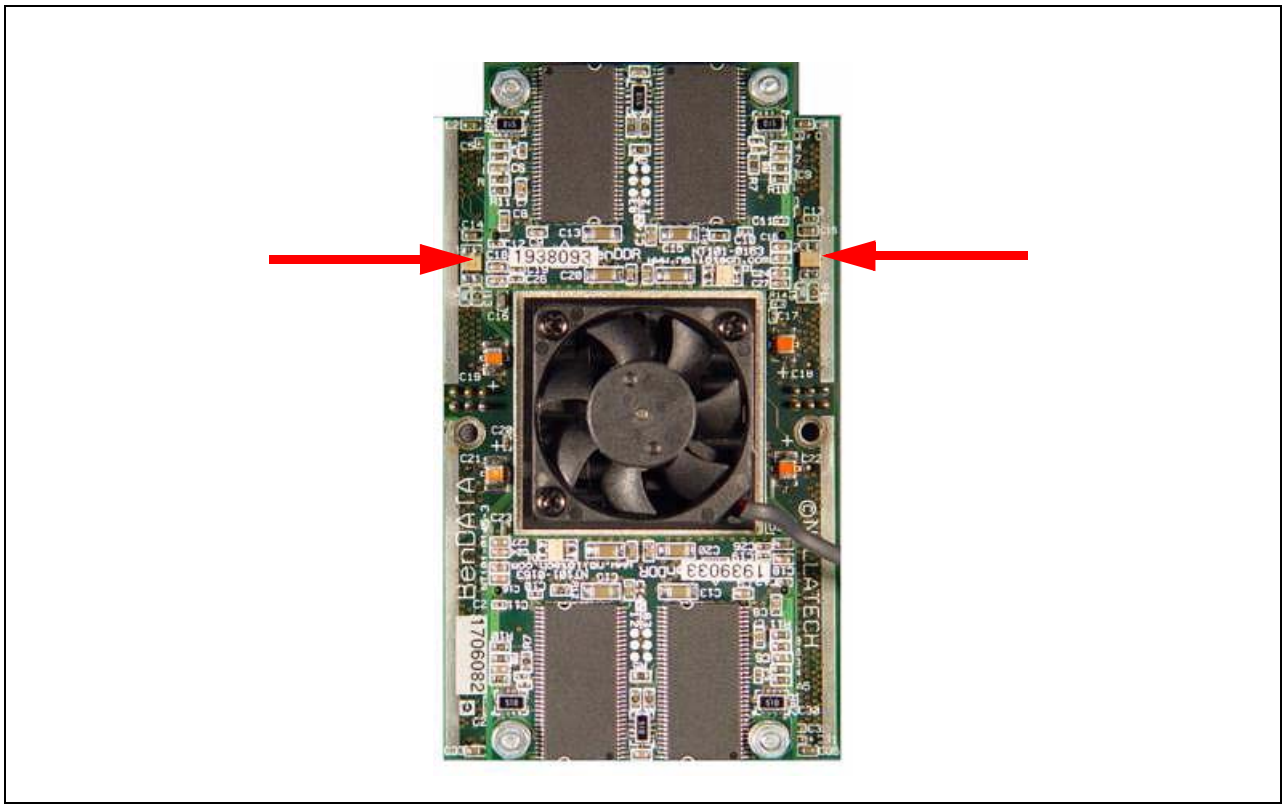


Figure 19: Confidence Test 2 LEDs

The design continuously carries out writes to and then reads from different memory locations within each bank. Assuming the data written continues to match the data that is read, the LEDs will continue to flash. If any LED goes out this indicates a mis-match between the written and read data within the bank represented by that LED.

1.8 FPGA Configuration

The User FPGA on the BenDATA-DD can be configured via the following methods:

- Using the FUSE Probe Tool
- Using DIMEscript
- Using FUSE Software APIs
- Xilinx JTAG download cable (refer to your motherboard Reference Guide for information on programming the FPGA using this method).

1.8.1 FPGA Configuration using FUSE

The FUSE Software provides the following functionality:

- Configuring the BenDATA-DD's FPGA
- Controlling reset signals

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- Controlling programmable clock frequencies
- Sending data to designs running in the User FPGA
- Reading data from designs running in the User FPGA
- Resetting PCI FIFOs.

This functionality is provided by the following tools:

- FUSE Probe tool
- DIMEscript
- FUSE Software development APIs.

FPGA Configuration using FUSE Probe Tool

The FUSE Probe tool is an easy to use software interface, which allows users to access a subset of the functionality provided by FUSE.

- Full instructions on how to use the Probe Tool are provided in the **FUSE System Software User Guide** on the supplied FUSE CD in the following directory '<CDROM Drive>:\Documentation\FUSE\'.

FPGA Configuration using DIMEscript

DIMEscript is a high-level scripting language, which provides users with a simple and easy to use language for the configuration and control of DIME systems. DIMEscript uses a simple command set, eliminating the need for developers to use complicated programming interfaces to control and communicate with application designs running in FPGAs. DIMEscript also offers platform portability through ASCII based scripts, allowing users to deploy DIMEscript on both Windows and Linux installations.

DIMEscript can be used either to write script files, which can then be executed as a single process, or it can be used from a command line interface, with the user executing commands as required.

- Full instructions on how to use DIMEscript are provided in the **DIMEscript User Guide** on the supplied FUSE CD in the following directory '<CDROM Drive>:\Documentation\FUSE\'.

FPGA Configuration using the FUSE APIs

The FUSE Software development API is a software development API, enabling users to call functions to control DIME hardware in their own programs. This allows users to develop software applications to complement the FPGA application designs running on DIME hardware. FUSE APIs are available to support a number of development languages, including C, C++, Matlab and Java.

- Full instructions on how to use the APIs are provided in the **FUSE C/C++ API Developers Guide** on the supplied FUSE CD in the following directory '<CDROM Drive>:\Documentation\FUSE\'.

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1.9 FPGA Application Design

1.9.1 Interfacing to the FPGA

It is assumed that most users will be familiar with the principles of FPGA design, or have appropriate resources/ support to complete FPGA designs. The following information is intended to detail any BenDATA-DD-specific issues in the design process.

A User Constraints File (UCF) for the user-accessible connections to the FPGA is provided with the BenDATA-DD, on the product CD. This allows you to quickly and easily link top-level HDL code to the FPGA I/O for implementation purposes.



Since the supplied UCF names are pre-defined, you can save development time by writing your top-level HDL code using the same port naming convention as the Nallatech UCF. This saves changing the UCF retrospectively to match your code.

There are a number of user-accessible interfaces from the User FPGA to other devices on the BenDATA-DD, which you can utilize for design purposes:

- User FPGA - DIME-II Signals
- User FPGA - DDR SDRAM Memory
- User FPGA - User LEDs

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1.9.2 Synthesis and Implementation Settings

This section details the synthesis and implementation settings, which should be used for the development of FPGA designs to run on Nallatech hardware. Developing FPGA designs to run on Nallatech hardware with on-board Xilinx FPGAs will ultimately require use of the Xilinx Implementation tools, to take the synthesized design to the hardware device. These tools are available in a variety of formats, including Alliance, Foundation and ISE.

When performing the implementation stage of the design process, some settings are mandatory and need to be specified for the design to configure and run on Nallatech hardware. These necessary settings are detailed below. Also detailed are some common additional settings for the implementation options. However, it should be stressed that the common settings are optional and you should select the most appropriate settings for your design.

Necessary Settings

1. Enable Readback and Reconfiguration
2. Select the JTAG Startup Clock (selected configuration clock)

See “File Generation Options” on page 26 for both these settings.

Common Settings

The rest of the settings are optional.

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Synthesis Options

When developing FPGA designs to run on Nallatech hardware, it is not necessary to select any specific settings for the synthesis of HDL code for FPGA designs.

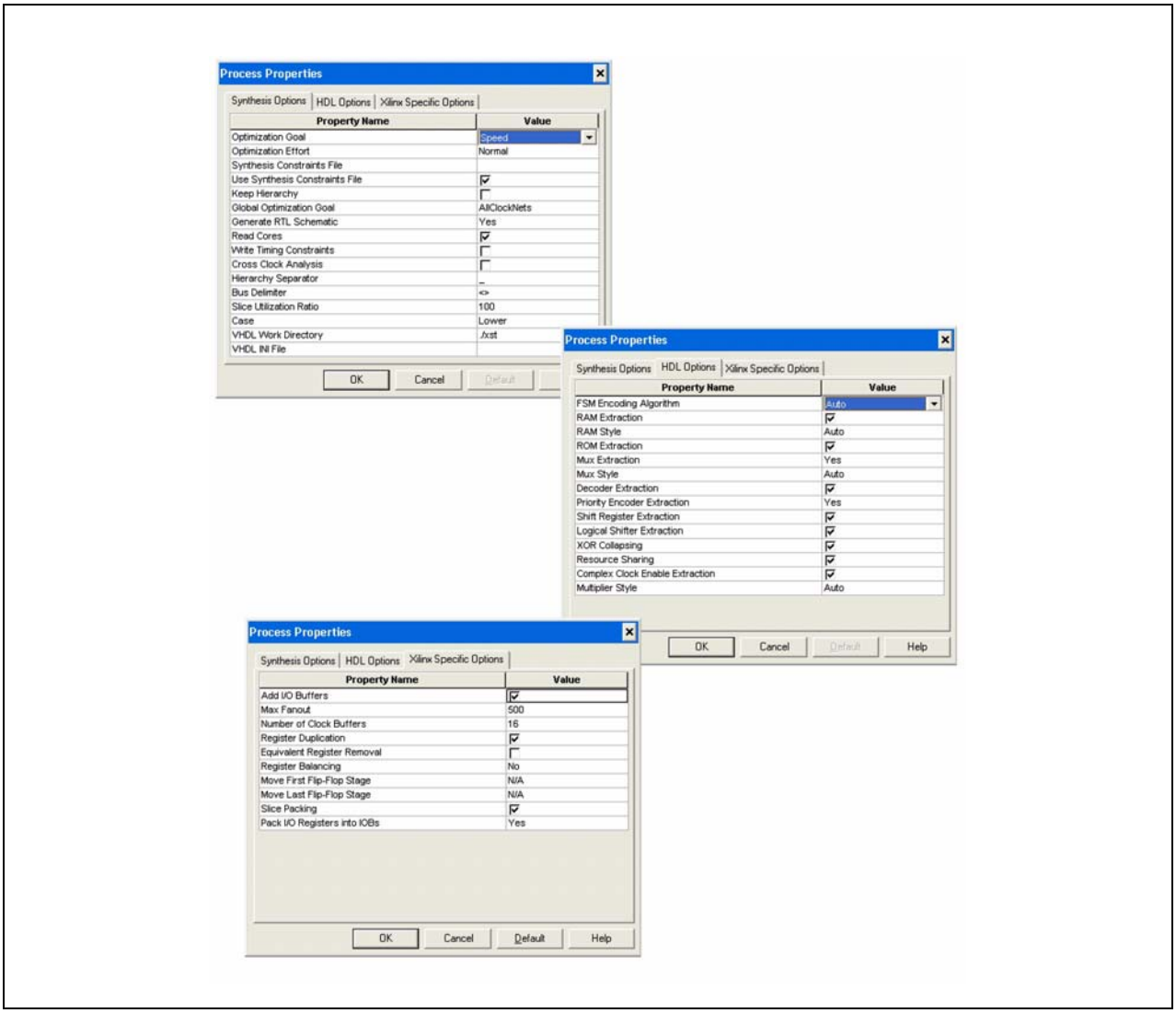


Figure 20: Synthesis Options Pages

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Implementation Options

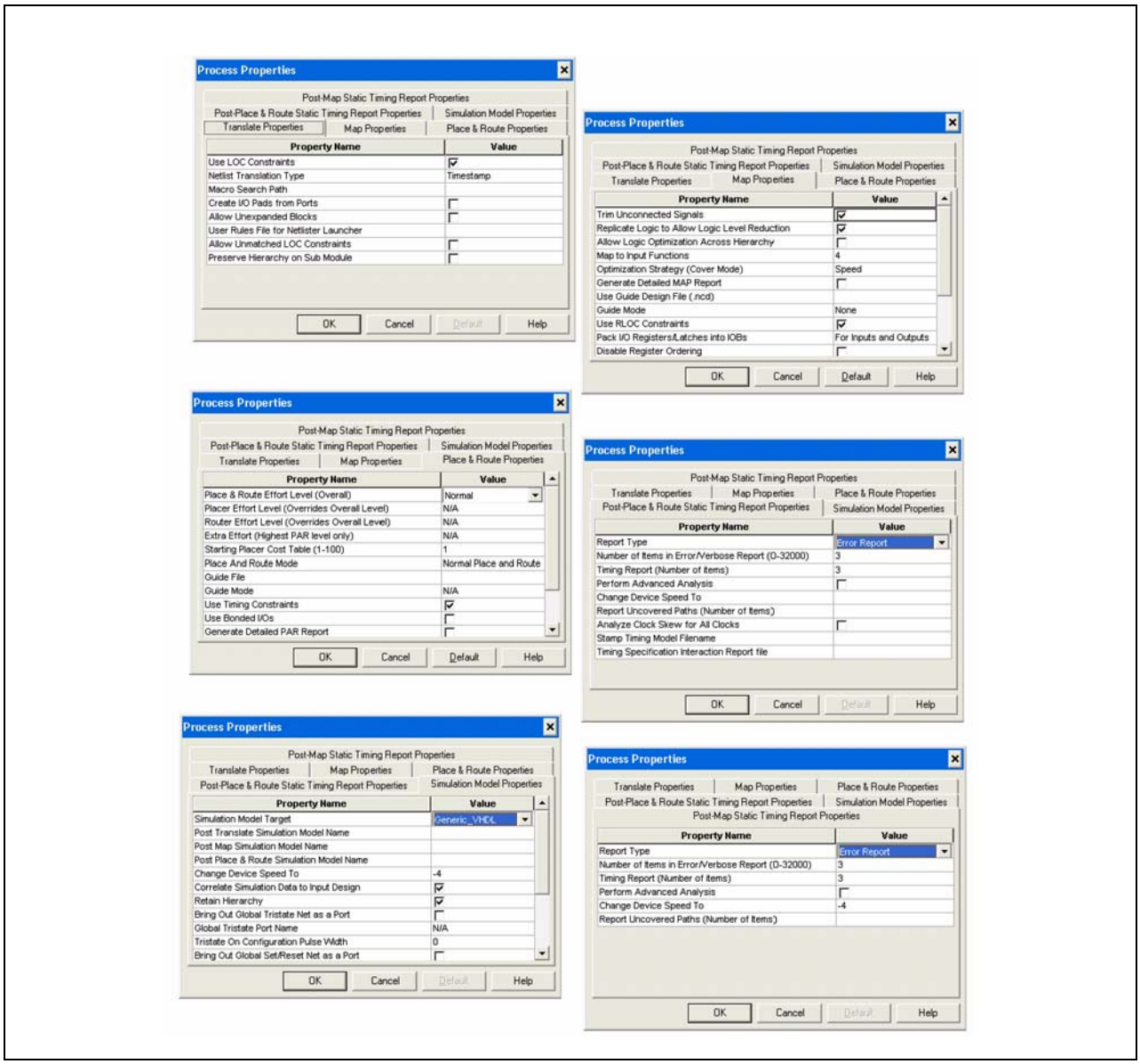


Figure 21: Implementation Options Pages

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File Generation Options

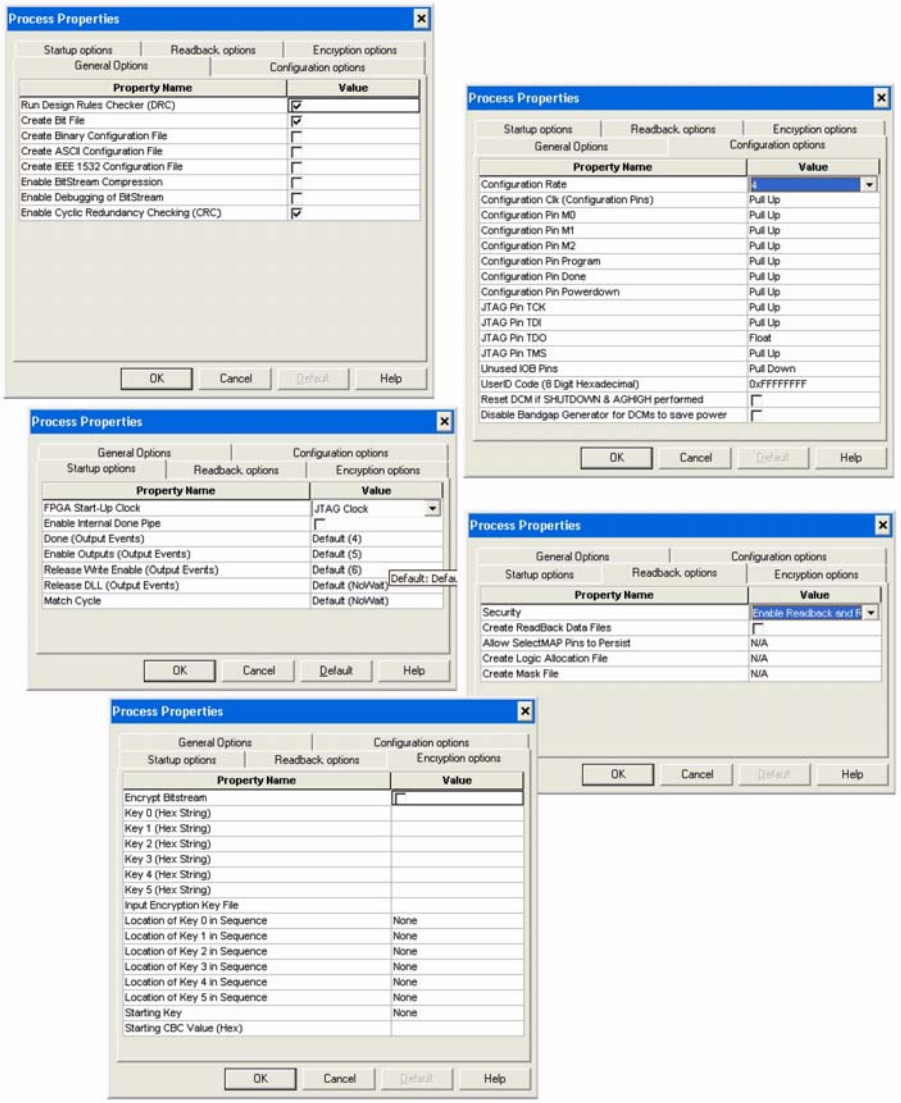


Figure 22: Generate Programming File

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Part II:Reference Information

This part of the Reference Guide provides information on all aspects of the BenDATA-DD including the module's physical layout, hardware features and pinout information.

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Section 2

Physical Layout

In this section:

- BenDATA-DD physical layout

2.1 BenDATA-DD Physical Layout

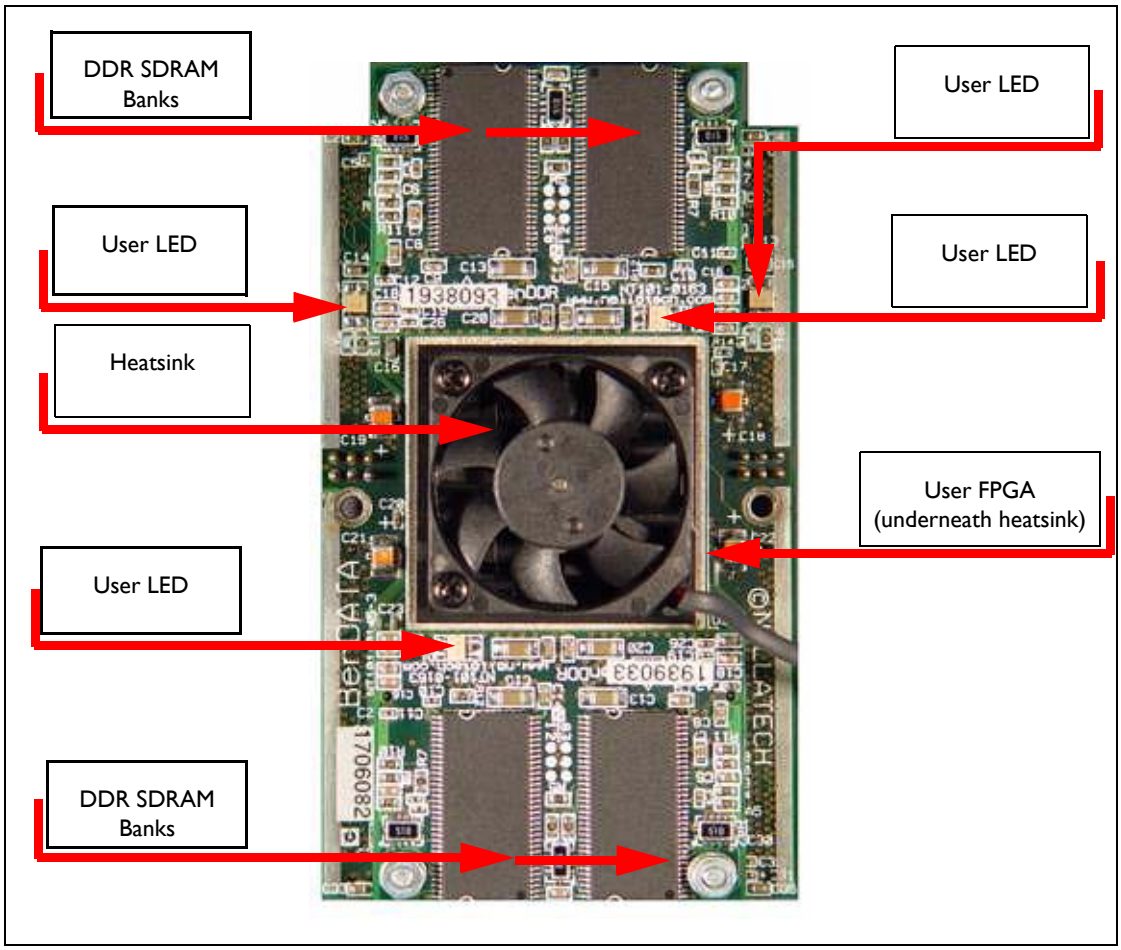


Figure 23: BenDATA-DD physical layout

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Section 3

Hardware Features

In this section:

- DDR SDRAM memory
- User FPGA
- Control and monitoring signals
- Temperature sensor
- Heatsink

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3.1 DDR SDRAM Memory

The BenDATA-DD supports four independent banks of DDR memory, with each bank consisting of 4 DDR SDRAM chips. The 1Gbyte version of the BenDATA-DD is populated with 512Mb DDR chips which are driven exclusively by the on-board User FPGA. Figure 24 on page 32 illustrates the inter-connect between one bank of DDR SDRAM and the User FPGA. Nallatech provide a DDR SDRAM controller core IP block to allow easy and efficient memory access from the FPGA.

- The core is included with the BenDATA-DD and is available on the BenDATA-DD CD in the following directory '<CDROM Drive>:\DDRCore\'.
- For details on using the core please refer to the **DDR SDRAM Controller Core Datasheet** on the BenDATA-DD CD in the following directory '<CDROM Drive>:\Documentation\Product\'.

3.1.1 Hardware Details

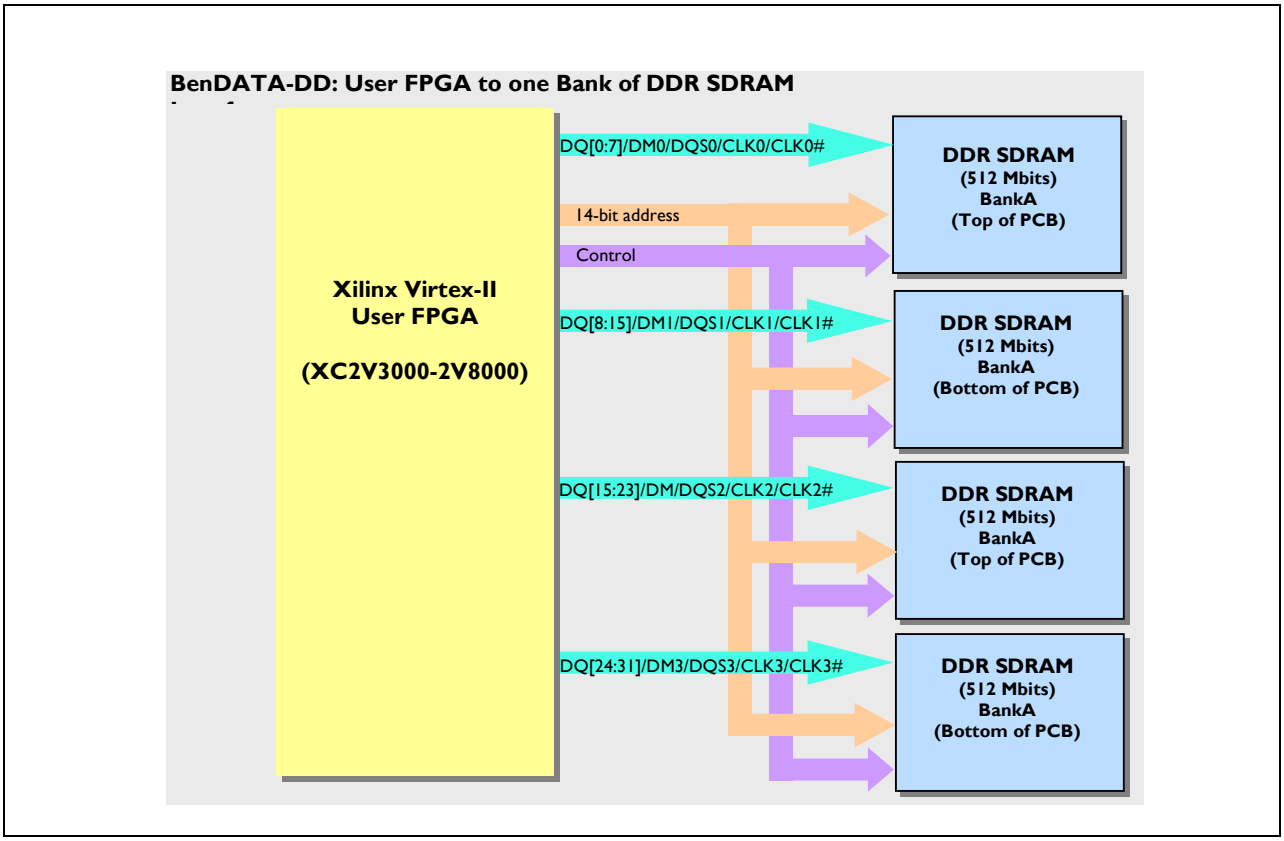


Figure 24: Functional Block Diagram of DDR SDRAM (BANK A) Interface

Each bank of DDR SDRAM consists of four DDR SDRAM chips which are described below.

DDR SDRAM Chips

The main features of the DDR SDRAM chips used in the BenDATA-DD's memory banks include:

- Internal, pipelined double-data-rate architecture; two data accesses per clock cycle.
- Differential clock inputs.
- Bi-directional data strobe signal.
- Commands entered on positive clock edge.
- Programmable burst lengths: 2, 4, or 8.

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- Pin/function compatibility with 512Mb DDR SDRAM chips.

Each chip also contains the following signals:

- Unique data bits - DQ0-7 for one chip, DQ8-15 for another chip and so on.
- Data mask signal - DM0 for one chip, DM1 for another chip and so on.
- Data strobe signal - DQS0 for one chip, DQS1 for another chip and so on
- Unique differential clock signal - CLK0/CLK0# for one chip, CLK1/CLK# for another chip and so on.
- All address bits (A0 - A13) are shared between the four chips in a bank.
- All control signals (BA0, BA1, RAS#, CAS#, WE#, CKE#, and CS#) are shared between the four chips in a bank.

3.1.2 DDR SDRAM Clocking

Each DDR SDRAM chip has a unique differential clock signal. All clock signals are matched to the data, data-strobe and data mask signals in length which minimizes the skew between these signals. Additionally the clock at the DDR SDRAM chips and the feedback pins have coincident clock edges with minimum skew.

Driving the DDR SDRAM differential clocks from the User FPGA ensures maximum flexibility in the clocking mechanism during system design, as the clocks can be derived from any of the DIME-II system clocks (CLKA, CLKB or CLKC), which enter the module through the DIME-II connectors.

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3.2 User FPGA

3.2.1 Overview

The BenDATA-DD utilizes the powerful processing capability of a Xilinx Virtex-II FPGA to support various FPGA sizes and speed grades. This provides the flexibility to choose the most appropriate FPGA to meet processing requirements. Figure 25 on page 34 outlines all the possible DIME-II communications.

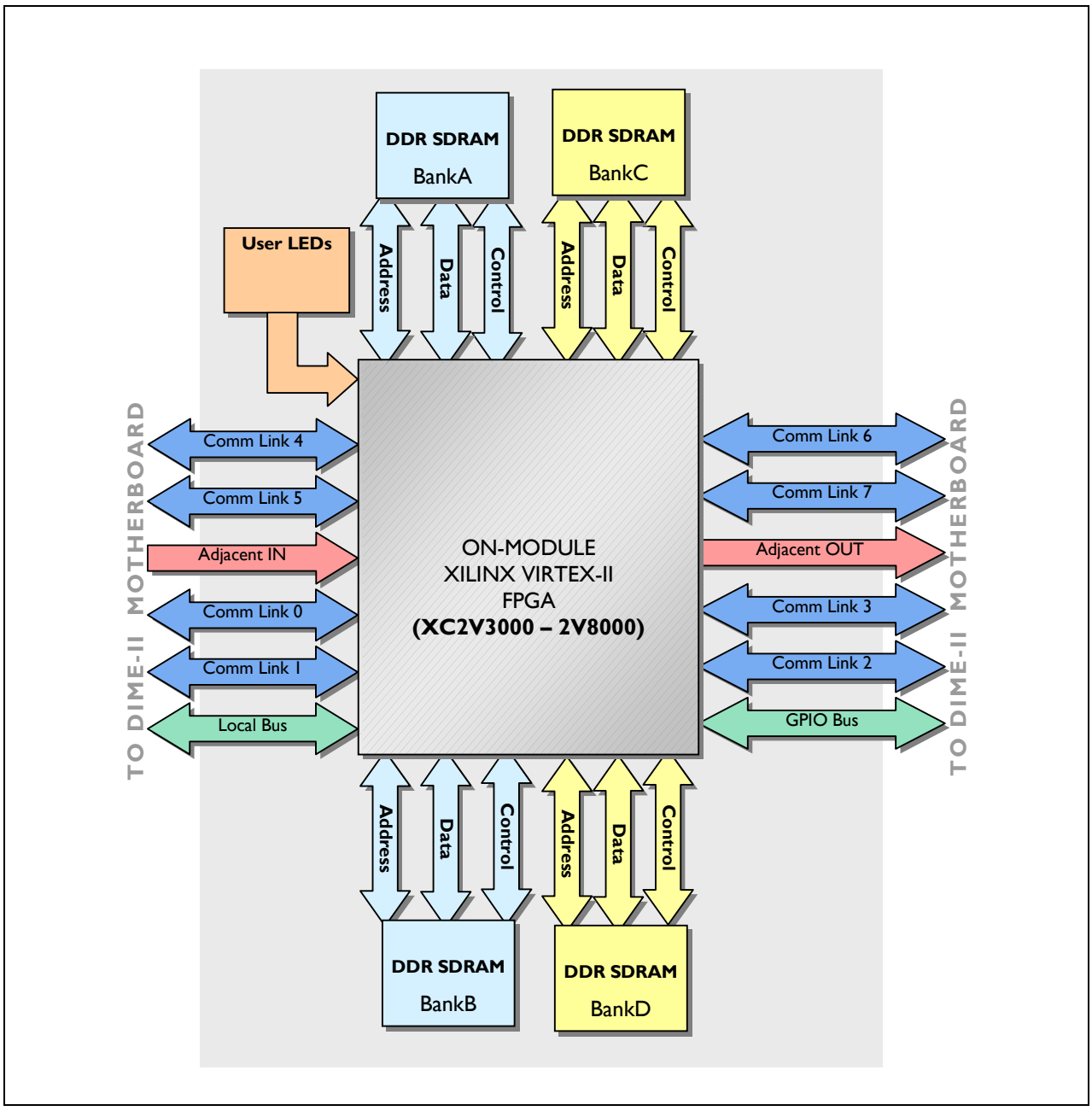


Figure 25: User FPGA interfacing Overview

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3.2.2 DIME-II Communication Busses

To support the large volume of communications between DIME-II modules and DIME-II motherboards, the following busses provide a robust infrastructure for these communications:

- Adjacent In Bus.
- Adjacent Out Bus.
- Comm Links 0 - 7 busses.
- Local Bus.
- GP IO Bus.

The infrastructure of these communication busses is described in the relevant motherboard Reference Guide. Table 3 on page 35 outlines the size of each communication bus relative to FPGA size.



Note that all busses listed in Table 3 on page 35 are bi-directional.

Communication Bus	2V3000 FF1152	2V6000 FF1152	2V8000 FF1152
Adjacent IN	64 bits	64 bits	64 bits
Adjacent OUT	64 bits	64 bits	64 bits
Comm Link 0	12 bits	12 bits	12 bits
Comm Link 1	12 bits	12 bits	12 bits
Comm Link 2	12 bits	12 bits	12 bits
Comm Link 3	12 bits	12 bits	12 bits
Comm Link 4	12 bits	12 bits	12 bits
Comm Link 5	12 bits	12 bits	12 bits
Comm Link 6	12 bits	12 bits	12 bits
Comm Link 7	12 bits	12 bits	12 bits
Local Bus	64 bits	64 bits	64 bits
GP IO Bus	21 bits	21 bits	21 bits

Table 3: Communication Bus Summary

3.2.3 DIME-II System Clocks

The BenDATA-DD has three system clocks available for use in the User FPGA - CLKA, CLKB and CLKC. All of these clock signals are generated on the DIME-II motherboard and are routed into the module site where the BenDATA-DD is placed. These clocks, which can be freely controlled by the user, are routed to Global Clock pins to provide maximum flexibility on the User FPGA. For full details of the generation of these clock signals prior to use on the module site, consult the relevant motherboard Reference Guide.

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3.3 Control and Monitoring Signals

The BenDATA-DD produces a range of signals that allow the user to control and monitor the on-board module behavior.

- 'Reset': The Reset signal is used to clear the memory of the on-board User FPGA
- 'JTAG': The JTAG chain is used for test and configuration purposes
- 'Config DONE': This signal is related to the configuration of the on-board User FPGA
- 'LEDs': There are up to four tricolor LEDs on the BenDATA-DD that are free to be used for the chosen application
- 'Temperature Sensor': Used to monitor the temperature of the User FPGA

3.3.1 BenDATA-DD FPGA Reset

The BenDATA-DD has a RESETI signal connected directly to the on-board User FPGA. RESETI is driven by the DIME-II motherboard and is available through the FUSE Software. This signal is active LOW and will reset the on-board User FPGA when a LOW is applied.

DIME-II Connector PIN No	Signal Name	DIME-II Connector PIN No	User FPGA Pin (FF1152 package)
RESETI	RESETI	PC15	K27

Table 4: FPGA Reset Pinout

The pin location is also listed in the UCF on the BenDATA-DD CD in the following directory '<CDROM Drive>:\UCFs\'.

3.3.2 JTAG Chain

DIME-II modules have a JTAG based Plug and Play, PnP, facility to enable auto-detection of the modules present in a system. Each DIME-II module has a unique ID number. The BenDATA-DD IDs are listed in Table 5 on page 36.

ID Number (Hex)	Description
31980033	User FPGA: XC2V3000 (FF1152)
31983033	User FPGA: XC2V6000 (FF1152)
31986033	User FPGA: XC2V8000 (FF1152)

Table 5: BenDATA-DD Assigned MDF Code Listing

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3.3.3 Config DONE

The DIME-II standard allows a design to be implemented based on the status of the entire system. The Config DONE signal provides built-in control that can be used if the System Designer wishes. This feature allows a designer to synchronize all aspects of the complete system.

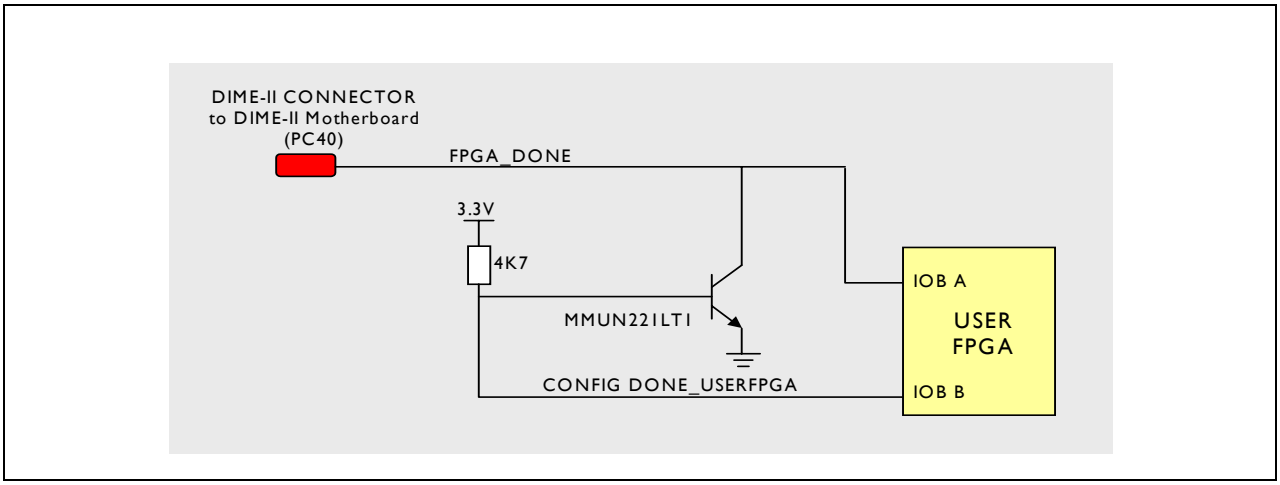


Figure 26: Config DONE circuit

Figure 26 on page 37 shows the set-up of the 'CONFIGURATION DONE' operation on the BenDATA-DD. The FPGA_DONE signal to the on-board FPGA determines the status of the FPGA on the module. The FPGA_DONE signal is connected directly to the carrier motherboard where it is then connected to all other module sites and the PCI FPGA. This signal has a weak pull-up applied to it on the motherboard.

When the FPGA on the BenDATA-DD is NOT configured, the base of the transistor (MMUN2211LT1) will be switched on by the 3.3V pull-up. With the base of the transistor switched on, the FPGA_DONE signal (connected to the motherboard via the DIME-II connector) will be pulled LOW through the transistor.

Once the FPGA has been configured, the user should send out a LOW signal on the appropriate CONFIG_DONE pin (in this case, a LOW would be driven out of 'IOB B' on the FPGA). This turns the base of the transistor off; meaning the FPGA_DONE value is now subject to the status of the complete system. Once all other FPGAs in the system are configured, the FPGA_DONE signal will be HIGH via the pull-up on the motherboard. However, if one FPGA is not configured, the FPGA_DONE signal from that device will still be pulled LOW, meaning that FPGA_DONE for the entire system would be LOW. The system designer will therefore be able to read the value of FPGA_DONE, via FUSE software, at the 'IOB A' input on the various FPGAs to determine the overall state of the system.

If the 'CONFIG DONE' signal is utilized in a system, ensure that IOB B is driven low once the FPGA has been successfully configured. Alternatively, if a system initialization sequence is required IOB B can be driven low after this. The FPGA then polls IOB A to see that all other FPGAs in the system have been configured.

The pin locations for this Config DONE signal are listed in “DIME-II control and monitoring signals” on page 52.

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3.3.4 User LEDs

The BenDATA-DD has up to four LEDs, which can be used for specific design purposes, such as displaying status.

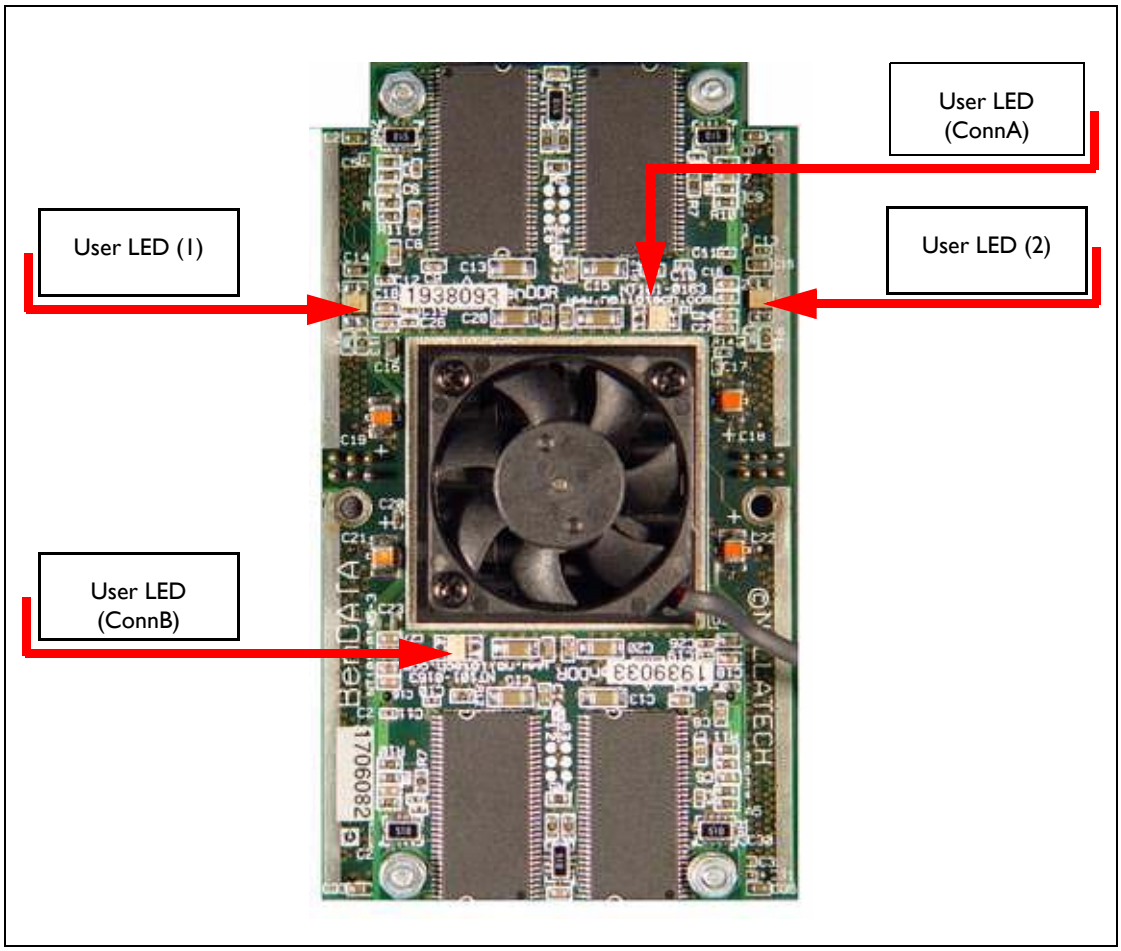


Figure 27: User LEDs

The LEDs are illuminated when the corresponding pin is logic 0, otherwise the LED is not illuminated (Active LOW). The LEDs used on the BenDATA-DD are tricolor, which means that each LED can act as three individual LEDs. Each LED has a RED and GREEN diode inside their chip. Applying logic 0 to either Cathode will cause that color to illuminate and applying logic 0 to both Cathodes (green and red) will cause a third color, yellow, to illuminate.

Signal Description	Signal Name	User FPGA Pin (FF1152 package)
Green Diode for LED1	LED1_Green	AJ31
Red Diode for LED1	LED1_Red	AK31
Green Diode for LED2	LED2_Green	AL32
Red Diode for LED2	LED2_Red	AK32
Red Diode for LED_ConnA	LED_red_connA	AN10*
Red Diode for LED_ConnB	LED_red_connB	B25*

Table 6: LED signals

*LED_red_connA and LED_red_connB are ONLY available when a XC2V6000 FF1152 User FPGA or higher is populated and applying a logic 0 to these pins will illuminate the red LED.

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3.4 Temperature Sensor

The BenDATA-DD can be supplied with various sizes of User FPGAs which can become very hot when running at full potential. As a result, the BenDATA-DD is fitted with a temperature device that monitors the junction temperature within the User FPGA. Figure 28 on page 39 shows the BenDATA-DD temperature sensor interface.

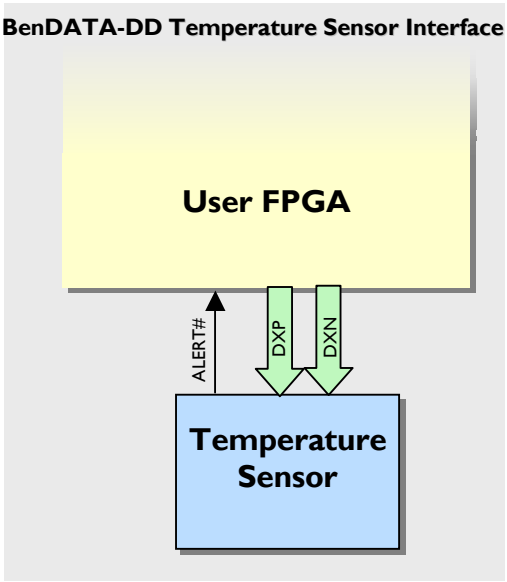


Figure 28: Temperature Sensor Interface

The DXN (Diode Return Current Sink) and DXP (Diode Current Source) signals from the temperature sensor are connected directly to the dedicated DXN and DXP pins on the User FPGA. The ALERTI signal is also connected directly to an IO pin on the User FPGA.

Software functions through the FUSE API provide temperature-monitoring capability for the on-board FPGA. The API functions provide the ability to readback the junction of the FPGA and the external PCB temperature. Other functions include the ability to set the minimum and maximum temperature thresholds. The temperature thresholds are linked to the ALERTI signal - when either threshold is reached the ALERTI signal to the on-board FPGA will be asserted.



Incorporating the ALERTI signal into an FPGA design provides thermal protection to the FPGA.



Extreme care should be taken with the temperature levels of the FPGA. Commercial grade silicon has a junction temperature range of 0°C - 85°C, and -40°C - 100°C for Industrial grade silicon.

- For further information on the FUSE API functions for the temperature sensor, please refer to the **FUSE C/C++ API Developer Guide** on the supplied FUSE CD.

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3.5 BenDATA-DD Heatsink

3.5.1 FPGA thermal considerations

All high power semiconductor devices require some form of cooling to function within their working tolerances or to improve their performance. The modern FPGA, with its user-specified design, is a new concept to the thermal design engineer. It can function effectively without any form of cooling for small designs, but as the designer begins to understand the technology and its capabilities, the need for larger more complex designs increases. Consequently the power consumption of the FPGA also increases. For FPGA designers it is vital to understand the factors involved in the thermal performance of a system. Thermal performance can be viewed in two ways.

1. For a given fixed power consumption, the cooler the surrounding air temperature, the smaller the cooling element has to be on the component to remove the heat.

2. Alternatively, if the cooling element has the same physical properties across the temperature range, the cooler the surrounding air temperature the more power can be consumed by the device before the maximum junction temperature is exceeded.

The second option is the case with an FPGA as a cooler air temperature enables bigger designs to be implemented in the device without the need to increase the cooling requirements for the system.

It is therefore difficult to pick an 'average' power consumption for a particular FPGA, so Nallatech recommend using the Xilinx power estimation tool available on the Xilinx website (http://www.xilinx.com/ise/power_tools/spreadsheet_pt.htm). This tool gives an estimation of power consumption from a user design and requires input from the reports that are produced when compiling a design in ISE. The results can be used to decide if the FPGA requires additional cooling to function within the manufacturers' specified limits.

DIME-II products from Nallatech are supplied with a heatsink fitted to the FPGA, which improves performance and allows large designs to be implemented in the FPGA. However this approach also has a power limit - as the power densities of the FPGA increase (due to lower core voltages), cooling at the component level rapidly approaches a maximum due to physical restrictions. For example, the restriction of heatsink height on a PCI board due to the PCI specification R2.2, which states that the maximum component height must not exceed 14.48mm from the topside on the PCB. Restrictions in component cooling become more challenging when considering the PC/104-*Plus* form-factor specification.

Therefore Nallatech recommend use of the heatsink supplied with the DIME-II products for designs < 16watts. For higher powered designs where increased cooling of the FPGA at the component level or system level cooling is required, please consult Nallatech for more information.

3.5.2 BenDATA-DD

Mounted on a PCI platform

The heatsink attached to the BenDATA-DD exceeds the height restriction in PCI specification revision 2.2 by 12.5mm (the specification states that no component shall be higher than 14.48mm above the card). This is done to improve the thermal characteristics of the BenDATA-DD so that reasonable-sized user designs can be implemented. See “Customer-specific solutions” on page 43 for additional information.

Mounted on a Compact PCI platform

There is no height restriction in the cPCI specification version 2.0 revision 3, except that a Compact PCI card needs to be a multiple of 4HP wide i.e. 4HP (single width card), 8HP (double width card) etc. The BenERA cPCI motherboard is designed as a double width card, however the heatsink attached to the BenDATA-DD exceeds the height limit for a double width card by 11mm, which means a BenERA loaded with one or more BenDATA-DD modules will become a 12HP wide card taking up 3 slots of the cPCI backplane (1 behind and 2 in front of the card). See “Customer-specific solutions” on page 43 for additional information.

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Mounted on a PC/104-*Plus* platform

Although the BenDATA-DD can be mounted in the top module slot of a PC/104-*Plus* stack Nallatech do not recommend using the standard heatsink for this form factor. Please contact Nallatech as alternatives can be offered to ensure these modules fully comply with your system requirements.

Limitations with standard heatsink

Each bank of DDR memory requires a DDR IP core (supplied) to function correctly. If the user implements all 4 banks of DDR memory then 30% of a 2V3000 FPGA resource is used and the power required to run all 4 cores at 133MHz (266MHz data rate) is 6.42 Watts. The total number of slices for a total of 4 DDR IP core is given below.

Number of SLICEs	2973 out of 14336
Number of RAMB16s	20 out of 96
Number of DCMs	3 out of 12
Number of BUFGMUXs	5 out of 16
Number of External IOBs	281 out of 720

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Figure 29 on page 42 shows the maximum power available to the user design for a given ambient air temperature. If you wish to calculate the junction temperature of the FPGA (using the standard heatsink attached to the BenDATA-DD) for a particular ambient air temperature and power consumption, please use the "Calculation Example" on page 42 as a guide. A basic knowledge of thermal analysis will aid in understanding the example. The Xilinx Power Estimator can be used to estimate the power requirements of application designs. For more information on the Xilinx Power Estimator see: http://support.xilinx.com/ise/power_tools/index.htm. Nallatech recommend removal of the DDR core from the figures which are input into the Xilinx power estimation tool.

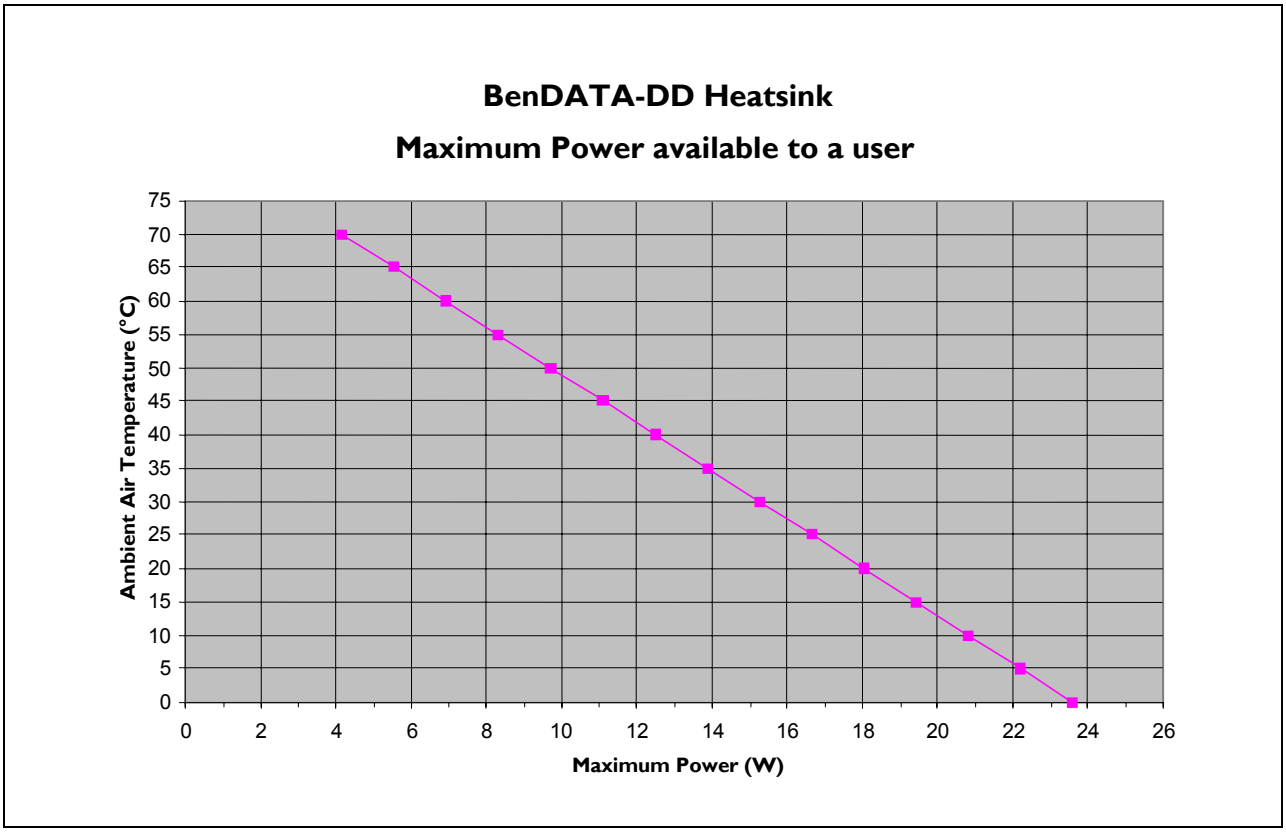


Figure 29: Maximum Power

Calculation Example

Below is a list of the information required to calculate the junction temperature.

- Ambient Air Temperature (T_{AMB}): this is the temperature around the FPGA and also the temperature of air entering the fan. For this example a temperature of 30°C has been chosen.
- Maximum Junction Temperature (T_{JMAX}): Xilinx recommend a maximum junction temperature for the Virtex-II devices in a FF1152 package does not exceed 85°C.
- Function to Case Thermal Resistance (θ_{JC}): this figure is package dependent and is quoted by the manufacturer. The Junction to Case thermal resistance is 1.1°C/W for an FF1152 package.
- Interface Material Thermal Resistance (θ_{CS}): this is the adhesive, compound or tape that is usually found between the device and heatsink. For the BenDATA-DD Nallatech use thermal tape with a thermal resistance of 0.22°C/W.
- Heatsink Thermal Resistance (θ_{HS}): this figure is quoted by the heatsink manufacturer, the standard heatsink fitted to the BenDATA-DD has a thermal resistance of 2.28°C/W.
- Power consumption from your design: please remember to add the 6.42W required by the 4 DDR IP cores.

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We can now calculate the total thermal resistance (θ_T):

$$\theta_T = \theta_{JC} + \theta_{CS} + \theta_{HS}$$
$$\theta_T = 1.1 + 0.22 + 2.28$$
$$\theta_T = 3.6°C / W$$

If the design requires 5W (remember to add 6.42W for the 4 DDR IP cores) then the junction temperature will be:

$$\text{Junction temperature}(T_J) = (\theta_T \times W) + T_{AMB}$$

$$\text{Junction temperature}(T_J) = (3.6 \times (5 + 6.42)) + 30$$

$$\text{Juntion temperature}(T_J) = 71.11°C$$

This falls below the maximum of 85°C specified by the manufacturer.

3.5.3 Customer-specific solutions

If the infringement of the PCI specification is a concern, you require the BenERA cPCI card to remain as an 8HP width card, or you require higher density designs to be implemented within the FPGA, please contact Nallatech as customer-specific alternatives can be offered.

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Section 4

Pinout Information

In this section:

- User FPGA to DIME-II motherboard communication
- DIME-II control and monitoring signals
- Pinouts for DDR SDRAM Banks

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4.1 XC2V3000/XC26000/XC2V8000 FF1152

4.1.1 User FPGA to DIME-II motherboard communication

Local Bus Pinouts

Signal Name	DIME-II Connector PIN No	User FPGA (2V3000/2V6000/ 2V8000) PIN No	Signal Name	DIME-II Connector PIN No	User FPGA (2V3000/2V6000/ 2V8000) PIN No
LBUS<0>	PB1	H7	LBUS<32>	PB37	AE11
LBUS<1>	PB2	J9	LBUS<33>	PB38	AE10
LBUS<2>	PB3	J8	LBUS<34>	PB39	AG9
LBUS<3>	PB4	J7	LBUS<35>	PB40	AD9
LBUS<4>	PB6	K9	LBUS<36>	PB42	AE9
LBUS<5>	PB7	K8	LBUS<37>	PB43	AF10
LBUS<6>	PB8	K7	LBUS<38>	PB44	AD10
LBUS<7>	PB9	L10	LBUS<39>	PB45	AF11
LBUS<8>	PB10	L9	LBUS<40>	PB46	AE8
LBUS<9>	PB11	L8	LBUS<41>	PB47	AF9
LBUS<10>	PB12	L7	LBUS<42>	PB48	AD8
LBUS<11>	PB13	M10	LBUS<43>	PB49	AF8
LBUS<12>	PB15	M9	LBUS<44>	PB51	AH6
LBUS<13>	PB16	M8	LBUS<45>	PB52	AG7
LBUS<14>	PB17	M7	LBUS<46>	PB53	AB7
LBUS<15>	PB18	N10	LBUS<47>	PB54	AF7
LBUS<16>	PB19	N9	LBUS<48>	PB55	AD7
LBUS<17>	PB20	N8	LBUS<49>	PB56	AE7
LBUS<18>	PB21	N7	LBUS<50>	PB57	AB8
LBUS<19>	PB22	P8	LBUS<51>	PB58	AH3
LBUS<20>	PB24	U9	LBUS<52>	PB60	AJ3
LBUS<21>	PB25	U8	LBUS<53>	PB61	AJ4
LBUS<22>	PB26	V10	LBUS<54>	PB62	AJ5
LBUS<23>	PB27	W10	LBUS<55>	PB63	N2
LBUS<24>	PB28	AB9	LBUS<56>	PB64	P2
LBUS<25>	PB29	AB10	LBUS<57>	PB65	R1
LBUS<26>	PB30	AH5	LBUS<58>	PB66	T2
LBUS<27>	PB31	AG4	LBUS<59>	PB67	U2
LBUS<28>	PB33	AC10	LBUS<60>	PB69	U1
LBUS<29>	PB34	AC9	LBUS<61>	PB70	V2
LBUS<30>	PB35	AC8	LBUS<62>	PB71	V1

Table 7: Local Bus Pinouts (2V3000/6000/8000)

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Signal Name	DIME-II Connector PIN No	User FPGA (2V3000/2V6000/ 2V8000) PIN No	Signal Name	DIME-II Connector PIN No	User FPGA (2V3000/2V6000/ 2V8000) PIN No
LBUS<31>	PB36	AC7	LBUS<63>	PB72	AA1

Table 7: Local Bus Pinouts (2V3000/6000/8000)

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Adjacent IN Bus - User FPGA communications

Signal Name	DIME-II Connector PIN No	User FPGA (2V3000/2V6000/ 2V8000) PIN No	Signal Name	DIME-II Connector PIN No	User FPGA (2V3000/2V6000/ 2V8000) PIN No
ADJIN<0>	PA29	H16	ADJIN<32>	PA65	AE6
ADJIN<1>	PA30	H17	ADJIN<33>	PA66	AD6
ADJIN<2>	PA31	H4	ADJIN<34>	PA67	AG6
ADJIN<3>	PA32	J4	ADJIN<35>	PA68	AF6
ADJIN<4>	PA33	H3	ADJIN<36>	PA69	AG5
ADJIN<5>	PA34	J3	ADJIN<37>	PA70	AF5
ADJIN<6>	PA35	K6	ADJIN<38>	PA71	AG3
ADJIN<7>	PA36	J6	ADJIN<39>	PA72	AF3
ADJIN<8>	PA38	K5	ADJIN<40>	SA2	P6
ADJIN<9>	PA39	L5	ADJIN<41>	SB1	N6
ADJIN<10>	PA40	M6	ADJIN<42>	SA3	N5
ADJIN<11>	PA41	L6	ADJIN<43>	SB2	P5
ADJIN<12>	PA42	K4	ADJIN<44>	SA4	N3
ADJIN<13>	PA43	L4	ADJIN<45>	SB3	P3
ADJIN<14>	PA44	L3	ADJIN<46>	SA5	R10
ADJIN<15>	PA45	M3	ADJIN<47>	SB4	P10
ADJIN<16>	PA47	U6	ADJIN<48>	SA6	R9
ADJIN<17>	PA48	T6	ADJIN<49>	SB6	P9
ADJIN<18>	PA49	V4	ADJIN<50>	SA7	P4
ADJIN<19>	PA50	U3	ADJIN<51>	SB7	R4
ADJIN<20>	PA51	W6	ADJIN<52>	SA8	T8
ADJIN<21>	PA52	V6	ADJIN<53>	SB8	R8
ADJIN<22>	PA53	W5	ADJIN<54>	SA9	R3
ADJIN<23>	PA54	V5	ADJIN<55>	SB9	T3
ADJIN<24>	PA56	Y3	ADJIN<56>	SA11	T7
ADJIN<25>	PA57	W3	ADJIN<57>	SB10	U7
ADJIN<26>	PA58	AD4	ADJIN<58>	SA12	W7
ADJIN<27>	PA59	AC4	ADJIN<59>	SB11	V7
ADJIN<28>	PA60	AE5	ADJIN<60>	SA13	AA6
ADJIN<29>	PA61	AD5	ADJIN<61>	SB12	Y6
ADJIN<30>	PA62	AF4	ADJIN<62>	SA14	AB4
ADJIN<31>	PA63	AE4	ADJIN<63>	SB13	AA4

Table 8: Adjacent IN BUS Pinouts - User FPGA (2V3000/6000/8000)

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Adjacent OUT Bus - User FPGA connections

Signal Name	DIME-II Connector PIN No	User FPGA (2V3000/2V6000/ 2V8000) PIN No	Signal Name	DIME-II Connector PIN No	User FPGA (2V3000/2V6000/ 2V8000) PIN No
ADJOUT<0>	PD29	H32	ADJOUT<32>	PD65	AF18
ADJOUT<1>	PD30	J32	ADJOUT<33>	PD66	AG18
ADJOUT<2>	PD31	H31	ADJOUT<34>	PD67	AB27
ADJOUT<3>	PD32	J31	ADJOUT<35>	PD68	AA27
ADJOUT<4>	PD33	J30	ADJOUT<36>	PD69	AC31
ADJOUT<5>	PD34	H30	ADJOUT<37>	PD70	AD31
ADJOUT<6>	PD35	J28	ADJOUT<38>	PD71	AD29
ADJOUT<7>	PD36	J27	ADJOUT<39>	PD72	AC29
ADJOUT<8>	PD38	K30	ADJOUT<40>	SD2	AD27
ADJOUT<9>	PD39	K31	ADJOUT<41>	SC1	AC27
ADJOUT<10>	PD40	L26	ADJOUT<42>	SD3	AE31
ADJOUT<11>	PD41	K26	ADJOUT<43>	SC2	AD32
ADJOUT<12>	PD42	K28	ADJOUT<44>	SD4	AE30
ADJOUT<13>	PD43	L28	ADJOUT<45>	SC3	AD30
ADJOUT<14>	PD44	L31	ADJOUT<46>	SD5	AE28
ADJOUT<15>	PD45	M31	ADJOUT<47>	SC4	AD28
ADJOUT<16>	PD47	M29	ADJOUT<48>	SD6	AF29
ADJOUT<17>	PD48	L29	ADJOUT<49>	SC6	AE29
ADJOUT<18>	PD49	M28	ADJOUT<50>	SD7	AF27
ADJOUT<19>	PD50	N28	ADJOUT<51>	SC7	AE27
ADJOUT<20>	PD51	T30	ADJOUT<52>	SD8	AF32
ADJOUT<21>	PD52	U30	ADJOUT<53>	SC8	AG32
ADJOUT<22>	PD53	U29	ADJOUT<54>	SD9	AF31
ADJOUT<23>	PD54	T29	ADJOUT<55>	SC9	AG31
ADJOUT<24>	PD56	U31	ADJOUT<56>	SD11	AG30
ADJOUT<25>	PD57	V31	ADJOUT<57>	SC10	AF30
ADJOUT<26>	PD58	V32	ADJOUT<58>	SD12	AG28
ADJOUT<27>	PD59	W32	ADJOUT<59>	SC11	AF28
ADJOUT<28>	PD60	W30	ADJOUT<60>	SD13	AH29
ADJOUT<29>	PD61	V30	ADJOUT<61>	SC12	AG29
ADJOUT<30>	PD62	Y31	ADJOUT<62>	SD14	AJ32
ADJOUT<31>	PD63	W31	ADJOUT<63>	SC13	AH32

Table 9: Adjacent OUT BUS Pinouts - User FPGA (2V3000/6000/8000)

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PLINKS connected to the User FPGA: PLINKS 0, 1, 2 and 3

Signal Name	DIME-II Connector PIN No	User FPGA (2V3000/2V6000/ 2V8000) PIN No	Signal Name	DIME-II Connector PIN No	User FPGA (2V3000/2V6000/ 2V8000) PIN No
PP0LK<0>	PA2	D3	PP2LK<0>	PD2	D32
PP0LK<1>	PA3	E3	PP2LK<1>	PD3	E32
PP0LK<2>	PA4	E4	PP2LK<2>	PD4	E31
PP0LK<3>	PA5	F4	PP2LK<3>	PD5	F31
PP0LK<4>	PA6	G5	PP2LK<4>	PD6	G30
PP0LK<5>	PA7	F5	PP2LK<5>	PD7	F30
PP0LK<6>	PA8	F3	PP2LK<6>	PD8	F32
PP0LK<7>	PA9	G3	PP2LK<7>	PD9	G32
PP0LK<8>	PA11	G6	PP2LK<8>	PD11	G29
PP0LK<9>	PA12	H6	PP2LK<9>	PD12	H29
PP0LK<10>	PA13	H5	PP2LK<10>	PD13	N25
PP0LK<11>	PA14	J5	PP2LK<11>	PD14	M25
PP1LK<0>	PA15	D2	PP3LK<0>	PD15	D34
PP1LK<1>	PA16	E2	PP3LK<1>	PD16	E34
PP1LK<2>	PA17	D1	PP3LK<2>	PD17	F34
PP1LK<3>	PA18	E1	PP3LK<3>	PD18	G34
PP1LK<4>	PA20	F2	PP3LK<4>	PD20	H33
PP1LK<5>	PA21	G2	PP3LK<5>	PD21	J34
PP1LK<6>	PA22	F1	PP3LK<6>	PD22	L33
PP1LK<7>	PA23	G1	PP3LK<7>	PD23	M33
PP1LK<8>	PA24	H2	PP3LK<8>	PD24	L34
PP1LK<9>	PA25	J1	PP3LK<9>	PD25	M34
PP1LK<10>	PA26	L2	PP3LK<10>	PD26	N31
PP1LK<11>	PA27	M2	PP3LK<11>	PD27	P31

Table 10: PLINK Pinouts - User FPGA (2V3000/6000/8000)

PLINKS connected to the User FPGA: PLINKS 4, 5, 6 and 7

Signal Name	DIME-II Connector PIN No	User FPGA (2V3000/2V6000/ 2V8000) PIN No	Signal Name	DIME-II Connector PIN No	User FPGA (2V3000/2V6000/ 2V8000) PIN No
PP4LK<0>	SA48	AF1	PP6LK<0>	SD48	AD33
PP4LK<1>	SA49	AE2	PP6LK<1>	SD49	AC33
PP4LK<2>	SA50	AG2	PP6LK<2>	SD50	AF33

Table 11: PLINK Pinouts - User FPGA (2V3000/6000/8000)

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Signal Name	DIME-II Connector PIN No	User FPGA (2V3000/2V6000/ 2V8000) PIN No	Signal Name	DIME-II Connector PIN No	User FPGA (2V3000/2V6000/ 2V8000) PIN No
PP4LK<3>	SA51	AF2	PP6LK<3>	SD51	AG33
PP4LK<4>	SA52	AJ2	PP6LK<4>	SD52	AJ34
PP4LK<5>	SA53	AH2	PP6LK<5>	SD53	AH34
PP4LK<6>	SA54	AJ1	PP6LK<6>	SD54	AJ33
PP4LK<7>	SA56	AH1	PP6LK<7>	SD56	AH33
PP4LK<8>	SA57	AL2	PP6LK<8>	SD57	AL34
PP4LK<9>	SA58	AK2	PP6LK<9>	SD58	AK34
PP4LK<10>	SA59	AK1	PP6LK<10>	SD59	AK33
PP4LK<11>	SA60	AL1	PP6LK<11>	SD60	AL33
PP5LK<0>	SB47	AA10	PP7LK<0>	SC47	AA30
PP5LK<1>	SB48	Y10	PP7LK<1>	SC48	AB30
PP5LK<2>	SB49	Y9	PP7LK<2>	SC49	AA25
PP5LK<3>	SB51	AA9	PP7LK<3>	SC51	Y25
PP5LK<4>	SB52	AA8	PP7LK<4>	SC52	AA26
PP5LK<5>	SB53	Y7	PP7LK<5>	SC53	Y26
PP5LK<6>	SB54	AB5	PP7LK<6>	SC54	AB29
PP5LK<7>	SB55	AA5	PP7LK<7>	SC55	AA29
PP5LK<8>	SB56	AC6	PP7LK<8>	SC56	AC32
PP5LK<9>	SB57	AB6	PP7LK<9>	SC57	AB32
PP5LK<10>	SB58	AD3	PP7LK<10>	SC58	AC28
PP5LK<11>	SB60	AC3	PP7LK<11>	SC60	AB28

Table 11: PLINK Pinouts - User FPGA (2V3000/6000/8000)

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General Purpose IO

Signal Name	DIME-II Connector PIN No	User FPGA (2V3000/2V6000/ 2V8000) PIN No	Signal Name	DIME-II Connector PIN No	User FPGA (2V3000/2V6000/ 2V8000) PIN No
GP_IO<0>	PC72	AG26	GP_IO<11>	PC28	AC25
GP_IO<1>	PC70	AF25	GP_IO<12>	PC17	AB26
GP_IO<2>	PC10	V27	GP_IO<13>	PC16	AB25
GP_IO<3>	PC9	V26	GP_IO<14>	PC8	U27
GP_IO<4>	PC69	AF26	GP_IO<15>	PC7	U26
GP_IO<5>	PC67	AE25	GP_IO<16>	PC6	M27
GP_IO<6>	PC66	AE26	GP_IO<17>	PC4	L30
GP_IO<7>	PC65	AE24	GP_IO<18>	PC3	L27
GP_IO<8>	PC55	AD26	GP_IO<19>	PC2	L25
GP_IO<9>	PC54	AD25	GP_IO<20>	PC1	K24
GP_IO<10>	PC48	AC26			

Table 12: GP_IO Pinouts - User FPGA (2V3000/6000/8000)

4.1.2 DIME-II control and monitoring signals

DIME-II Specific Pins

DIME-II Connector PIN Name	Signal Name	DIME-II Connector PIN No	User FPGA (2V3000/ 2V6000/2V8000) PIN No
CONFIG_DONE	FPGA_DONE	PC40	N26
N/C	CONFIG_DONE*	N/a	M26
CLK0	CLKA	PC24	E19
CLK1	CLKB	PC31	AG17
CLK2	CLKC	PC42	E18
RESETI	RESETI	PC15	K27

Table 13: User FPGA Specific Pinouts (2V3000/6000/8000)

*CONFIG_DONE is driven from the IO of the Virtex-II into the base of the transistor to signal that the on-board User FPGA has been configured successfully. User to drive this pin LOW once the FPGA is configured.

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User LEDs

Signal Name	User FPGA (2V3000/2V6000/2V8000) PIN No
LED1_Green	AJ31
LED1_Red	AK31
LED2_Green	AL32
LED2_Red	AK32
LED_Red_ConnA	AN10**
LED_Red_ConnB	B25**

Table 14: User LED Pinouts - User FPGA (2V3000/6000/8000)

** Pin AN10 and B26 are NOT available on the 2V3000 device; it is only available on a 2V6000 FPGA or higher.

On-board Temperature Sensor

Signal Name	User FPGA (2V3000/2V6000/2V8000) PIN No
ALERTI	J26

Table 15: Temperature Sensor Pinout (2V3000/6000/8000)

4.1.3 DDR SDRAM Bank A

Clock Signals for DDR Bank A

Signal Name	User FPGA (2V3000/2V6000/2V8000) PIN No
DDRA_CK<0>	AG14
DDRA_CK<0>I	AG13
DDRA_CK<1>	AL11
DDRA_CK<1>I	AM11
DDRA_CK<2>	AJ18
DDRA_CK<2>I	AJ19
DDRA_CK<3>	AJ23
DDRA_CK<3>I	AJ24
DDR_BANKA_FB_IN	AK17
DDR_BANKA_FB_INI	AK16
DDR_BANKA_FB_OUT	AJ16
DDR_BANKA_FB_OUTI	AJ17

Table 16: DDR Clock Signals Pinouts - Bank A (2V3000/6000/8000)

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DDR Address Signals - Bank A

Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRA_A<0>	AL8	DDRA_A<7>	AJ10
DDRA_A<1>	AJ9	DDRA_A<8>	AK8
DDRA_A<2>	AH9	DDRA_A<9>	AM8
DDRA_A<3>	AG12	DDRA_A<10>	AK7
DDRA_A<4>	AG11	DDRA_A<11>	AM6
DDRA_A<5>	AG10	DDRA_A<12>	AM7
DDRA_A<6>	AH11	DDRA_A<13>*	AL18

Table 17: DDR Address Signals Pinouts - Bank A (2V3000/6000/8000)

*DDRA_A<13> is a reserved pin and is not used on the 1GByte (512Mbit DDR chips) version of the BenDATA-DD.

DDR Command Signals - Bank A

Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRA_BA<0>	AE13	DDRA_RASI	AL10
DDRA_BA<1>	AE12	DDRA_CASI	AL9
DDRA_CSI	AL5	DDRA_WEI	AM4
DDRA_CKEI	AM9		

Table 18: DDR Command Signals Pinouts - Bank A (2V3000/6000/8000)

DDR Data Signals - Bank A

Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRA_D<0>	AF17	DDRA_D<16>	AM26
DDRA_D<1>	AF13	DDRA_D<17>	AM27
DDRA_D<2>	AM17	DDRA_D<18>	AK27
DDRA_D<3>	AL17	DDRA_D<19>	AH26
DDRA_D<4>	AK11	DDRA_D<20>	AG23
DDRA_D<5>	AJ11	DDRA_D<21>	AJ25
DDRA_D<6>	AK10	DDRA_D<22>	AF23

Table 19: DDR Data Signals Pinouts - Bank A (2V3000/6000/8000)

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Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRA_D<7>	AF12	DDRA_D<23>	AF22
DDRA_D<8>	AK24	DDRA_D<24>	AF24
DDRA_D<9>	AH23	DDRA_D<25>	AG24
DDRA_D<10>	AH22	DDRA_D<26>	AJ26
DDRA_D<11>	AM19	DDRA_D<27>	AG25
DDRA_D<12>	AL24	DDRA_D<28>	AL30
DDRA_D<13>	AH25	DDRA_D<29>	AM31
DDRA_D<14>	AK25	DDRA_D<30>	AM28
DDRA_D<15>	AL25	DDRA_D<31>	AJ27

Table 19: DDR Data Signals Pinouts - Bank A (2V3000/6000/8000)

DDR Data Mask and Strobe Signals - Bank A

Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRA_UUDM<0>	AH12	DDRA_UDQS<0>	AH13
DDRA_UUDM<1>	AG21	DDRA_UDQS<1>	AG22
DDRA_UUDM<2>	AL27	DDRA_UDQS<2>	AL26
DDRA_UUDM<3>	AL29	DDRA_UDQS<3>	AK28

Table 20: DDR Data Mask and Strobe Signals Pinouts - Bank A (2V3000/6000/8000)

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4.1.4 DDR SDRAM Bank B

Clock Signals for DDR Bank B

Signal Name	User FPGA (2V3000/2V6000/2V8000) PIN No
DDRB_CK<0>	D11
DDRB_CK<0>I	D10
DDRB_CK<1>	G13
DDRB_CK<1>I	G12
DDRB_CK<2>	D23
DDRB_CK<2>I	D22
DDRB_CK<3>	F19
DDRB_CK<3>I	F18
DDR_BANKB_FB_IN	E16
DDR_BANKB_FB_INI	E17
DDR_BANKB_FB_OUT	F17
DDR_BANKB_FB_OUTI	F16

Table 21: DDR Clock Signals Pinouts - Bank B (2V3000/6000/8000)

DDR Address Signals - Bank B

Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRB_A<0>	E9	DDRB_A<7>	E10
DDRB_A<1>	G10	DDRB_A<8>	E8
DDRB_A<2>	H12	DDRB_A<9>	C9
DDRB_A<3>	K12	DDRB_A<10>	D9
DDRB_A<4>	J13	DDRB_A<11>	C8
DDRB_A<5>	H13	DDRB_A<12>	C7
DDRB_A<6>	G11	DDRB_A<13>*	D15**

Table 22: DDR Address Signals Pinouts - Bank B (2V3000/6000/8000)

*DDRB_A<13> is a reserved pin and is not used on the 1GByte (512Mbit DDR chips) version of the BenDATA-DD.

**Pin D15 is NOT available on the 2V3000 device, it is only available on a 2V6000 FPGA or higher.

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DDR Command Signals - Bank B

Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRB_BA<0>	G19	DDRB_RASI	C18
DDRB_BA<1>	G18	DDRB_CASI	D17
DDRB_CSI	K13	DDRB_WEI	C16
DDRB_CKEI	K14		

Table 23: DDR Command Signals Pinouts - Bank B (2V3000/6000/8000)

DDR Data Signals - Bank B

Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRB_D<0>	D6	DDRB_D<16>	G24
DDRB_D<1>	D8	DDRB_D<17>	J23
DDRB_D<2>	H9	DDRB_D<18>	K22
DDRB_D<3>	G9	DDRB_D<19>	K23
DDRB_D<4>	J12	DDRB_D<20>	D25
DDRB_D<5>	J11	DDRB_D<21>	E25
DDRB_D<6>	H10	DDRB_D<22>	C27
DDRB_D<7>	J10	DDRB_D<23>	G25
DDRB_D<8>	C24	DDRB_D<24>	E26
DDRB_D<9>	D24	DDRB_D<25>	F27
DDRB_D<10>	D26	DDRB_D<26>	C29
DDRB_D<11>	F24	DDRB_D<27>	D29
DDRB_D<12>	H22	DDRB_D<28>	H26
DDRB_D<13>	H23	DDRB_D<29>	G26
DDRB_D<14>	D18	DDRB_D<30>	H24
DDRB_D<15>	F23	DDRB_D<31>	J24

Table 24: DDR Data Signals Pinouts - Bank B (2V3000/6000/8000)

DDR Data Mask and Strobe Signals - Bank B

Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRB_UDM<0>	C6	DDRB_UDQS<0>	H11

Table 25: DDR Data Mask and Strobe Signals Pinouts - Bank B (2V3000/6000/8000)

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Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRB_UDM<1>	J21	DDRB_UDQS<1>	J22
DDRB_UDM<2>	D27	DDRB_UDQS<2>	C26
DDRB_UDM<3>	F26	DDRB_UDQS<3>	H25

Table 25: DDR Data Mask and Strobe Signals Pinouts - Bank B (2V3000/6000/8000)

4.1.5 DDR SDRAM BANK C

Clock Signals for DDR Bank C

Signal Name	User FPGA (2V3000/2V6000/2V8000) PIN No
DDRC_CK<0>	AF21
DDRC_CK<0>I	AF20
DDRC_CK<1>	AN21
DDRC_CK<1>I	AN22
DDRC_CK<2>	AK13
DDRC_CK<2>I	AK14
DDRC_CK<3>	AP13
DDRC_CK<3>I	AP14
DDR_BANKC_FB_IN	AK19
DDR_BANKC_FB_INI	AK18
DDR_BANKC_FB_OUT	AH18
DDR_BANKC_FB_OUTI	AH19

Table 26: DDR Clock Signals Pinouts - Bank C (2V3000/6000/8000)

DDR Address Signals - Bank C

Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRC_A<0>	AD17	DDRC_A<7>	AG20
DDRC_A<1>	AD18	DDRC_A<8>	AG19
DDRC_A<2>	AE20	DDRC_A<9>	AJ22
DDRC_A<3>	AE15	DDRC_A<10>	AN14
DDRC_A<4>	AE21	DDRC_A<11>	AH20
DDRC_A<5>	AD19	DDRC_A<12>	AP28
DDRC_A<6>	AD16	DDRC_A<13>*	AN9**

Table 27: DDR Address Signals Pinouts - Bank C (2V3000/6000/8000)

*DDRC_A<13> is a reserved pin and is not used on the 1GByte (512Mbit DDR chips) version of the BenDATA-DD.

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**Pin AN9 is NOT available on the 2V3000 device, it is only available on a 2V6000 FPGA or higher.

DDR Command Signals - Bank C

Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRC_BA<0>	AF15	DDRC_RASI	AG16
DDRC_BA<1>	AE14	DDRC_CASI	AM14
DDRC_CSI	AF14	DDRC_WEI	AM15
DDRC_CKEI	AG15		

Table 28: DDR Command Signals Pinouts - Bank C (2V3000/6000/8000)

DDR Data Signals - Bank C

Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRC_D<0>	AN30	DDRC_D<16>	AM13
DDRC_D<1>	AN31	DDRC_D<17>	AM12
DDRC_D<2>	AN28	DDRC_D<18>	AL12
DDRC_D<3>	AN29	DDRC_D<19>	AL13
DDRC_D<4>	AN24	DDRC_D<20>	AN11
DDRC_D<5>	AN23	DDRC_D<21>	AP9
DDRC_D<6>	AP26	DDRC_D<22>	AN4
DDRC_D<7>	AN27	DDRC_D<23>	AN5
DDRC_D<8>	AP23	DDRC_D<24>	AN3
DDRC_D<9>	AP24	DDRC_D<25>	AM2
DDRC_D<10>	AL23	DDRC_D<26>	AP5
DDRC_D<11>	AL22	DDRC_D<27>	AP4
DDRC_D<12>	AM24	DDRC_D<28>	AP6
DDRC_D<13>	AP30	DDRC_D<29>	AP12
DDRC_D<14>	AM33	DDRC_D<30>	AP11
DDRC_D<15>	AN32	DDRC_D<31>	AP7

Table 29: DDR Data Signals Pinouts - Bank C (2V3000/6000/8000)

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DDR Data Mask and Strobe Signals - Bank C

Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRC_UDM<0>	AK22	DDRC_UDQS<0>	AK21
DDRC_UDM<1>	AP31	DDRC_UDQS<1>	AM23
DDRC_UDM<2>	AN8	DDRC_UDQS<2>	AN12
DDRC_UDM<3>	AJ13	DDRC_UDQS<3>	AN7

Table 30: DDR Data Mask and Strobe Signals Pinouts - Bank C (2V3000/6000/8000)

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4.1.6 DDR SDRAM BANK D

Clock Signals for DDR Bank D

Signal Name	User FPGA (2V3000/2V6000/2V8000) PIN No
DDRD_CK<0>	J14
DDRD_CK<0>I	J15
DDRD_CK<1>	E14
DDRD_CK<1>I	E13
DDRD_CK<2>	E22
DDRD_CK<2>I	E21
DDRD_CK<3>	B22
DDRD_CK<3>I	B21
DDR_BANKD_FB_IN	J18
DDR_BANKD_FB_INI	K18
DDR_BANKD_FB_OUT	D21
DDR_BANKD_FB_OUTI	D20

Table 31: DDR Clock Signals Pinouts - Bank D (2V3000/6000/8000)

DDR Address Signals - Bank D

Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRD_A<0>	B14	DDRD_A<7>	C14
DDRD_A<1>	K16	DDRD_A<8>	C13
DDRD_A<2>	H15	DDRD_A<9>	F13
DDRD_A<3>	G17	DDRD_A<10>	G20
DDRD_A<4>	H14	DDRD_A<11>	G15
DDRD_A<5>	K15	DDRD_A<12>	A9
DDRD_A<6>	B13	DDRD_A<13>*	B26**

Table 32: DDR Address Signals Pinouts - Bank D (2V3000/6000/8000)

*DDRD_A<13> is a reserved pin and is not used on the 1GByte (512Mbit DDR chips) version of the BenDATA-DD.

**Pin B26 is NOT available on the 2V3000 device; it is only available on a 2V6000 FPGA or higher.

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DDR Command Signals - Bank D

Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRD_BA<0>	K20	DDRD_RASI	K19
DDRD_BA<1>	G16	DDRD_CASI	H20
DDRD_CSI	K21	DDRD_WEI	H21
DDRD_CKEI	J20		

Table 33: DDR Command Signals Pinouts - Bank D (2V3000/6000/8000)

DDR Data Signals - Bank D

Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRD_D<0>	B5	DDRD_D<16>	C22
DDRD_D<1>	B4	DDRD_D<17>	C23
DDRD_D<2>	B7	DDRD_D<18>	G23
DDRD_D<3>	B6	DDRD_D<19>	G22
DDRD_D<4>	C11	DDRD_D<20>	B24
DDRD_D<5>	C12	DDRD_D<21>	A26
DDRD_D<6>	A7	DDRD_D<22>	B29
DDRD_D<7>	A6	DDRD_D<23>	B28
DDRD_D<8>	B12	DDRD_D<24>	B32
DDRD_D<9>	B11	DDRD_D<25>	C33
DDRD_D<10>	A11	DDRD_D<26>	B30
DDRD_D<11>	A12	DDRD_D<27>	B31
DDRD_D<12>	B9	DDRD_D<28>	A31
DDRD_D<13>	A5	DDRD_D<29>	A23
DDRD_D<14>	C2	DDRD_D<30>	A24
DDRD_D<15>	B3	DDRD_D<31>	A30

Table 34: DDR Data Signals Pinouts - Bank D (2V3000/6000/8000)

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DDR Data Mask and Strobe Signals - Bank D

Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No	Signal Name	User FPGA (2V3000/ 2V6000/2V8000) PIN No
DDRD_UDM<0>	D12	DDRD_UDQS<0>	D13
DDRD_UDM<1>	A4	DDRD_UDQS<1>	B10
DDRD_UDM<2>	B27	DDRD_UDQS<2>	B23
DDRD_UDM<3>	F22	DDRD_UDQS<3>	A28

Table 35: DDR Data Mask and Strobe Signals Pinouts - Bank D (2V3000/6000/8000)

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The company reserves the right to vary the specification or withdraw from the offer any of its products without prior warning.

The company reserves the right to refuse to accept any contract that is deemed to be contrary to the companies policies in force at the time.

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All prices shown on the company's price list, or on quotations offered by them, are based upon the acceptance of these conditions. Any variation of these conditions requested by the buyer could result in changes in the offered pricing or refusal to supply.

All quoted pricing is in Pounds Sterling and is exclusive of Value Added Tax (VAT) and delivery. In addition to the invoiced value the buyer is liable for all import duty as may be applicable in the buyer's location. If there is any documentation required for import formalities, whether or not for the purposes of duty assessment, the buyer shall make this clear at the time of order.

Quotations are made by Nallatech upon the customer's request but there is no obligation for either party until Nallatech accepts the customer's order.

Nallatech reserves the right to increase the price of goods agreed to be sold in proportion to any increase of costs to Nallatech between the date of acceptance of the order and the date of delivery or where the increase is due to any act or default of the customer, including the cancellation or rescheduling by the customer of part of any order.

Nallatech reserves the right (without prejudice to any other remedy) to cancel any uncompleted order or to suspend delivery in the event of any of the customer's commitment with Nallatech not being met.

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All delivery times offered by the company are to be treated as best estimates and no penalty can be accepted for non compliance with them.

Delivery shall be made by the company using a courier service of its choice. The cost of the delivery plus a nominal fee for administration will be added to the invoice issued. Payment of all inward customs duties and fees are the sole responsibility of the buyer. If multiple shipments are requested by the buyer, multiple delivery charges will be made. In the case of multiple deliveries separate invoices will be raised.

If requested at the time of ordering an alternative delivery service can be used, but only if account details are supplied to the company so that the delivery can be invoiced directly to the buyer by the delivery service.

The buyer accepts that any 'to be advised' scheduled orders not completed within twelve months from the date of acceptance of the original order, or orders held up by the buyers lack of action regarding delivery, can be shipped and invoiced by the company and paid in full by the buyer, immediately after completion of that twelve month period.

INSURANCE

All shipments from the company are insured by them. If any goods received by the buyer are in an unsatisfactory condition, the following courses of action shall be taken.

If the outer packaging is visibly damaged, then the goods should not be accepted from the courier, or they should be signed for only after noting that the packaging has sustained damage.

If the goods are found to be damaged after unpacking, the company must be informed immediately.

Under no circumstances should the damaged goods be returned, unless expressly authorized by the company.

If the damage is not reported within 48 hours of receipt, the insurers of the company shall bear no liability.

Any returns made to the company for any reason, at any time shall be packaged in the original packaging, or its direct equivalent and must be adequately insured by the buyer.

Any equipment sent to the company for any purpose, including but not limited to equipment originally supplied by the company must be adequately insured by the buyer while on the premises of the company.

PAYMENT

Nallatech Ltd. terms of payment are 30 days net.

Any charges incurred in making the payment, either

currency conversion or otherwise shall be paid by the buyer.

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The company reserves the right to charge interest at a rate of 2% above the base rate of the Bank of Scotland PLC on any overdue accounts. The interest will be charged on any outstanding amount from said due date of payment, until payment is made in full, such interest will accrue on a daily basis.

TECHNICAL SUPPORT

The company offers a dedicated technical support via telephone and an E-mail address. It will also accept faxed support queries.

Technical support will be given free of charge for 90 days from the date of invoice, for queries regarding the use of the products in the system configuration for which they were sold. Features not documented in the user manual or a written offer of the company will not be supported. Interfacing with other products other than those that are pre-approved by the company as compatible will not be supported. If the development tools and system hardware is demonstrably working, no support can be given with application level problems.

WARRANTY

The company offers as part of a purchase contract 12 months warranty against parts and defective workmanship of hardware elements of a system. The basis of this warranty is that the fault be discussed with the companies technical support staff before any return is made. If it is agreed that a return for repair is necessary then the faulty item and any other component of the system as requested by those staff shall be returned carriage paid to the company. Insurance terms as discussed in the INSURANCE Section will apply.

Returned goods will not be accepted by the company unless this has been expressly authorized.

After warranty repair, goods will be returned to the buyer carriage paid by the company using their preferred method.

Faults incurred by abuse of the product (as defined by the company) are not covered by the warranty.

Attempted repair or alteration of the goods as supplied by the company, by another party immediately invalidates the warranty offered.

The said warranty is contingent upon the proper use of the goods by the customer and does not cover any part of the goods which has been modified without Nallatech's prior written consent or which has been subjected to unusual physical or electrical stress or on which the original identification marks have been removed or altered. Nor will such warranty apply if repair or parts required as a result of causes other than ordinary authorized use including without limitation accident, air conditioning, humidity control or other environmental conditions.

Under no circumstances will the company be liable for any incidental or consequential damage or expense of any kind, including, but not limited to, personal injuries and loss of profits arising in connection with any contract or with the use, abuse, unsafe use or inability to use the companies goods. The company's maximum liability shall not exceed and the customers remedy is limited to, either:

i. repair or replacement of the defective part or product or at the companies option.
ii. return of the product and refund of the purchase price and such remedy shall be the customer's entire and exclusive remedy.

Warranty of the software written by the company shall be limited to 90 days warranty that the media is free from defects and no warranty express or implied is given that the computer software will be free from error or will meet the specification requirements of the buyer.

The terms of any warranty offered by a third party whose software is supplied by the company will be honoured by the company exactly. No other warranty is offered by the company on these products.

Return of faulty equipment after the warranty period has expired, the company may at its discretion make a quotation for repair of the equipment or declare that the equipment is beyond repair.

PASSING OF RISK AND TITLE

The passing of risk for any supply made by the company shall occur at the time of delivery. The title however shall not pass to the buyer until payment has been received in full by the company. And no other sums whatever shall be due from the customer to Nallatech.

If the customer (who shall in such case act on his own account and not as agent for Nallatech) shall sell the goods prior to making payment in full for them, the beneficial entitlement of Nallatech therein shall attach to the proceeds of such sale or to the claim for such proceeds.

The customer shall store any goods owned by Nallatech in such a way that they are clearly identifiable as Nallatech's property and shall maintain records of them identifying them as Nallatech's property. The customer will allow Nallatech to inspect these records and the goods themselves upon request.

In the event of failure by the customer to pay any part of the price of the goods, in addition to any other remedies available to Nallatech under these terms and conditions or otherwise, Nallatech shall be entitled to repossess the goods. The customer will assist and allow Nallatech to repossess the goods as aforesaid and for this purpose admit or procure the admission of Nallatech or its employees and agents to the premises in which the goods are situated.

INTELLECTUAL PROPERTY

The buyer agrees to preserve the Intellectual Property Rights (IPR) of the company at all times and that no contract for supply of goods involves loss of IPR by the company unless expressly offered as part of the contract by the company.

GOVERNING LAW

This agreement and performance of both parties shall be governed by Scottish law.

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Any disputes under any contract entered into by the company shall be settled in a court if the company's choice operating under Scottish law and the buyer agrees to attend any such proceedings. No action can be brought arising out of any contract more than 12 months after the completion of the contract.

INDEMNITY

The buyer shall indemnify the company against all claims made against the company by a third party in respect of the goods supplied by the company.

SEVERABILITY

If any part of these terms and conditions is found to be illegal, void or unenforceable for any reason, then such clause or Section shall be severable from the remaining clauses and Sections of these terms and conditions which shall remain in force.

NOTICES

Any notice to be given hereunder shall be in writing and shall be deemed to have been duly given if sent or delivered to the party concerned at its address specified on the invoice or such other addresses as that party may from time to time notify in writing and shall be deemed to have been served, if sent by post, 48 hours after posting.

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