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National Instruments

GPIB11V-1

Operating and Service Manual

Part Number 320002-01

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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

This section contains general information about National Instruments' GPIB11V-1 interface kit which is pictured in Figure 1.1. This information includes a brief description of the GPIB11V-1 kit, a list of equipment supplied, a list of optional equipment, a list of applicable reference documents, and a brief description of the remainder of this manual.

1.2 GPIB11V-1 INTERFACE KIT DESCRIPTION

The GPIB11V-1 is a single dual-height card which interfaces the LSI-11 to the IEEE Std 488-1978 instrumentation bus (General Purpose Interface Bus). The GPIB11V-1 provides a means to implement LSI-11 test and measurement systems with standard interconnecting cables. The GPIB11V-1 interface kit includes hardware and software to implement the GPIB functions. A cable is supplied for interconnection with other devices on the GPIB. Utility software is distributed on either paper tape or RT-11 compatible floppy disks. Comprehensive manuals provide the user with instructions for use of the kit.

1.3 EQUIPMENT SUPPLIED

Table 1.1 lists the equipment supplied in the National Instruments' GPIB11V-1 interface kit. Optional items are listed in Table 1.2.

1.4 APPLICABLE DOCUMENTS

The following documents are references which cover in greater detail specific topics introduced in this manual.

IEEE Std 488-1978, Standard Digital Interface
for Programmable Instrumentation
DEC Microcomputer Handbook

1.5 SCOPE

This manual provides the user with a general description of the General Purpose Interface Bus, installation and programming information for the GPIB11V-1, and finally, the theory of operation, logic diagram, and replacement parts lists for proper use and maintenance of the GPIB11V-1.

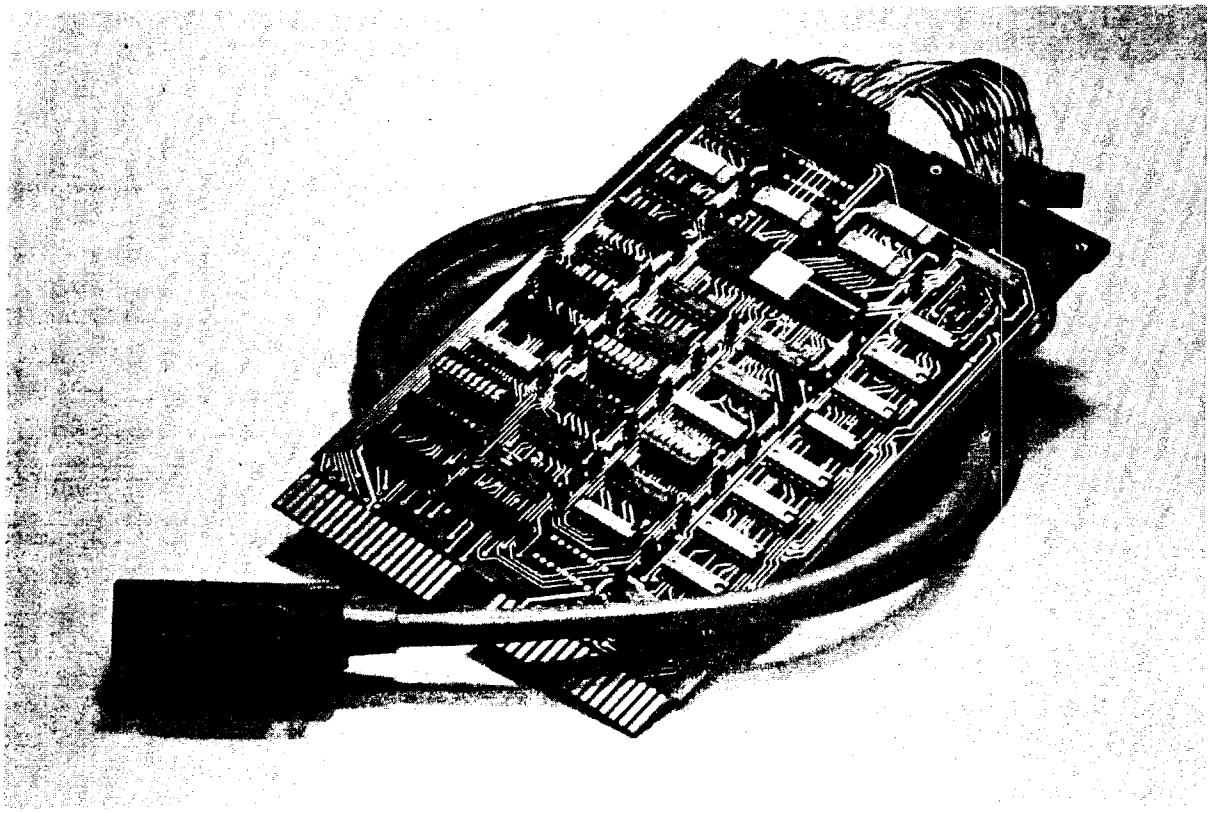


FIGURE 1.1

GPIB11V-1 INTERFACE

TABLE 1.1

EQUIPMENT SUPPLIED IN BASIC KIT

Description	Part Number
Bus Interface Card	178009-01
Interface Cable Assembly, 4 Meter	178040-04
Operating and Service Manual	320002-02
Software Reference Manual	310001-01
Floppy Disk Software Distribution Kit	420003-01

TABLE 1.2

OPTIONAL EQUIPMENT

Paper Tape Software Distribution Kit	410003-01
Mag Tape Software Distribution Kit	430003-01
RK05 Software Distribution Kit	440003-01
UNIX software - Paper Tape Kit	410004-01
UNIX Software - Floppy Disk Kit	420004-01
UNIX Software - Mag Tape Kit	430004-01
UNIX Software - RK05 Kit	440004-01
One Meter Extension Cable	763001-01
Two Meter Extension Cable	763001-02
Four Meter Extension Cable	763001-03

The manual is divided into seven major sections: General Information, GPIB11V-1 Description, Installation and Configuration, Programming Information, Theory of Operation, Parts List, and Schematic Diagrams. An ASCII chart and list of bus messages is given in Appendix A.

CHAPTER 2

GPIB11V-1 DESCRIPTION

2.1 SPECIFICATIONS

2.1.1 Electrical Specifications

Bus Signal Lines: The interface system contains a set of sixteen signal lines which include:

DIO1-8	Date Bus Lines 1-8
DAV	Data Valid
NRFD	Not Ready for Data
NDAC	Not Data Accepted
IFC	Interface Clear
ATN	Attention
SRQ	Service Request
REN	Remote Enable
EOI	End or Identify

Electrical Signal Levels:

High >= 2.0V
Low <= 0.8V

All signals are low = true.
Termination: Each of the 16 signal lines is terminated by a resistive load which establishes a steady state voltage when all drivers on the line are disabled. Each of the lines are terminated with 3k ohm to Vcc and 6.2k ohm to ground by each device on the bus.
Line Drivers: The sixteen signal lines have drivers with the following characteristics:

Low State: Open collector with < +0.4V at +48 ma sink current
High State: Determined by termination

Line Receivers: Each line receiver has the following specification:

Type: Schmitt-Trigger with hysteresis of
Vt pos - Vt neg >= +0.4V

Low State: Negative threshold Vt neg >= 0.8V
High State: Positive threshold voltage +2.0V >= Vt pos

Maximum Cable Length: 4 meters for any individual cable, 2 meters per device connected. 20 meters total.

Operating Temperature: 0 - 40 degrees Celsius.

Power Requirements: The card requires the following power from the computer or the extension mounting box:

Supply	Maximum Current Required
+5 Vdc	1A

2.1.2 Physical Specifications

The GPIB11V-1 interface card is packaged on a single dual-height module that can be plugged into a LSI-11, LSI-11/2, or LSI-11/23 device slot. The module has a single 26 pin Berg connector, which inter-connects the board to the standard bus cable with a standard bus connector on the outboard end.

Card Dimensions:

Width: 5.25 inches
Height: 9 inches

2.2 DESCRIPTION OF THE GENERAL PURPOSE INTERFACE BUS

2.2.1 General

The IEEE Std 488-1978 Interface Bus provides a means for communications among a group of interconnected devices. Two type of messages are carried by the bus:

1. Messages used for bus management or interface messages.

2. Device dependent messages which are communicated between the various devices via the interface bus but are not used or processed by the bus.

The three types of devices which are required to organize and manage the flow of information on the bus are: 1) a Listener, 2) a Talker, and 3) a Controller. A Listener has the capability of being addressed by an interface message to receive device dependent messages. A Talker has the capability of being addressed by an interface message to send device dependent messages. A Controller can address devices to Listen or Talk. A Controller can also send interface messages to command other specific actions within interfaced devices. A single bus may have one or more Controllers. If more than one Controller is connected to the bus, one is designated as the System Controller and may temporarily pass control to any other Controller.

The GPIB11V-1 is capable of being a Listener, a Talker, a Controller, and, in particular, a System Controller.

2.2.2 GPIB Operation

This section contains a simplified description of the operation of the instrumentation bus. For more details the reader is referred to the IEEE standard.

Bus operation is divided into two logical functions: interface function (for bus management), and device functions (for device control and communication). The interface functions, which are described herein, are basically used to establish an environment in which device functions may be performed. The device functions are unique to the individual instrument and are not addressed here.

The source handshake (SH) and acceptor handshake (AH) interface functins are used to transmit and receive bit-parallel, byte-serial messages ("multiline messages") on the bus. These messages are interpreted either as commands to the interface or data bytes for the device depending on the status of the bus signal line, attention (ATN). ATN is asserted for interface commands.

The Talker (T) or Extended Talker (TE) and Listener (L) or Extended Listener (LE) interface functions are used to establish device function communication (which uses the handshake). When an interface has been addressed as a Talker, its associated device function is allowed to use the interface source handshake function to transmit data bytes. The device functions of any interfaces which were addressed as Listeners must use the acceptor handshake function to receive the data bytes. Only one device at a time may by the Talker, although multiple Listeners may exist.

The Controller function (C) is the originator of all interface messages. Only one interface at a time may be the Controller in charge, and protocol exists to pass the controlling ability among interfaces. On the bus, at any time there is at most one interface which has the capability to make itself the Controller. It is referred to as the System Controller.

The Controller is responsible for addressing and unaddressing Talkers and Listeners, as well as performing other bus management operations. These other operations include: conducting a parallel poll using the uniline message, Identify (IDY); setting device functions in remote or local mode using the uniline message, Remote Enable (REN); and initializing the bus by asserting the uniline message Interface Clear (IFC). The latter two operations are actually capabilities only of the System Controller and are not transferrable by the transfer of control protocol.

2.2.3 GPIB Lines

A total of 24 lines are used to implement the bus. Of these lines, 16 are signal lines, one is ground, one is the cable shield, and six are twisted pair common for six of the signal lines. The 16 signal lines are used to carry all information, interface messages, and device dependent messages among interconnected devices. The bus is organized into three sets of signal lines:

1. Data Bus, eight signal lines

2. Three handshake lines

3. Five interface management signal lines.

The eight data lines carry all data including input, output, and device dependent messages. In many instruments, data is based on the seven bit ASCII code set.

The three handshake lines, NRFD, DAV, and NDAC, are used to effect the transfer of each byte of data on the DIO lines from an addressed Talker to all addressed listeners. The three handshake lines provide a means to asynchronously transfer data between instruments.

The NRFD (Not Ready For Data) line is used to indicate the condition of readiness of devices to accept data. All instruments drive NRFD false when ATN is true. Only addressed listeners drive NRFD false when ATN is false. The NRFD line is monitored by the Controller when ATN is true and by the addressed Talker when ATN is false. The NRFD line is false when all Listeners are ready for data and true when one or more Listeners are not ready for data.

The DAV line (Data Valid) is used to indicate the validity of data on the data lines. DAV is driven true by the Controller when ATN is true and by the addressed Talker when ATN is false. The DAV line is monitored by all instruments if ATN is true and by addressed Listeners when ATN is false.

THE NDAC (Not Data Accepted) line is used to indicate acceptance of data by addressed Listeners. Listeners indicate acceptance of data by setting NDAC false. When NDAC is true, one or more Listeners have not accepted the data.

The five bus management lines are IFC, ATN, SRQ, REN, and EOI. IFC and ATN are used by all instruments while the remaining three may or may not be used by a particular instrument.

The ATN (Attention) line is used by the active Controller to indicate how data on the data lines is to be interpreted and which devices must respond to data. The ATN line must be monitored by all instruments other than the Active Controller at all times. When the ATN line is true, the Active Controller can send interface messages and addresses to instruments on the bus. Device dependent messages can be sent by the active Talker to active Listeners when the ATN line is false.

The IFC (Interface Clear) line is used by the System Controller to place the bus in a known quiescent state. The IFC line can only be driven true by the System Controller and must be monitored by all other instruments. In order to clear a device, the IFC line must be set true for at least 100 microseconds. IFC may be set true by the System Controller at any time.

The REN (Remote Enable) line is used to operate an instrument under remote control. A true value for the Remote Enable line is one of the conditions for operation of an instrument in remote mode. The use of the remote function is optional. The REN line is driven true only by the System Controller and may be changed at any time. Instruments which use the REN line must monitor it at all times and return to local control whenever it becomes

false.

The SRQ (Service Request) line is used by an instrument to asynchronously request service from the Controller in charge of the GPIB. The SRQ line is sensed by the Active Controller.

The EOI (End or Identify) line is used to indicate the end of a data string provided the ATN signal is false. When the ATN line is false, the addressed Talker may indicate the end of its data by setting EOI true at the same time it places the last byte on the data lines. The Active Controller may initiate a Parallel Poll of all instruments with Parallel Polling capability by setting ATN and EOI true simultaneously.

2.2.4 GPIB Physical Characteristics

Bus cables are used for interconnection of instruments. A maximum length of two meters per device is allowed. The instruments can be interconnected in a linear or star configuration with a maximum of 20 meters total of interconnecting cable. Two 24 pin piggy-back connectors, one male and one female, are used on either end of the interconnecting cables. An overall shield is used to reduce susceptibility to noise. This shield is grounded only at the System Controller. Figure 2.1 shows the pin connections for the GPIB cable.

2.3 GPIB11V-1 FUNCTIONAL DESCRIPTION

2.3.1 Hardware Description

The GPIB11V-1 is a dual-height card which interfaces the LSI-11 computer to the General Purpose Interface Bus. Figure 2.2a shows an implementation of a GPIB11V-1 and an LSI-11 computer. The GPIB11V-1 allows the LSI-11 to control remotely programmable instrumentation. This GPIB system can also be configured to allow multiple processors to share common instrumentation and provide interprocessor communication (Figure 2.2b).

Figure 2.3 is a functional block diagram of the GPIB11V-1. The GPIB11V-1 interface to the LSI-11 Q-Bus consists of 14 devices registers: Interrupt Status Register (ISR), Interrupt Mask Register (IMR), Command Status Register (CSR), Address Status Register (ASR), Address Mode Register (AMR), Auxiliary Command Register (ACR), Address Switch Register (ASWR), Address Register (ADR), Serial Poll Register (SPR), Command Pass Through Register (CPTR), Parallel Poll Register (PPR), Data In Register (DIR), Data Out Register (DOR), Controller Status Register (CTSR), and Controller Command Register (CCR). These registers are described in detail in Section 4.1 of this manual. The Q-Bus Interface circuitry provides buffering and Q-Bus address decoding for the GPIB11V-1. The Interrupt Control circuitry handles interrupt transactions of the Q-Bus. The GPIB Control logic provides the GPIB11V-1 with the capability of being a GPIB Controller. The GPIB Interface logic provides the remaining GPIB interface functions. Signals are buffered to and from the GPIB via the GPIB Tranceivers. The GPIB Address logic provides selectable GPIB Listen and Talk addresses.

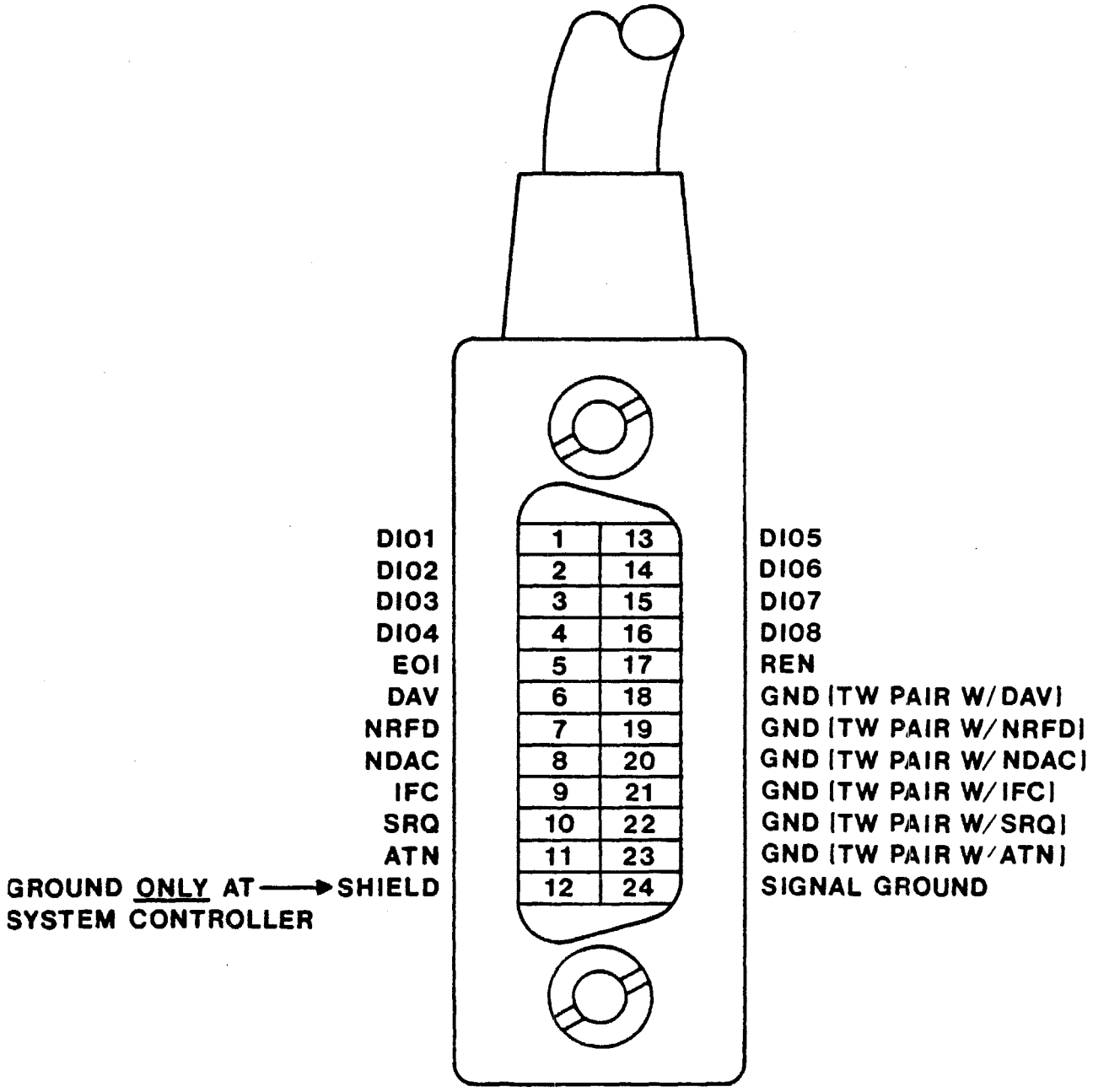


FIGURE 2.1

PIN CONNECTIONS FOR GPIB CABLE

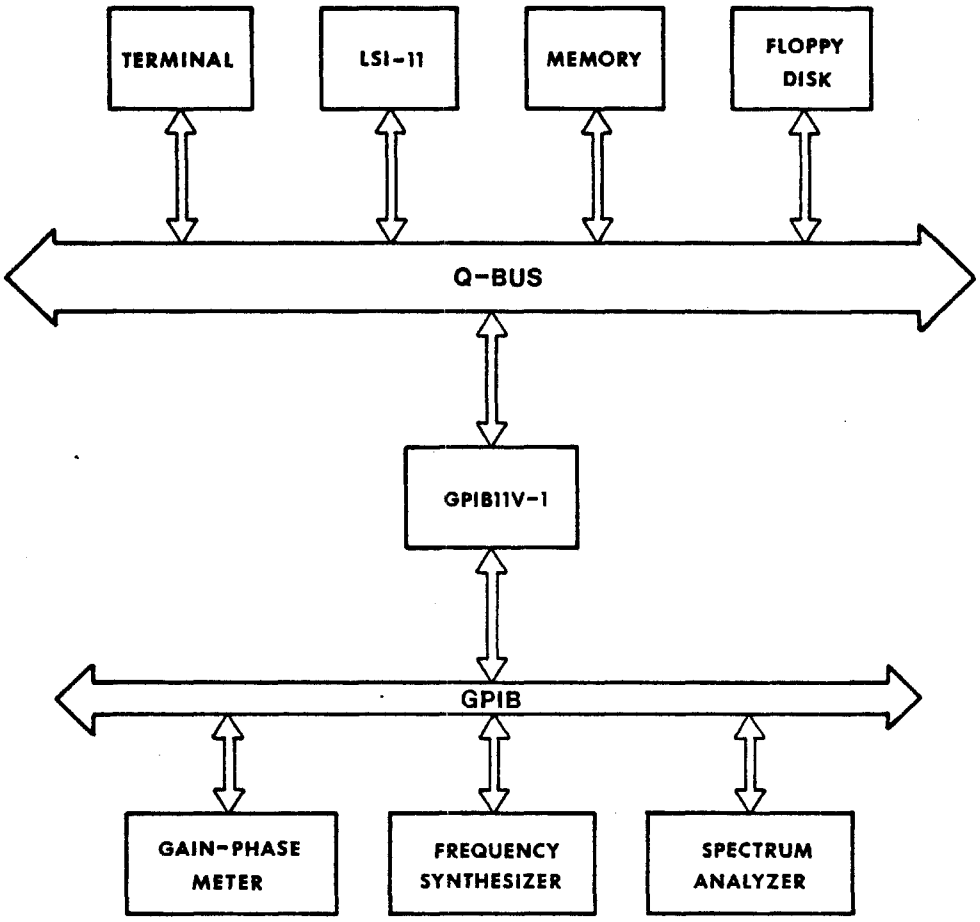


FIGURE 2.2A

IMPLEMENTATION OF A GPIB11V-1 SYSTEM

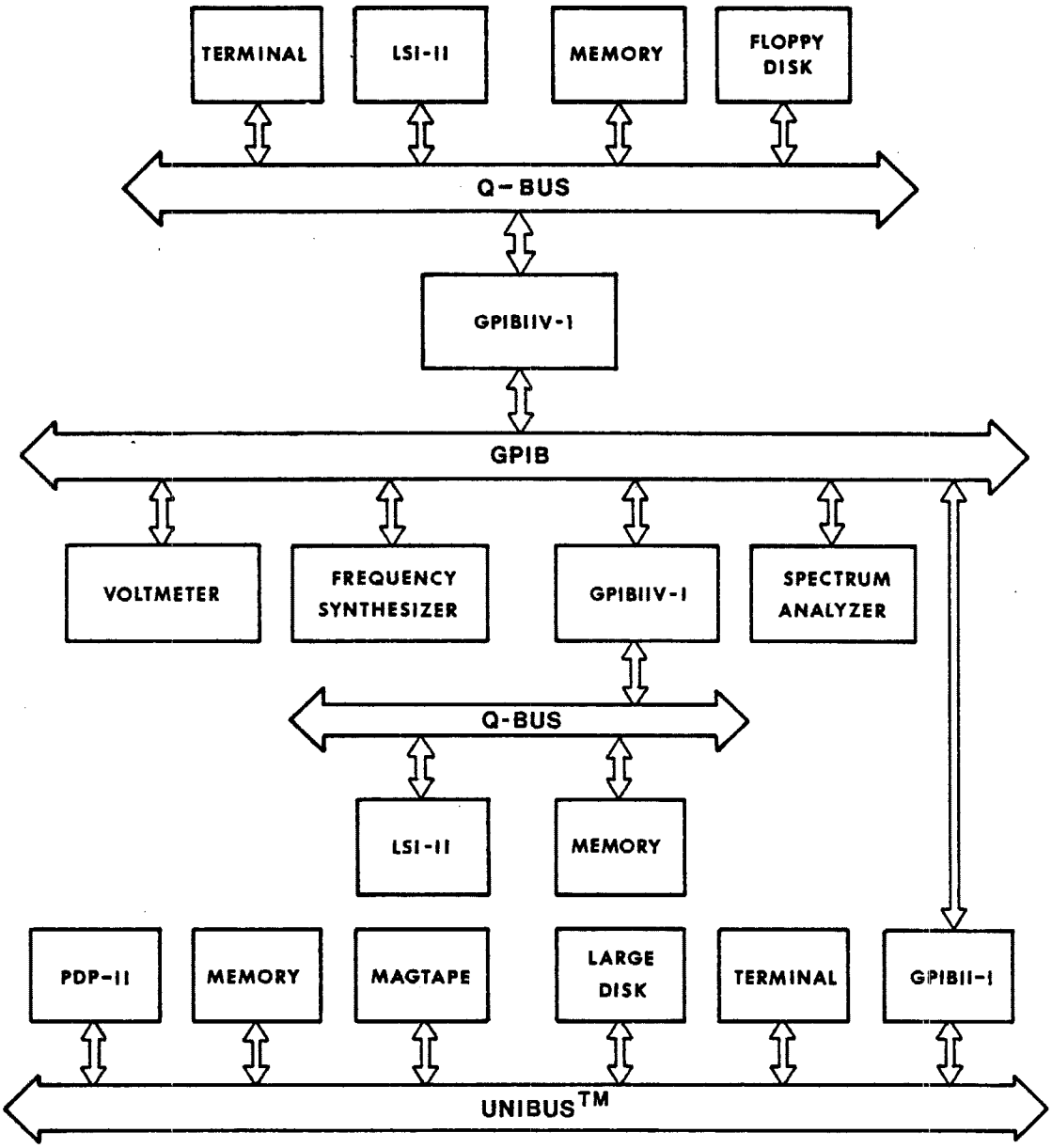


FIGURE 2.2B

A MULTI-CONTROLLER SYSTEM

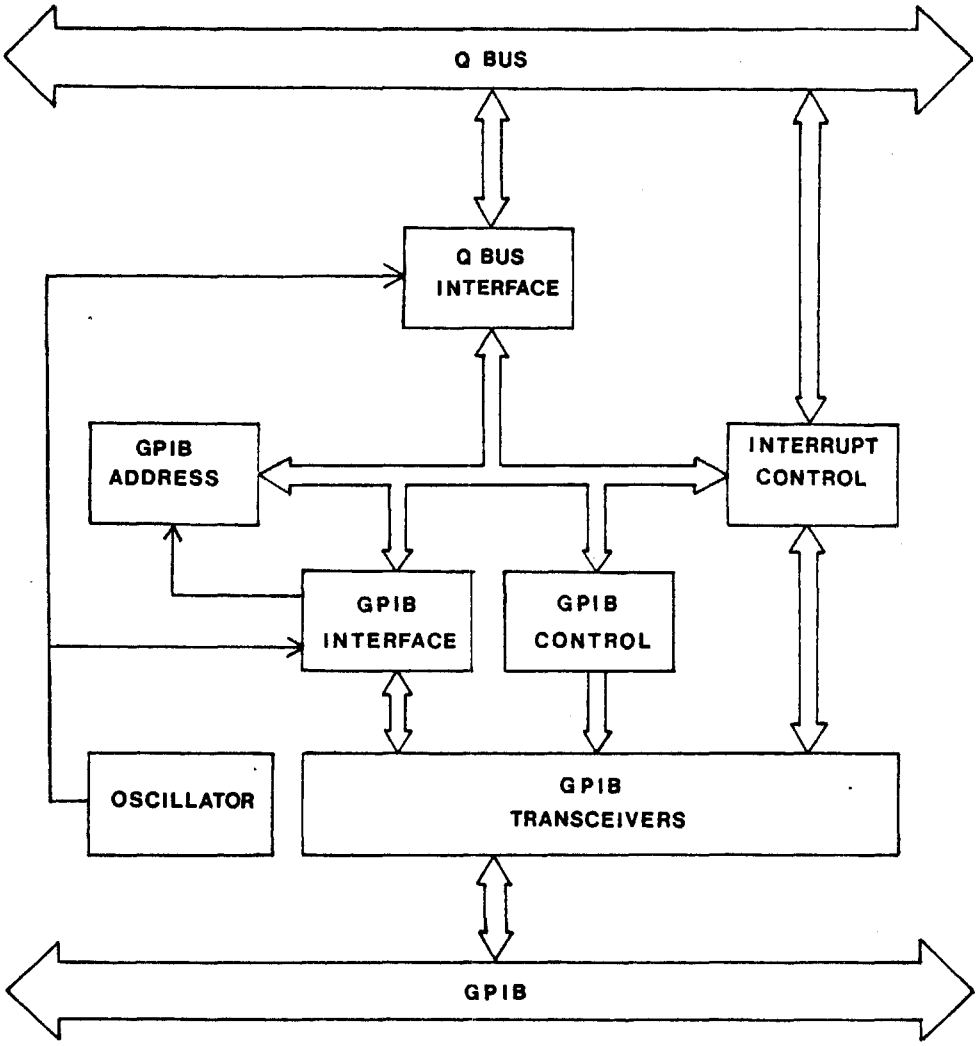


FIGURE 2.3

FUNCTIONAL BLOCK DIAGRAM OF GPIB11V-1

The Interrupt Control logic will selectively interrupt the LSI-11 when the appropriate enable bits are set and:

1. The GPIB11V-1 is the Talker and is ready to send another data byte, or the GPIB11V-1 is the Active Controller and is ready to send another command message;

2. The GPIB11V-1 is a Listener and a byte has been received from a Talker;

3. The GPIB11V-1 is the Active Controller and an instrument on the GPIB is requesting service;

4. The GPIB11V-1 is a Listener and an end-of-data message is received with a data byte;

5. The GPIB11V-1 is monitoring another controller and receives a command message;

6. The GPIB11V-1 receives a Secondary Address command message;

7. The GPIB11V-1 receives a Group Execute Trigger command message (GET);

8. The GPIB11V-1 is not the System Controller and the interface receives the Interface Clear command message (IFC).

The GPIB11V-1 can be configured by the Controller to respond to a Parallel Poll. Hardware decoding of the appropriate bus messages allows the Parallel Poll response to be transparent to the software.

2.3.2 GPIB Functions Implemented by the GPIB11V-1

Table 2.1 lists the capabilities of the GPIB11V-1 in terms of the codes in Appendix C of IEEE Std 488-1978.

TABLE 2.1

GPIB11V-1 INTERFACE CAPABILITIES

Capability Code	Interface Function
SH1	Source Handshake
AH1	Acceptor Handshake
TS, TES	Talker, Extended Talker
L3, LEZ	Listener, Extended Listener
SR1	Service Request
RL1	Remote Local
PP1	Parallel Poll
DC1	Device Clear
DT1	Device Trigger
C1, C2, C3, C4, C9	Controller

The GPIB11V-1 has complete Source and Acceptor Handshake capability. The GPIB11V-1 can operate as a basic Talker or Extended Talker and can respond to a Serial Poll. It can be placed in a talk only mode and will be

unaddressed if it received its Listen address. The interface can operate as a basic Listener or Extended Listener. It can be placed in a listen only mode and will be unaddressed as a listener when it received its Talk address. The GPIB11V-1 has full capabilities for requesting service from another Controller. The ability to place the GPIB11V-1 in local mode is unused. Parallel Poll capability required software assistance to configure. Device Clear and Trigger capability is included but unused. All Controller functions as specified by the IEEE Std 488-1978 are included in the GPIB11V-1. These include the capability to:

1. Be System Controller
2. Initialize the interface
3. Send Remote Enable
4. Respond to Service Request
5. Send multiline command messages
6. Receive control
7. Pass control
8. Conduct a Parallel Poll
9. Take control synchronously or asynchronously.

CHAPTER 3

GPIB11V-1 INSTALLATION AND CONFIGURATION

3.1 INTRODUCTION

This chapter describes the physical components which constitute the methods of configuring and connecting the GPIB11V-1 to other devices. The chapter is divided into three sections: Configuration, Installation, and Cabling.

3.2 CONFIGURATION

Each GPIB11V-1 basically consists of a dual-height printed wire board and an associated cable(s). Before installing the GPIB11V-1, the user must set the following switch-selectable options on the card:

1. Q-Bus address
2. Q-Bus interrupt vector
3. GPIB address
4. System Active Controller
5. GPIB Extended or Normal Addressing

The locations of the switches and user-selectable options are show in Figures 3.1, 3.2, and 3.3.

3.2.1 LSI-11 Q-Bus Address

Each GPIB11V-1 has a unique Q-Bus address, determined by the position of the switch located at U9. The "off" position selects a logic 1 for the corresponding address bit. Starting addresses from 760000 to 777760 can be selected. (See Figure 3.2.)

3.2.2 LSI-11 Q-Bus Interrupt Vector

Each GPIB11V-1 has a unique Q-Bus Interrupt Vector which is determined by the position of the switches located at U18. The "off" position selects a logic 1 for the corresponding vector bit. Vectors from 000 to 774 can be selected; however, it is recommended that the vector be selected according to the Priority Ranking for Floating Vectors found in the LSI-11 Peripherals Handbook. (See Figure 3.2.)

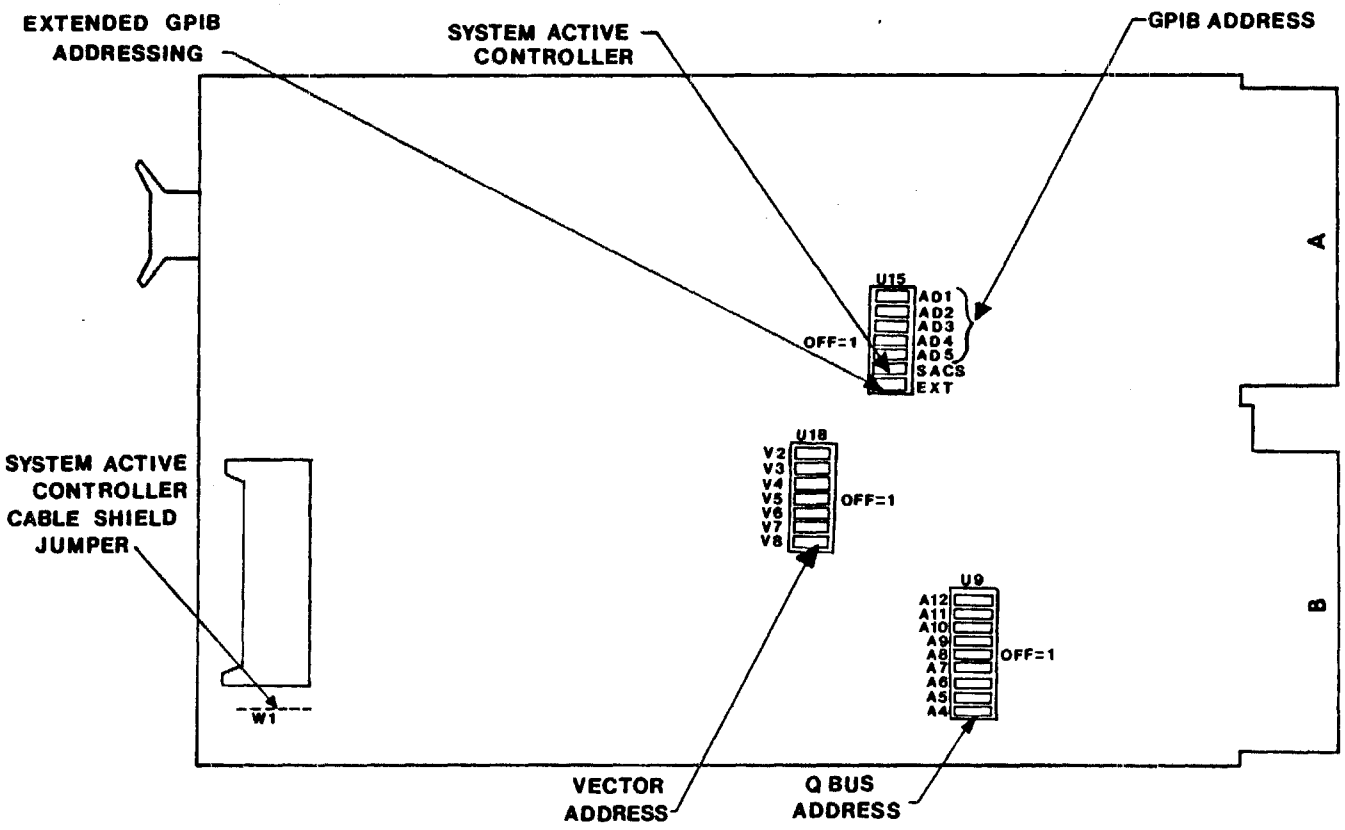


FIGURE 3.1

LOCATION OF SWITCHES AND USER SELECTED OPTIONS

1. ENTER THE Q-BUS AND INTERRUPT VECTOR ADDRESSES TO BE USED WITH THE GPIB11V-1 IN THE TABLES BELOW. NOTICE THAT SOME BITS ARE PRESET.
2. IF THE ADDRESSES ARE ENTERED IN OCTAL, CONVERT TO BINARY ON THE ADJACENT LINE.
3. FOR EACH BIT (A12-A4, V8-V2) FIND THE CORRESPONDING SWITCH. IF THE BIT IS:

   0, SET THE SWITCH ON (CLOSED)

   1, SET THE SWITCH OFF (OPEN)

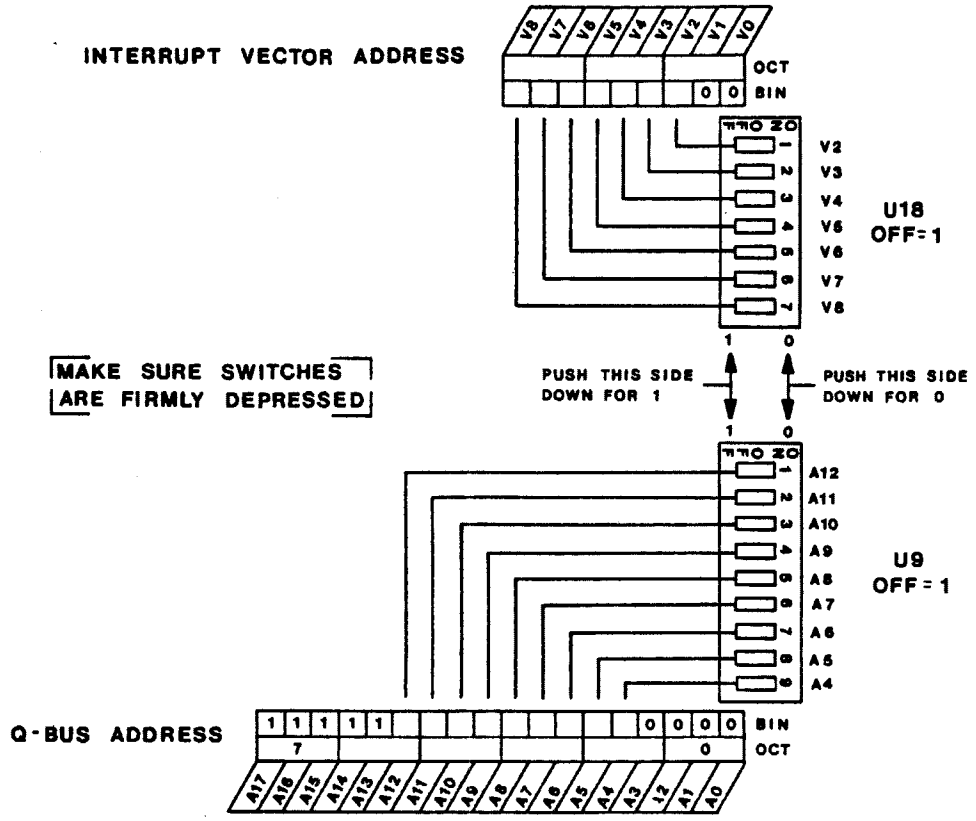


FIGURE 3.2

SETTING THE GPIB11V-1 Q-BUS AND INTERRUPT VECTOR ADDRESSES

3.2.3 GPIB Extended or Normal Addressing

Normal GPIB addresses consist of one byte and allow 31 addresses for instruments on the bus. In addition, however, the GPIB provides the alternative function of extended addressing using two bytes and allowing 961 independent addresses. The GPIB11V-1 user can select either mode of operation with a switch located in U15. (See Figure 3.3.)

3.2.4 GPIB Address

The GPIB11V-1 has a unique GPIB address to which it can respond for being addressed as a Listener or a Talker. This address is selected by the switches in U15. When in the "off" position, each switch selects a logic 1 for the corresponding address bit. As implemented on the GPIB11V-1, the secondary address (used only when Extended Addressing is selected) is determined by the LSI-11 program. (See Figure 3.3.)

3.2.5 System Active Controller

The GPIB11V-1 can be configured as the GPIB System Active Controller by setting the U15 SACS switch to the "off" position. Being configured as System Active Controller allows the GPIB11V-1 to send the Interface Clear (IFC) and Remote Enable (REN) uniline commands. If the GPIB11V-1 is configured as System Active Controller, the shield of the GPIB cable must be connected to the circuit card ground. This is accomplished by insertion of a wire jumper near the right-angle header. If the GPIB11V-1 is not System Active Controller, the jumper should be removed. (See Figure 3.3.)

3.2.6 Q-BUS Interrupt Priority

The GPIB11V-1 interrupts only at level BIRQ4 and operates only as a position-dependent or position-defined interrupt arbitration device as described in Chapter 12 (LSI-11 Bus) of the DEC Microcomputers and Memories handbook. On LSI-11/23 processors which support 4-level interrupts, the GPIB11V-1 must be placed <u>electrically</u> past all position-independent (distributed arbitration) devices and past all higher level position-dependent devices. Bear in mind that the physical and electrical positions of device slots on Q-Bus backplanes can differ considerably.

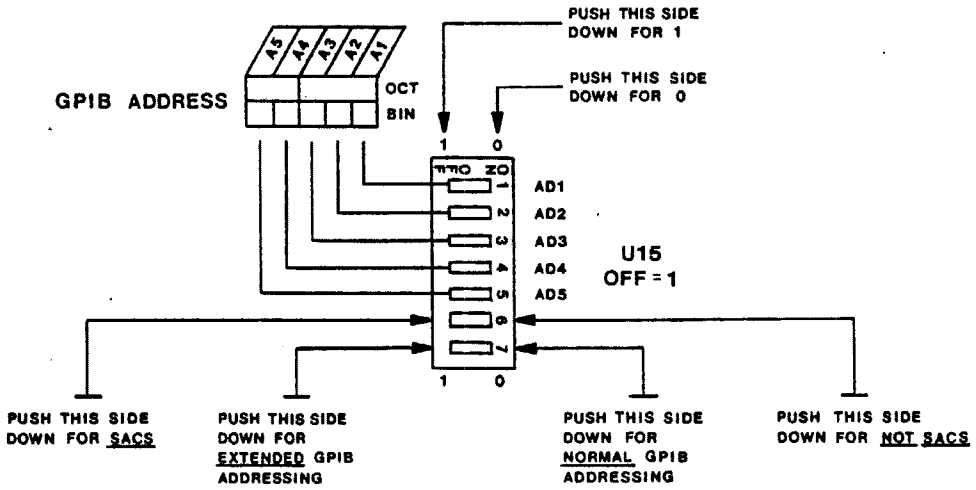
3.3 INSTALLATION

The GPIB11V-1 can be mounted in any LSI-11 device slot except as noted in Section 3.2.6 above. Power connections to the GPIB11V-1 are provided by the associated LSI-11 system power supply or an expansion chassis power supply. A listing of all signal names used by the GPIB11V-1 from the Q-Bus and their associated pin numbers is shown in Table 3.1.

1. ENTER THE GPIB ADDRESS TO BE USED WITH THE GPIB11V-1 IN THE TABLE BELOW.
2. IF THE ADDRESS IS ENTERED IN OCTAL, CONVERT TO BINARY ON THE LINE BELOW.
3. FOR EACH BIT (A5-A1), FIND THE CORRESPONDING SWITCH. IF THE BIT IS:

   0, SET THE SWITCH ON (CLOSED)

   1, SET THE SWITCH OFF (OPEN)



MAKE SURE SWITCHES ARE FIRMLY DEPRESSED

FIGURE 3.3

SETTING THE GPIB11V-1 GPIB ADDRESS, ADDRESS MODE, AND SYSTEM ACTIVE CONTROLLER OPTIONS

TABLE 3.1 - GPIB11V-1 Q-Bus Pin Assignments

Signal Name	Q-Bus Pin # (row:pin:side)	Signal Name	Q-Bus Pin # (row:pin:side)
BDALØ L	AU2	BIRQ L	AL2
BDAL1 L	AV2		
BDAL2 L	BE2	BDOUT L	AE2
BDAL3 L	BF2	BRPLY L	AF2
BDAL4 L	BH2	BDIN L	AH2
BDAL5 L	BJ2	BSYNC L	AJ2
BDAL6 L	BK2	BWTBT L	AK2
BDAL7 L	BL2		
BDAL8 L	BM2	BINIT L	AT2
BDAL9 L	BN2		
BDAL1Ø L	BP2	+5 VDC	AA2
BDAL11 L	BR2		
BDAL12 L	BS2		
BDAL13 L	BT2		
BDAL14 L	BU2		
BDAL15 L	BV2	GND	AT1
BBS7 L	AP2		BM1
BDMGI L	AR2		
BDMGO L	AS2		
BIAKI L	AM2		
BIAKO L	AN2		

3.4 CABLING

A cable is supplied with the GPIB11V-1. The 26-pin Berg minilatch connector is connected to the shielded right-angle header mounted on the GPIB11V-1 circuit board. The piggy-back connector end is connected to another device on the GPIB. Other devices may be connected to another device on the GPIB. Other devices may be connected to the GPIB by using the bus cables listed in Table 1.2.

CHAPTER 4

PROGRAMMING INFORMATION

4.1 SCOPE

This section describes general programming concepts for software control of the GPIB11V-1. It is beyond the scope of this manual to provide program examples. For more information about the software package supplied with the kit, refer to the GPIB11V-1 Software Reference Manual.

4.2 DEVICE REGISTERS

All software control of the GPIB11V-1 is performed by means of fourteen device registers. These registers are assigned consecutive addresses and can be read or written using any LSI-11 instruction which refers to their addresses. Table 4.1 lists the device registers and typical address assignments.

In the following descriptions the word "transmit" refers to those registers and bits involved in sending data from the LSI-11 to the GPIB. The word "receive" refers to those register and bits involved in receiving data from the GPIB for transfer to the LSI-11. The unused and write only (WO) bits are undefined when read. Writing to unused or read only (RO) bits has no effect. The mnemonic INIT refers to the initialization signal sent by the LSI-11 processor during a RESET instruction.

For the purposes of the following bit descriptions, true, set, one, high, and on, are synonymous, as are false, clear, zero, low, and off.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CTSR – Read 767701	XATN	XREN	XIDY	XIFC	MASTER IE	SRQ IE	IFC	–	INT	BO	GET	–	APT	CMD	END	BI	Read – ISR 767700
Write	–	–	–	–	–	–	–	–	INT IE	BO IE	GET IE	–	APT IE	CMD IE	END IE	BI IE	Write – IMR
CTSR – Read 767703	XATN	XREN	XIDY	XIFC	MASTER IE	SRQ IE	IFC	–	UACG	REM	LOK	–	RLC	SPAS	DCAS	UUCG	Read – CSR 767702
Write	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	Write
CTSR – Read 767705	XATN	XREN	XIDY	XIFC	MASTER IE	SRQ IE	IFC	–	ms	to	lo	ATN	TACS	LACS	LPAS	TPAS	Read – ASR 767704
Write	–	–	–	–	–	–	–	–	del	to	lo	–	hlde	hlds	–	apte	Write – AMR
CTSR – Read 767707	XATN	XREN	XIDY	XIFC	MASTER IE	SRQ IE	IFC	–	reset	DAC	$\overline{DAV}$	RFD	msa	rtl	ulpa	fget	Read – ACR 767706
Write	–	–	–	–	–	–	–	–		rfdr	feoi	dscr			dacd		Write – ACR
CTSR – Read 767711	XATN	XREN	XIDY	XIFC	MASTER IE	SRQ IE	IFC	–	SRQ	EXT	SACS	AD5	AD4	AD3	AD2	AD1	Read – ASWR 767710
Write	–	–	–	–	–	–	–	–	lsbe	del	dat	AD5	AD4	AD3	AD2	AD1	Write – ADR
CTSR – Read 767713	XATN	XREN	XIDY	XIFC	MASTER IE	SRQ IE	IFC	–	S8	SROS	S6	S5	S4	S3	S2	S1	Read – SPR 767712
Write	–	–	–	–	–	–	–	–		rsv							Write – SPR
CTSR – Read 767715	XATN	XREN	XIDY	XIFC	MASTER IE	SRQ IE	IFC	–	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	Read – CPTR 767714
CCR – Write	XATN	XREN	XIDY	XIFC	MASTER IE	SRQ IE	–	–	PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1	Write – PPR
CTSR – Read 767717	XATN	XREN	XIDY	XIFC	MASTER IE	SRQ IE	IFC	–	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	Read – DIR 767716
Write	–	–	–	–	–	–	–	–	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	Write – DOR

–: undefined/not used (read/write)

TABLE 4.1

TYPICAL GPIB11V-1 DEVICE REGISTER ASSIGNMENTS

INTERRUPT STATUS REGISTER (ISR) Read Only

Address: 111 11X XXX XXX XX0 000

X: user selectable

Typical address: 767700

7	6	5	4	3	2	1	0
INT	BO	GET	-	APT	CMD	END	BI

Bit 0: BI When set indicates a byte from the GPIB has been read and is available to the LSI-11 program in the DIR. Cleared when the LSI-11 program reads the DIR. Cleared by INIT and reset.

Bit 1: END When set indicates a data byte has been read from the GPIB with the EOI line in a true state (signifying end-of-data). Cleared when data is read from DIR. Cleared by INIT and reset.

Bit 2: CMD This bit is the logical "or" of several conditions -

1) The state of the Remote Enable line has changed,
2) The GPIB11V-1 is being serially polled and is in the serial poll active state (SPAS),
3) dsel is off and an unrecognized universal command group (UCG) or addressed command group (ACG) message has been received, or the GPIB11V-1 is in the device clear active state (DCAS) having received the device clear (DCL) message or the selected device clear (SDC) message.

The command status register can be checked to determine which condition actually caused the interrupt. The CPTR can be read to interpret the UCG or ACG message and dacr set to allow the handshake to complete.

Bit 3: APT When set, this bit indicates a secondary address is available for examination by the user program in the DIR. For this to happen, Bit 0 of the AMR must have been set, the GPIB11V-1's primary address must have been received, and a Secondary Command Group message (containing the secondary address) must have been received, in that order. A typical response for a valid secondary address would be to set Bit 3 of ACR (msa) and Bit 4 of ACR (dacr), releasing the GPIB DAC handshake. Cleared when byte is read from DIR. Cleared by INIT and reset.

Bit 4: Not Used

Bit 5: GET When set, indicates a Group Execute Trigger command message has been received from the GPIB Active Controller. Cleared by INIT and reset.

Bit 6: BO — When set, indicates that the DOR is empty and the GPIB11V-1 is the talker or controller. Cleared by writing a byte to DOR or if the GPIB11V-1 is unaddressed to talk.

Bit 7: INT — This bit is the logical "or" of all other bits in the ISR logically "anded" with the respective bits in the interrupt mask register.

INTERRUPT MASK REGISTER (IMR) Write Only

Address: 111 11X XXX XXX XX0 000

X: user selectable

Typical address: 767700

7	6	5	4	3	2	1	0
INT IE	BO IE	GET IE	-	APT IE	CMD IE	END IE	BI IE

The Interrupt Mask Register is a seven bit storage register used to select the particular events that will cause an interrupt.

Bit 0: BI IE When set by the LSI-11 program, this bit will allow interrupts on each data byte read from the GPIB. Set and cleared by LSI-11 program. Cleared by INT and reset.

Bit 1: END IE When set by the LSI-11 program, this bit will allow interrupts when the end-of-data message is received with a data byte. Set and cleared by LSI-11 program. Cleared by INIT and reset.

Bit 2: CMD IE When set by the LSI-11 program, this bit will allow interrupts when the GPIB11V-1 is being serially polled, when the Remote Enable line changes state, when the device message (DCL) or selected device clear message (SCD) is received, or when an unrecognized command is received.

Bit 3: APT IE When set by the LSI-11 program, this bit allows an interrupt to occur, indicating that a secondary address is available in the DIR (if Bit 0 of the AMR is set, listener or talker primary address is received, and a Secondary Command Group message is received). A typical response for a valid secondary address would be for the user to set msa (Bit 3 of the ACR) and dacr (Bit 4 of the ACT), releasing the DAC handshake. Set and cleared by the LSI-11 program. Cleared by INIT and reset.

Bit 4: Not Used

Bit 5: GET IE When set by the LSI-11 program, this will allow an interrupt to occur if a Group Execute Trigger command message has been received. Cleared and set by LSI-11 program. Cleared by INIT and reset.

Bit 6: BO IE When set by the LSI-11 program, this bit will allow an interrupt whenever the data out register (DOR) is empty. Cleared and set by the LSI-11 program. Cleared by INIT and reset.

Bit 7: INT IE When set by the LSI-11 program, this bit will allow an interrupt condition (from bits 0-6 of the IMR and ISR) to be passed to the LSI-11 bus. Cleared and set by LSI-11 program. Cleared by INIT and reset.

COMMAND STATUS REGISTER (CSR) Read Only

Address: 111 11X XXX XXX XX0 010

X: user selectable

Typical address: 767702

7	6	5	4	3	2	1	0
UACG	REM	LOK	-	RLC	SPAS	DCAS	UUCG

Bit 0: UUCG When set, indicates that an unrecognized universal command has been received. Cleared by INIT and reset.

Bit 1: DCAS When set, indicates that the Device Clear (DCL) or Selected Device Clear (SDC) command message has been received, activating the device clear function. Cleared by INIT and reset.

Bit 2: SPAS When set, indicates that the Serial Poll Enable (SPE) command message has been received, activating the device serial poll function. Cleared by INIT and reset.

Bit 3: RLC When set, indicates that there has been a change of level of the Remote Enable line, indicating a change from remote to local mode, or local to remote mode. Cleared when the CSR is read and by INIT and reset.

Bit 4: Not Used

Bit 5: LOK When set, indicates that the Local Lockout (LLO) command message has been received. Cleared by INIT and reset.

Bit 6: REM Follows the state of the GPIB Remote Enable line.

Bit 7: UACG When set, indicates that an unrecognized address command has been received. Cleared by INIT and reset.

ADDRESS STATUS REGISTER (ASR) Read Only

Address: 111 11X XXX XXX XX0 100

X: user selectable

Typical address: 767704

7	6	5	4	3	2	1	0
ma	to	lo	ATN	TACS	LACS	LPAS	TPAS

The Address Status Register indicates the addressed state of the listener/talker functions of the GPIB11V-1 as well as flags that specify whether the interface is in the talk only or listen only mode.

Bit 0: TPAS When set, indicates that the GPIB11V-1 is in the Talker Primary Addressed State (i.e., addressed as a Talker, but not yet an active one). Cleared by INIT and reset.

Bit 1: LPAS When set, indicates that the GPIB11V-1 is in the Listener Primary Addressed State. Cleared by INIT and reset.

Bit 2: LACS When set, indicates that the GPIB11V-1 is in the Listener Active State. Cleared by INIT and reset.

Bit 3: TACS When set, indicates that the GPIB11V-1 is in the Talker Active State. Cleared by INIT and reset.

Bit 4: ATN When set, indicates the GPIB ATN command is asserted by the Active Controller (if the Active Controller is not the GPIB11V-1). Follows the state of the GPIB ATN line.

Bit 5: lo When set, indicates the GPIB11V-1 is in the listen-only mode of operation. Indicates state of Bit 5 of AMR. Cleared by INIT and reset.

Bit 6: to When set, indicates the GPIB11V-1 is in the talk-only mode of operation. Indicates state of Bit 6 of AMR. Cleared by INIT and reset.

Bit 7: ma When set, indicates that the GPIB11V-1's address has been received and the interface is in one of the following states:

TACS - Talker Active State
TADS - Talker Addressed State
LACS - Listener Active State
LADS - Listener Addressed State
SPAS - Serial Poll Active State

ADDRESS MODE REGISTER (AMR) Write Only

Address: 111 11X XXX XXX XX0 100

X: user selectable

Typical address: 767704

7	6	5	4	3	2	1	0
dsel	to	lo	-	hlde	hlda	-	apte

Bit 0: apte When set, GPIB extended addressing is enabled. See Bit 3 of ISR. Cleared by INIT and reset.

Bit 1: Not Used

Bit 2: hlda When set by the LSI-11 program this bit will cause the GPIB11V-1 to hold off sending RFD after a GPIB handshake (on a data transfer) until the program sets rfdr (Bit 6 of ACR). Cleared and set by program. Cleared by INIT and reset.

Bit 3: hlda When set by the LSI-11 program this bit will cause the GPIB11V-1 to hold off sending RFD after a GPIB handshake (on a data transfer with EOI true) until the program sets rfdr (Bit 6 of ACR). Set and cleared by program. Cleared by INIT and reset.

Bit 4: Not Used

Bit 5: lo When set by the LSI-11 program this bit sets the GPIB11V-1 to listener-only mode of operation. Only one of to or lo may be set simultaneously. Set and cleared by program. Cleared by INIT and reset.

Bit 6: to When set by the LSI-11 program this bit sets the GPIB11V-1 to talk-only mode of operation. Only one of to or lo may be set simultaneously. Set and cleared by program. Cleared by INIT and reset.

Bit 7: dsel When set by the LSI-11 program this bit will configure the GPIB11V-1 for automatic completion of the GPIB handshake sequence on occurrance of the GET, UACG, UUCG, SDC, or DCL commands (see ISR for GET and CSR for UACG, UUCG, SDC and DCL). Set and cleared by program. Cleared by INIT and reset.

AUXILIARY COMMAND REGISTER (ACR) Read/Write

Address: 111 11X XXX XXX XX0 110

X: user selectable

Typical address: 767706

7	6	5	4	3	2	1	0	
reset	rfdr DAC	feoi DAV	dacr RFD	msa	rtl	dacd ulps	fget	Write Read

Bit 0: fget (r/w) This bit, when set by the LSI-11 program, forces the GPIB11V-1 to execute a simulated GET (Group Execute Trigger), just as if the GET message had been received from a controller. Set and cleared by program. Cleared by INIT and reset.

Bit 1: dacd (w) The "data accept disable" bit, when set by the LSI-11 program, will prevent automatic GPIB handshake on all Command Messages. The acceptor handshake will be held in Accept Data State (ACDS) until the program releases it by writing a 1 into dacr (Bit 4 of ACR). Set and cleared by program. Cleared by INIT and reset.

ulpa (r) This bit indicates the state of the least significant bit of the last primary address received. See lsbe (Bit 7 of ADR). Cleared by INIT and reset.

Bit 2: rtl (r/w) The "return to local" bit, when set by the program, forces the GPIB11V-1 into local mode (if the Local Lockout Command has not been received). Cleared by INIT and reset.

Bit 3: msa (r/w) The "my secondary address" bit should be set by the program when a valid secondary address has been received (assuming extended addressing is being used on the bus). The bit will be cleared when the GPIB11V-1 is unaddressed by the Active Controller. This bit can also be cleared by the program, reset, or INIT.

Bit 4: dacr (w) The "DAC handshake release" bit should be set by the program program after a secondary address or a command message has been examined, releasing the GPIB handshake by allowing the DAC line to go passively true. This is a set-only bit which is cleared automatically by the GPIB11V-1.

RFD (r) This bit corresponds to the GPIB RFD (Ready for Data) message. It is a 1 when all devices on the bus are ready to receive data and 0 otherwise.

Bit 5: feoi (w) The "force end or identify" bit when set by the program, forces the GPIB11V-1 to send the End-of-Data Message (EOI line true) with the next data byte transmitted. The EOI line will be cleared to a passive false state automatically after

the data byte has been sent. This bit is set-only and is automatically cleared by the GPIB11V-1. If this bit is set when the GPIB11V-1 is not in TACS, it will be ignored by the interface.

$\overline{\text{DAV}}$ (r) This bit follows the inverted value of the GPIB DAV (Data Valid) Message. When a 0, it means data on the bus is valid. When a 1, data is not valid.

Bit 6: rfdr (w) The "release RFD handshake", when set by the program, allows the GPIB handshake that was stopped by RFD (Ready for Data) holdoff commands hlda and hlde (Bits 2 and and 3 of AMR). This bit is set-only and is automatically cleared by the GPIB11V-1. If set when not in either RFD holdoff mode, it is ignored by the interface.

DAC (r) This bit follows the state of the GPIB DAC (Data Accepted) Message. When a 1, it indicates that all devices on the bus have accepted the last data or command byte, otherwise the bit will read as a 0.

Bit 7: reset This bit, when set, indicates that the GPIB11V-1 is in a reset, or power-on, state. It is set by INIT or by the LSI-11 program. Before any operations using the GPIB11V-1 can be initiated, this bit must be cleared by the LSI-11 program. The reset bit forces the GPIB11V-1 into the following status:

1. all interrupts cleared
2. SIDS (Source Handshake Idle State)
3. AIDS (Acceptor Han.spake Idle State)
4. TIDS (Talker Idle State)
5. LIDS (Listener Idle State)
6. LOCS (Local State)
7. PPIS (Parallel Poll Idle State)
8. PUCS (Parallel Poll Unaddressed to Configure State)
9. PPO (No Parallel Poll Capability)

ADDRESS SWITCH REGISTER (ASWR) Read Only

Address: 111 11X XXX XXX XX1 000

X: user selectable

Typical address: 767710

7	6	5	4	3	2	1	0
SRQ	EXT	SACS	AD5	AD4	AD3	AD2	AD1

Bits 0-4: AD1-AD5 These bits are used to specify the five least significant bits of the GPIB address of the interface. They are selectable by a DIP switch located at U15 on the interface card.

Bit 5: SACS This bit, when set, indicates the GPIB11V-1 is configured as the System Active Controller. It is controlled by a DIP switch located at U15 on the interface card.

Bit 6: EXT This bit, when set, indicates the GPIB uses extended addressing. It is controlled by a DIP switch located at U15 on the interface card.

Bit 7: SRQ This bit follows the state of the GPIB SRQ line. It is a 1 when any device on the bus is requesting service. When set along with SRQ IE (Bit 2 of CTR) and MASTER IE (Bit 3 of CTR), an interrupt is generated.

ADDRESS REGISTER (ADR) Write Only

Address: 111 11X XXX XXX XX1 000

X: user selectable

Typical address: 767710

7	6	5	4	3	2	1	0
lsbe	dal	dat	AD5	AD4	AD3	AD2	AD1

The Address Register is an 8-bit storage register. The purpose of this register is to carry the primary address of the GPIB11V-1. Generally, the least significant 5 bits of the ASWR are read by the user program and then written into the least significant 5 bits of the ADR.

Bits 0-4 AD1-AD5 These bits hold the least significant 5 bits of the GPIB address of the interface. Cleared by INIT or program.

Bit 5: dat When set, this bit disables the Talker function of the GPIB11V-1. Cleared by INIT or program.

Bit 6: dal When set, this bit disables the Listener function of the GPIB11V-1. Cleared by INIT or program.

Bit 7: lsbe This bit, when set, is used to enable the GPIB11V-1's dual primary addressing mode. This mode allows the interface to respond to two consecutive GPIB addresses; one with AD1 equal to 0 and the other with AD1 equal to 1. For example, if the GPIB11V-1's address is set to 04 and the lsbe bit is set, the interface will respond to addresses 04 and 05. Cleared by INIT and program. (See bit 1 of ACR, ulpa).

Note: This register is not cleared by reset.

SERIAL POLL REGISTER (SPR) Read/Write

Address: 111 11X XXX XXX XX1 010

X: user selectable

Typical address: 767712

7	6	5	4	3	2	1	0	
S8	SRQS rsv	S6	S5	S4	S3	S2	S1	Read Write

The Serial Poll Register is used for establishing the status byte that the chip sends out when it is serially polled. Status is placed by the user program in Bits 0-5 and Bit 7.

Bits 0-5: S1-S6 (r/w) Status bits. Cleared and set by program. Cleared by INIT and reset.

Bit 6: SRQS (r) This bit, when set, indicates the interface is in the Service Request Status State.

rsv (w) This bit is set by the LSI-11 program to enable the GPIB11V-1 to send the SRQ message to the Active Controller. Cleared and set by program. Cleared by INIT and reset.

Bit 7: S8 (r/w) Status bit. Cleared and set by program. Cleared by INIT and reset.

COMMAND PASS THROUGH REGISTER (CPTR) Read-Only

Address: 111 11X XXX XXX XX1 100

X: user selectable

Typical address: 767714

7	6	5	4	3	2	1	0
DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01

Bits 0-7: DI01-DI08 These bits directly follow the state of the 8 GPIB data input/output lines.

PARALLEL POLL REGISTER (PPR) Read-Only

Address: 111 11X XXX XXX XX1 100

X: user selectable

Typical address: 767714

7	6	5	4	3	2	1	0
PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1

This register is loaded by the user program with the Parallel Poll response. The GPIB11V-1 will respond to a Parallel Poll by automatically writing out bits PP1-PP8 to the Controller. The GPIB11V-1, when INIT or reset is asserted, assumes the PP0 state (Parallel Poll no capability). The Parallel Poll interface function is executed by the interface using the PP2 subset (Omit Controller Configuration Capability). Full PP1 capability may be simulated with program assistance.

Bits 0-7: PP1-PP8 Parallel Poll response bits. Set and cleared by program. Cleared by INIT and reset.

DATA-IN REGISTER (DIR) Read Only

Address: 111 11X XXX XXX XX1 110

X: user selectable

Typical address: 767716

7	6	5	4	3	2	1	0
DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1

Bits 0-7: DI1-DI8 This register contains the last byte read from the GPIB using the handshake protocol. Corresponds to DI01-DI08 of GPIB.

DATA-OUT REGISTER (DOR) Write-Only

Address: 111 11X XXX XXX XX1 110

X: user selectable

Typical address: 767716

7	6	5	4	3	2	1	0
DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1

Bits 0-7: DO1-DO8 This register is used by the program when the GPIB11V-1 is Talker or Active Controller to send bytes onto the GPIB using the handshake protocol. Writing a byte into this register when BO is set (Bit 6 of ISR) will cause the interface to send the byte out to the bus. Corresponds to DIO1-DIO8 of GPIB.

CONTROLLER STATUS REGISTER (CTSR) Read Only

Address: 111 11X XXX XXX XX- --1

X: user selectable

-: don't care

Typical address: 767701, 767703, 767705, 767707, 767711, 767713, 767715, 767717 (all addresses)

(15)	(14)	(13)	(12)	(11)	(10)	(9)	(8)
7	6	5	4	3	2	1	0
XATN	XREN	XIDY	XIFC	MASTER IE	SRQ IE	IFC	-

Bit 0: Not Used

Bit 1: IFC — Follows state of GPIB IFC (Interface Clear) line. If the GPIB11V-1 is not the system controller, this bit will cause an interrupt (if Master IE is set) and remain set until cleared by the program.

Bit 2: SRQ IE — Indicates an interrupt is allowed if the GPIB11V-1 receives SRQ.

Bit 3: MASTER IE — Indicates GPIB11V-1 interrupts are enabled. No interrupts can occur if this bit is cleared.

Bit 4: XIFC — When set, indicates the GPIB11V-1 is sending the Interface Clear signal (IFC).

Bit 5: XIDY — When set, indicates the GPIB11V-1 is asserting the GPIB EOI line, sending the IDY (Identify) message during a Parallel Poll.

Bit 6: XREN — When set, indicates the GPIB11V-1 is asserting the GPIB REN line (Remote Enable).

Bit 7: XATN — When set, indicates the GPIB11V-1 is asserting the GPIB ATN line (Attention).

CONTROLLER COMMAND REGISTER (CCR) Write Only

Address: 111 11X XXX XXX XX1 101

X: user selectable

Typical address: 767715

(15) 7	(14) 6	(13) 5	(12) 4	(11) 3	(10) 2	(9) 1	(8) 0
XATN	XREN	XIDY	XIFC	MASTER IE	SRQ IE	-	-

Bit 0: Not Used

Bit 1: Not Used

Bit 2: SRQ IE — When set by program, allows SRQ to generate an interrupt. Set and cleared by program. Cleared by INIT.

Bit 3: MASTER IE — When set, allows interrupts generated by all interrupting conditions to be passed to the LSI-bus and actually request an interrupt. When cleared, no interrupts can be generated. Set and cleared by program. Cleared by INIT.

Bit 4: XIFC — When set, asserts the GPIB IFC (Interface Clear) line (legal only if the GPIB11V-1 is configured as System Active Controller). Set and cleared by program. Cleared by INIT.

Bit 5: XIDY — When set, asserts the GPIB EOI (End or Identify) line (legal only if the GPIB11V-1 is system Active Controller). Set and cleared by program. Cleared by INIT.

Bit 6: XREN — When set, asserts the GPIB REN (Remote Enable) line (legal only if the GPIB11V-1 is System Active Controller). Set and cleared by program. Cleared by INIT.

Bit 7: XATN — When set, asserts the GPIB ATN (Attention) line (legal only if the GPIB11V-1 is the Active Controller). Set and cleared by program. Cleared by INIT.

CHAPTER 5

THEORY OF OPERATION

This chapter will explain the detailed logic operation of the GPIB11V-1. Readers should refer to the functional block diagram, Figure 2.3, and the schematic diagram when reading this chapter.

5.1 Q-BUS INTERFACE

The GPIB11V-1 is connected to the LSI-11's Q-Bus by integrated circuits U4, U1, U21, U2 and U12. These are bus receivers, drivers and tranceivers which isolate the Q-Bus from the rest of the circuitry of the GPIB11V-1.

The data/address lines received by U1, U2, and U21 are sent to circuits (U5 and U17) which compare the user selected address in U9 with the address present on the Q-Bus. When addressed, the GPIB11V-1 then decodes the Q-Bus command lines, BDIN, BDOUT, BWTBT into signals which are used by the rest of the circuitry. These include IN, BUS RD EN, BUS IN EN, WB LOW and WB HI, which are generated by U8 (8), U23 (6), U23 (8), U22 (3), and U28 (1), respectively. The BUS IN EN signal is true when: 1) data is to be enabled from the GPIB11V-1 onto the Q-Bus (i.e., BUS RD EN is true); 2) when the GPIB11V-1 is enabling its interrupt vector onto the Q-Bus data/address lines.

When IN is true, it signifies data is to be enabled onto the LSI-11 Q-Bus. The BUS RD EN signal is true whenever data is being read from the GPIB11V-1 (i.e., IN is true), or from the GPIB Address switches (ASE is true).

WB LOW and WB HI are true when data is being transferred from the Q-Bus to the GPIB11V-1. WB LOW is true if the low-order byte (bits 0-7) are being written, and WB HI is true if the high-order byte (bits 8-15) are being written. Both signals can be true simultaneously.

Latch U6 is used to store the low-order word address bits for decoding into 8 unique word addresses by U27 and U30. U7 and U10 are used to interface data bytes to and from the GPIB interface logic, U30. Chips U24, U31 and parts of U16 and U28, along with discrete components C1, CR1, and R5 provide the control interface between the asynchronous Q-Bus and the synchronous nature of U30. Signals generated include RD CS and WR CS, which are used to select U30, and RPLY WRT and RPLY RD DLY, which are used to continue Q-Bus operation.

5.2 GPIB ADDRESS

Integrated circuits U11 and U14 are used to select 1) the interrupt vector or, 2) the card's GPIB address for transfer to the Q-Bus data/address lines. Dip switch U15 allows selection of the GPIB11V-1's primary GPIB Listen and Talk address (low order 5 bits), and dip switch U18 allows selection of

the GPIB11V-1's interrupt vector. U15 also includes two additional switches, one of which is used to specify that the GPIB11V-1 is the System Active Controller (SACS). The other switch is used to signal the user program which GPIB addressing mode is to be used, NORMAL or EXTENDED.

5.3 GPIB INTERFACE

Most of the card's GPIB maintenance and interfacing is done with a 40 pin Large Scale Integrated Circuit, U30. Because this integrated circuit is synchronous in nature, an oscillator is used to provide a synchronous clock which controls Q-Bus access and operation of U30 (part of U40 and parts of U33, along with discrete components C2, R6 and R7).

5.4 GPIB CONTROL

Integrated circuit U25 is used to store the signals used to control the GPIB when the GPIB11V-1 is the Active Controller. These signals include XATN, which will cause the GPIB11V-1 to transmit the GPIB ATN signal; XREN, which will cause the GPIB11V-1 to transmit the GPIB REN signal (only, however, if the GPIB11V-1 is configured as the System Active Controller); XIDY, which will transmit the GPIB EOI (identify) signal; and XIFC, which is used to transmit the GPIB IFC signal (again, only if configured as the System Active Controller). Circuit U32 buffers these signals to the GPIB Tranceivers.

5.5 GPIB TRANCEIVERS

All signals to and from the GPIB are buffered using IEEE Std 488 compatible open collector output bus tranceivers.

5.6 INTERRUPT CONTROL

Three internal signals on the GPIB11V-1 are used to request interrupts. They include IRQ from U30, which can become true for a variety of reasons (see description of Interrupt Status Register in Chapter 4 of this manual); SRQ INT, which is true if a device on the GPIB is requesting service and the SRQ IE (Service Request Interrupt Enable bit is set); and LATCHED IFC, which is true if a GPIB System Controller (not the GPIB11V-1) sends IFC (Interface Clear). LATCHED IFC must be cleared by the LSI-11 program.

If any of these three conditions are true the Q-Bus interrupt request line (BIRQ) will be asserted. Interrupt handshaking is done by chips U20, U12 and a part of U16. Interrupt acknowledge signals (BIAKI) are processed by the GPIB11V-1 before being allowed to continue on to other devices on the Q-Bus (BIAKO). If the GPIB11V-1 is requesting an interrupt at the time it receives the BIAKI signal from the Q-Bus, it inhibits asserting the BIAKO signal and asserts its interrupt vector onto the Q-Bus data/address lines.

CHAPTER 6

PARTS LIST

This section contains a list of parts for the the GPIB11V-1.

ITEM NO	QTY REQD	MFR FSCM NO	PART/DWG STOCK NO	DESCRIPTION REFERENCE DESIGNATION
1	1	NI	178008-01	PRINTED WIRE BOARD, GPIB11V-1
		7U296	178008-01	
2	REF	NI	178006-01	SCHEMATIC DIAGRAM, Q-BUS TO GPIB INTFC
		7U296	178006-01	
3	28	CLB	UK50-103	CAPACITOR, RDL LEAD, 50 V, 20%, .01 UF
		71950	715003-01	
4	1	KMT	T322D106M035AS	CAPACITOR, AXIAL LEAD, 35 V, 20%, 10 UF
			715002-01	
5	1	SAN	D7-1-C-471-J-0	CAPACITOR, RDL LEAD, 100 V, 5%, 470 PF
		00853	715006-01	C1
6	1	SAN	D7-1-C-821-J-0	CAPACITOR, RDL LEAD, 100 V, 5%, 820 PF
		00853	715008-01	C2
7	1	GE	1N4148	DIODE, SILICON, SWITCHING
		15413	730001-01	CR1
8	2	-	RC07GF391J	RESISTOR, 1/4 W, 5%, 390 OHM
		71785	711008-01	R1, 4
9	3	-	RC07GF181J	RESISTOR, 1/4 W, 5%, 180 OHM
		71785	711006-01	R2, 3, 6
10	2	-	RC07GF102J	RESISTOR, 1/4 W, 5%, 1K OHM
		71785	711009-01	R5, 8
11	1	-	RC07GF331J	RESISTOR, 1/4 W, 5%, 330 OHM
		71785	711007-01	R7
12	4	NS	DS8838N	IC, QUAD UN BUS XCVR
			700041-01	U1, 2, 21, 29
13	1	NS	DS8837N	IC, HEX UN BUS RCVR
			700040-01	U4
14	2	NS	DM8136N	IC, 6-BIT UN BUS COMPTR
			700039-01	U5, 17
15	1	TI	SN74LS175N	IC, QUAD D-TYPE FF
		06668	700020-01	U6
16	2	SIG	N8T28N	IC, 3-STATE QUAD BUS XCVR
		18324	700030-01	U7, 10
17	1	TI	SN74LS10N	IC, TPL 3-INPUT NAND GATE
		06668	700005-01	U8
18	1	AMP	435668-8	SWITCH, DIP, SPST, LOW PF, 9-POSITION
		00779	720005-01	U9

TITLE	FSCM NO	DWG NO	REV
PARTS LIST- CCA,		PL 178009-01	B
Q-BUS TO GPIB INTERFACE, GPIB11V-1		Fri Apr 6 15:18:14 1984	

NATIONAL INSTRUMENTS

ITEM NO	QTY REQD	MFR FSCM NO	PART/DWG STOCK NO	DESCRIPTION REFERENCE DESIGNATION
19	2	TI	SN74LS257AN	IC, QUAD 2-TO-1 LINE SEL/MULTIPLEXER
		06668	700021-01	U11,14
20	1	SIG	N8881N	IC, QUAD 2-INPUT NAND BFR
		18324	700031-01	U12
21	2	CTS	761-1-R1K	RESISTOR, DIP, 16-PIN, 2%, 15 X 1K OHM
		00079	710002-01	U13,19
22	2	AMP	435668-6	SWITCH, DIP, SPST, LOW PF, 7-POSITION
		00779	720003-01	U15,18
23	2	TI	SN74LS08N	IC, QUAD 2-INPUT & GATE
		06668	700004-01	U16,23
24	3	TI	SN74LS74AN	IC, DUAL D-TYPE FF
		06668	700013-01	U20,24,31
25	1	TI	SN74LS32N	IC, QUAD 2-INPUT OR GATE
		06668	700011-01	U22
26	1	TI	SN74LS174N	IC, HEX D-TYPE FF
		06668	700019-01	U25
27	1	TI	SN74LS04N	IC, 14-PIN DIP, PLASTIC, HEX INVERTER
		06668	700003-01	U26
28	1	TI	SN74LS20N	IC, DUAL 4-INPUT NAND GATE
		06668	700008-01	U27
29	1	MOT	MC68488P	IC, GP INTFC ADPTR
		04713	700037-01	U30
30	1	TI	SN74LS368AN	IC, HEX INVG BUS DRVR
		06668	700024-01	U32
31	1	TI	SN74LS14N	IC, HEX SCHMITT-TRIGGER INV
		06668	700007-01	U33
32	4	MOT	MC3448AP	IC, QUAD 3-STATE/OPEN C GPIB XCVR
		04713	700035-01	U34,35,36,39
33	1	TI	SN74LS00N	IC, QUAD 2-INPUT NAND GATE
		06668	700001-01	U40
34	.5 in	BEL	8538-3	WIRE, VINYL, RED, SOLID, 24 AWG
		70903	763021-01	W1
35	1	BERG	65268-009	HEADER, SHLDED, .1 CTR, 26-POSITION
		22526	760010-01	J1
36	2	AMP	435238-4	COVER, PROT, SWITCH, DIP, 7 POSN
		00779	720009-01	

TITLE	FSCM NO	DWG NO	REV
PARTS LIST- CCA,		PL 178009-01	B
Q-BUS TO GPIB INTERFACE, GPIB11V-1	Fri Apr	6 15:18:14 1984	

NATIONAL INSTRUMENTS

ITEM NO	QTY REQD	MFR FSCM NO	PART/DWG STOCK NO	DESCRIPTION REFERENCE DESIGNATION
37	1	AMP	435238-6	COVER, PROT, SWITCH, DIP, 9 POSN
		00779	720010-01	
38	1	CAL	SERIES 110-GREEN	HANDLE, PRINTED CIRCUIT BOARD, GREEN
			745004-01	
39	2	USM	SE47, Brass Nickel Plated	EYELET, RLD FLG, NP BRASS
			745000-01	
40	2	TI	SN74LS02N	IC, QUAD 2-INPUT NOR GATE
		06668	700002-01	U28,37

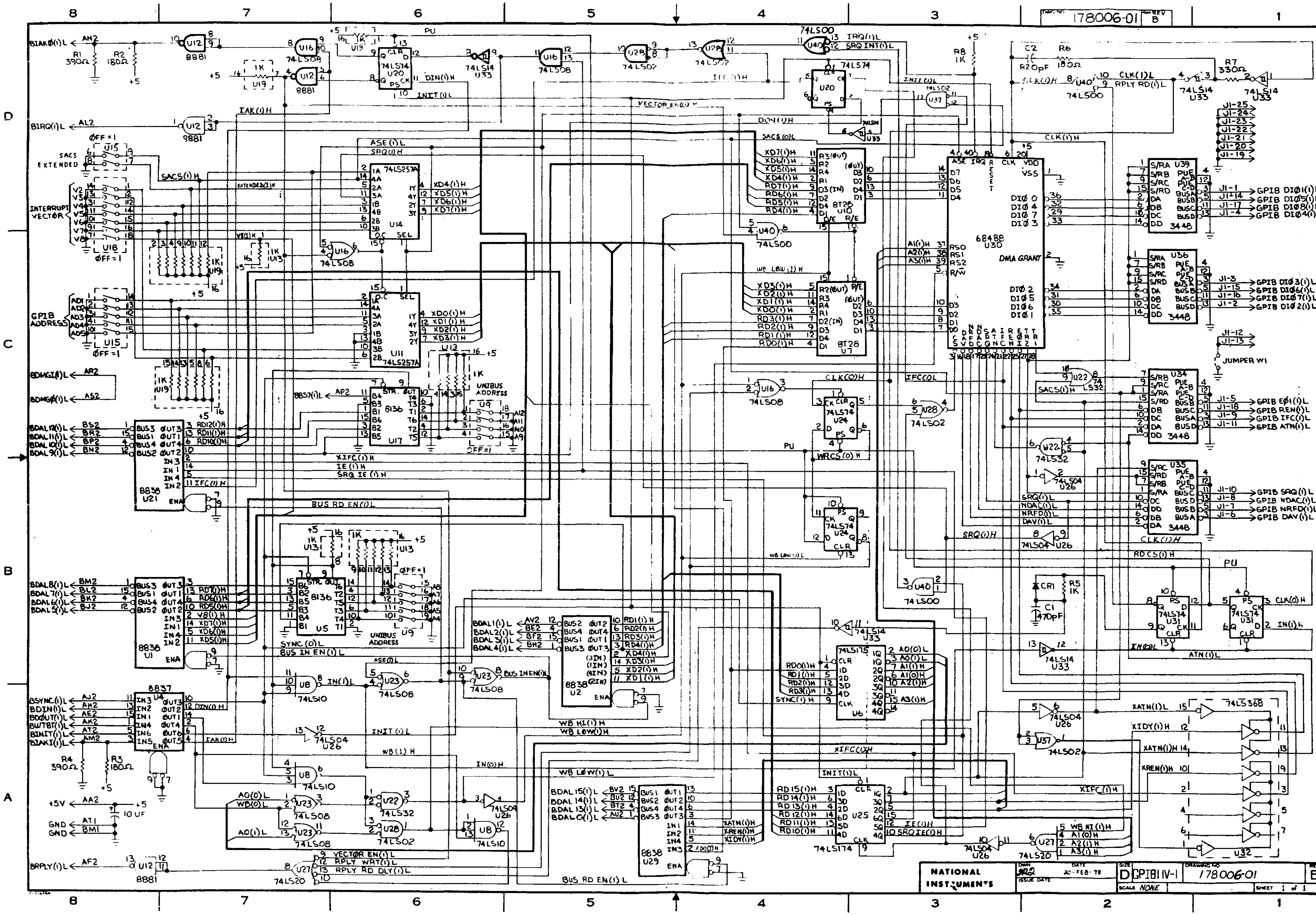
TITLE	FSCM NO	DWG NO	REV
PARTS LIST- CCA,		PL 178009-01	B
Q-BUS TO GPIB INTERFACE, GPIB11V-1	Fri Apr	6 15:18:14 1984	

NATIONAL INSTRUMENTS

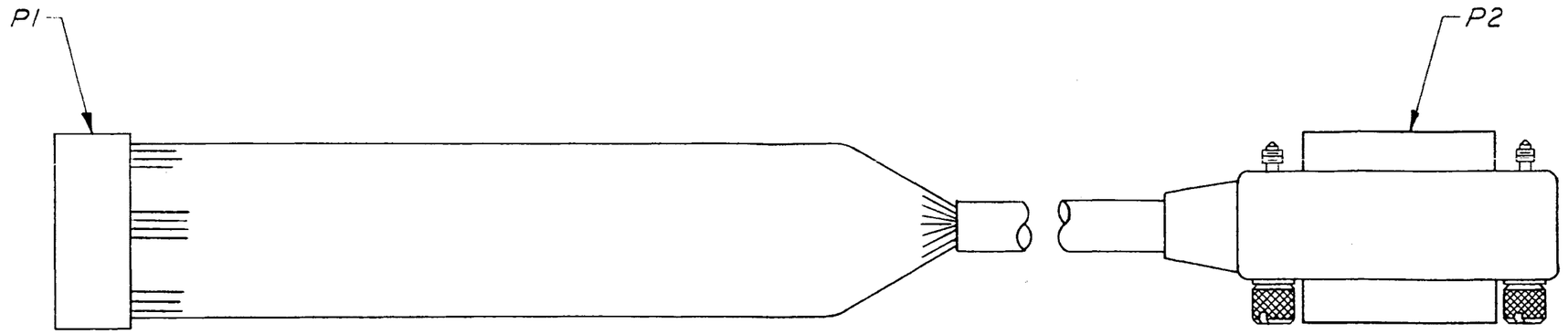
CHAPTER 7

DRAWINGS

This section contains assembly drawings and the schematic diagram of the GPIB11V-1.

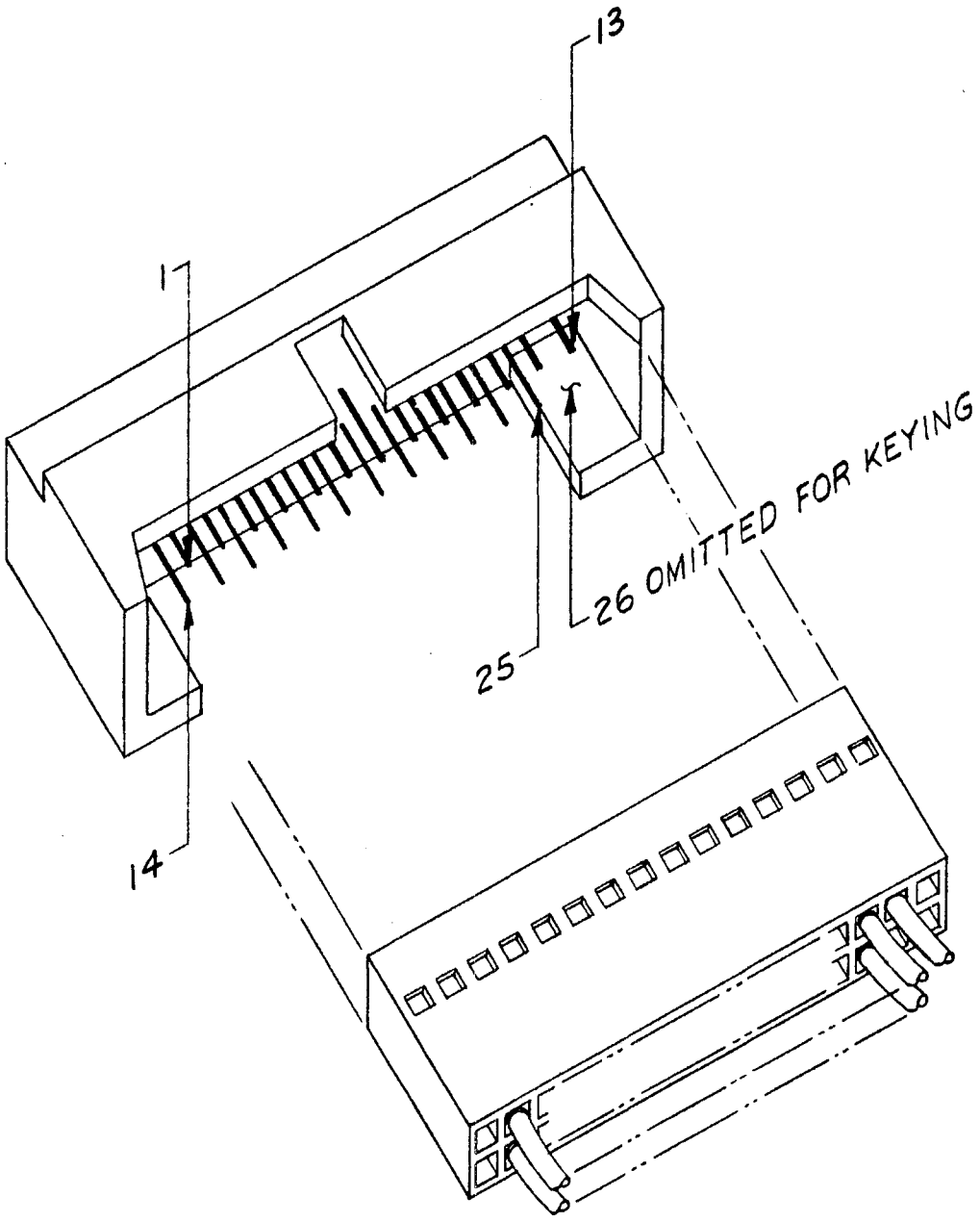


GPIB11V-1 SCHEMATIC DIAGRAM



FROM	TO	SIGNAL	WIRE COLOR	REMARKS	FROM	TO	SIGNAL	WIRE COLOR
P1-1	P2-1	DIO1	BRN	← TWISTED PAIR →	P1-14	P2-13	DIO5	WHT/ORN
P1-2	P2-2	DIO2	RED	← TWISTED PAIR →	P1-15	P2-14	DIO6	WHT/YEL
P1-3	P2-3	DIO3	ORN	← TWISTED PAIR →	P1-16	P2-15	DIO7	WHT/GRN
P1-4	P2-4	DIO4	YEL	← TWISTED PAIR →	P1-17	P2-16	DIO8	WHT/BLU
P1-5	P2-5	EOI	GRN	← TWISTED PAIR →	P1-18	P2-17	REN	WHT/VIO
P1-6	P2-6	DAV	BLU	← TWISTED PAIR →	P1-19	P2-18	GND	WHT/GRY
P1-7	P2-7	NRFD	VIO	← TWISTED PAIR →	P1-20	P2-19	GND	WHT/BLK/BRN
P1-8	P2-8	NDAC	GRY	← TWISTED PAIR →	P1-21	P2-20	GND	WHT/BLK/RED
P1-9	P2-9	IFC	WHT	← TWISTED PAIR →	P1-22	P2-21	GND	WHT/BLK/ORN
P1-10	P2-10	SRQ	WHT/BLK	← TWISTED PAIR →	P1-23	P2-22	GND	WHT/BLK/YEL
P1-11	P2-11	ATN	WHT/BRN	← TWISTED PAIR →	P1-24	P2-23	GND	WHT/BLK/GRN
P1-12	P2-12	SHIELD	BLK	← TWISTED PAIR →	P1-25	P2-24	GND	WHT/BLK/BLU
P1-13	SHLD	SHIELD	BLK	← SHIELD TAP	P1-26	—	KEY	KEY PLUG

INTERFACE CABLE ASSEMBLY



CONNECTOR J1 ASSEMBLY

APPENDIX A

MULTILINE INTERFACE MESSAGES

Multiline interface messages are sent and received with ATN TRUE.

MULTILINE INTERFACE MESSAGES

Hex	Octal	Decimal	ASCII	Message	Hex	Octal	Decimal	ASCII	Message
00	000	0	NUL		20	040	32	SP	MLA0
01	001	1	SOH	GTL	21	041	33	!	MLA1
02	002	2	STX		22	042	34	"	MLA2
03	003	3	ETX		23	043	35	#	MLA3
04	004	4	EOT	SDC	24	044	36	$	MLA4
05	005	5	ENQ	SDC	25	045	37	%	MLA5
06	006	6	ACK		26	046	38	&	MLA6
07	007	7	BEL		27	047	39	'	MLA7
08	008	8	BS	GET	28	050	40	(	MLA8
09	009	9	HT	TCT	29	051	41	)	MLA9
0A	012	10	LF		2A	052	42	*	MLA10
0B	013	11	VT		2B	053	43	+	MLA11
0C	014	12	FF		2C	054	44	,	MLA12
0D	015	13	CR		2D	055	45	-	MLA13
0E	016	14	SO		2E	056	46	.	MLA14
0F	017	15	SI		2F	057	47	/	MLA15
10	020	16	DLE		30	060	48	0	MLA16
11	021	17	DC1	LLO	31	061	49	1	MLA17
12	022	18	DC2		32	062	50	2	MLA18
13	023	19	DC3		33	063	51	3	MLA19
14	024	20	DC4	DCL	34	064	52	4	MLA20
15	025	21	NAK	PPU	35	065	53	5	MLA21
16	026	22	SYN		36	066	54	6	MLA22
17	027	23	ETB		37	067	55	7	MLA23
18	030	24	CAN	SPE	38	070	56	8	MLA24
19	031	25	EM	SPD	39	071	57	9	MLA25
1A	032	26	SUB		3A	072	58	:	MLA26
1B	033	27	ESC		3B	073	59	;	MLA27
1C	034	28	FS		3C	074	60	<	MLA28
1D	035	29	GS		3D	075	61	=	MLA29
1E	036	30	RS		3E	076	62	>	MLA30
1F	037	31	US		3F	077	63	?	UNL

MULTILINE INTERFACE MESSAGES

Hex	Octal	Decimal	ASCII	Message	Hex	Octal	Decimal	ASCII	Message
40	100	64	@	MTA0	60	140	96	`	MSA0,PPE
41	101	65	A	MTA1	61	141	97	a	MSA1,PPE
42	102	66	B	MTA2	62	142	98	b	MSA2,PPE
43	103	67	C	MTA3	63	143	99	c	MSA3,PPE
44	104	68	D	MTA4	64	144	100	d	MSA4,PPE
45	105	69	E	MTA5	65	145	101	e	MSA5,PPE
46	106	70	F	MTA6	66	146	102	f	MSA6,PPE
47	107	71	G	MTA7	67	147	103	g	MSA7,PPE
48	110	72	H	MTA8	68	150	104	h	MSA8,PPE
49	111	73	I	MTA9	69	151	105	i	MSA9,PPE
4A	112	74	J	MTA10	6A	152	106	j	MSA10,PPE
4B	113	75	K	MTA11	6B	153	107	k	MSA11,PPE
4C	114	76	L	MTA12	6C	154	108	l	MSA12,PPE
4D	115	77	M	MTA13	6D	155	109	m	MSA13,PPE
4E	116	78	N	MTA14	6E	156	110	n	MSA14,PPE
4F	117	79	O	MTA15	6F	157	111	o	MSA15,PPE
50	120	80	P	MTA16	70	160	112	p	MSA16,PPD
51	121	81	Q	MTA17	71	161	113	q	MSA17,PPD
52	122	82	R	MTA18	72	162	114	r	MSA18,PPD
53	123	83	S	MTA19	73	163	115	s	MSA19,PPD
54	124	84	T	MTA20	74	164	116	t	MSA20,PPD
55	125	85	U	MTA21	75	165	117	u	MSA21,PPD
56	126	86	V	MTA22	76	166	118	v	MSA22,PPD
57	127	87	W	MTA23	77	167	119	w	MSA23,PPD
58	130	88	X	MTA24	78	170	120	x	MSA24,PPD
59	131	89	Y	MTA25	79	171	121	y	MSA25,PPD
5A	132	90	Z	MTA26	7A	172	122	z	MSA26,PPD
5B	133	91	[	MTA27	7B	173	123	{	MSA27,PPD
5C	134	92	\	MTA28	7C	174	124	|	MSA28,PPD
5D	135	93	]	MTA29	7D	175	125	}	MSA29,PPD
5E	136	94	^	MTA30	7E	176	126	~	MSA30,PPD
5F	137	95	_	UNT	7F	177	127	DEL	

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