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GPIB11V-2

Operating and Service Manual

Part Number 320006-01

October 1988 Edition

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- Relocate the equipment with respect to the receiver.
- Reorient the receiver's antenna.
- Be sure the equipment is plugged into a grounded outlet and that the grounding has not been defeated with a cheater plug.

If necessary, consult National Instruments or an experienced radio/television technician for additional suggestions. The following booklet prepared by the Federal Communications Commission may also be helpful: "How to Identify and Resolve Radio-TV Interference Problems." This booklet is available from the U.S. Government Printing Office, Washington DC 20402, Stock Number 004-000-00345-4.

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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

This section contains general information about National Instruments' GPIB11V-2 interface kit which is pictured in Figure 1.1. This information includes a brief description of the GPIB11V-2 kit, a list of equipment supplied, a list of optional equipment, a list of applicable reference documents, and a brief description of the remainder of this manual.

1.2 GPIB11V-2 INTERFACE KIT DESCRIPTION

The GPIB11V-2 is a single dual-height card which interfaces the LSI-11 bus, or Q-BUS, to the IEEE Std 488-1978 instrumentation bus, also known as the General Purpose Interface Bus or GPIB. Hereafter, the standard will be referred to as IEEE Std 488, and the bus will be called the GPIB. The GPIB11V-2 provides a means to implement LSI-11 test and measurements systems with standard interconnecting cables. The GPIB11V-2 interface kit includes hardware and software to implement the GPIB functions. A cable is supplied for interconnection with other devices on the GPIB. Utility software is distributed on floppy disk, RK-05 disk, paper tape, or magnetic tape for RT-11, RSX-11/M, or UNIX operating systems. Comprehensive hardware and software manuals provide the user with instructions for use of the kit.

1.3 EQUIPMENT SUPPLIED

Table 1.1 lists the equipment supplied in the National Instruments' GPIB11V-2 interface kit. Optional items are listed in Table 1.2. Accessories are given in Table 1.3.

1.4 APPLICABLE DOCUMENTS

The following documents are references which cover in greater detail specific topics introduced in this manual:

IEEE Std 488-1978, Standard Digital Interface for Programmable Instrumentation

DEC Microcomputer Processor Handbook

DEC Microcomputer Interfaces Handbook

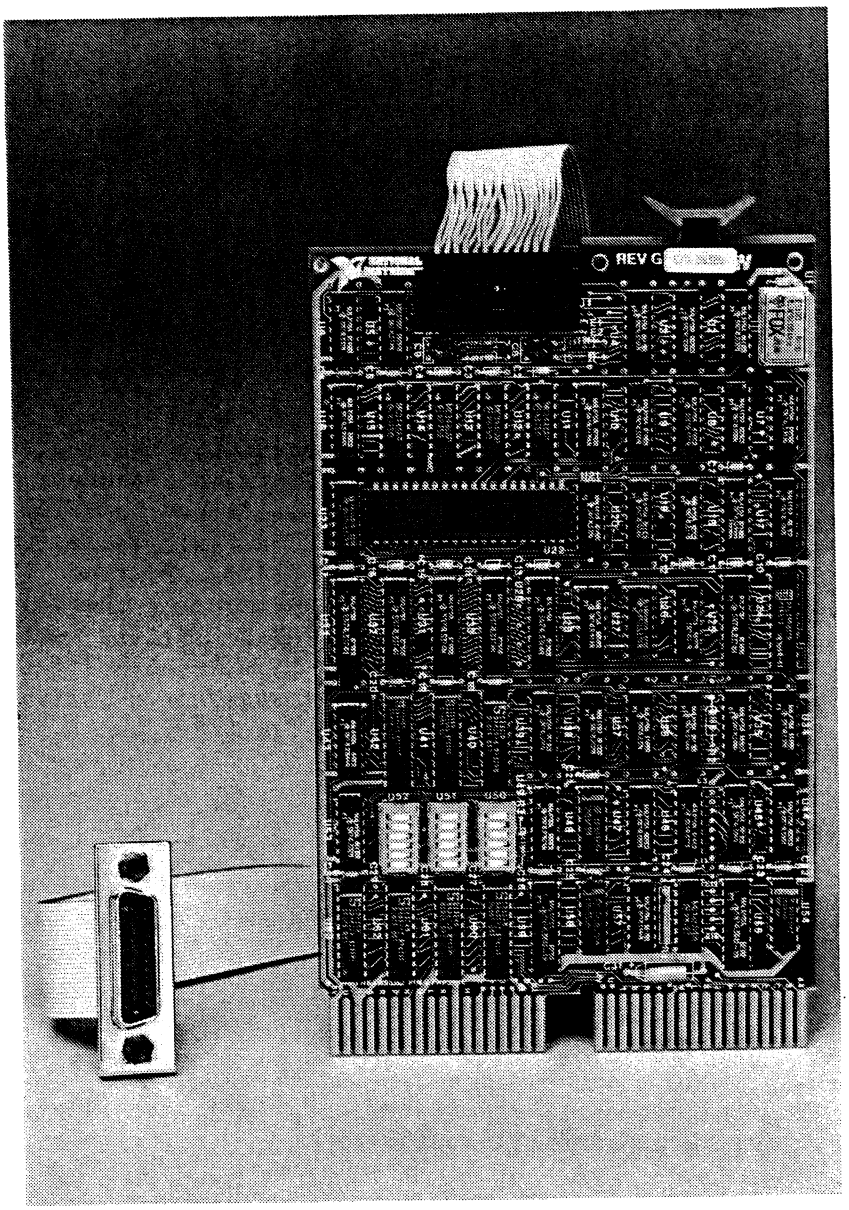


Figure 1.1

GPIB11V-2 Interface

TABLE 1.1

EQUIPMENT SUPPLIED IN BASIC KIT

Description	NI Part Number
Bus Interface Card	179055-01
Interface Cable Assembly - 4 meter	178040-04
Operating and Service Manual	320006-01
Software Reference Manual	310001-01
Floppy Disk - Distribution Software (includes Stand-alone Routine, RT-11 Driver, RSX-11/M Driver)	420007-01

TABLE 1.2

OPTIONAL EQUIPMENT

Description	NI Part Number
Paper Tape - Distribution Software	410007-01
Mag Tape - Distribution Software	430007-01
RK05 Disk - Distribution Software	440007-01
Paper Tape - UNIX Software	410008-01
Floppy Disk - UNIX Software	420008-01
Mag Tape - UNIX Software	430008-01
RK05 Disk - UNIX Software	440008-01
Interface Cable Assy - 2 meter	178040-02

TABLE 1.3

ACCESSORIES

Description	NI Part Number
GPIB Extension Cable - 1 meter	763001-01
GPIB Extension Cable - 2 meter	763001-02
GPIB Extension Cable - 4 meter	763001-03

1.5 SCOPE

This manual provides the user with a general description of the General Purpose Interface Bus, installation and programming information for the GPIB11V-2, and finally, the theory of operation, logic diagrams, and replacement parts list for proper use and maintenance of the GPIB11V-2. The manual is divided into seven major sections: General Information, GPIB11V-2 Description, Installation and Configuration, Programming Information, Theory of Operation, Parts List, and Drawings. An ASCII chart and list of bus messages is given in Appendix A.

1.6 DIFFERENCES BETWEEN THE GPIB11V-2 AND GPIB11-2

The GPIB11V-2's operation and functionality are similar to those of the National Instruments GPIB11-2 DMA UNIBUS interface to the GPIB for the PDP-11 family of processors. Except for the Talker/Listener Logic, the hardware implementation is considerably different, but from the user's (or programmer's) point of view, these are the relevant differences.

1. The GPIB11V-2 supports up to 22 bit addressing, and access for all the extended address bits, BA21-16, is through the upper byte of the Carry Cycle Function/Extended Address Register. (In the GPIB11-2, access to the extended address bits, XBA17-16, is through bits 5 and 4 of the Control Status Register.)

2. The GPIB11V-2 automatically makes itself the System Controller when the IFC bit in the Control Status Register is set.

3. The position of the Three-State/Open Collector selection switch on the GPIB11V-2 is readable via the OC bit on the Control Status Registers. (The GPIB11-2 cannot monitor the position.)

4. Unused bits in the GPIB11V-2 Q-BUS registers read as ones. (Those in the GPIB11-2's UNIBUS registers read as zeros.)

5. The power on state of the GPIB11V-2's Byte Count and Bus Address Registers are undefined. (On the GPIB11-2, these registers are cleared.)

6. The GPIB11V-2 uses a 5 MHz clock (versus a 6MHz clock on the GPIB11-2.)

Because of these and other differences in implementation and nomenclature, users who are familiar to the GPIB11-2 should nonetheless refer to this manual rather than assume a similiarity between the two interfaces.

CHAPTER 2

GPIB11V-2 DESCRIPTION

2.1 SPECIFICATIONS

2.1.1 Electrical Specifications

2.1.1.1 GPIB Signals, Logic Status, and Electrical Levels

The GPIB interface system contains a set of 16 signal lines:

DIO1	Data Bus Line 1
.	.
.	.
.	.
DIO8	Data Bus Line 8
DAV	Data Valid
NRFD	Not Ready for Data
NDAC	Not Data Accepted
IFC	Interface Clear
ATN	Attention
SRQ	Service Request
REN	Remote Enable
EOI	End or Identify

Negative logic with standard TTL levels is used on the GPIB. That is, a false (0) logic state corresponds to a TTL high level of 2.0 V or higher, and a true (1) logic state corresponds to a TTL low level of 0.8 V or lower.

2.1.1.2 Terminiation

Each of the 16 signal lines is terminated by a resistive load that establishes a steady state voltage when all drivers on the line are disabled. Each of the lines are terminated with 3000 ohms to Vcc and 6200 ohms to ground by each device on the bus.

2.1.1.3 Line Drivers

The NDAC, NRFD, SRQ, and REN signals are transmitted with open collector drivers. The data lines, DIO1-8, and the EOI, DAV, IFC, and ATN signal lines are switch selectable for either open collector or three-state. The specifications for each type of driver are listed below:

Type	Low State	High State
Open Collector	<+0.5 V at 48 mA sink current	determined by termination
Three-State	<+0.5 V at 48 mA sink current	> = +2.4 V at -5.2 mA

2.1.1.4 Line Receivers

Each line receiver has the following specifications:

Type	Low State	High State
Schmitt-Trigger with hysteresis equal to or better than 0.4V	Vt- <= 0.8V	Vt+ >= 2.0V

2.1.1.5 Cable Length

Maximum length of single span: 4 meters

Maximum total length: 20 meters

Maximum average length: 2 meters

2.1.1.6 Operating Temperature

0 - 40 degrees Celsius

2.1.1.7 Power Requirements

The card requires the following power from the computer or extension mounting box:

Supply	Current Required (A)
+5 Vdc	1.5 Typ 2.0 Max

2.1.2 Physical Specifications

The GPIB11V-2 interface card in packaged on a single module that can be plugged into a dual-height Q-BUS slot. The module has a single 26 pin Berg connector that interconnects the board to the standard bus cable with a standard bus connector on the outboard end.

Card Dimensions (Inches)

Height	5.2
Length	8.4

2.2 DESCRIPTION OF THE GENERAL PURPOSE INTERFACE BUS

2.2.1 General

The IEEE Std 488 GPIB provides a means for communications among a group of interconnected devices. Two types of messages are carried by the bus:

1. Interface messages are used for bus management.

2. Device dependent messages are communicated between the various devices via the interface bus, but are not used or processed by the bus.

The three types of devices which are required to organize and manage the flow of information on the bus are a Listener, a Talker, and a Controller. A Listener has the capability of being addressed by an interface message to receive device dependent messages. A Talker has the capability of being addressed by an interface message to send device dependent messages. A Controller can address devices to Listen or Talk. A Controller can also send interface messages to command other specific actions within interfaced devices. A single bus may have one or more Controllers. If more than one Controller is connected to the bus, one is designated as the System Controller and may temporarily pass control to any other Controller.

The GPIB11V-2 is capable of being a Listener, a Talker, a Controller, and, in particular, a System Controller.

2.2.2 GPIB Operation

This section contains a simplified description of the operation of the instrumentation bus. For more details the reader is referred to the IEEE Std 488.

Bus operation is divided into two logical functions: interface functions (for bus management) and device functions (for device control and communication). The interface functions, which are described herein, are basically used to establish an enviroment in which device functions may be performed. The device functions are unique to the individual instrument and are not addressed here.

The Source Handshake (SH) and Acceptor Handshake (AH) interface functions are used to transmit and receive bit-parallel, byte-serial messages ("multiline messages") on the bus. These messages are interpreted either as commands to the interface or as data bytes for the device, depending on the status of the bus signal line, Attention (ATN). ATN is asserted for interface commands.

The Talker (T) or Extended Talker (TE) and Listener (L) or Extended Listener (LE) interface functions are used to set up devices for data transfers. The transfers are made using the handshake functions. When an interface has been addressed as a Talker, its associated device function is allowed to use the interface Source Handshake function to transmit data bytes. The device functions of any interfaces which were addressed as Listeners must

use the Acceptor Handshake function to receive the data bytes. Only one device at a time may be the Talker although multiple Listeners may exist.

The Controller (C) function is the originator of all interface messages. Only one interface at a time may be the Controller-in-charge and protocol exists to pass the controlling ability among interfaces. When the Controller-in-charge is asserting the Attention line, it is in its active state and is often referred to as the Active Controller. When not asserting Attention, it is in its standby state. Any controller that is not the Controller-in-charge remains in its idle state. At any time, there is at most one interface on the bus that has the capability to make itself the Controller-in-charge. It is referred to as the System Controller.

The Controller is responsible for addressing and unaddressing Talkers and Listeners, as well as performing other bus management operations. These other operations include conducting a Parallel Poll using the uniline message Identify (IDY); setting device functions in remote or local mode using the uniline message Remote Enable (REN); and initializing the bus by asserting the uniline message Interface Clear (IFC). The latter two operations are actually capabilities only of the System Controller and are not transferrable by the transfer of control protocol.

2.2.3 GPIB Lines

A total of 24 lines are used to implement the bus. Of these lines, 16 are signal lines, one is ground, one is the cable shield, and six are twisted pair common for six of the signal lines. The 16 signal lines are used to carry all information, interface messages, and device dependent messages among interconnected devices. The bus is organized into three sets of signal lines:

8 data input/output lines

3 handshake lines

5 interface management signal lines

The eight data lines, DIO1-8, carry all data, including input, output, and device dependent messages. In many instruments data is based on the seven bit ASCII code set.

The three handshake lines, NRFD, DAV, and NDAC, are used to effect the transfer of each byte of data on the DIO lines from an addressed Talker to all addressed Listeners. The three handshake lines provide a means to asynchronously transfer data between instruments.

The NRFD (Not Ready for Data) line is used to indicate the condition of readiness of devices to accept data. All instruments drive NRFD false when ATN is true. Only addressed Listeners drive NRFD false when ATN is false. The NRFD line is monitored by the Controller when ATN is true and by the addressed Talker when ATN is false. The NRFD line is false when all Listeners are ready for data and true when one or more Listeners are not ready for data.

The DAV (Data Valid) line is used to indicate the validity of data on the data lines. DAV is driven by the Controller when ATN is true and by the addressed Talker when ATN is false. The DAV line is monitored by all

instruments if ATN is true and by addressed Listeners when ATN is false.

The NDAC (Not Data Accepted) line is used to indicate acceptance of data by addressed Listeners when ATN is false and acceptance of commands by all devices when ATN is true. Listeners indicate acceptance of data by setting NDAC false. When NDAC is true, one or more Listeners have not accepted the data.

The five bus management lines are ATN, IFC, REN, SRQ, and EOI. ATN and IFC are used by all instruments while the remaining three may or may not be used by a particular instrument.

All devices on the GPIB must monitor the ATN (Attention) line. This line is set true by the Controller-in-charge when it sends interface messages, such as device talk and listen addresses, secondary addresses, and polling configuration messages. When ATN is false, the active Talker can send device dependent messages, such as data and programming information, to active Listeners.

The IFC (Interface Clear) line is used by the System Controller to place the bus in a known quiescent state. The IFC line can only be driven true by the System Controller and must be monitored by all other instruments. In order to clear a device, the IFC line must be set true for at least 100 microseconds. IFC may be set true by the System Controller at any time.

The REN (Remote Enable) line is used to operate an instrument under remote control. A true value for the Remote Enable line is one of the conditions for operation of an instrument in remote mode. The use of the remote function is optional. The REN line is driven true only by the System Controller and may be changed at any time. Instruments which use the REN line must monitor it at all times and return to local control whenever it becomes false.

The SRQ (Service Request) line is used by an instrument to asynchronously request service from the Controller-in-charge.

The EOI (End or Identify) line is used either to indicate the end of a data string or to conduct a Parallel Poll, depending on the state of the ATN line. When ATN is false, the addressed Talker may send the END message to indicate the end of its data by setting EOI true at the same time it places the last data byte on the DIO lines. The Controller-in-charge may send the IDY message to initiate a Parallel Poll of all instruments with Parallel Poll capability by setting ATN and EOI true simultaneously.

2.2.4 GPIB Physical Characteristics

Bus cables are used to interconnect instruments. There are three basic restrictions on cable length. First, the maximum length of any single span between two instruments is 4 meters. Second, the maximum average length is 2 meters per device. Third, the maximum total length for all interconnected instruments is 20 meters. Instruments may be connected in a linear or star configuration.

Two 24 pin piggy-back connectors, one male and one female, are used on either end of the interconnecting cables. An overall cable shield is used to

reduce susceptibility to noise. This shield is grounded only at one instrument, usually the System Controller. Figure 2.1 shows the pin connections for the GPIB cable.

2.3 GPIB11V-2 FUNCTIONAL DESCRIPTION

2.3.1 Hardware Description

The GPIB11V-2 is a dual-height card which interfaces the LSI-11 computer to the General Purpose Interface Bus. Figure 2.2 shows an implementation of a GPIB11V-2 and a LSI-11 computer. This system allows the LSI-11 computer to control remotely programmable instrumentation. The GPIB11V-2 can also be used in a multi-processor system to provide interprocessor communication and shared usage of the instrumentation. Such a system is shown in Figure 2.3.

Figure 2.4 is a block diagram of the GPIB11V-2. The interface consists of these major sections that are discussed in greater detail in Chapters 4 and 5:

Q-BUS Addressable Registers

- Byte Count Register (BCR)
- Byte Address Register (BAR)
- Control Status Register (CSR)
- Carry Cycle Function/Extended Address Register (CCF/XAR)

DMA Port

Q-BUS Control Logic

GPIB Controller Logic

GPIB Talker/Listener Logic

Clock and State Machine

Q-BUS and GPIB Receivers/Drivers

The four Q-BUS registers are used to configure, control, and monitor direct memory access (DMA) data transfers between the Q-BUS and the GPIB or between the Q-BUS and internal registers within the GPIB Talker/Listener Logic. These transfers take place through a Data Input/Output Register or DMA Port. The Q-BUS Control Logic handles the receipt and transmission of data and addresses to the Q-BUS, the routing of data on the internal data bus, and the execution of service request interrupt protocol. The GPIB Talker/Listener Logic, which is contained mostly on one large scale integrated circuit component, implements the GPIB functions of Talker, Extended Talker, Listener, Extended Listener, Source Handshake, Acceptor Handshake, Service Request, Remote/Local, Device Clear, and Device Trigger. The GPIB Controller Logic assists in implementing these functions and, in addition, implements the GPIB Controller function. Synchronization between Q-BUS and GPIB activities is attained with a logic State Machine and a high-frequency system clock. Bus compatible receivers, drivers, or transceivers buffer signals to and from the

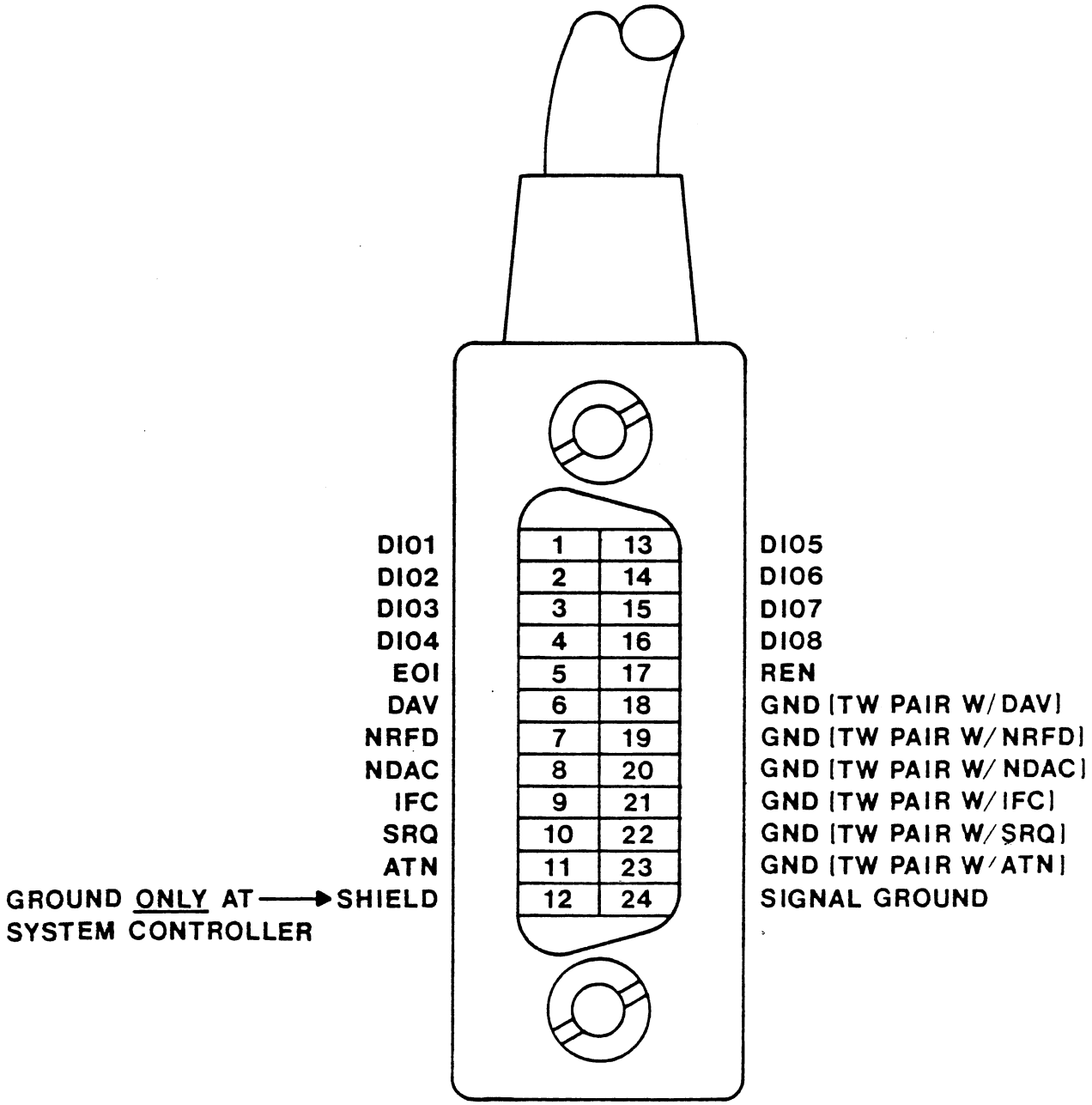


FIGURE 2.1

PIN CONNECTIONS FOR GPIB CABLE

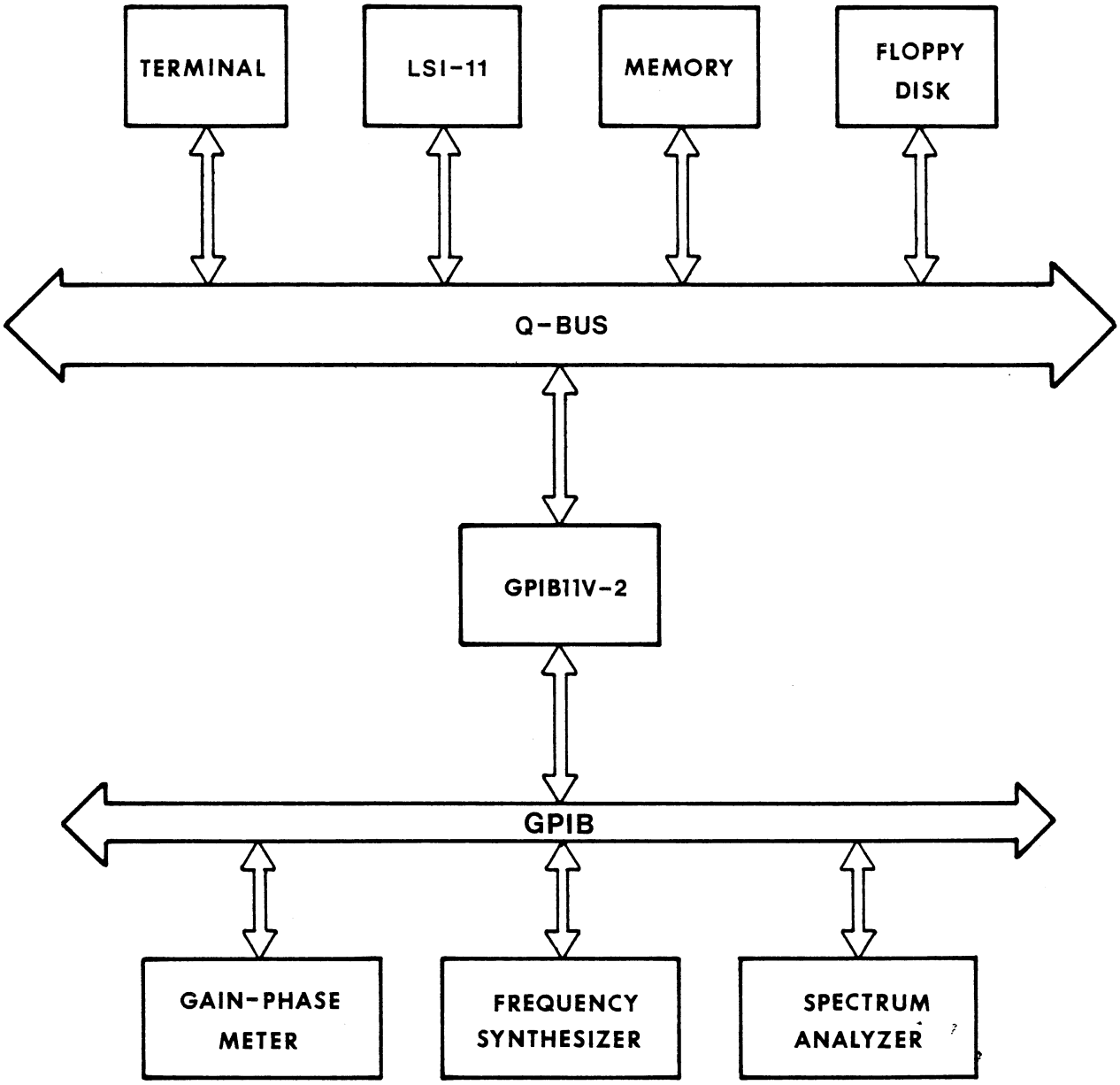


FIGURE 2.2

IMPLEMENTATION OF A GPIB11V-2 SYSTEM

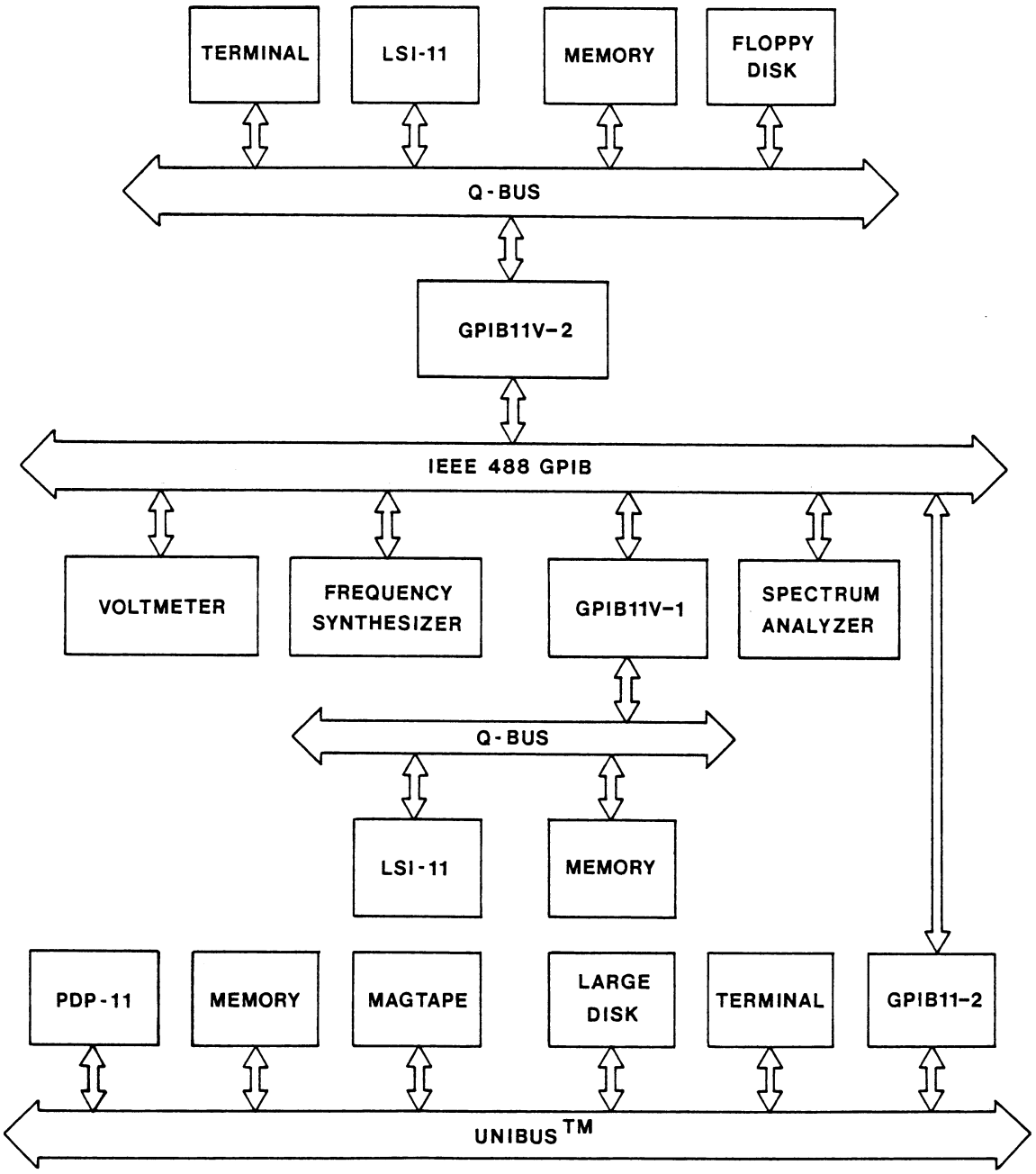


FIGURE 2.3

A MULTICONTROLLER SYSTEM

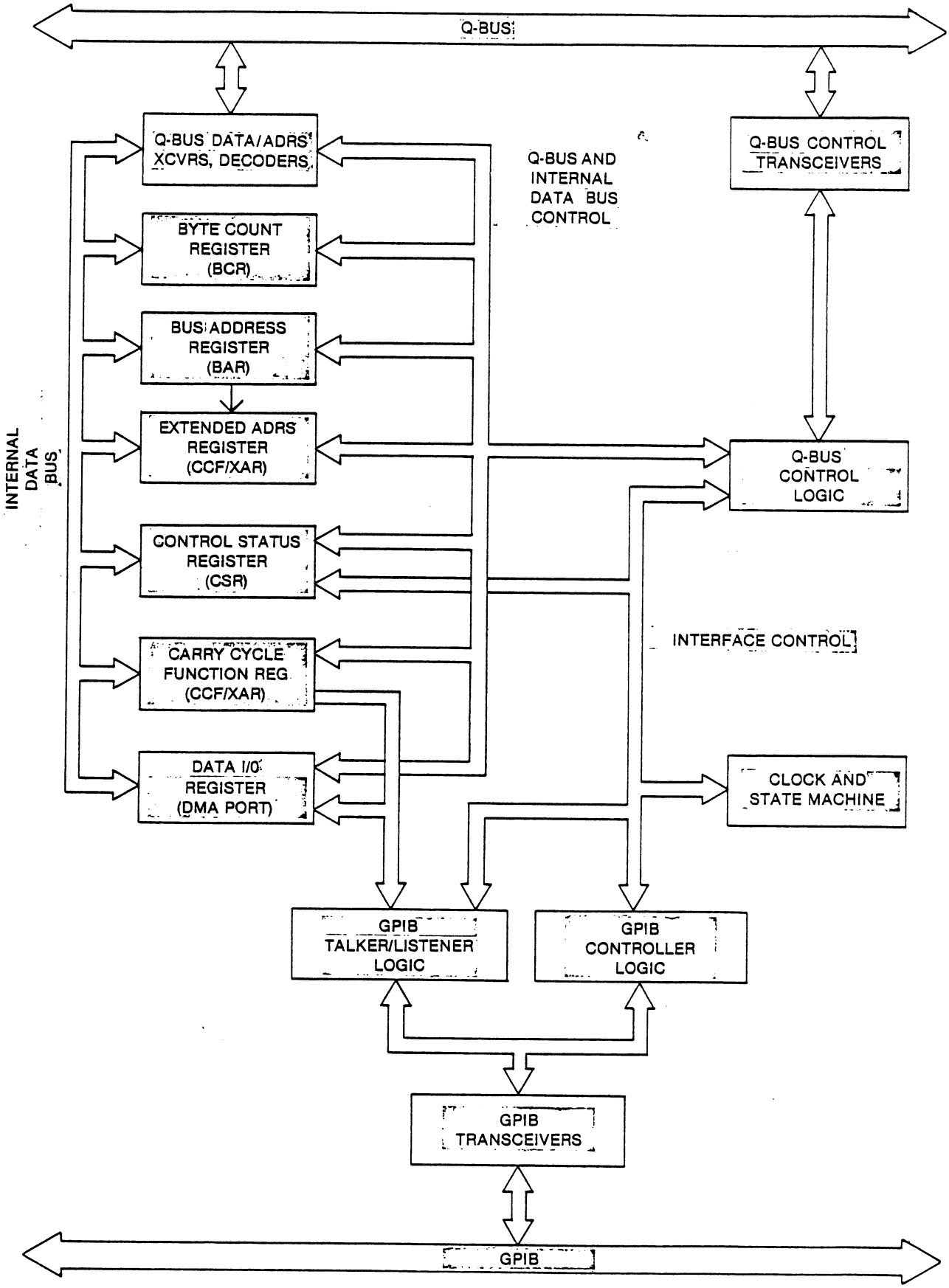


FIGURE 2.4

FUNCTIONAL BLOCK DIAGRAM OF THE GPIB11V-2

interface.

The Q-BUS Control Logic will selectively interrupt the LSI-11 processor for service when:

1. A DMA between memory and the GPIB or between memory and the internal registers completes normally, or aborts due to reading non-existent memory;

2. GPIB IFC (Interface Clear) is detected and the GPIB11V-2 interface is not the System Controller (this condition will interrupt an in-progress GPIB DMA, but not an internal register DMA; the interrupted GPIB DMA cannot be resumed);

3. GPIB SRQ (Service Request) is detected and the GPIB11V-2 interface is the Controller-in-charge (this condition will interrupt an in-progress GPIB DMA, but not an internal register DMA; the interrupted GPIB DMA may be resumed);

4. One or more of twelve GPIB conditions or events occurs (these conditions or events are described in Chapter 4 under Interrupt Status and Mask Registers).

2.3.2 GPIB Functions Implemented by the GPIB11V-2

Table 2.1 lists the capabilities of the GPIB11V-2 in terms of the codes in Appendix C of IEEE Std 488.

TABLE 2.1

GPIB11V-2 INTERFACE CAPABILITIES

Interface Function	Capability Code
Source Handshake	SH1
Acceptor Handshake	AH1
Talker, Extended Talker	T5, TE5
Listener, Extended Listener	L3, LE3
Service Request	SR1
Remote Local	RL1
Parallel Poll	PP2 (PP1 with software assist)
Device Clear	DC1
Device Trigger	DT1
Controller	C1,2,3,4,9

The GPIB11V-2 has complete Source and Acceptor Handshake capability. The GPIB11V-2 can operate as a basic Talker or Extended Talker and can respond to a Serial Poll. It may be placed in a Talk Only mode, and it will be unaddresssed to Talk when it receives its Listen address. The interface can operate as a basic Listener or Extended Listener. It may be placed in a Listen Only mode, and it will be unaddressed to Listen when it receives its Talk address. The GPIB11V-2 has full capabilities for requesting service from another Controller. The ability to place the GPIB11V-2 in local mode is included but the interpretation of remote versus local mode is software

dependent. Full Parallel Poll capability is included in the interface although remote configuration requires software assistance. Device Clear and Trigger capability is included in the interface but the interpretation is software dependent. All Controller functions as specified by the IEEE Std 488 are included in the GPIB11V-2. These include the capability to:

1. Be System Controller.
2. Initialize the interface.
3. Send Remote Enable.
4. Respond to Service Request.
5. Send multiline command messages.
6. Receive control.
7. Pass control.
8. Conduct a Parallel Poll.
9. Take control synchronously or asynchronously.

CHAPTER 3

GPIB11V-2 INSTALLATION AND CONFIGURATION

3.1 INTRODUCTION

This chapter describes the configuration and connection of the GPIB11V-2 to other devices. The chapter is divided into three sections: configuration, installation, and cabling.

3.2 CONFIGURATION

Each GPIB11V-2 basically consists of a dual-height circuit card assembly and associated cable. Before installing the GPIB11V-2, the user must set the following options with switches or jumpers:

Q-BUS Address

Q-BUS Interrupt Vector

GPIB Driver Three-State/Open Collector Selection

Q-BUS Interrupt Priority

GPIB Cable Shield Grounding

The locations of the switches and jumpers are shown in Figure 3.1. In addition, the following options are configured in software:

GPIB Talk, Listen, and Extended Addresses

GPIB System Controller Selection

3.2.1 Q-BUS Address

Each GPIB11V-2 has a unique set of consecutive Q-BUS addresses for its four interface registers, determined by the position of the switches located at U50, U51, and U52. (See Figure 3.2 for details.) The on or closed position selects a logic 1 for the corresponding address bit. Octal addresses from 760000 to 777770 can be selected; however, it is recommended that the addresses lie within the range 764000-767770 in order to avoid conflicts with standard DEC peripherals. The upper and lower bits of the Q-BUS address are not user selectable.

When shipped, the Q-BUS address is set to 767710.

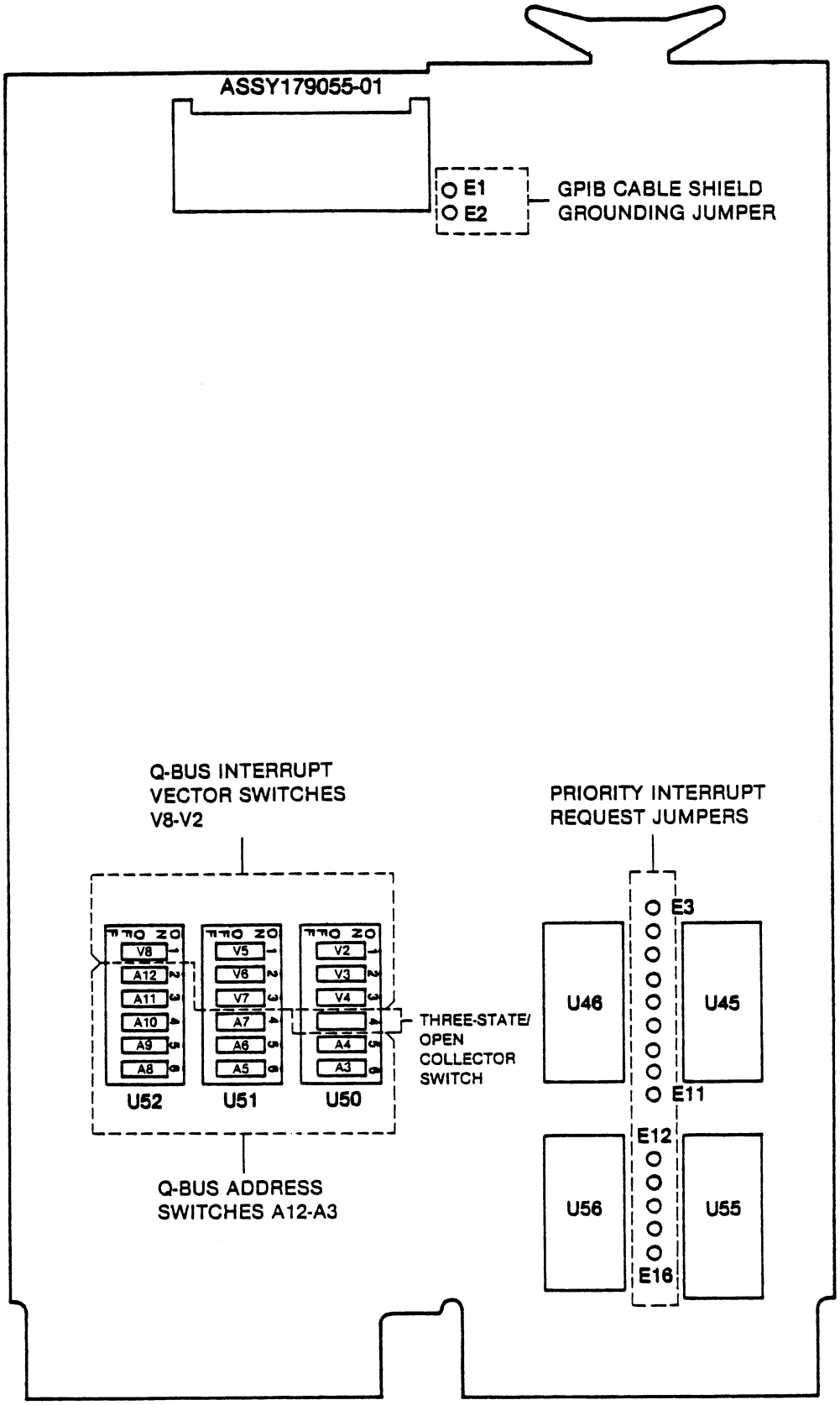
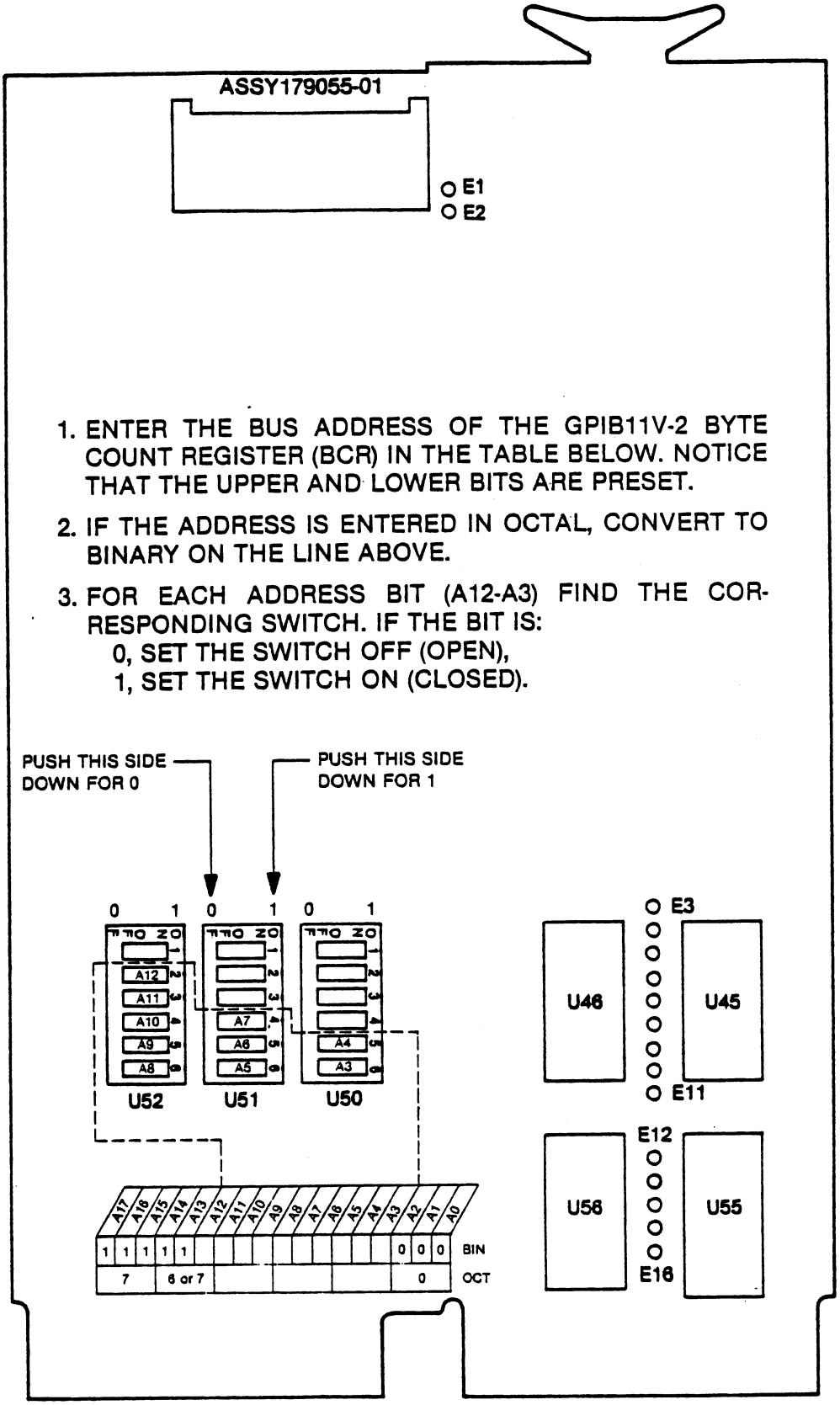


FIGURE 3.1

GPIB11V-2 SWITCH AND JUMPER POSITIONS



SETTING THE GPIB11V-2 Q-BUS ADDRESS

3.2.2 Q-BUS Interrupt Vector

Each GPIB11V-2 has a unique Q-BUS Interrupt Vector which is determined by the position of the switches located at U50, U51, and U52. (See Figure 3.3 for details). The on or closed position selects a logic 1 for the corresponding vector bit. Octal vectors from 000 to 774 can be selected; however, it is recommended that the vector be selected according to the assignment convention described in Appendix A of the DEC Microcomputer Interfaces Handbook (300-774). The upper and lower bits of the Q-BUS interrupt vector are not user selectable.

When shipped, the interrupt vector is set to 310.

3.2.3 GPIB Driver Three-State/Open Collector Selection

The GPIB11V-2 drivers for the GPIB data lines and certain control lines can be configured for either open collector or three-state operation. Switch 4 of U50 is used to select which mode is used. (See Figure 3.4 for details). The GPIB11V-2 is configured for three-state operation with the active pull-ups enabled when the switch is off or open. Conversely, the GPIB11V-2 is configured for open collector operation when the switch is on or closed. The three-state mode allows GPIB data message transfers at rates up to 500,000 bytes/sec but the Parallel Poll feature is disallowed. The open collector mode allows operation at rates up to 250,000 bytes/sec. (These are minimum rates that are set by timing criteria contained in the IEEE Std 488, and the GPIB11V-2 is capable of exceeding these speeds under proper conditions. However, because the GPIB11V-2 is an interface between two asynchronous communications buses, the actual rate attainable in a real system depends on many factors that are outside the interface's control. These include the speed of the processor and memory, the speed of the GPIB device(s), the software overhead associated with each DMA operation, and the number of transfers within one operation.)

In addition to setting this switch, the user must also program two internal parameters to insure correct operation. See Section 4.2.3 on the Hidden Clock Register and the TRI bit in Auxiliary Register B.

Switch 4 of U50 enables the three-state driver output for the data lines DIO1-DIO8 and the signal lines EOI, DAV, IFC, and ATN. The NDAC, NRFD, SRQ, and REN lines are not affected by the switch and remain open collector at all times.

When shipped, this switch is set for open collector operation.

3.2.4 GPIB Cable Shield Grounding

Connect a jumper from E1 to E2 (see Figure 3.1) to ground the GPIB cable shield. Since the GPIB11V-2 will usually be the System Controller in the user system, this jumper is installed when shipped. This jumper should be removed if the GPIB cable is to be grounded at another device on the bus.

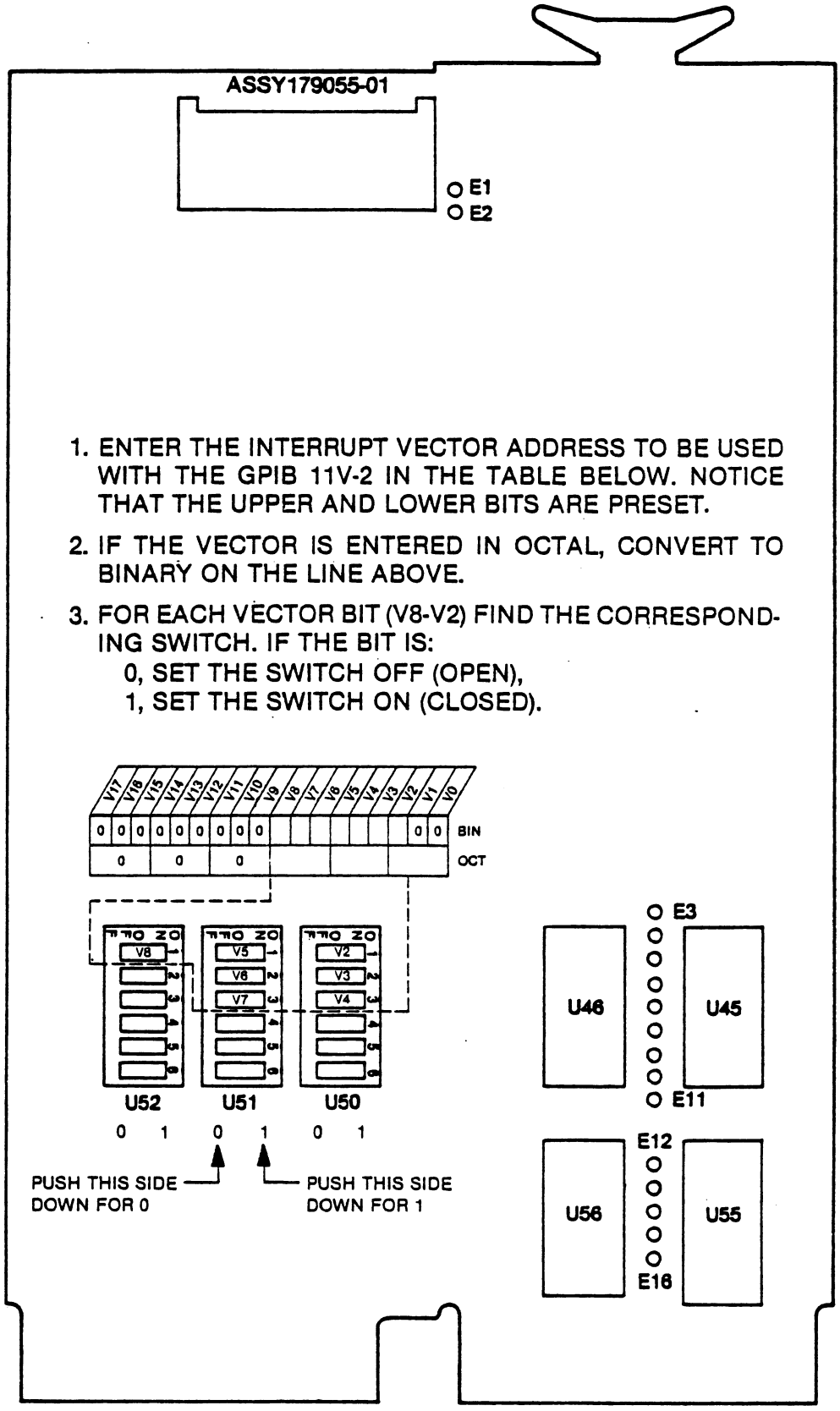


FIGURE 3.3

SETTING THE GPIB11V-2 INTERRUPT VECTOR

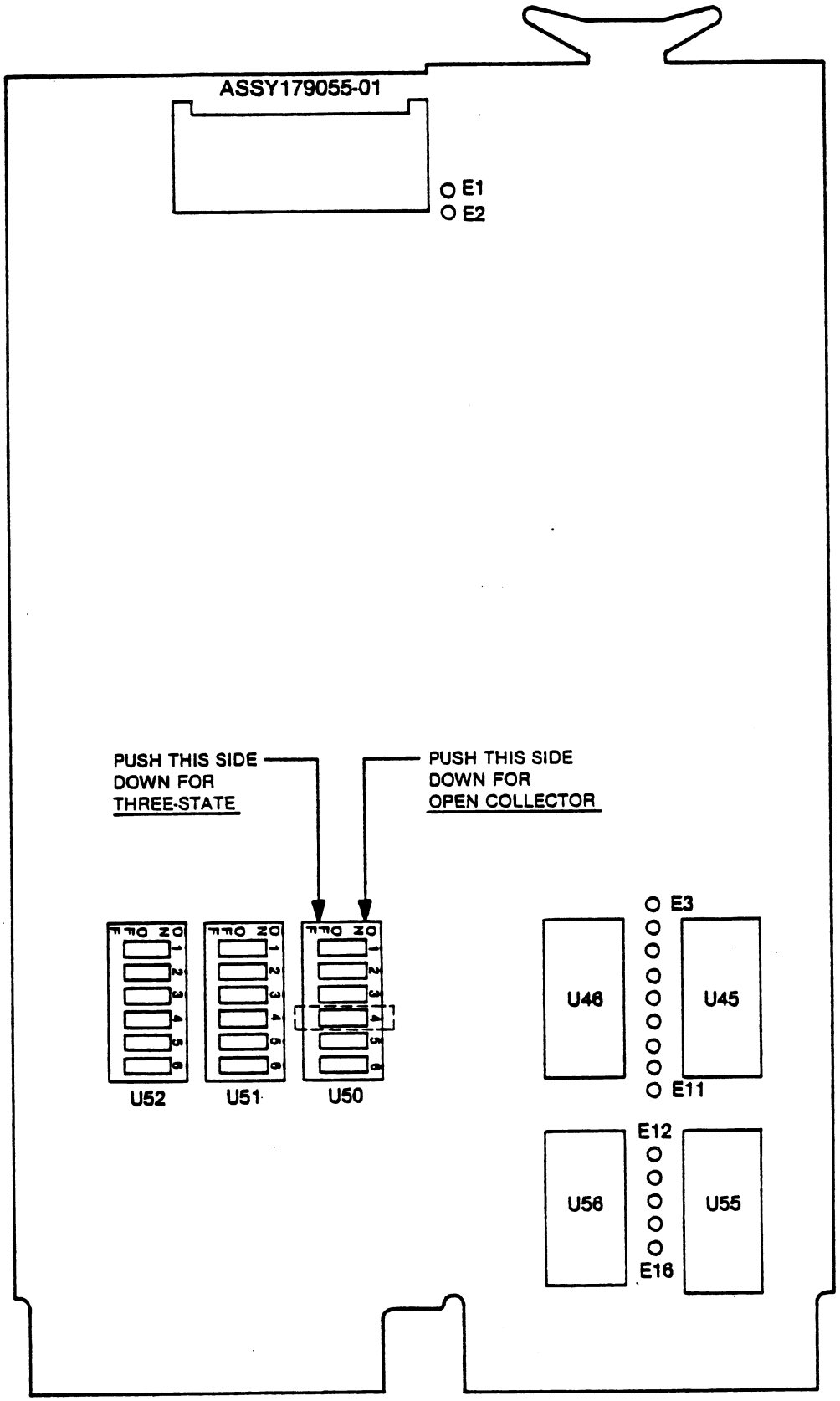


FIGURE 3.4

SETTING THE GPIB11V-2 THREE-STATE/OPEN COLLECTOR OPTION

3.2.5 Q-BUS Interrupt Priority

The GPIB11V-2 suports full, 4-level interrupt capability in either position-dependent or position-independent configuration as described in the DEC Microcomputer Processor Handbook. The interface, as shipped, is set to interrupt at priority level 4 in the position-independent configuration. That is, BIRQ4 is asserted while BIRQ5-7 are monitored. If another interrupt scheme is desired, the user must remove and/or add jumpers as shown in Figure 3.5 or Figure 3.6.

Figure 3.5 shows the jumper arrangements for a position-independent Q-BUS configuration. In this configuration, the peripheral devices on the bus are not arranged in order of interrupt priority. Therefore, each device must monitor higher level interrupt request signals before asserting its own signal or signals, as follows.

Interrupt Level	Position-Independent Device Monitors	Asserts
4	BIRQ5,6,7	BIRQ4
5	BIRQ6,7	BIRQ4,5
6	BIRQ7	BIRQ4,6
7	None	BIRQ4,6,7

Figure 3.6 shows the jumper arrangements for a position-dependent Q-BUS configuration. In this configuration, the peripheral devices on the bus are physically arranged in order of priority, with the highest priority device closest to the processor. None of the devices needs to monitor the interrupt request lines since the interrupt acknowledge signal (BIAK) is received and passed in physical order of priority and the first device requesting an interrupt inhibits BIAK from passing to the following devices. Each device monitors and asserts request lines as follows:

Interrupt Level	Position-Dependent Device Monitors	Asserts
4	none	BIRQ4
5	none	BIRQ4,5
6	none	BIRQ4,6
7	none	BIRQ4,7

3.2.6 GPIB Addresses

The software driver routine supplied with the GPIB11V-2 kit contains user-editable parameters for assigning the primary GPIB address for Talk and Listen functions. In addition, the user can select normal or extended addressing, and if the latter, the secondary address of the interface. (Refer to the Software Reference Manual for additional information.)

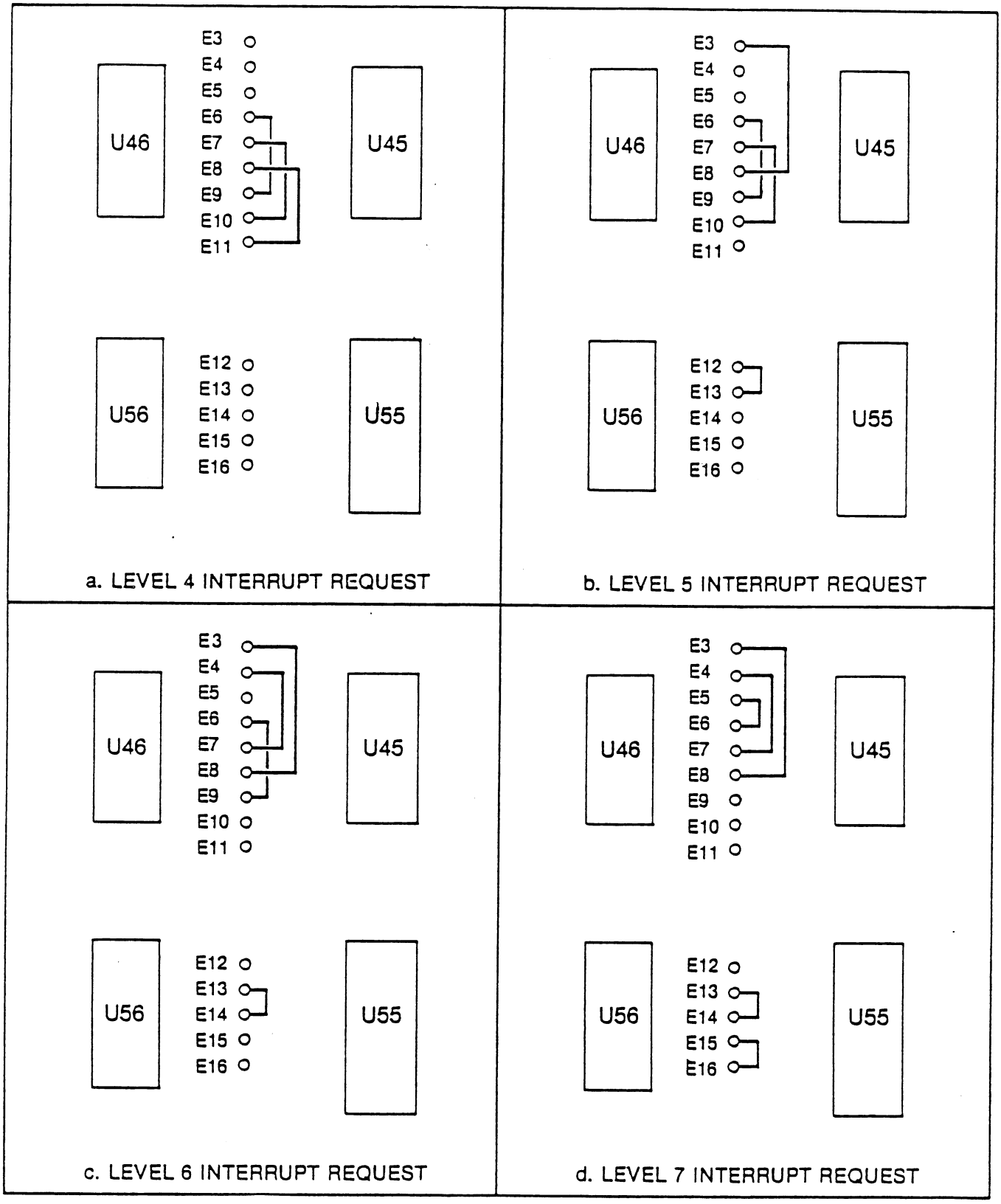


FIGURE 3.5

SETTING THE CPIB11V-2 PRIORITY INTERRUPT REQUEST JUMPERS -
POSITION-INDEPENDENT CONFIGURATION

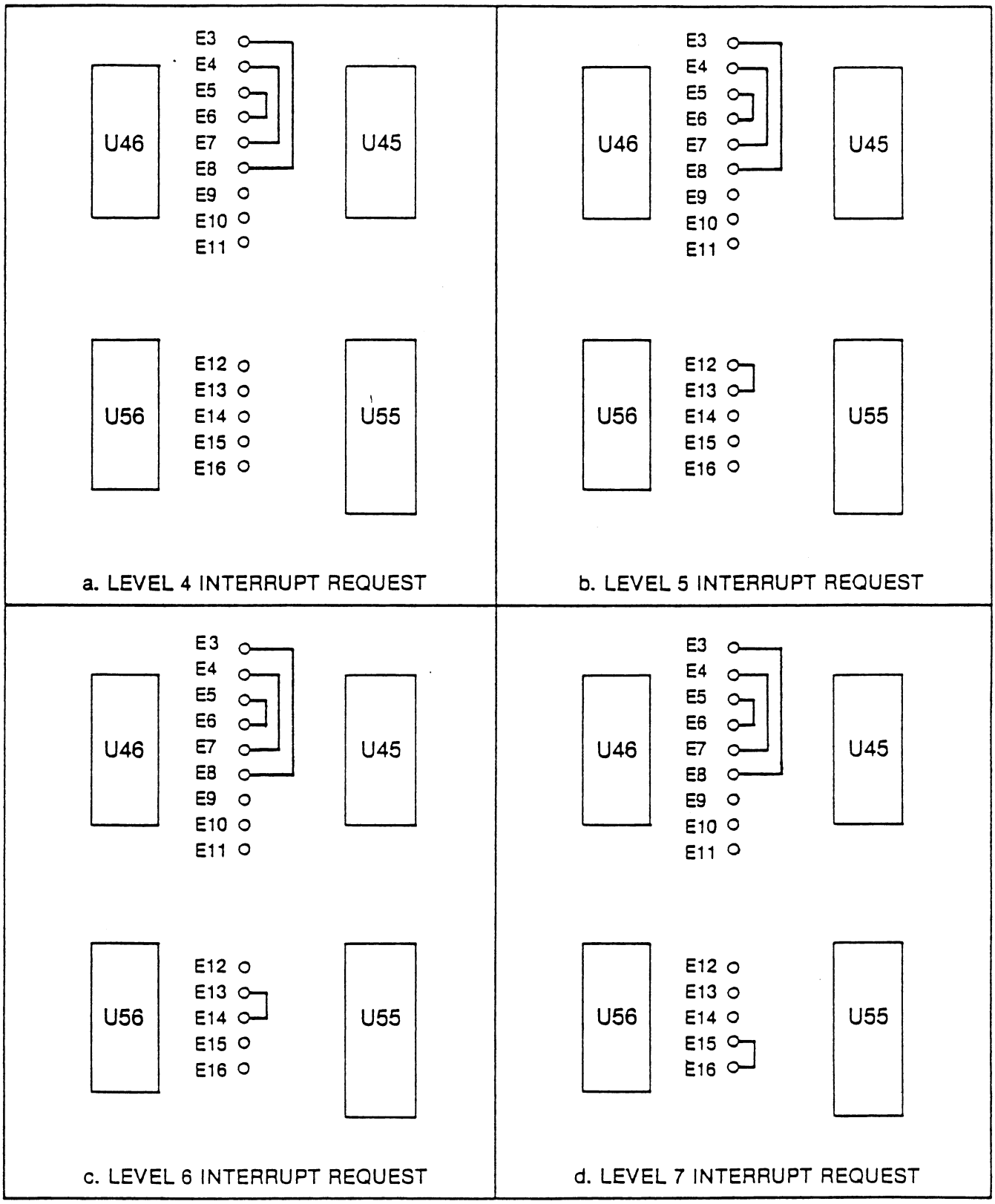


FIGURE 3.6

SETTING THE GPIB11V-2 PRIORITY INTERRUPT REQUEST JUMPERS -
POSITION-DEPENDENT CONFIGURATION

3.2.7 System Controller

The software driver routine also contains an editable parameter that allows the user to specify the GPIB11V-2 as the GPIB System Controller. When so selected, the GPIB11V-2 assumes the role of System Controller and enters the System Controller active state when the user's operating program executes an Interface Clear command. (Refer to the Software Reference Manual for additional information.)

3.3 Installation

The GPIB11V-2 is mounted in a dual-height Q-BUS slot. Power connections to the GPIB11V-2 are provided by the associated LSI-11 system power supply or an expansion chassis power supply. A listing of all signal names used by the GPIB11V-2 from the Q-Bus slot and their associated pin numbers is shown in Table 3.1. Software installation is covered in the Software Reference Manual.

3.4 Cabling

A cable that connects the interface to the GPIB is supplied with the GPIB11V-2 kit. The 26-pin Berg minilatch connector is connected to the shielded right-angle header mounted on the GPIB11V-2 circuit board. The piggy-back connector end is connected to another device on the GPIB. Other devices may be connected to the GPIB by using the bus cables listed in Table 1.3.

TABLE 3.1

GPIB11V-2 Q-BUS PIN ASSIGNMENTS

Signal Name*	Q-BUS Pin Number (row:pin:side)
Data/Address:	
BDAL0 L	AU2
BDAL1 L	AV2
BDAL2 L	BE2
BDAL3 L	BF2
BDAL4 L	BH2
BDAL5 L	BJ2
BDAL6 L	BK2
BDAL7 L	BL2
BDAL8 L	BM2
BDAL9 L	BN2
BDAL10 L	BP2
BDAL11 L	BR2
BDAL12 L	BS2
BDAL13 L	BT2
BDAL14 L	BU2
BDAL15 L	BV2
BDAL16 L	AC1
BDAL17 L	AD1
BDAL18 L	BC1
BDAL19 L	BD1
BDAL20 L	BE1
BDAL21 L	BF1
Power:	
GND	AC2
GND	AJ1
GND	AT1
GND	BJ1
GND	BM1
GND	BT1
+5 VDC	AA2
+5 VDC	BA2
+5 VDC	BV1

Signal Name*	Q-BUS Pin Number (row:pin:side)
Data Transfer Control:	
BBS7 L	AP2
BDIN L	AH2
BDOUT L	AE2
BRPLY L	AF2
BSYNC L	AJ2
BWTBT L	AK2
Direct Memory Access Control:	
BDMGI L	AR2
BDMGO L	AS2
BDMR L	AN1
BSACK L	BN1
Interrupt Control:	
BIAKI L	AM2
BIAKO L	AN2
BIRQ4 L	AL2
BIRQ5 L	AA1
BIRQ6 L	AB1
BIRQ7 L	BP1
System Control:	
BINIT L	AT2

*Note: Only these Q-BUS signals are used by the GPIB11V-2.

CHAPTER 4

PROGRAMMING INFORMATION

4.1. SCOPE

This section describes the general programming concepts for controlling the GPIB11V-2.

4.2 INTERFACE REGISTERS

All software control of the GPIB11V-2 is performed by means of four registers with Q-BUS addresses, 16 internal registers that are accessed using the direct memory access (DMA) logic of the interface board, and four "hidden" registers that are accessed through one of the internal registers.

These registers and their contents are discussed in the following three sections. Registers are referenced by three character mnemonics, such as BCR for Byte Count Register, and by a register number, which is essentially its relative address. The BCR, for example, is register 0 of the four Q-BUS addressable registers. Register contents are referenced by the mnemonic, bit position(s), read/write accessability, and signature. Thus, the device's secondary GPIB address, SAD5-1, is located in bits 4 through 0 of the internal write-only Address 1 Register (or AD1[4-0]w).

For the purposes of the following register and bit descriptions only, the terms true, set, one, on, high, and asserted are all synonymous, as are the terms false, clear, zero, off, low, and unasserted.

The asterisk symbol (*) denotes a logical AND operation within a logical expression. A plus sign (+) denotes a logical OR operation. The unary operator (~) denotes negation.

The "initialized" states of the device registers are affected by several signals. The mnemonic INIT refers to asserting the Q-BUS BINIT signal, either by means of an initialization switch or by executing a RESET instruction. The mnemonic LMR refers to asserting Local Master Reset, CSR[7]w. MR, or Master Reset, is the logical OR of INIT and LMR. PON (Local Power On) and IR (Internal Reset) are programmable subsets of the MR function. GPIB IFC refers to receiving the GPIB Interface Clear message when the interface is not the System Controller. See Section 4.4 for additional information.

4.2.1 Q-BUS Addressable Registers

The Q-BUS registers occupy four consecutive address locations in the octal range 760000 to 777776 with typical selections shown in Table 4.1. These address assignments are switch selectable as explained in Section 3.2.1 of this manual. The four device registers are shown in Figure 4.1.

TABLE 4.1

TYPICAL GPIB11V-2 Q-BUS REGISTER ASSIGNMENTS

Register	Mnemonic	Register No.	Typical Address
Byte Count Register	BCR	0	767710
Bus Address Register	BAR	2	767712
Control Status Register	CSR	4	767714
Carry Cycle Function/ Extended Address Register	CCF/XAR	6	767716

BAR (0)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	BC 15	BC 14	BC 13	BC 12	BC 11	BC 10	BC9	BC8	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0

BCR (2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	BA 15	BA 14	BA 13	BA 12	BA 11	BA 10	BA9	BA8	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0

CSR (4)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IFC	NEX	INT	SRQ	DAV	OC	ATN	CIC	DONE	IE	1	1	1	1	1	1
W	IFC	REN	DMA EN	SRQ IE	TCS	EOI	ATN	CIC	LMR	IE			ECC	SEL	OUT	GO

CCF/XAR (6)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	1	1	BA 21	BA 20	BA 19	BA 18	BA 17	BA 16	1	1	1	1	1	1	1	1
W			BA 21	BA 20	BA 19	BA 18	BA 17	BA 16	CC2	CC1	CC0	CF4	CF3	CF2	CF1	CF0

FIGURE 4.1

GPIB11V-2 BUS REGISTERS

BCR 0 Byte Count Register

BCR [15-0]rw BC15-0 Byte Count

This register is loaded with the two's complement of the number of bytes to transfer betwen memory and the GPIB, or between memory and internal GPIB11V-2 registers, under DMA control. The count is incremented by one as each byte is transferred. If the DMA operation terminates abnormally, this register may be examined to determine the actual number of bytes transferred. When a DMA operation between memory and the internal registers is performed (CSR[2]w, SEL=1) the BCR splits into two byte registers. The upper byte, BC[15-8], contains the 8-bit two's complement of the number of bytes to transfer. The least significant three bits of the low byte, BC[2-0], specify the internal register address, which is incremented for each byte transferred.

The BCR is unaffected by MR, PON, or IR. It must be explicity programmed.

BAR 2 Bus Address Register

BAR [15-0] rw — BA15-0 Bus address

This register is loaded with the memory address of the first byte to transfer in or out under DMA control. The address is incremented by one as each byte is transferred, with the carry, if any, being propogated to the extended bus address bits BA21-16 (see CCF/XAR[13-8]). When the DMA terminates, this register will contain the address of the byte following the last byte transferred.

The BAR is unaffected by MR, PON, or IR. It must be explicity programmed.

CSR 4 Control Status Register

CSR[15]rw IFC Interface Clear

The read bit is cleared by MR and by reading the CSR. This bit is set whenever the interface is not the System Controller and the GPIB IFC message is received. This occurrence will terminate a GPIB DMA (SEL=0) that is in progress. If IE (CSR[6]) is set when IFC becomes true an interrupt will be generated. IFC will not interrupt an internal register DMA (SEL=1). Reading the CSR clears this bit if the GPIB IFC message has ceased being transmitted. If the interface is the System Controller this bit will always read as 0.

The write bit is cleared by MR and GPIB IFC. This bit is set/cleared to assert/unassert the GPIB IFC line. The GPIB11V-2 is enabled as the System Controller when a 1 is written to this bit. The interface will remain the System Controller until Local Master Reset (CSR[7]w) or INIT is asserted. The interface is not the System Active Controller prior to the assertion of the IFC bit. This bit should not be written to with a 1 unless the interface is intended to be the System Active Controller. If a GPIB DMA (SEL=0) is in progress when IFC is set it will terminate. IFC should be asserted for minimum of 100 microseconds to conform to the IEEE Std 488.

CSR[14]r NEX Non-existent Memory

Cleared by MR and by reading the CSR. This bit is set if a DMA operation terminates due to a Q-BUS time out. This occurs if the BAR/XAR points to a non-existent Q-BUS address during a DMA cycle. NEX will terminate a GPIB DMA as well as an internal register DMA.

CSR[14]w REN Remote Enable

Cleared by MR. This bit may be set/cleared to assert/unassert the GPIB REN line when the interface is the System Controller. Writing to this bit has no effect when the interface is not the System Controller. After clearing this bit it should not be set again for at least 100 microseconds to conform to the IEEE Std 488.

CSR[13]r INT Interrupt

Cleared by MR. This bit is set if a mask selected GPIB condition has occurred. This bit essentially duplicates the INT bit of the second internal Interrupt Status Register, ISR2[7]r, and is included in the CSR for convenience. The occurrence of a selected GPIB condition will stop a GPIB DMA

(SEL=0) that is in progress. To terminate the DMA from this stopped condition, it is necessary to clear DMA EN (CSR[13]w).

CSR[13]w DMA EN — DMA Enable

Cleared by MR. This bit must be set in order to enable the DMA controller, although the DMA does not actually begin until GO (CSR[0]w) is set. Clearing DMA EN during a DMA will cause the DMA to stop immediately, simultaneously setting DONE (CSR[7]r). In this way a DMA to an unresponsive GPIB device can be aborted without having to reset the entire interface (refer to Section 4.4 on reset procedure).

CSR[12]r SRQ — Service Request

This bit follows the state of the GPIB SRQ line whenever the CIC (CSR[8]) is true. If SRQ IE (CSR[12]w) and IE (CSR[6]) are set when SRQ is asserted, an interrupt will be generated. If CIC is not set, SRQ will read as zero.

CSR[12]w SRQ IE — Service Request Interrupt Enable

Cleared by MR and GPIB IFC. Setting this bit and IE will allow an interrupt to occur when SRQ is asserted if CIC is set also.

CSR[11]r DAV — Data Valid

This bit follows the state of the GPIB DAV line and may be read to determine the state of the Source and Acceptor Handshakes.

CSR[11]w TCS — Take Control Synchronously

Cleared by INIT and GPIB IFC. This bit may be set along with GO to hold off DONE (CSR[7]r) and the DONE interrupt, until DAV becomes unasserted. This is the normal mode of operation for the interface, as Active Controller, to regain control after a Listen function. Synchronous take control after a Listen function also requires that the Acceptor Handshake be held off. See the description of the hidden register, AUXA.

CSR[10]r OC Open Collector

This bit monitors the state of the GPIB driver three-state/open collector selection switch (U50, Switch 4), according to the following truth table.

OC	GPIB signals that are driven Open Collector:	Three-State:
0	NRFD, NDAC, RQ, REN	DIO1-8, ATN, EOI, DAV, IFC
1	All	None

CSR[10]w EOI End or Identify

Cleared by MR and GPIB IFC. This bit may be set/cleared to assert/unassert the GPIB EOI line when the interface is the Controller-in-charge. When set along with ATN, the GPIB IDY message is generated, thus performing a Parallel Poll. The poll response should be read in the Command Pass Through internal register (CPT) before clearing EOI. The interface contains built-in delays to ensure the Parallel Poll sequence conforms to the IEEE Std 488. Setting EOI has no effect unless ATN is set also. The Parallel Poll feature is only available on open collector GPIBs. Unless OC=1, the IDY message must not be generated.

Note: When the GPIB11V-2 is the Controller-in-charge, it will not respond to its own Parallel Poll. Also, in order to read the proper poll response the TON bit (ADM[7]w) must be cleared.

CSR[9]rw ATN Attention

Cleared by MR and GPIB IFC. This bit is used to send the uniline Attention message, ATN, when the interface is the Controller-in-charge of the GPIB. This bit should not be set unless the proper take control protocol is followed or it will result in a violation of the IEEE Std 488. When the interface is not asserting ATN, this bit follows the state of the GPIB ATN line. Setting this bit after a Talk or Listen operation will implement an asynchronous take control (tca). To perform a synchronous take control (tcs) the interface should be a Listener and the Acceptor Handshake should be held off (in the Acceptor Not Ready for Data State, ANRS) prior to setting ATN (see hidden auxiliary register A, AUXA). DAV may be read to determine if the handshake is in fact held off, or TCS may be set to insure that DONE is set synchronously. The interface logic contains built-in delays when setting and clearing ATN to ensure the timing conforms to the IEEE Std 488.

When ATN is asserted by the interface the features usually associated with the Talker function are applied to the

Controller function. In particular, command bytes may be sent in the same way as data bytes are sent as a Talker, using the TON capability for example. However, when ATN is asserted by the interface it will not be able to respond to its own command bytes.

CSR[8]rw CIC Controller In Charge

Cleared by INIT and GPIB IFC. This bit reflects the status of the interface as Controller-in-charge. It should be set whenever control is passed to the interface by another GPIB Controller or when control is usurped via IFC if the interface becomes the System Controller. It should be cleared when control is successfully passed to another Controller. It is automatically cleared if another Controller is the System Controller and sends IFC. When the CIC bit is set it allows the interface to sense the GPIB SRQ line. Otherwise, the SRQ bit will read as zero.

CSR[7]r DONE DMA Operation Complete

Cleared by setting GO (CSR[0]w). Set by MR and completion or termination of a DMA operation. If IE is set when DONE becomes true an interrupt will be generated. A DMA operation completes normally when the BCR increments to zero. It completes abnormally when NEX is detected or if DMA EN is cleared. Upon normal completion of a GPIB DMA, DONE is deferred until DAV becomes unasserted if TCS was set along with GO when the DMA was initiated. Receiving GPIB IFC will terminate a GPIB DMA but not an internal register DMA (See SEL).

CSR[7]w LMR Local Master Reset

Writing a 1 to LMR resets the interface to its initialized state as described in Sections 4.2 and 4.4. LMR provides a way to selectively initialize the interface without a Q-BUS BINIT signal. LMR is ORed with INIT to get MR. Any DMA in progress is aborted immediately.

CSR[6]rw IE Interrupt Enable

Cleared by MR. Setting IE allows the following conditions to cause an interrupt:

1. The DMA operation completes normally or terminates abnormally; and DONE gets set, perhaps along with IFC or NEX.

2. GPIB SRQ is asserted and SRQ IE and CIC have been set.

3. GPIB IFC is asserted and the interface is not the System

Controller (IFC reads as one).

4. One or more of the 12 conditions or events represented by the internal Interrupt Status/Mask Registers has occurred (INT reads as one).

CSR[5-4]rw
CSR[3-0]r

Unused

These bits read as ones. Writing to bits 4 and 5 has no effect.

CSR[3]w ECC Enable Carry Cycle

Cleared by MR. This bit is used to enable the carry cycle function performed during a DMA. If ECC is set, the contents of the CCF byte (low byte of the CCF/XAR register) are written to the AUX internal register just prior to performing the last DMA cycle. For DMA out, loading the CCF with octal 006 specifies that the uniline message, END (EOI * ~ATN), is to be sent along with the last data byte. For DMA in, loading CCF with octal 201 specifies that the Acceptor Handshake is to be held up (in ANRS) after the last byte is input. (See hidden Auxiliary register A, AUXA).

CSR[2]w SEL DMA Location Selection

Cleared by MR. SEL specifies whether the DMA operation is between memory and the GPIB or between memory and the GPIB11V-2's internal registers as follows:

SEL	DMA is Between Q-BUS Memory And
0	GPIB
1	Internal Registers

CSR[1]w OUT DMA Direction

Cleared by MR. This bit specifies the direction of the DMA data transfer with respect to Q-BUS memory, according to the following:

OUT	Data Transfer Is	Type of Bus Cycle
0	Into Q-BUS Memory	Write (DATO)
1	Out of Q-BUS Memory	Read (DATI)

In Q-BUS terminology, data transfer directions are referenced to the device that is bus master. When reading or writing to the four Q-BUS registers, the processor is the master and the GPIB11V-2 is the slave. During DMA

transfers, the GPIB11V-2 is the master and the Q-BUS memory device is the slave. A DMA DATO, therefore, is a bus write cycle and a DMA DATI is a bus read cycle.

CSR[0]w GO Start DMA

Writing a one to this bit initiates a DMA operation if DMA EN is also set. Writing a zero to this bit has no effect. While a DMA is in progress, GO should not be set again or the DMA will malfunction. GO may be set at the same time as the rest of the bits in the CSR that configure the DMA operation.

CCF/XAR 6 Carry Cycle Function/Extended Address Register

The CCF/XAR is a dual purpose register. The lower byte is used to pass the Carry Cycle Function code to one of the internal registers. The upper byte, the XAR, is an extension of the BAR when processors with more than 16 address bits are used.

CCF/XAR [15-14]rw Unused

These bits read as ones. Writing to them has no effect.

CCF/XAR [13-8]rw BA 21-16 Extended Bus Address

The XAR is cleared by MR. These bits are used with processors and memory capable of operating up to 22 address bits. They are latched into the extended address counter when the CCF/XAR is loaded. The counter is incremented by the overflow carry from the BAR.

The LSI-11 and LSI-11/2 processors use 16 bit addressing, while the LSI-11/23 uses 18 bit addressing. Future processors are expected to use 22 bit addressing. The GPIB11V-2 is designed to operate with any current or future addressing scheme without hardware modification. The user should set unused address bits in the XAR to zero when configuring the Q-BUS registers for a DMA operation.

CCF/XAR [7-0]r Unused

These bits read as ones.

CCF/XAR [7-5]w CC2-0 Carry Control Code

CCF/XAR [4-0]w CF4-0 Carry Function Code

The CCF register holds the byte to be written to the internal Auxiliary Function Register, AUX, just prior to the last DMA transfer if the Enable Carry Cycle bit, ECC, of the CSR has been set for the DMA. See the AUX register description in Section 4.2.2. The CCF register is unaffected by MR, PON, and IR. It must be explicitly programmed.

4.2.2 Internal Registers

The GPIB11V-2 internal registers are shown in Figure 4.2 and are explained on the following pages. Unlike the four Q-BUS registers that are directly accessible to the user through simple read/write instructions, the internal registers, which contain most of the programming information necessary to operate the GPIB11V-2, are accessible only through DMA operations and only if the Q-BUS registers are correctly configured. To access the internal registers, the user must, as a minimum:

1. Set BCR[15-8] to the two's complement of the number of bytes to transfer to the internal registers.

2. Set BCR[2-0] to the first internal register to be addressed.

3. Set BAR[15-0] and if necessary CFF/XAR[21-16] to the memory address of the data array to be transferred.

4. Set CSR[13]w, DMA EN.

5. Set CSR[6], IE, if an interrupt is desired upon DMA completion.

6. Set CSR[2]w, SEL.

7. Set or clear CSR[1]w, OUT, to write to or read from the internal registers, respectively.

8. Set CSR[0]w, GO.

	7	6	5	4	3	2	1	0		
R	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0	DIR	(0)
W	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0	DOR	
R	CPT	APT	GET	END	DEC	ERR	BO	BI	ISR1	(1)
W	CPT IE	APT IE	GET IE	END IE	DEC IE	ERR IE	BO IE	BI IE	IMR1	
R	INT	SPAS	LLO	REM	SPASC	LLOC	REMC	ADSC	ISR2	(2)
W	0	0	DMAO	DMAI	SPASC IE	LLOC IE	REMC IE	ADSC IE	IMR2	
R	S8	SRQS	S6	S5	S4	S3	S2	S1	SPS	(3)
W	S8	RSV	S6	S5	S4	S3	S2	S1	SPM	
R	TON	LON	EOI	LPAS	TPAS	LA	TA	MJMN	ADS	(4)
W	TON	LON	0	0	0	0	ADM1	ADM0	ADM	
R	CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0	CPT	(5)
W	C2	C1	C0	F4	F3	F2	F1	F0	AUX	
R	X	DPT	DPL	PAD5	PAD4	PAD3	PAD2	PAD1	ADO	(6)
W	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1	ADR	
R	X	DST	DSL	SAD5	SAD4	SAD3	SAD2	SAD1	AD1	(7)
W	E7	E6	E5	E4	E3	E2	E1	E0	EOS	

FIGURE 4.2

GPIB11V-2 INTERNAL REGISTERS

DIR 0 Data-in Register

DIR[7-0]r DIR7-0 Data-in Byte

The DIR is used to move data from the GPIB to the Q-BUS when the interface is a Listener. Incoming information is separately latched by this register and is not destroyed by a write to the data-out register, DOR. The ready for data message, GPIB RFD, is held false until the byte is removed from the DIR, either by a DMA from the DIR (SEL=1) or by a DMA in from the GPIB (SEL=0). The Acceptor Handshake (AH) then completes automatically. In RFD hold off mode (see hidden auxiliary register A, AUXA) the handshake is not finished until the internal Finish Handshake (FH) command (AUX = octal 003) is issued telling the interface to release the holdoff. In this way, the same byte may be read several times, or an anxious Talker may be held off until all available data has been processed.

With SEL=1, a DMA in from the DIR essentially effects a per character GPIB mode of operation. With SEL=0, a DMA in operation automatically accesses the DIR to fetch successive GPIB bytes and store them into memory.

The DIR is unaffected by MR, PON, or IR.

DOR 0 Data-out Register

DOR[7-0]w DOR7-0 Data-out Byte

The DOR register is used to move data from the processor to the GPIB when the interface is the Talker or the Controller. Outgoing data is separately latched by this register and is not destroyed by a read from the DIR. When a byte is written to the DOR, the Source Handshake (SH) is initiated and the byte is transferred to the GPIB.

With SEL=1, a DMA out to the DOR essentially effects a per character GPIB mode of operation. With SEL=0, a DMA out operation automatically loads the DOR with successive bytes fetched from memory to transfer them to the GPIB.

The DOR is unaffected by MR, PON, or IR.

IMR1	1	Interrupt Mask Register 1
ISR1	1	Interrupt Status Register 1
IMR2	2	Interrupt Mask Register 2
ISR2	2	Interrupt Status Register 2

The Interrupt Status Registers are cleared when read and by MR, PON, or IR. The state of the Interrupt Mask Registers following these signals is undefined. With the Interrupt Mask Registers, the interface can be configured to generate an interrupt on the occurrence of any of 12 conditions or events on the GPIB. Upon receipt of an interrupt, the processor must read the Interrupt Status registers to determine which event has occurred. Each of the 12 interrupt status bits has a matching enable bit in the associated Interrupt Mask Register. Setting any of these mask bits enables the corresponding status bit to generate an interrupt (IE must be set to actually generate the interrupt). Bits in the Interrupt Status registers are set regardless of the states of the enable bits. If an event occurs while an Interrupt Status Register is being read, the event is typically held until after the register is cleared and then placed in the register.

ISR1[7]r CPT Command Pass-Through
IMR1[7]w CPT IE Command Pass-Through Interrupt Enable

The CPT bit flags the occurrence of an undefined command and of each subsequent secondary command when the Command pass-through feature is enabled (by the CPT ENAB bit of the hidden Auxiliary Register B, AUXB). Any message not decoded by the interface hardware is treated the same as an undefined command (for example, the take control command, TCT). However, any addressed command is automatically ignored when the interface is not addressed.

Undefined commands are read by the processor in the CPT internal register. The interface will hold off the Acceptor Handshake in the Accept Data State (ACDS) until the Valid Secondary Command function code, VSC, is written in the AUX register (AUX = octal 017). If the CPT feature is not enabled, undefined commands are simply ignored.

ISR1[6]r APT Address Pass-Through
ISR1[6]w APT IE Address Pass-Through Interrupt Enable

The APT bit indicates to the processor that a secondary address has been received and is available in the CPT register for inspection. APT will only occur if Mode 3 addressing is in effect. In Mode 2, secondary addresses will be recognized automatically. In Mode 1 they will be ignored (see internal register ADM).

The interface will hold off the Acceptor Handshake in ACDS until the VSC or NVSC (Non-Valid Secondary Command, AUX =

octal 007) function code is written in the AUX register to signal that the Secondary address is valid or not valid, respectively.

ISR1[5]r GET Group Execute Trigger
IMR1[5]w GET IE Group Execute Trigger Interrupt Enable

The GET bit indicates that the Group Execute Trigger (GET) command has been received while the interface was a Listener.

ISR1[4]r END End Received
IMR1[4]w END IE End Received Interrupt Enable

The END bit is set when the interface is a Listener and the uniline message, END (EOI * ~ATN), is received or the data byte in the DIR matches the contents of the EOS register (the latter feature is enabled by the REOS bit of the hidden Auxiliary register A, AUXA)

ISR1[3]r DEC Device Clear
IMR1[3]w DEC IE Device Clear Interrupt Enable

The DEC bit indicates that the Device Clear (DCL) command has been received or that the Selected Device Clear (SDC) command has been received while the interface was a Listener.

ISR1[2]r ERR Error
IMR1[2]w ERR IE Error Interrupt Enable

The ERR bit indicates that a possible GPIB error situation exists in that the interface is a Talker and there are no Listeners on the bus or the interface is the Controller-in-charge and there are no other devices on the bus. This condition is recognized when an attempt is made to send out a data byte or command byte.

ISR1[1]r BO Byte Out
IMR1[1]w BO IE Byte Out Interrupt Enable

The BO bit indicates that the interface is ready to accept another byte for transmission onto the GPIB, either a data byte as Talker or a command byte as Active Controller. The BO condition is cleared when a byte is written to the DOR and also when the interface ceases to be the active Talker or the Active Controller. If BO IE is true when the BO condition is asserted an interrupt will be generated. When performing a DMA out operation, BO IE should be clear so than an interrupt will not occur; instead, DMAO (ISR2[5]w) should be set to enable a DMA cycle when BO is asserted.

ISR1[0]r BI Byte In
IMR1[0]w BI EN Byte In Interrupt Enable

The BI bit indicates that the interface, as a Listener, has accepted a data byte from the GPIB. The BI condition is cleared when the byte is read from the DIR. Until it is read, the Acceptor Handshake will not be allowed to proceed past the Acceptor Not Ready for Data State, ANRS. If one of the holdoff functions is enabled in the hidden Auxiliary Register A, AUXA, the handshake will be held up even after the DIR is read. If BI IE is true when the BI condition is asserted an interrupt will be generated. When performing a DMA in operation, BI IE should be clear so that an interrupt will not occur; instead, DMAI (ISR2[4]w) should be set to enable a DMA cycle when BI is asserted.

ISR2[7]r INT Interrupt

This bit is the logical OR of all the enabled interrupt status bits in both ISRI and ISR2. There is no corresponding mask bit for INT. This bit may be read in the CSR also.

ISR2[7]w Unused

ISR2[6]r SPAS Serial Poll Active State

This bit is true whenever the interface is in the Serial Poll Active State (SPAS). This state occurs when another Controller is in charge of the GPIB and it serially polls the interface for a status byte. There is no corresponding mask bit for SPAS.

ISR2[6]w Unused

ISR2[5]r LLO Local Lockout

This bit is true whenever the interface is in a local lockout state (LWLS or RWLS). This state occurs when another Controller is in charge of the GPIB and it addresses the interface as a Listener and sends the local lockout (LLO) command. There is no corresponding mask bit for LLO.

IMR2[5]w DMAO DMA Out Enable

This bit must be set to allow a DMA out to the GPIB to operate. BO IE should be clear and DMAO should be set whenever a GPIB DMA out is initiated. In this way, the BO condition causes a DMA cycle to occur rather than an interrupt.

ISR2[4]r REM Remote

This bit is true whenever the interface is in a remote state (REMS or RWLS). This state occurs when the System Controller has asserted the Remote Enable line (REN), and the Controller-in-charge addresses the interface as a Listener. There is no corresponding mask bit for REM.

IMR2[4]w DMAI DMA In Enable

This bit must be set to execute a DMA in from the GPIB. The BI interrupt enable should be clear and DMAI should be set whenever a GPIB DMA in is initiated. In this way the BI condition causes a DMA cycle to occur rather than an interrupt.

ISR2[3]r SPASC Serial Poll Active State Change
IMR2[3]w SPASC IE Serial Poll Active State Change Interrupt Enable

SPASC is set whenever there is a change in the SPAS bit, ISR2[6]r. If SPASC IE is true when that occurs, an interrupt will be generated.

ISR2[2]r LLOC Local Lockout Change
IMR2[2]w LLOC IE Local Lockout Change Interrupt Enable

LLOC is set whenever there is a change in the LLO bit, ISR2[5]r. If LLOC IE is true when that occurs an interrupt will be generated.

ISR2[1]r REMC Remote Change
IMR2[1]w REMC IE Remote Change Interrupt Enable

REMC is set whenever there is a change in the REM bit, ISR2[4]r. If REMC IE is true when that occurs an interrupt will be generated.

ISR2[0]r ADSC Addressed Status Change
IMR2[0]w ADSC IE Addressed Status Change Interrupt Enable

ADSC is set whenever there is a change in the addressed status of the interface. This condition occurs when the Controller-in-charge addresses the interface as a Talker or Listener, or when it unaddresses the interface. If ADSC IE is true when that occurs, an interrupt will be generated. Bits 4 through 0 in the ADS register reflect the latest addressed status of the interface.

SPS	3	Serial Poll Status Register
SPM	3	Serial Poll Mode Register

SPS/SPM [7,5-0]rw — S8, S6-S1 — Serial Poll Status Byte

Cleared by MR and IR. These bits are available for sending status information over the GPIB when the interface is serially polled. When the interface is addressed as Talker and receives the multiline serial poll enable command message, SPE, it automatically transmits one byte of status information, SPM[7-0], onto the GPIB.

SPS[6]r — SRQS — Service Request State

This bit corresponds to the Service Request State (SRQS), which is entered when RSV is set. When a serial poll is conducted and the status byte is read by the Controller-in-charge the SRQS bit is cleared (also causing the interface to stop asserting the SRQ line). The RSV bit should then be cleared by the processor.

SPM[6]w — RSV — Request Service

Cleared by MR and IR. This is the local "rsv" or request service message. When set, the GPIB SRQ message is asserted. It should be cleared after the interface has been serially polled and, in any case, before attempting to request service again.

ADS 4 Address Status Register

The ADS contains information that can be used by the processor to monitor its own GPIB address status.

ADS[7]r TON Talk Only

This bit reflects the status of the programmable Talker-only function. The Talker-only function is used by the interface while it is the Controller-in-charge. See ADM[7]w.

ADS[6]r LON Listen Only

This bit reflects the status of the programmable Listen-only function. See ADM[6]w.

ADS[5]r EOI End or Identify

Cleared by MR and IR. This bit is true if the uniline END message (EOI * ~ATN) is asserted with the last data byte received by the interface.

ADS[4]r LPAS Listener Primary Active State

Cleared by MR, IR, and PON. This bit indicates that the interface has received its primary Listen address. In Mode 3 addressing the processor is thus informed that the secondary address being passed through represents the extended Listen address.

ADS[3]r TPAS Talker Primary Active State

This bit indicates that the interface has received its primary Talk address. In Mode 3 addressing, the processor is thus informed that the secondary address being passed through represents the extended Talk address.

ADS[2]r LA Listener Active

Cleared by MR and IR. Set or cleared by PON if LON (ADM[6]w) is set or cleared. This bit is true whenever the interface has been addressed or programmed as Listener (i.e., the interface is in the Listener Active State, LACS, or the Listener Addressed State, LADS).

If the interface is addressed to Listen, it will automatically be unaddressed to Talk; however, the interface may be programmed to simultaneously Talk and Listen.

ADS[1]r TA Talker Active

Cleared by MR and IR. Set or cleared by PON if TON (ADM[7]w) is set or cleared. This bit is true whenever the interface has been addressed or programmed as Talker (i.e., the interface is in the Talker Active State, TACS, the Talker Addressed State, TADS, or the Serial Poll Active State, SPAS). When the interface is the Controller-in-charge the Talker function is used to send command messages.

If the interface is addressed to Talk it will automatically be unaddressed to Listen; however, the interface may be programmed to simultaneously Talk and Listen.

ADS[0]r MJMN Major-Minor

This bit is used to determine whether the information in the other ADS bits applies to the Major or Minor Talker/Listener. It is set to "1" when the Minor Talker/Listener is addressed. It should be noted that only one Talker/Listener may be active at any one time. Thus, the MJMN bit will indicate which, if either, of the Talkers/Listeners is addressed or active. MJMN will always be zero unless a dual primary addressing mode (Mode 1 or Mode 3) is enabled.

ADM 4 Address Mode Register

ADM[7]w TON Talk Only

Setting this bit enables the programmable Talk function. It is used by the interface when it is the Controller-in-charge since the interface cannot respond to addressing information that it transmits as Active Controller. If TON is set, the address mode (ADM[1-0]w) must be zero. See also ADS[7]r.

Note: In changing to a programmed (as opposed to addressed) Talker/Listener Active State (LA/TA) using TON/LON, respectively, the local power on message, PON, must be sent to clear the current TA or LA state. See AUX register.

ADM[6]w LON Listen Only

Setting this bit enables the programmable Listen function. It is used by the interface when it is the Controller-in-charge since the interface cannot respond to addressing information that it transmits as Active Controller. If LON is set, the address mode (ADM[1-0]w) must be zero. See also ADS[6]r and note above.

ADM[5-2]w Unused

Writing to these bits has no effect.

ADM[1-0]w ADM1-0 Address Mode

These bits specify the addressing mode which is in effect; i.e., the manner in which the information in the internal address registers, AD0 and AD1, is to be interpreted. If both bits are 0 then the interface will not respond to any address commands. The TON and LON bits must be cleared if Mode 1, 2, or 3 addressing is selected.

In Mode 1 (ADM1=0, ADM0=1), AD0 and AD1 contain the major and minor addresses, respectively, for dual primary address applications. In applications where only one address is needed, the major Talker/Listener is used and the minor Talker/Listener should be disabled.

In Mode 2 (ADM1=1, ADM0=0), the interface recognizes two sequential address bytes, a primary followed by a secondary. Both address bytes must be received in order to enable the device to Talk or Listen. In this manner, Mode 2 addressing implements the Extended Talker and Listener functions as defined in IEEE Std 488, without requiring processor intervention. In Mode 2, AD0 and AD1 contain the primary and secondary addresses, respectively.

In Mode 3 (ADM1=1, ADM0=1), the interface handles addressing just as it does in Mode 1, except that each major or minor primary address must be followed by a secondary address. All secondary addresses must be verified by the processor when Mode 3 is used. When the interface is in TPAS or LPAS (Talker/ Listener Primary Addressed State), and a secondary address byte is on the DIO lines, the APT bit of ISR2 is set and the secondary address may be inspected in the CPT internal register. The Acceptor Handshake is held up in the Accept Data State (ACDS) until the VSC or NVSC function code is written to the AUX internal register, signalling a valid or invalid secondary address, respectively. ADM0 and ADM1 should both be cleared when either the programmable TON or LON, bit is set.

CPT 5 Command Pass Through Register

CPT[7-0]r CPT7-0 Command Pass Through Byte

This register is used to transfer undefined multiline command messages from the GPIB to the processor. When the CPT feature is enabled (AUXB[0]w, CPT ENAB = 1), any primary command group (PCG) message not decoded by the interface is treated as an undefined command. All secondary command group (SCG) messages following an undefined PCG message are also treated as undefined. In such a case, when an undefined message is encountered, it is held in this register and the Acceptor Handshake is held off (in ACDS) until the VSC function code is written to the AUX internal register. This register is also used to inspect secondary addresses when Mode 3 addressing is used. The Acceptor Handshake is held off (in ACDS) until the VSC or NVSC function code is written to the AUX internal register. The recommended use of the undefined command capabilities is for a Controller configured Parallel Poll and the Take Control (TCT) protocol. The PPC message is an undefined primary command typically followed by PPE, an undefined secondary command. For details on this procedure, refer to Section 4.3 on Parallel Poll Protocol and Section 4.5 on TCT protocol.

The CPT register follows the state of the GPIB DIO lines and may be inspected at any time. In particular, it is read during a Parallel Poll operation to fetch the Parallel Poll response.

AUX 5 Auxiliary Function Register

This register is used to perform special interface functions. It is also used to program the four hidden registers, AUXA, AUXB, PPR, and CLKR. Tables 4.2 and 4.3 list the control and function codes which are implemented. Writing an unimplemented code to the AUX register has no effect.

AUX[7-5]w C2-0 Control Code

These bits specify the control code; i.e., the manner in which the information in bits F4-0 is to be used. If C2-0 are all 0 then the special function selected by F4-0 is executed. Otherwise the hidden register selected by C2-0 is is loaded from the data in F4-0. See Table 4.2.

AUX[4-0]w F4-0 Function Code

These bits specify the function code of the special function if the control code is 0. Table 4.3 lists the implemented special functions. If the control code is not 0, then these bits are used to load one of the four hidden registers. See Table 4.2.

TABLE 4.2

AUXILIARY MODE AND HIDDEN REGISTERS

Control Code (AUX[7-5])			Function Code (AUX[4-0])					Description
C2	C1	C0	F4	F3	F2	F1	F0	
0	0	0	See Table 4.3					Execute the Special Interface Functions.
			Clock Register (1)					
0	0	1	0	CLK3	CLK2	CLK1	CLK0	Load CLKR[4-0] with F4-0.
			Parallel Poll Register (3)					
0	1	1	U	S	P3	P2	P1	Load PPR[4-0] with F4-0.
			Auxiliary Register A (4)					
1	0	0	BIN	XEOS	REOS	HLDE	HLDA	Load AUXA[4-0] with F4-0.
			Auxiliary Register B (5)					
1	0	1	RFDH ENAB	INV	TRI	SPEOI	CPT ENAB	Load AUXB[4-0] with F4-0.

TABLE 4.3

SPECIAL INTERFACE FUNCTIONS

The following functions are executed when the Auxiliary Mode Register (AUX) Control Code C2-0 is loaded with 0 and the Function Code F4-0 is loaded as shown below.

Function Code					Description (AUX[4-0])
F4	F3	F2	F1	F0	
0	0	0	0	0	Local Power On (PON) This function resets some internal interface functions (it is the local pon message as defined in IEEE Std 488) but leaves the DMA and Controller functions unaffected. PON forces the Source and Acceptor Handshakes functions back to the idle states. It also clears RSV (SPM[6]w) and the Parallel Poll register, PPR. PON sets/clears Talker Active State (or Listener Active State) if TON (or LON) is set/cleared, respectively. PON is also used to release the "initialize" state which takes effect on MR or IR. For more information, see Section 4.4.
0	0	0	1	0	Internal Reset (IR) This function is similar to an MR pulse except that only the internal registers are reset, while the DMA and Controller functions are unaffected. When IR is issued (or MR occurs) an "initialize" state takes effect and is not released until a PON special function is performed. In addition to the resetting described under PON, IR also resets all internal and hidden registers and clears the Parallel Poll Flag, ist. For more information, see Section 4.4.
0	0	0	1	1	Finish Handshake (FH) This command finishes a handshake that was stopped because of a holdoff on RFD or DAV. Refer to hidden Auxiliary Register A, AUXA.
0	0	1	0	0	Force Group Execute Trigger (FGET) Executing this function has the same effect as receiving a GET command issued by the Controller-in-charge of the GPIB, but does not cause a GET interrupt if GET IE (ISR1[5]w) is set.

TABLE 4.3 (continued)

0 0 1 0 1	Return to Local (RTL)

This function implements the local "rtl" message as defined by IEEE Std 488. If LLO (ISR2[5]r) is not set, the GPIB Talker/Listener Logic will go to a local state.

0 0 1 1 0	Send EOI (SEOI)

This command causes EOI to go true with the next byte transmitted. The EOI line is then cleared upon completion of the handshake for that byte.

0 0 1 1 1	Non-Valid Secondary Command or Address (NVSC)
0 1 1 1 1	Valid Secondary Command or Address (VSC)

This command informs the interface that the secondary address read by the processor was valid or invalid. When Mode 3 addressing is used, the processor must field each extended address which is passed through and respond to it, or the GPIB will malfunction. Note that the F3 bit is the valid flag. VSC also used to tell the interface to continue from the command pass through state.

0 0 0 0 1	Cleared Parallel Poll Flag (ist = 0)
0 1 0 0 1	Set Parallel Poll Flag (ist = 1)

Cleared by MR or IR. This is the local "ist" or individual status message defined by IEEE Std 488. If ist matches the sense bit, S, of the hidden Parallel Poll Register, PPR[3]w, the DIO line encoded in PPR[2-0]w is asserted true in response to a GPIB Parallel Poll IDY command (ATN * EOI). See Section 4.5 for additional information.

ADO 6 Address 0 Register

Cleared by MR and IR. In addressing Mode 2, this register contains the address and enable bits for the primary address of the interface. In dual primary addressing (Modes 1 and 3) this register contains the information for the major primary address.

ADO[7]r Unused

This bit will always read as 0.

ADO[6]r DPT Disable Primary Talk Address

If this bit is set it means the Mode 2 primary (or Mode 1 and 3 major) Talker is not enabled; i.e., the interface will not respond to a Talk address formed from bits PAD5-1.

ADO[5]r DPL Disable Primary Listen Address

If this bit is set it means the Mode 2 primary (or Mode 1 and 3 major) Listener is not eneabled; i.e., the interface will not respond to a Listen address formed from bits PAD5-1.

ADO[4-0]r PAD5-1 Mode 2 Primary GPIB Address

These bits specify the primary (or major) address of the interface. The primary Talk address is formed by adding octal 100 to PAD5-1, while the Listen address is formed by adding octal 40.

ADR 6 Address Register

This register is used to load the internal registers, AD0 and AD1. Both these registers must be loaded for all addressing modes.

ADR[7]w ARS Address Register Select

This bit is 0 or 1 to select whether the remaining bits are to be loaded into internal registers AD0 or AD1, respectively.

ADR[6]w DT Disable Talker

This bit should be set if the Talk address formed from AD5-1 (ADR[4-0]w) is not to be enabled.

ADR[5]w DL Disable Listener

This bit should be set if the Listen address formed from AD5-1 is not to be enabled.

ADR[4-0]w AD5-1 Address

These bits specify the GPIB address that is to be recognized. The corresponding Talk address is formed by adding octal 100 to AD5-1, while the corresponding Listen address is formed by adding octal 40. AD5-1 should not all be 1, since the corresponding Talk and Listen addresses would conflict with the GPIB Untalk (UNT) and Unlisten (UNL) commands.

AD1 7 Address 1 Register

Cleared by MR and IP. This register contains the address and enable bits for the secondary address of the interface if Mode 2 addressing is used, or the minor primary address of the interface if dual primary addressing is used (Modes 1 and 3). If Mode 1 addressing is used and only a single primary address is needed then both the Talk and Listen addresses should be disabled in this register. If Mode 2 addressing is used then the Talk and Listen disable bits in this register should match those in the AD0 register.

AD1[7]r Unused

This bit will always read as 0.

AD1[6]r DST Disable Secondary Talk Address

If this bit is set it means the Mode 2 secondary (or Mode 1 and 3 minor) Talker is not enabled; i.e., the interface will not respond to a secondary address (or minor primary talk address) formed from bits SAD5-1. If DST is 0 the secondary address is checked only if the interface received its primary Talk address (i.e., is in TPAS).

AD1[5]r DSL Disable Secondary Listen Address

If this bit is set it means the Mode 2 secondary (or Mode 1 and 3 minor) Listener is not enabled; i.e., the interface will not respond to a secondary address (or minor primary Listen address) formed from bits SAD5-1. If DSL is 0 the secondary address is checked only if the interface received its primary Listen address (i.e., is in LPAS).

AD1[4-0]r SAD5-1 Mode 2 Secondary GPIB Address

These bits specify the secondary address of the interface if Mode 2 addressing is in effect. They specify the minor primary address of the interface if dual primary addressing (Modes 1 and 3) is in effect.

The secondary address is formed by adding octal 140 to bits SAD5-1.

EOS 7 End of Sequence Register

EOS[7-0] EOS7-0 End of Sequence Byte.

Cleared by MR and IR. Using this register offers an alternative to the "Send EOI" function code (AUX = octal 006). A seven or eight bit byte (ASCII or binary) may be placed in the register to flag the end of a block of data. The type of EOS comparison to be used is selected by the BIN bit in the hidden Auxiliary Register A, AUXA[4]w.

If the interface is a Listener and the "End on EOS Received" is enabled by the REOS bit, AUXA[2]w, then END is set in the ISR1 whenever the byte in the DIR matches the EOS register. If the interface is a Talker and "Transmit END with EOS" is enabled by the XEOS bit, AUXA[1]w, then the EOI line is asserted along with the data byte whenever the contents of the DOR matches the EOS register.

4.2.3 Hidden Registers

The hidden GPIB1V-2 registers are shown in Table 4.2 and are described on the following pages. These registers are loaded through the Auxiliary Function Register, AUX. AUX[7-5] is loaded with the hidden register number, and AUX[4-0] is loaded with the data to be transferred to that register. These registers cannot be read and in some cases the contents are setable only; i.e., they can be cleared or reset to initialized conditions only by MR, IR, or PON.

CLKR 1 Clock Register

CLKR[4-0]w CLK4-0 Clock Count N

The clock count, N, where N is the decimal equivalent of the binary word CLK4-0, is used to set an internal counter that divides the system clock, with frequency F, to obtain the time delay for the settling of data on the DIO lines. This time is defined as T1 in IEEE Std 488 and appears in the Source Handshake state diagram between SDYS and STRS. Data Valid, DAV, is asserted T1 after the DIO lines are driven. Consequently, T1 is a major factor in determining the data transfer rate over the GPIB.

N is initialized by MR and IR to the decimal value 8 and may be programmed to an integer number from 1 to 8. When open collector transceivers are used for connection to the GPIB, T1 is defined by IEEE Std 488 to be 2 microseconds. In this case, T1 is obtained as follows:

$$T1 \text{ (in microseconds)} = (2*N)/F + Tsync$$

When CLKR is loaded with N=(F/1 MHz), a 2 microseconds T1 delay will be generated before each DAV asserted.

Tsync is a synchronization error, greater than zero and less than the longer of the two clock phases. (For a 50% duty cycle clock, Tsync is less than half the clock period.) The GPIB11V-2 uses a 50% duty cycle 5 MHz clock; thus, for normal operation, set N=5.

When three-state tranceivers are used IEEE Std 488 allows a higher transfer rate (lower T1). Use of the interface in this mode is enabled by setting TRI in hidden Auxiliary Register B, AUXB[2]w, and opening or setting off the TRI EN switch (U50, Switch 4) on the interface board. In this case, setting N=(F/1 MHz) causes a T1 delay of 2 micrseconds to be generated for the first byte transmitted, while all subsequent bytes will have a delay of 500 micrseconds, according to the following equation:

$$T1 \text{ (in microseconds)} = N/(2*F) + Tsync$$

Should a particular GPIB system configuration necessitate a higher or lower T1 delay, N can be programmed accordingly. The user is cautioned that lowering N below 5 may violate the IEEE Std 488 timing restrictions and may cause bus errors.

PPR 3 Parallel Poll Register

Cleared by MR, IR, or PON. The PPR is used by the interface to determine whether and how to respond to a GPIB Parallel Poll message, IDY (EOI * ATN). Refer to Section 4.3 for additional information on Parallel Poll protocol.

PPR[4]w U Parallel Poll Unconfigure

If U=0, the interface is configured to participate in the Parallel Poll and will respond appropriately after evaluating PPR[3-0], S and P3-1. If U=1, the interface will not participate in the poll.

PPR[3]w S Parallel Poll Sense

If participating in the Parallel Poll (U=0), S is compared to the value of the previously received "ist" or individual status message (AUX written with octal 001 or 011). If S=ist, the interface will respond to IDY by asserting true the appropriate DIO line encoded in the Parallel Poll Response, P3-1. Otherwise, the interface will not assert any DIO lines.

PPR[2-0]w P3-1 Parallel Poll Response

This is the encoded 1-of-8 DIO line that the interface is to assert true during a Parallel Poll if U=0 and S=ist.

AUXA 4 Auxiliary Register A

Cleared by MR and IR.

AUXA[4]w BIN Binary

Setting this bit causes the EOS register to be treated as a full 8-bit byte. When it is not set, the EOS Register is treated as a 7-bit register (for ASCII characters) and only a 7-bit comparison is done with the data on the GPIB.

AUXA[3]w XEOS Transmit END on EOS

If this bit is set and the byte in the DOR matches the contents of the EOS register, the EOI line is set true along with the data.

AUXA[2]w REOS End on EOS Received

If this bit is set and the byte in the DIR matches the byte in the EOS register, the END bit, ISR1[4]r, is set.

AUXA[1]w HLDE Holdoff on End

This bit enables the handshake holdoff described below on EOI or EOS (if enabled). No Holdoff will be in effect on any other data bytes, however. See note below.

AUXA[0]w HLDA Holdoff on All

This bit enables the handshake holdoff feature. If the interface is a Listener, GPIB RFD will not be set true after receipt of a data byte until the "finish handshake" auxiliary command (FH) is issued by the processor. The holdoff will be in effect for each data byte.

Note: If both HLDA and HLDE are set, a special "continuous Acceptor Handshake cycling" mode is enabled. It provides a continuous cycling through the Acceptor Handshake state diagram, requiring no local messages from the processor; the "rdy" local message is automatically generated when in ANRS. Thus, the Controller may cycle through the Acceptor Handshake without delaying the data transfer in progress.

AUXB 5 Auxiliary Register B

Cleared by MR and IR.

AUXB[4]w RFDH ENAB RFD Holdoff Enable

Setting this bit causes an RFD holdoff after GET,SDC, and DCL commands are received. The VSC auxiliary command clears the holdoff.

AUXB[3]w INV Invert

Setting this bit causes the polarity of the INT bit to be reversed. This will result in interrupt errors and so should never be set except for diagnostic purposes.

AUXB[2]w TRI Three-State Timing Enable

This bit may be set to enable high speed data transfers when three-state GPIB drivers are used. That is, the TRI EN switch (U50, Switch 4) on the GPIB11V-2 interface card is off or open. See CSR[10]r, OC, and the CLKR registers.

AUXB[1]w SPEOI Send Serial Poll EOI

This bit causess EOI to be asserted with the status byte: if set, EOI is sent true in the Serial Poll Active state; otherwise, EOI is sent false in SPAS.

AUXB[0]w CPT ENAB Command Pass Through Enable

When set, this bit enables the Undefined Command Pass Through feature; this feature allows any commands not recognized by the interface to be handled in software. If enabled, this feature will cause the interface to holdoff the Acceptor handshake (in the Accept Data State, ACDS) when an undefined command is received. The processor must then read the command from the CPT Register and write the VSC auxiliary command. Until the VSC command is written, the handshake is held off.

4.3 PARALLEL POLL PROTOCOL

If a PP2 implmentation (local configuration as defined in IEEE Std 488) is desired, the interface will typically be configured by the processor for Parallel Poll immediately after initialization by setting PPR[4,2-0] (U and P3-1) to predetermined values. During normal operation, the processor will set or clear the Parallel Poll Flag (ist) according to the need for service. Subsequently, the interface will automatically give the proper response to IDY (EOI * ATN) without directly involving the processor.

If a PP1 implementation (remote configuration as defined in the IEEE Std 488) is desired, the undefined command features of the interface must be used. In PP1, the interface is indirectly configured for Parallel Poll by the Active Controller on the GPIB. The sequence that the interface being configured must follow is:

1. The GPIB Parallel Poll Configure, PPC, message is received. Being an undefined command, it is available in the Command Pass Through Register, CPT, and the CPT bit in ISR1 is set. The handshake is automatically held off.

2. The processor reads the CPT register and writes the VSC function code to the AUX internal register, releasing the handshake.

3. Having received an undefined primary command, the interface is set up to receive an undefined secondary command, namely the Parallel Poll Enable, PPE, message. This message is also received in the CPT register, the handshake is held off, and the CPT bit is set again.

4. The processor reads the PPE message and loads the least significant five bits into the hidden Parallel Poll Register, PPR. Finally, the processor writes the VSC function code and the handshake is released.

Note: Parallel Poll is an IEEE Std 488 feature which can only be used on an open-collector bus. The processor must monitor the TRI EN switch via OC CSR[10]r and accordingly program the interface to participate or not participate in Parallel Poll via the U bit in the PPR and to enable three-state or open collector timing via the TRI bit in AUXB.

4.4 RESET PROCEDURE

The GPIB11V-2 interface is reset to its power on state by the Q-BUS BINIT signal or by setting the Local Master Reset, LMR, bit in the CSR. MR, the logical OR of these signals, is the interface Master Reset pulse that initializes the Q-BUS Control Logic, Control Status Register, Extended Address Register, GPIB Talker/Listener Logic, GPIB Controller Logic, and State Machine. The programmable Internal Reset function, IR, resets the GPIB Talker/Listener Logic, including the internal and hidden registers. The programmable Local Power On function, PON, resets a subset of the GPIB Talker/Listener Logic in addition to releasing the initialization state that is activated by MR.

Clearing DMA EN (CSR[13]w) while a DMA is in progress will reset the DMA function within the Q-BUS Control Logic but not otherwise affect other functions.

The following conditions constitute the interface initialize state following MR:

1. The Q-BUS Control Logic is inactive, ready to be addressed by the processor.

2. CSR and XAR are cleared; the BCR, BAR, and CCF register are undefined.

3. All Talker and Listener functions are disabled.

4. All interrupt status bits (ISR1 and ISR2) are cleared.

5. AUXA, AUXB, SPS, and SPM are cleared; CLKR is set to octal 010.

6. The Parallel Poll Flag (ist) is cleared (AUX = octal 001).

7. EOI in ADS is cleared.

8. The interface is not System Controller.

9. The State Machine is at TM0, with all output signals false.

The interface is designed to power up in certain states, as specified in the IEEE Std 488 state diagrams. Thus, the following states are in effect in the initialize or power up state: SIDS, AIDS, TIDS, LIDS, NPRS, LOCS, PPIS, and CIDS.

A typical programmed initialization would involve the following steps:

1. Issue the Internal Reset command by writing octal 010 to the internal Auxiliary Function Register, AUX, or set the Local Master Reset bit, LMR, in the CSR.

2. Set the desired initial conditions by loading the hidden registers AUXA, AUXB, and CLKR and loading the internal registers IMR1-2, SPM, ADM, ADO-1, and EOS.

3. Release the initialization state by issuing the PON special function (writing 0 to the internal Auxiliary Function Register, AUX).

4. Load PPR if desired; set RSV in SPM and set the Parallel Poll Flag (ist) via the AUX register. if desired.

4.5 SOFTWARE CONSIDERATIONS

4.5.1 General

Both the internal register and the Q-BUS registers contain read-only and write-only bits and this has software implications, especially for the Q-BUS registers.

For example, instructions with an implied read (INC, DEC, BIC, BIS, etc.) will not behave as expected when addressing a register with write-only bits; this is easily seen with the following code:

```
MOV #20002, @#CSR ;  DMA ENABLE, OUT
MOV # -10, @#BCR ;  TRANSFER 8 BYTES
INC @#CSR         ;  GO
```

The obvious intent of the INC instruction is to set the GO bit and start the DMA; however since the DMA EN and OUT bits are both write only (and presuming INT is not being asserted), the implied read will read zero, increment it to 1, and write it to the CSR. The effect will be to set the GO bit, and clear the OUT and DMA EN bits, and thus abort the DMA operation.

The proper method for programming registers of this sort is to keep a copy in memory of the last thing written to each register. When it is necessary to change the contents of a register, first modify the memory copy and then write the new memory value to the register. In this way unmodified memory bits are left unmodified in the device register also.

4.5.2 Software Requirements

For compliance with IEEE Std 488, certain timing constraints must be adhered to by the software. These apply when the GPIB11V-2 is configured as the System Controller. When asserting Interface Clear (IFC) to clear the GPIB, the software must ensure that IFC remains asserted for a minimum of 100 microseconds. When unasserting the Remote Enable line (REN) to put all interfaced equipment in local mode, the software must ensure that REN is not re-asserted for a minimum of 100 microseconds.

In addition to the timing constraints, there are other software requirements which must be addressed when dealing with a multi-controller GPIB environment, especially in the case where the GPIB11V-2 is not the System Controller. Of particular importance in the latter situation is the prompt relinquishing of control when the System Controller asserts IFC, should the GPIB11V-2 be the Active Controller at the time. The interface hardware ensures that Attention, ATN, is unasserted if it is being driven and that any DMA operation in progress is stopped; however, it is up to the software to restore the GPIB address mode (see description of the internal register ADM). As mentioned previously, the Talk-only, TON, feature must be used when the GPIB11V-2 is the Active Controller; but, whenever TON is on, the GPIB DIO lines are being driven by the interface. Thus, whenever control is relinquished, the DIO lines must be relinquished also and this is accomplished by changing the address mode from TON to Mode 1, 2, or 3 as appropriate.

Although the IFC response requirement is only applicable when the GPIB11V-2 is not the System Controller, the pass control protocol requirements apply for all multi-Controller GPIBs. Passing control is a voluntary operation which is performed by the software in the following manner:

1. A device with the Controller capability is addressed to Talk, the Take Control (TCT) command is sent, and ATN is turned off.

2. In conjunction with turning ATN off the TON mode must be changed just as in the involuntary pass control case described above.

3. The addressed device interprets ATN going off as a signal that it may now actively control the GPIB and assert ATN itself.

Once the software has passed control to another device it must not assert ATN again, until receiving control by the same protocol (or until usurping the GPIB with IFC, if the interface is the System Controller).

CHAPTER 5

THEORY OF OPERATION

Figure 2.3 is a block diagram of the major functional logic elements of the GPIB11V-2. These elements are discussed in detail in the following sections. Detailed schematic diagrams are shown in Chapter 7.

5.1 Q-BUS REGISTER INPUT/OUTPUT

The Q-BUS is composed of 20 control lines and from 18 to 22 time-multiplexed data/address lines, depending on the addressing capability of the processor. Table 3.1 lists the signals used by the GPIB11V-2. Figure 5.1 shows the Q-BUS transceivers and that portion of the Q-BUS Control Logic associated with address decoding and register I/O.

The GPIB11V-2 interface recognizes when it is addressed by the bus master by monitoring the low sixteen data/address lines, BDAL[15-0], and an encoded data transfer control signal, BBS7, that signifies that the BDAL[12-0] address lines pertain to an I/O device such as the interface. Multifunction transceiver logic cicuitry (U60-63) compares the bus address with the interface's switch selected address (U50-52) and signals the protocol logic circuitry (U40) when a match occurs.

The protocol logic decodes the three data transfer control signals, BSYNC, BDIN, and BDOUT, as well as the lower three time-demultiplexed address bits, D02-00, to generate register selection signals SEL0, 2, 4, and 6, and data direction signals, OUT LB and IN WD. These six signals are used to read and write to the four device registers: BAR, BCR, CSR, and CFF/XAR. The protocol logic also generates the data transfer control signal, BRPLY, that informs the bus master that the interface has responded correctly.

5.2 Q-BUS ADDRESSABLE REGISTERS

Figure 5.2 is a block diagram of the registers/counters that maintain the byte count and bus address during DMA operations.

The BAR and BCR are contained on two multipurpose logic cicuits (U41-42). Each IC contains independent 8 bit address and byte counters and the two ICs are cascaded to form two 16 bit counters. Common logic cicuitry decodes the selection and data direction signals and routes the data to and from the registers and the common internal data bus, D15-00. Because the BCR operates in two modes, depending on whether the programmed DMA is between the the Q-BUS and the GPIB or between the Q-BUS and the internal registers, additional cicuitry exists to perform this function.

The upper byte of the CCF/XAR contains the Extended Address Register (U48 and U58) which is cascaded with the BAR to form a 22 bit counter capable of addressing up to 2,097,152 words of memory. When performing a DMA, the

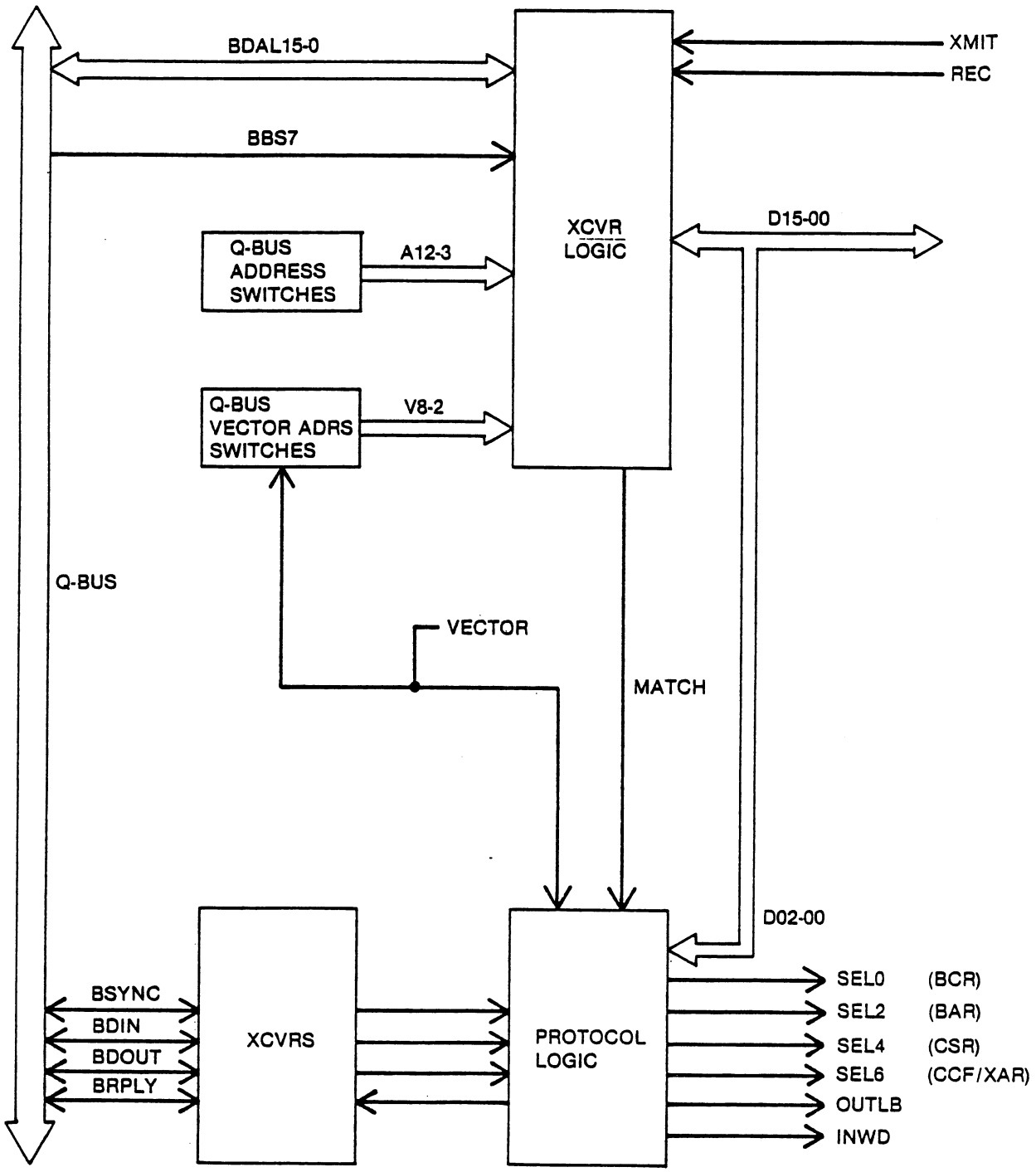


FIGURE 5.1

Q-BUS DATA/ADDRESS TRANSCEIVING AND REGISTER SELECTION

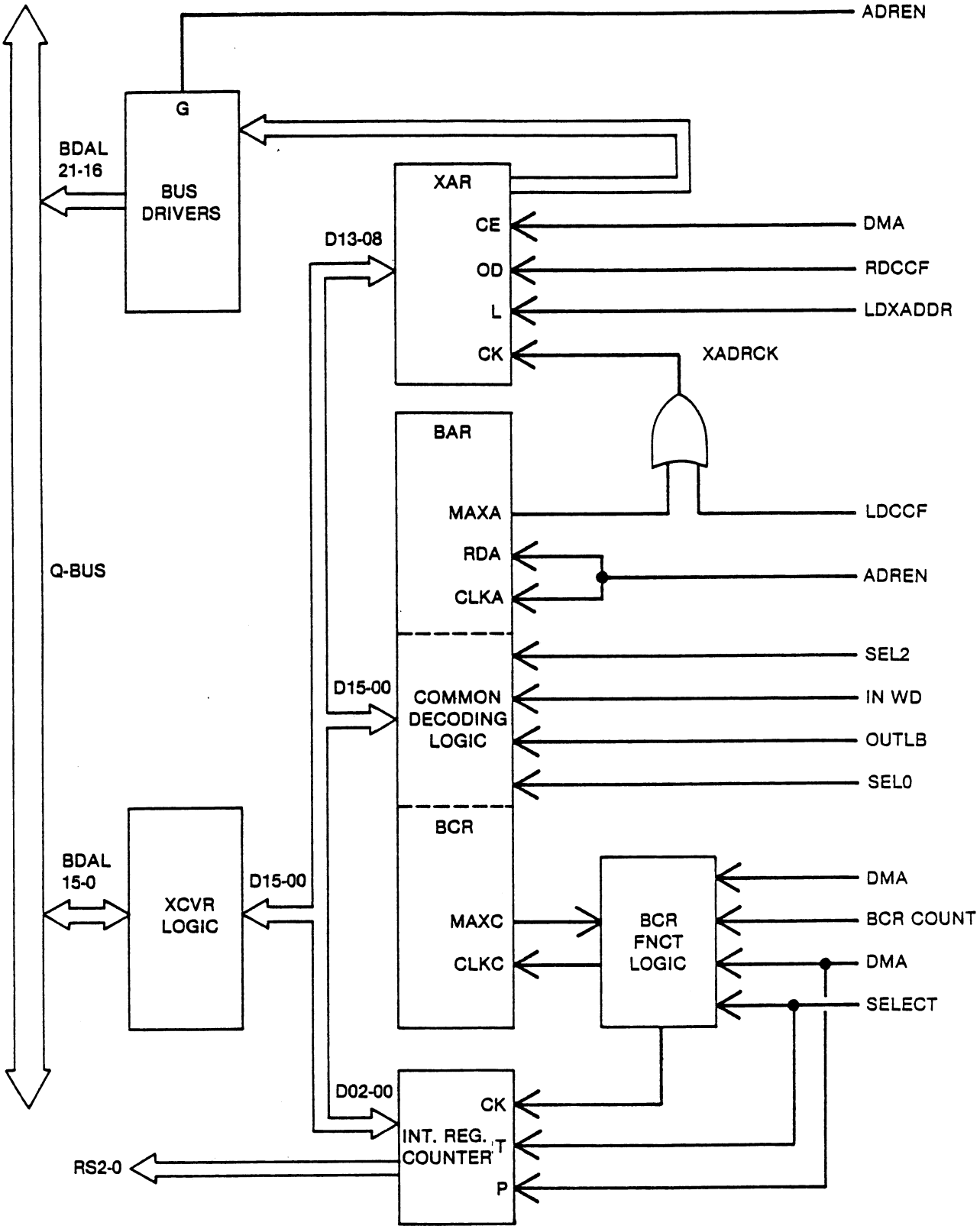


FIGURE 5.2

DMA BYTE AND BUS ADDRESS REGISTERS/COUNTERS

output of the BAR/XAR counter is time-multiplexed on to the BDAL[21-0] bus with the enabling signal ADREN.

The CSR is contained in several ICs (including U23, U26, U27, U43, and U49). The CSR provides the primary means for the Q-BUS processor to configure the interface control cicuitry for conducting DMA data transfers and to monitor the status of the interface.

The CSR signals GO, SEL, OUT, IE, LMR, DONE, DMA EN, and NEX pertain mostly to the Q-BUS side of the interface, while the signals ECC, CIC, ATN, EDI, TCS, DAV, SRQ, SRQ IE, INT, REM, and IFC pertain mostly to the GPIB side. See Chapter 4 for detailed descriptions of these signals.

The lower byte of the CCF/XAR (U30) contains the Carry Cycle Function information that is used in conjunction with the ECC bit of the CSR to perform a special function on the last data transfer of a DMA operation. The CCF byte is written by the Q-BUS processor and cannot be read by it.

5.3 Q-BUS CONTROL LOGIC

The Q-BUS processor, as bus master, writes to the four device registers when it configures and primes the interface, as bus slave, for a DMA operation. Once primed, the interface is triggered to begin the DMA when the CSR GO bit is set. From that point until the DMA finishes or terminates, the Q-BUS Control Logic is responsible for interrupting the Q-BUS process when service is required; for asserting itself as bus master in order to transfer data between memory, as bus slave, and the interface DMA port; to generate the associated data transfer control signals; and to recognize when memory addressed by the interface does not exist and to time out the DMA so that the processor is not hung. The Q-BUS Control Logic also interfaces with the GPIB Controller and Talker/Listener Logic to coordinate transfer of data and status information. The Q-BUS Control Logic is implemented with LSI and MSI circuits and is located mostly on sheets 2 and 3 of the schematic diagram.

An important part of the Q-BUS Control Logic is the Interrupt Control Logic, shown in Figure 5.3 and on sheet 1 of the schematic diagram. The interface will generate an interrupt request, IRQ, if interrupts are enabled (IE bit on the CSR) and any of several conditions exist. These conditions are described in Section 4.2. Depending on the interrupt scheme in which the interface is configured, IRQ causes one or more of the priority interrupt request lines, BIRQ4-7, to be asserted. At the same time, the interface monitors selected interrupt request lines. If a higher priority request from another bus device is pending, the incoming interrupt acknowledgement signal from the bus master, BIAKI, is simply routed to the next bus device as BIAKO. If a higher priority request is not pending, BIAKI is stopped by the Interrupt Control Logic and, in its place, the interface responds by placing its interrupt vector on the Q-BUS (see Figure 5.1) and dropping IRQ.

Non-existent memory (NEX) is detected when the addressed memory fails to respond to a read or write from the interface within 64 clock cycles (or 12.8 microseconds at 5 MHz). NEX terminates the DMA in progress, causing a DMA INT interrupt service request.

When acting as bus master during a DMA operation, the interface generates the required Q-BUS data transfer control signals (BRPLY, BDIN,

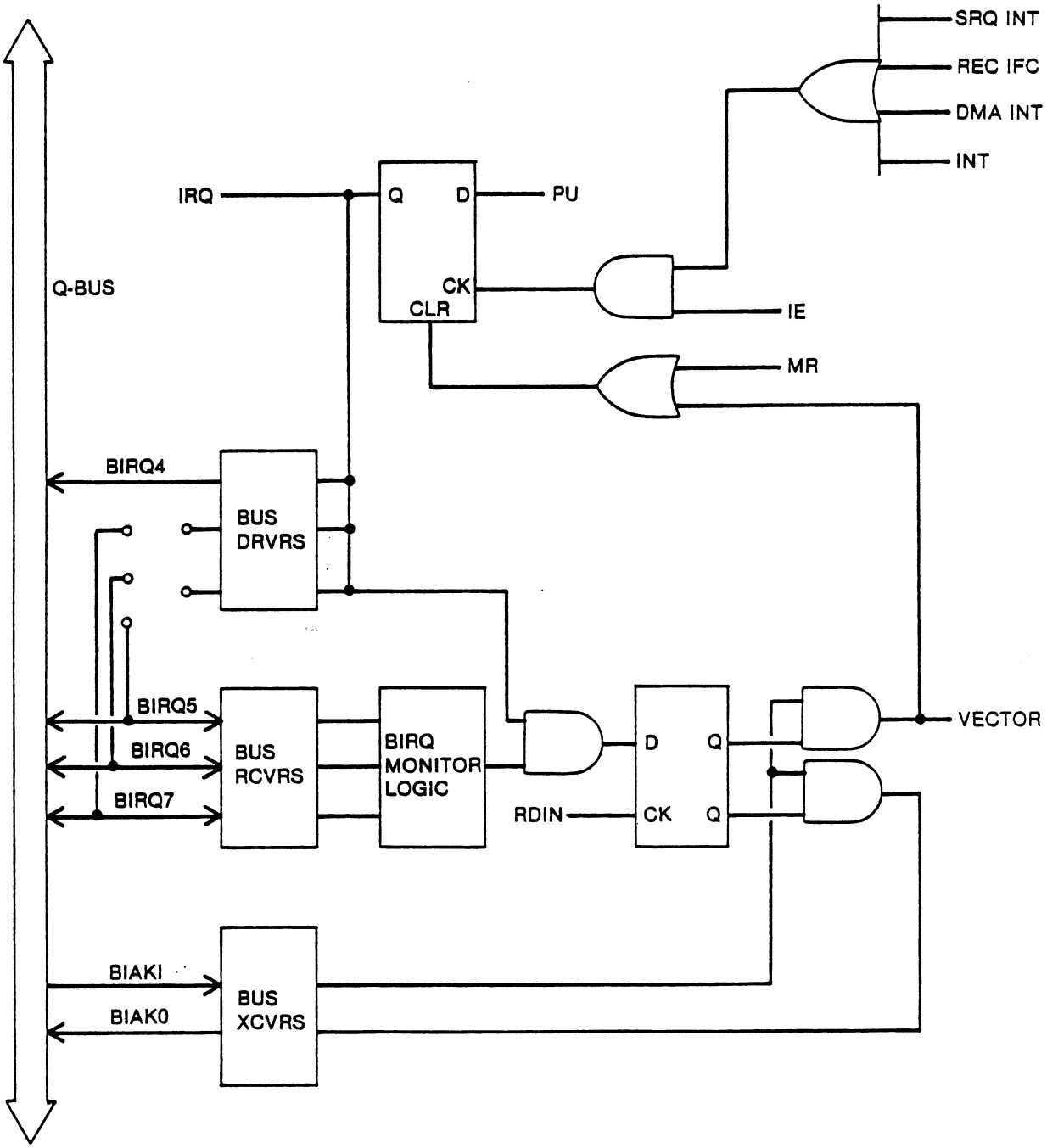


FIGURE 5.3

INTERRUPT CONTROL LOGIC

BDOUT, BSYNC, and BWTBT) and DMA control signals (BDMR and BSACK) based on the phase of each DMA cycle as determined by the State Machine and responses from other control cicuitry.

5.4 GPIB TALKER/LISTENER AND CONTROLLER LOGIC

On the GPIB side of the interface are the Talker/Listener Logic, the Controller Logic, and the transceivers that connect the interface to the CPIB.

The Talker/Listener Logic is a large-scale integrated circuit (U22) that performs most of the GPIB functions as defined in the IEEE Std 488. It also contains that data path through which data passes between the CPIB and the DMA Port to the Q-BUS. Finally, in order to select, control, and monitor the functions performed by this IC, it contains 16 internal registers (8 read and 8 write) and four so-called hidden registers.

The Q-BUS processor programs the Talker/Listener Logic by reading/writing to the internal registers with data transfers through the DMA port. The hidden registers and other functions are individually accessed through one of the internal registers.

Small and medium scale IC complement the Talker/Listener IC to implement the Controller function (see sheet 2 of the schematic diagram). The central element is a flip-flop (U4) that establishes the interface as System Controller when the interface asserts IFC (CSR[15]w). From this time until reset by INIT or LMR (CSR[7]w), the interface is enabled to send, in addition to IFC, the GPIB signal REN (CSR[4]). When CSR[9], ATN, is set, EOI (CSR[10]) can also be asserted, and it is a software responsibility to do this only in conjunction with setting CIC (CSR[8]).

The GPIB transceivers (U12-15) are programmed to send or receive as follows:

DIO1-8 and DAV are transmitted and NFRD and NDAC are received when the Talker/Listener Logic is programmed as Talker, and vice versa.

EOI is transmitted automatically if the interface sends the END or IDY message; otherwise EOI is received.

ATN is transmitted if the ATN bit of the CSR is set; otherwise it is received.

IFC and REN are transmitted if the interface is System Controller; otherwise, they are received.

SRQ is transmitted if the interface is not programmed as Controller-in-charge; otherwise, SRQ is received.

The DIO1-8, EOI, DAV, IFC, and ATN can be programmed to be driven either three-state or open collector by Switch 4 on U50. NRFD, NDAC, SRQ, and REN are always driven open collector.

5.5 CLOCK AND STATE MACHINE

A 5 MHz hybrid crystal oscillator (U1) provides synchronization between the State Machine and the asynchonous Q-BUS, GPIB, and interface logic.

Figure 5.4 shows a block diagram of the State Machine that provides the timing and control signals for the DMA operation. The state diagram for this function is shown in Figure 5.5. The twelve states (TM0 to TM11) are denoted by circles. All permissible transitions between states of the State Machine are represented graphically by arrows between them. Each transition has an expression whose value is either true or false. The State Machine must remain in its current state if all expressions leading to other states are false. The State Machine must enter the state pointed to if, and only if, one of the expressions come true.

If a time is specified, the expression can assume a true value only after the interface has been in the state originating the corresponding transition for the time value specified. The AND operator is represented by the symbol *. The OR operator is represented by the symbol +. the AND operator takes precedence over the OR operator within an expression unless otherwise specified by parenthesis. The NOT operator is represented by a unary operator ~ before the expression to be negated.

The State Machine must remain in each state for a minimum of one clock cycle. The implementaion of the State Machine is shown in sheet 3 of the schematic diagrams. The state machine is implemented using a programmable logic array (U24) and decoder (U18). Asynchronous inputs are synchronized by using a clocked latch (U25).

The states TM0 to TM11 have the following characteristics:

TM0 — The State Machine is in this state when there is no DMA in process. The GPIB11V-2 is initialized to TM0 by the Q-BUS BINIT signal and by LMR (CSR[7]w). The State Machine exits TM0 whenever GO (CSR[1]w) is asserted. The State Machine normally exits TM0 to go to TM5. However, the State Machine will go from TM0 to TM2 if the ECC bit (CSR[4]w) and the CARRY output of the byte counter are set, and the transfer is a DATO cycle. When the carry cycle is entered a word is written to the AUX register. This word would normally be a command to be executed by the Talker/Listener Logic before the last GPIB data word is received.

TM1 — This state is a wait state to insure that the GPIB is in the right state for taking control synchronously. The State Machine enters TM1 when a DMA is complete; that is, the signals FINISH and CARRY are present at TM7 or when FINISH, CARRY, and OUT are present at TM11. When TCS (CSR[12]w) is not set the State Machine will go to TM0. When the TCS bit is set the State Machine will wait for DAV to be false on a DATO cycle and will wait for a DAV and NDAC on a DATI cycle.

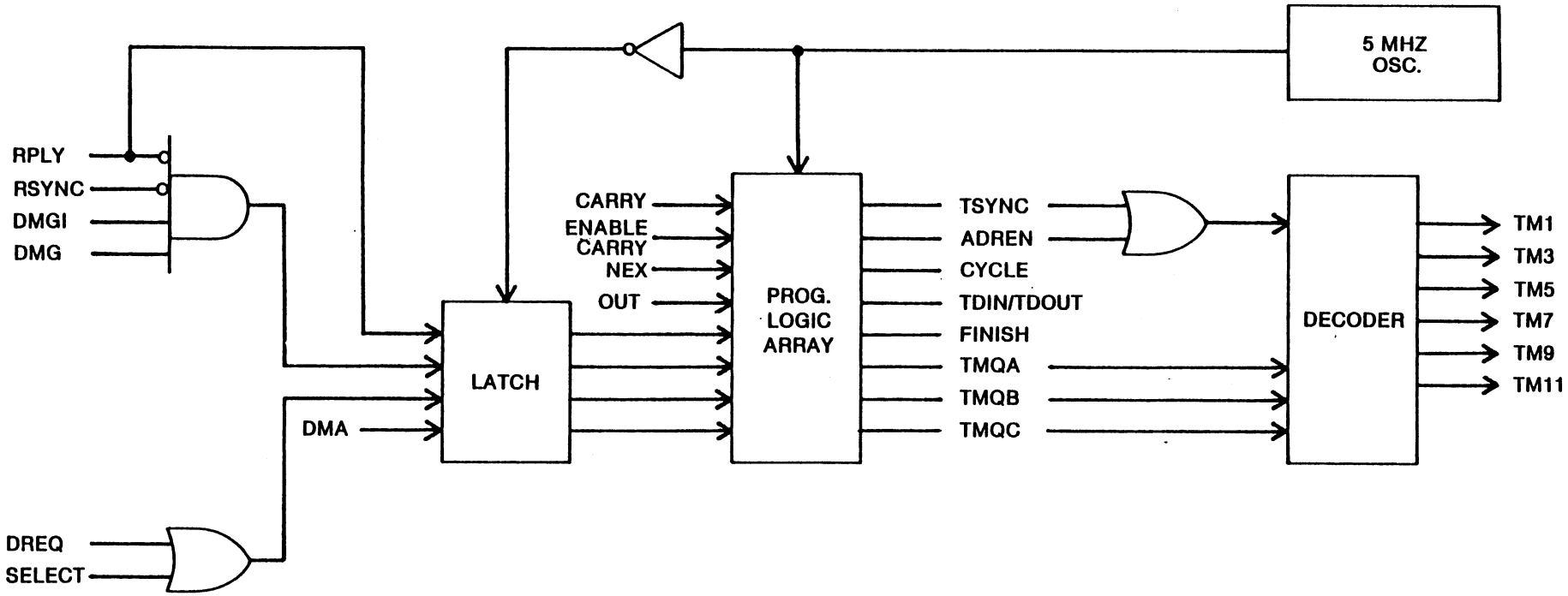


FIGURE 5.4

CLOCK AND STATE MACHINE

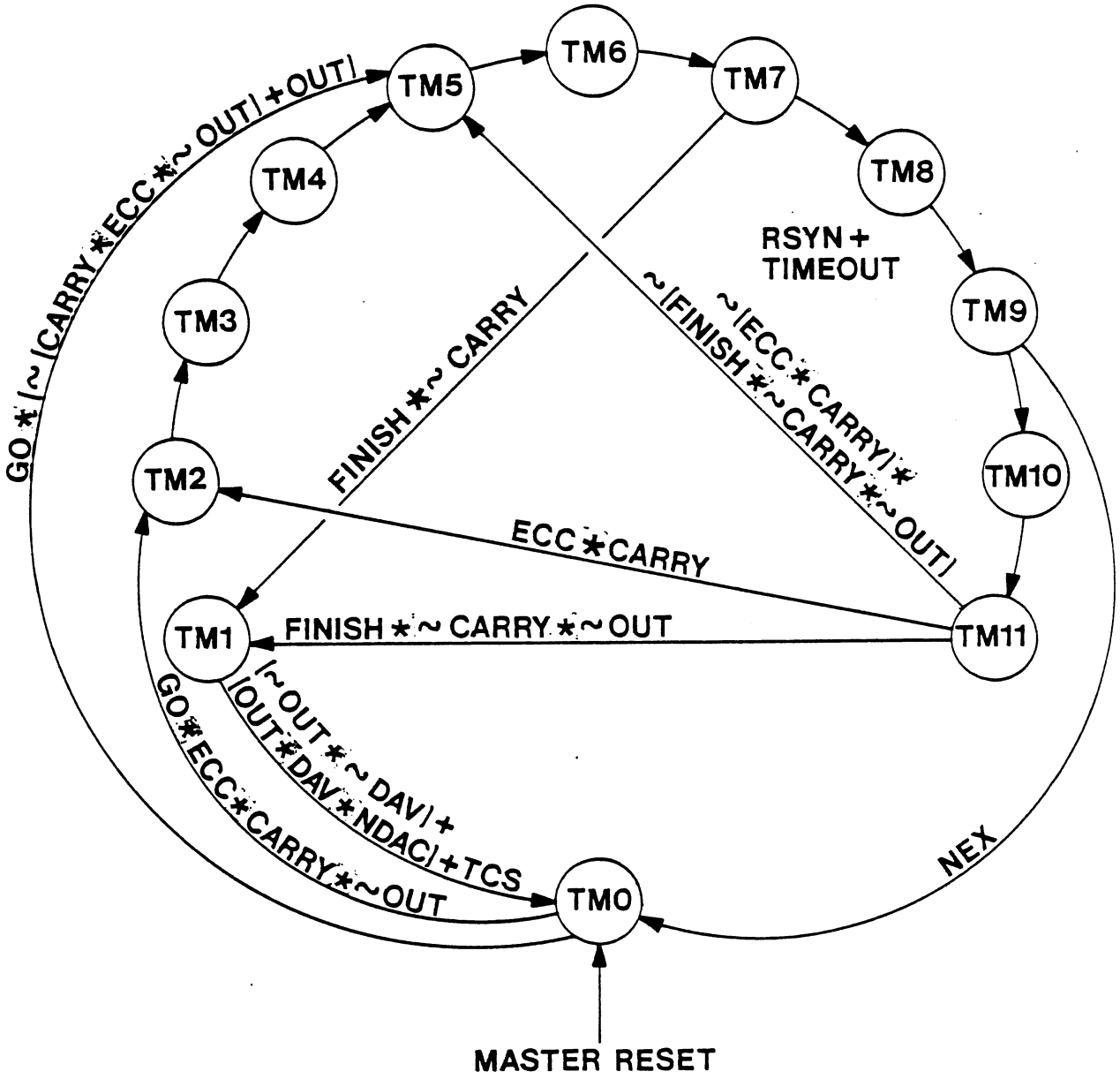


FIGURE 5.5

STATE MACHINE STATE DIAGRAM

TM2-TM3 These two states are used to write to the AUX register. This state is entered either from TM0 with GO, ECC, CARRY, and a DMA IN, or from TM11 with ECC and CARRY. The State Machine exits TM2 to TM3 after one clock cycle and waits for DREQ from the Talker/Listener Logic before exiting TM3.

TM4 This state is entered automatically from TM3. This state is not used except to transit from TM3 to TM5. The State Machine exits TM4 automatically after one clock cycle.

TM5 The TM5 state is the normal starting state for a DMA transaction. The state machine will enter this state from TM0 with the GO message whenever a carry cycle is not required. The State Machine will also enter TM5 from TM11 if a carry cycle is not required or if the DMA is not complete. The state machine exits TM5 to TM6 whenever DREQ, SELECT, or the first cycle of a DATI transfer is present.

TM6 The state TM6 is used to read or write to the Talker/Listener Logic. The write will be inhibited during the first cycle of a DATI transfer. The state machine exits TM6 to TM7 automatically after one clock cycle.

TM7 The State Machine continues to read or write line to the Talker/Listener Logic during TM7. Also, the interface asserts the DMA request line (BDMR) during TM7. The State Machine exits TM7 whenever the DMA grant (BIAKI) is received and the Q-BUS is not busy (i.e., BSYNC and BRPLY are not asserted). The State Machine will exit TM7 to TM1 if it is in its last DATI cycle. Otherwise the State Machine will exit to TM8.

TM8 During TM8, the interface asserts ADREN and enables the address lines onto the Q-BUS. The State Machine remains in TM8 for two clock counts. After one clock count the interface transmits BSYNC, which the slave device uses to strobe the address. The interface continues to assert BSYNC through TM11. BSYNC also starts the time out counter. If the counter times out before the DMA cycle is complete, the State Machine goes to TM0 and the NEX bit (CSR[14]r) is set.

TM9 During TM9 the interface will assert TDIN, signaling that a memory read (DATI) is in process. If the cycle is a memory write (DATO), the interface will assert the data onto the Q-BUS.

TM10 During TM10, the interface will continue to assert TDIN for DATI and will start to assert DOUT for a DATO cycle. The state machine will automatically remain in TM10 until the slave returns BRPLY.

TM11 The state machine tests several conditions during TM11 and exits to the appropriate state after BRPLY has ended. The State Machine exits to TM1 if the DMA transfer is complete (FINISH and CARRY); to TM3 if a carry cycle is present (ECC and CARRY); or to TM5 if none of the above conditions are present.

CHAPTER 6

PARTS LIST

6.1 ORDERING INFORMATION

Replaceable parts may be ordered from National Instruments by giving the National Instruments part number and the quantity required.

6.2 MANUFACTURERS CODE IDENTIFICATION

Manufacturer	Mfr. Code
AMP, Inc.	AMP
Belden	BEL
Berg Electronics	BERG
Calmark	CAL
Centralab Electronics	CLB
Dale	DALE
Digital Equipment Corporation	DEC
General Electric	GE
Intel	INT
Kemet, Union Carbide	KMT
MF Electronics	MFE
Motorola, Inc.	MOT
National Instruments	NI
National Semiconductor	NS
Rogers	ROG
Sangamo	SAN
Texas Instruments	TI
United Shoe Machine	USM

ITEM NO	QTY REQD	MFR FSCM NO	PART/DWG STOCK NO	DESCRIPTION REFERENCE DESIGNATION
1	1	NI	179056-01	PWB, Q-BUS TO GPIB DMA INTFC, GPIB11V-2
		7U296	179056-01	
2	REF	NI	179057-01	SCHEMATIC DIAGRAM, GPIB11V-2
		7U296	179057-01	
3	6	CLB	UK50-103	CAPACITOR, RDL LEAD, 50 V, 20%, .01 UF
		71950	715003-01	C1, C2, C3, C4, C5, C6
4	1	KMT	T322D476M010AS	CAPACITOR, AXIAL LEAD, 10 V, 20%, 47 UF
			715010-01	C7
5	2	SAN	D7-1-C-101-J-0	CAPACITOR, RDL LEAD, 100 V, 5%, 100 PF
		00853	715005-01	C8, C9
6	1	HP	5082-2811	DIODE, GP, 20 MA, SCHOTTKY
		04404	730002-01	D1
7	1	DALE	MSP06A05-681/331G	RESISTOR, 2%, QUAD 680/330 OHM, SIP
			711030-01	R1
8	1	-	RC07GF681J	RESISTOR, 1/4 W, 5%, 680 OHM
		71785	711031-01	R2
9	3	-	RC07GF102J	RESISTOR, 1/4 W, 5%, 1K OHM
		71785	711009-01	R3, R5, R6
10	1	-	RC07GF101J	RESISTOR, 1/4 W, 5%, 100 OHM
		71785	711005-01	R4
11	1	MFE	M1115-5M	OSCILLATOR, CRYSTAL, 5.000 MHZ, 0.1%
			738002-01	U1
12	3	TI	SN74LS02N	IC, QUAD 2-INPUT NOR GATE
		06668	700002-01	U2, U38, U53
13	5	TI	SN74LS08N	IC, QUAD 2-INPUT & GATE
		06668	700004-01	U3, U8, U35, U44, U47
14	3	TI	SN74LS74AN	IC, DUAL D-TYPE FF
		06668	700013-01	U4, 36, 57
15	1	TI	SN74LS14N	IC, HEX SCHMITT-TRIGGER INV
		06668	700007-01	U5
16	4	TI	SN74LS32N	IC, QUAD 2-INPUT OR GATE
		06668	700011-01	U6, U21, U34, U37
17	1	TI	SN74LS393N	IC, DUAL 4-BIT BIN CNTR
		06668	700049-01	U7
18	1	TI	SN74LS51N	IC, 2-WIDE 2-INPUT &-OR-INVERT GATE
		06668	700012-01	U9

TITLE
PARTS LIST- CCA,
Q-BUS TO GPIB DMA INTERFACE, GPIB11V-2

FSCM NO DWG NO REV
PL 179055-01 E
Tue May 29 17:45:39 1984

ITEM NO	QTY REQD	MFR FSCM NO	PART/DWG STOCK NO	DESCRIPTION REFERENCE DESIGNATION
19	1	TI	SN74LS00N	IC, QUAD 2-INPUT NAND GATE
		06668	700001-01	U10
20	1	TI	SN74LS139N	IC, DUAL 2-TO-4 LINE DCDR/MULTIPLEXER
		06668	700016-01	U11
21	4	MOT	MC3448AP	IC, QUAD 3-STATE/OPEN C GPIB XCVR
		04713	700035-01	U12, U13, U14, U15
22	2	TI	SN74LS368AN	IC, HEX INVG BUS DRVR
		06668	700024-01	U16, U43
23	4	TI	SN74LS04N	IC, 14-PIN DIP, PLASTIC, HEX INVERTER
		06668	700003-01	U17, U20, U39, U45
24	1	TI	SN74LS259N	IC, 8 BIT ADDRESSABLE LCH
		06668	700087-01	U18
25	1	TI	SN74LS11N	IC, TPL 3-INPUT & GATE
		06668	700006-01	U19
26	1	INT	P8291A	IC, TALKER/LISTENER, GPIB
			700050-02	U22
27	2	TI	SN74LS174N	IC, HEX D FF
		06668	700019-01	U23, U27
28	1	NI	700090-01	IC, PLA (GPIB11V-2 STATE MACHINE)
		7U296	700090-01	U24
29	6	TI	SN74LS374N	IC, OCTAL D-TYPE FF W/ 3-STATE OUTPUTS
		06668	700048-01	U25, U29, U30, U31, U32, U33
30	1	TI	SN74LS161AN	IC, BIN SYN 4-BIT CNTR W/ DIR CLR
		06668	700045-01	U28
31	1	DEC	DC004-KA	IC, LSI-11 BUS PROTOCOL CHIP
		15476	700089-01	U40
32	2	DEC	DC006-KA	IC, LSI-11 BUS WORD COUNT/BUS ADRS CHIP
		15476	700086-01	U41, U42
33	1	TI	SN74LS27N	IC, TPL 3-INPUT NOR GATE
		06668	700009-01	U46
34	2	NS	DM8556N	IC, SYN LD, CONV. & 3-STATE OUTPUTS
			700092-01	U48, U58
35	1	TI	SN74LS367AN	IC, HEX NONINVERTING BUS DRVR
		06668	700047-01	U49
36	3	AMP	435668-5	SWITCH, SPST, LOW PF, 6-POSITION, DIP
		00779	720002-01	U50, U51, U52

ITEM NO	QTY REQD	MFR FSCM NO	PART/DWG STOCK NO	DESCRIPTION REFERENCE DESIGNATION
37	1	NS	DS8838N	IC, QUAD UN BUS XCVR
			700041-01	U54
38	2	TI	SN74LS642-1N	IC, OPEN C, INVT OCTAL BUS XCVR
		06668	700091-01	U55, U59
39	1	NS	DS8837N	IC, HEX UN BUS RCVR
			700040-01	U56
40	4	DEC	DC005-KA	IC, LSI-11 BUS XCVR CHIP
		15476	700088-01	U60, U61, U62, U63
41	3	AMP	435238-3	COVER, PROT, SWITCH, 6 POSN, DIP
		00779	720006-01	
42	AR	BEL	9977	WIRE, HOOK-UP, 28 AWG., SOL, VINYL, GRN
		70903	763022-01	
43	1	BERG	65268-009	HEADER, SHLDED, .1 CTR, 26-POSITION
		22526	760010-01	J1
44	1	CAL	SERIES 110-GREEN	HANDLE, PRINTED CIRCUIT BOARD, GREEN
			745004-01	
45	2	USM	SE47, Brass Nickel Plated	EYELET, RLD FLG, NP BRASS
			745000-01	
46	5	ROG	GV2-9.5.3(.1)	BUS BAR, 0.3 OFFSET, 4.95 IN, 2 ELEMENT
			724002-10	
47	1	ROG	GV2-5.5.3(.1)	BUS BAR, 0.3 OFFSET, 2.95 IN, 2 ELEMENT
			724002-06	
48	1	TI	SN74S74N	IC, DUAL D-TYPE FF
		06668	700025-01	U26

TITLE
PARTS LIST- CCA,
Q-BUS TO GPIB DMA INTERFACE, GPIB11V-2

FSCM NO DWG NO REV
PL 179055-01 E
Tue May 29 17:45:39 1984

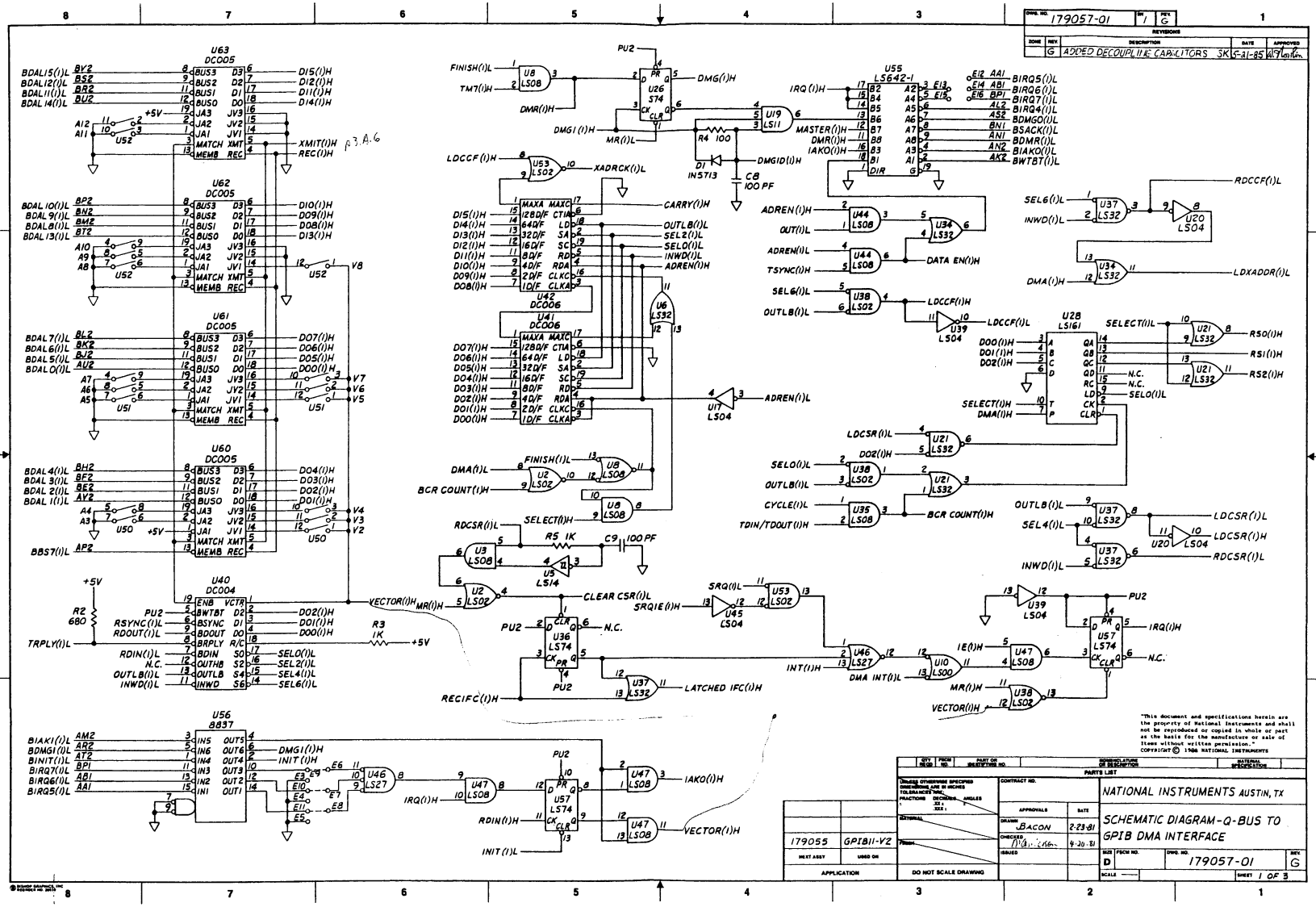
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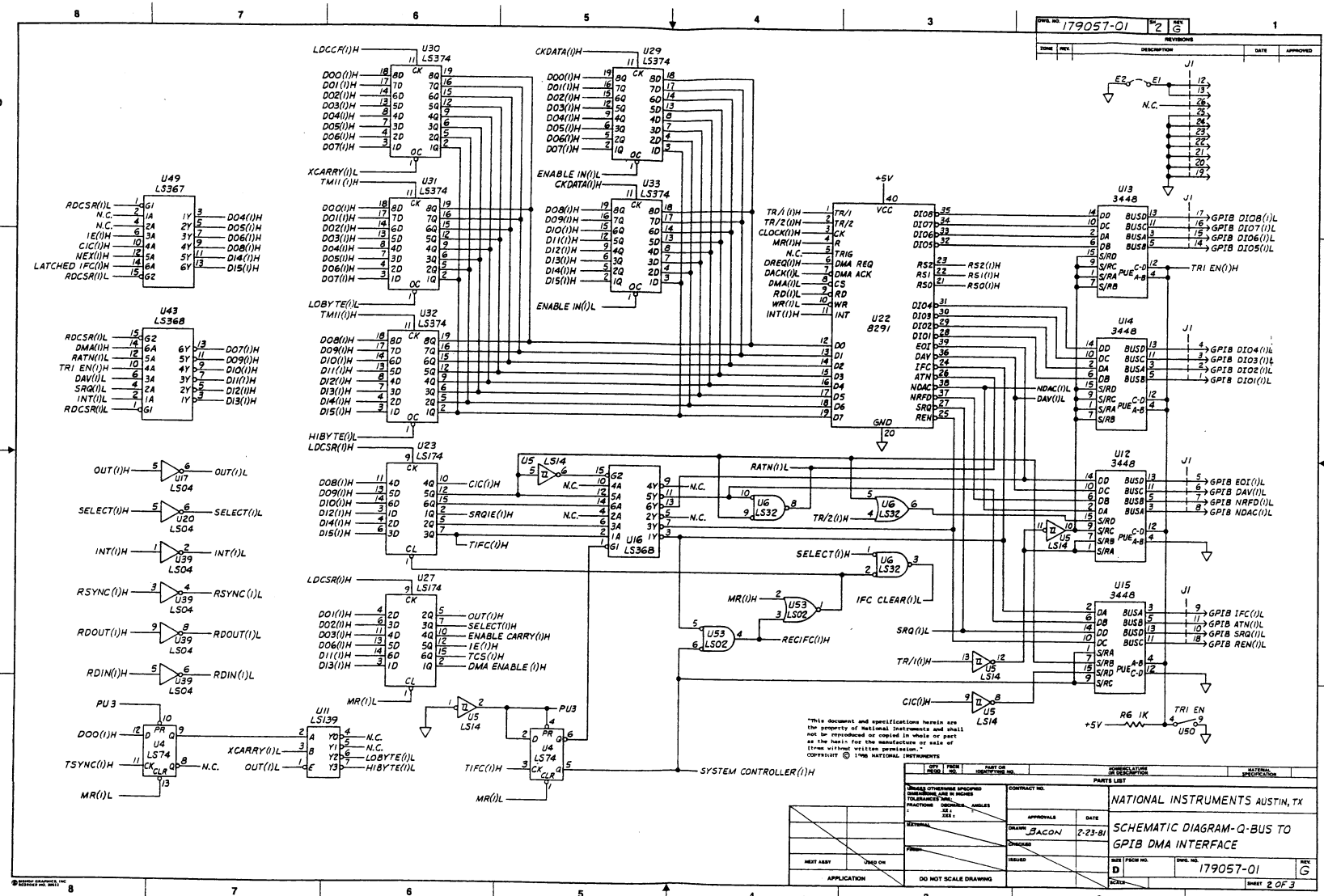
CHAPTER 7

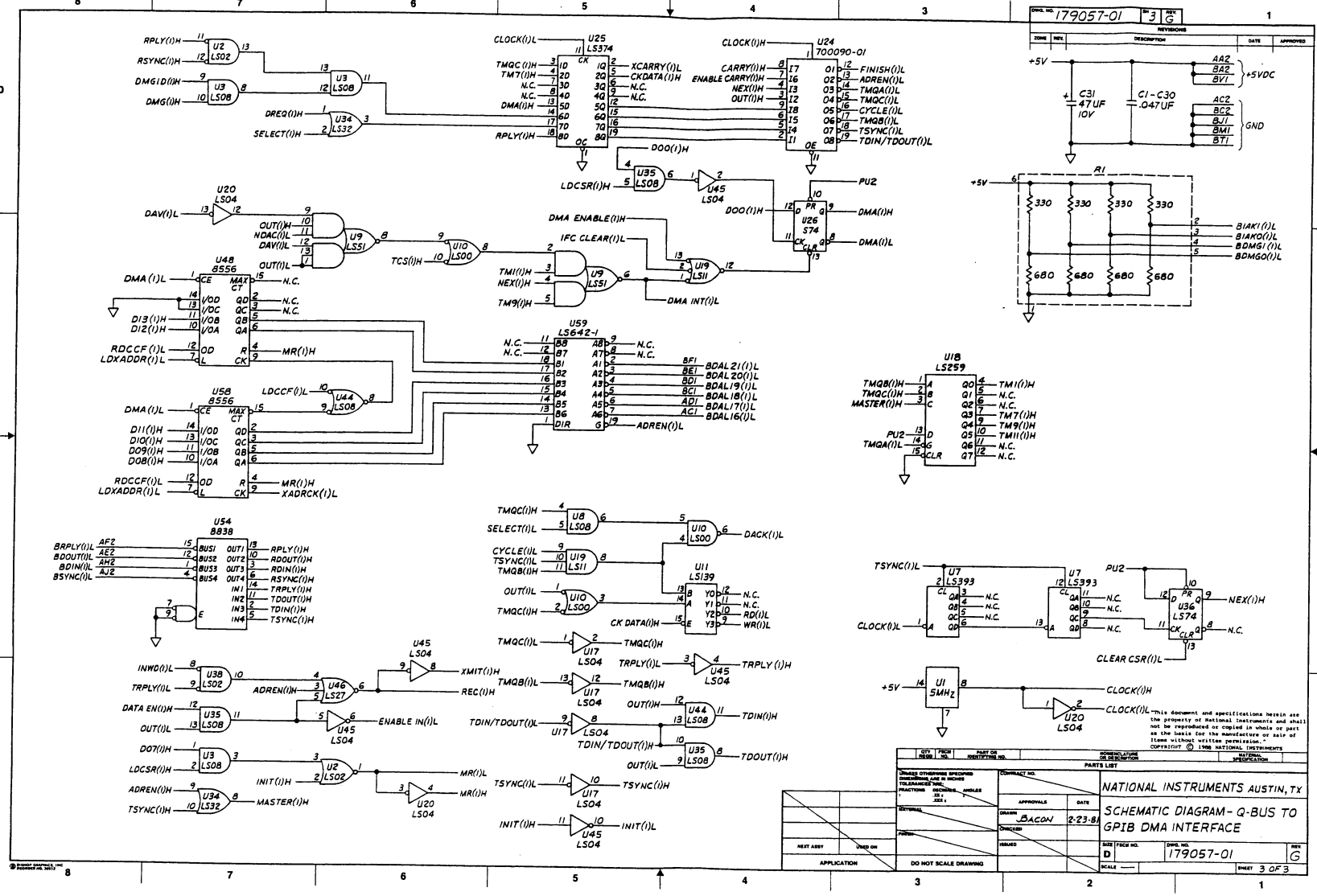
DRAWINGS

This section contains assembly drawings and the schematic diagrams of the GPIB11V-2.

Editor's note: Page numbers in Chapter 7 are intentionally odd-numbered. Original drawing sizes in the October 1988 printed manual used two pages. Drawings are resized for this PDF edition from 11x17 to 8x10, thus there are no odd-numbered pages.


DWG. NO. 179057-01 SH 1 REV G
REVISIONS
ZONE REV DESCRIPTION DATE APPROVED
G ADDED DECOUPLING CAPACITORS 5-31-85
U63 DC005
U62 DC005
U61 DC005
U60 DC005
U40 DC004
U56 8837
U55 LS642-1
U28 LS161
U42 DC006
U41 DC006
U36 LS74
U57 LS74
U47 LS74
U46 LS27
U53 LS02
U45 LS04
U39 LS04
U20 LS04
U37 LS32
U34 LS32
U21 LS32
U38 LS02
U44 LS08
U35 LS08
U10 LS00
U8 LS08
U2 LS02
U3 LS08
U5 LS14
U6 LS32
U7 LS04
U19 LS11
U52
U51
U50
PU2
DMG(I)H
DMG1(I)H
MR(I)L
R4 100
D1 IN5713
C8 100 PF
CARRY(I)H
OUTLB(I)L
SEL2(I)L
SEL0(I)L
INWD(I)L
ADREN(I)H
R5 1K
C9 100 PF
CLEAR CSR(I)L
N.C.
LATCHED IFC(I)H
R2 680
R3 1K
+5V
VECTOR(I)H
IRQ(I)H
INT(I)H
DMA INT(I)L
IE(I)H
MASTER(I)H
DMR(I)H
IAKO(I)H
BIRQ5(I)L
BIRQ6(I)L
BIRQ7(I)L
BIRQ4(I)L
BDMGO(I)L
BSACK(I)L
BDMR(I)L
BIAKO(I)L
BWTBT(I)L
ADREN(I)L
OUT(I)L
TSYNC(I)H
DATA EN(I)H
SEL6(I)L
LDCCF(I)L
LDXADDR(I)L
RDCCF(I)L
SELECT(I)L
DMA(I)H
RS0(I)H
RS1(I)H
RS2(I)H
LDCSR(I)L
LDCSR(I)H
RDCSR(I)L
SEL4(I)L
CYCLE(I)L
TDIN/TDOUT(I)H
BCR COUNT(I)H
SRQ(I)L
SRQIE(I)H
REQIFC(I)H
RDIN(I)L
INIT(I)L
IAKO(I)H
XMIT(I)H
REC(I)H
XADRCK(I)L
TRPLY(I)L
BBS7(I)L
179055 GPIB11-V2
APPLICATION
DO NOT SCALE DRAWING
NATIONAL INSTRUMENTS AUSTIN, TX
SCHEMATIC DIAGRAM-Q-BUS TO GPIB DMA INTERFACE
DRAWN BACON 2-23-81
CHECKED 4-20-81
SIZE D DWG. NO. 179057-01 REV G
SHEET 1 OF 3
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DWG. NO. 179057-01
SZ Z
REV G
REVISIONS
ZONE REV. DESCRIPTION DATE APPROVED
U30 LS374
U29 LS374
U31 LS374
U33 LS374
U32 LS374
U23 LS174
U27 LS174
U49 LS367
U43 LS368
U22 8291
U13 3448
U14 3448
U12 3448
U15 3448
U17 LS04
U20 LS04
U39 LS04
U4 LS74
U11 LS139
U5 LS14
U6 LS368
U53 LS02
U50
J1
LDCCR(I)H
CKDATA(I)H
XCARRY(I)L
TMII(I)H
ENABLE IN(I)L
CKDATA(I)H
LOBYTE(I)L
TMII(I)H
HIBYTE(I)L
LDCSR(I)H
LDCSR(I)H
MR(I)L
PU3
RDCSR(I)L
N.C.
IE(I)H
CIC(I)H
NEX(I)H
LATCHED IFC(I)H
RDCSA(I)L
DO4(I)H
DO5(I)H
DO6(I)H
DI4(I)H
DI5(I)H
DMA(I)H
RATN(I)L
TRI EN(I)H
DAV(I)L
SRQ(I)L
INT(I)L
DO7(I)H
DO9(I)H
DIO(I)H
DII(I)H
DI2(I)H
DI3(I)H
OUT(I)H
OUT(I)L
SELECT(I)H
SELECT(I)L
INT(I)H
INT(I)L
RSYNC(I)H
RSYNC(I)L
RDOUT(I)H
RDOUT(I)L
RDIN(I)H
RDIN(I)L
DOO(I)H
TSYNC(I)H
MR(I)L
CIC(I)H
SRQIE(I)H
TIFC(I)H
ENABLE CARRY(I)H
IE(I)H
TCS(I)H
DMA ENABLE(I)H
XCARRY(I)L
OUT(I)L
LOBYTE(I)L
HIBYTE(I)L
TIFC(I)H
SYSTEM CONTROLLER(I)H
TR/I(I)H
TR/2(I)H
CLOCK(I)H
MR(I)H
DREQ(I)H
DACK(I)L
DMA(I)L
RD(I)L
WR(I)L
INT(I)H
+5V
GND
RS2(I)H
RS1(I)H
RS0(I)H
NDAC(I)L
NRFD(I)H
REN(I)H
RATN(I)L
TR/2(I)H
SELECT(I)H
IFC CLEAR(I)L
MR(I)H
RECIFC(I)H
SRQ(I)L
TR/I(I)H
CIC(I)H
E2
E1
N.C.
GPIB DIO8(I)L
GPIB DIO7(I)L
GPIB DIO6(I)L
GPIB DIO5(I)L
TRI EN(I)H
GPIB DIO4(I)L
GPIB DIO3(I)L
GPIB DIO2(I)L
GPIB DIO1(I)L
GPIB EOI(I)L
GPIB DAV(I)L
GPIB NRFD(I)L
GPIB NDAC(I)L
GPIB IFC(I)L
GPIB ATN(I)L
GPIB SRQ(I)L
GPIB REN(I)L
R6 1K
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PARTS LIST
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SCHEMATIC DIAGRAM-Q-BUS TO GPIB DMA INTERFACE
DRAWN BACON 2-23-81
SIZE D FSCM NO. DWG. NO. 179057-01 REV G
SCALE SHEET 2 OF 3
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APPLICATION


DWG. NO. 179057-01 SH 3 REV G
REVISIONS
ZONE REV. DESCRIPTION DATE APPROVED
U2 LS02
U3 LS08
U34 LS32
U25 LS374
U24 700090-01
U35 LS08
U45 LS04
U26 S74
U20 LS04
U9 LS51
U10 LS00
U9 LS11
U48 8556
U59 LS642-1
U58 8556
U44 LS08
U54 8838
U8 LS08
U10 LS00
U9 LS11
U11 LS139
U10 LS00
U17 LS04
U45 LS04
U38 LS02
U46 LS27
U45 LS04
U35 LS08
U3 LS08
U2 LS02
U34 LS32
U20 LS04
U18 LS259
U7 LS393
U7 LS393
U36 LS74
U1 5MHz
U20 LS04
+5V
C31 47UF 10V
C1-C30 .047UF
+5VDC
GND
R1
330
680
DMA ENABLE(I)H
IFC CLEAR(I)L
DMA INT(L)
DACK(I)L
XMIT(I)H
REC(I)H
ENABLE IN(I)L
TRPLY(I)H
TDIN(I)H
TDOUT(I)H
CLOCK(I)H
CLOCK(I)L
NEX(I)H
CLEAR CSR(I)L
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ISSUED
NATIONAL INSTRUMENTS AUSTIN, TX
SCHEMATIC DIAGRAM- Q-BUS TO GPIB DMA INTERFACE
SIZE D FSCM NO. DWG. NO. 179057-01 REV G
SCALE — SHEET 3 OF 3

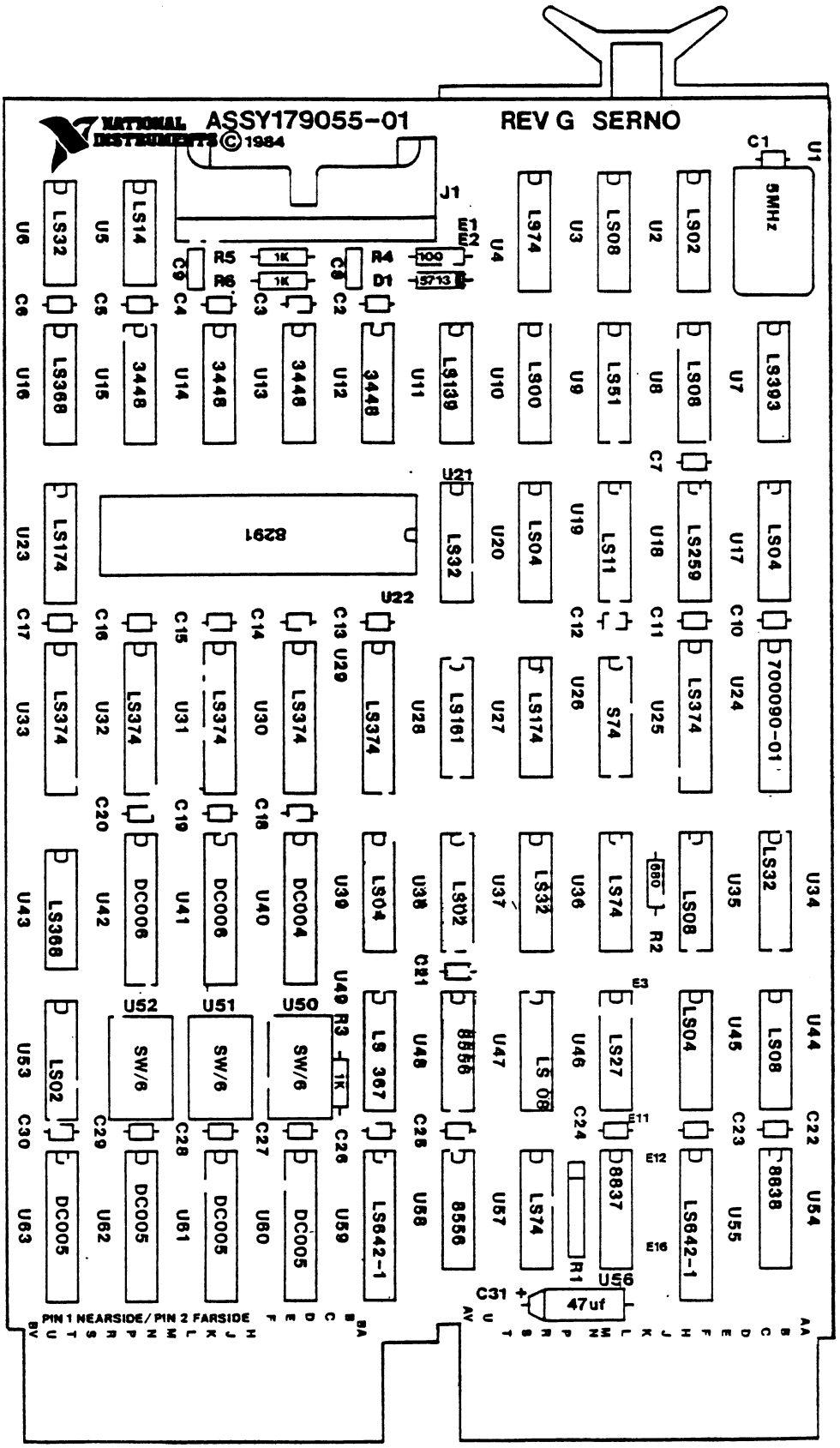


FIGURE 7.1

COMPONENT LOCATION

Appendix A
Multiline Interface Messages

The following tables are multiline interface messages (sent and received with ATN TRUE).

Multiline Interface Messages

Hex	Oct	Dec	ASCII	Msg	Hex	Oct	Dec	ASCII	Msg
00	000	0	NUL		20	040	32	SP	MLA0
01	001	1	SOH	GTL	21	041	33	!	MLA1
02	002	2	STX		22	042	34	"	MLA2
03	003	3	ETX		23	043	35	#	MLA3
04	004	4	EOT	SDC	24	044	36	$	MLA4
05	005	5	ENQ	PPC	25	045	37	%	MLA5
06	006	6	ACK		26	046	38	&	MLA6
07	007	7	BEL		27	047	39	'	MLA7
08	010	8	BS	GET	28	050	40	(	MLA8
09	011	9	HT	TCT	29	051	41	)	MLA9
0A	012	10	LF		2A	052	42	*	MLA10
0B	013	11	VT		2B	053	43	+	MLA11
0C	014	12	FF		2C	054	44	,	MLA12
0D	015	13	CR		2D	055	45	-	MLA13
0E	016	14	SO		2E	056	46	.	MLA14
0F	017	15	SI		2F	057	47	/	MLA15
10	020	16	DLE		30	060	48	0	MLA16
11	021	17	DC1	LLO	31	061	49	1	MLA17
12	022	18	DC2		32	062	50	2	MLA18
13	023	19	DC3		33	063	51	3	MLA19
14	024	20	DC4	DCL	34	064	52	4	MLA20
15	025	21	NAK	PPU	35	065	53	5	MLA21
16	026	22	SYN		36	066	54	6	MLA22
17	027	23	ETB		37	067	55	7	MLA23
18	030	24	CAN	SPE	38	070	56	8	MLA24
19	031	25	EM	SPD	39	071	57	9	MLA25
1A	032	26	SUB		3A	072	58	:	MLA26
1B	033	27	ESC		3B	073	59	;	MLA27
1C	034	28	FS		3C	074	60	<	MLA28
1D	035	29	GS		3D	075	61	=	MLA29
1E	036	30	RS		3E	076	62	>	MLA30
1F	037	31	US		3F	077	63	?	UNL

Multiline Interface Messages

Hex	Oct	Dec	ASCII	Msg	Hex	Oct	Dec	ASCII	Msg
40	100	64	@	MTA0	60	140	96	`	MSA0,PPE
41	101	65	A	MTA1	61	141	97	a	MSA1,PPE
42	102	66	B	MTA2	62	142	98	b	MSA2,PPE
43	103	67	C	MTA3	63	143	99	c	MSA3,PPE
44	104	68	D	MTA4	64	144	100	d	MSA4,PPE
45	105	69	E	MTA5	65	145	101	e	MSA5,PPE
46	106	70	F	MTA6	66	146	102	f	MSA6,PPE
47	107	71	G	MTA7	67	147	103	g	MSA7,PPE
48	110	72	H	MTA8	68	150	104	h	MSA8,PPE
49	111	73	I	MTA9	69	151	105	i	MSA9,PPE
4A	112	74	J	MTA10	6A	152	106	j	MSA10,PPE
4B	113	75	K	MTA11	6B	153	107	k	MSA11,PPE
4C	114	76	L	MTA12	6C	154	108	l	MSA12,PPE
4D	115	77	M	MTA13	6D	155	109	m	MSA13,PPE
4E	116	78	N	MTA14	6E	156	110	n	MSA14,PPE
4F	117	79	O	MTA15	6F	157	111	o	MSA15,PPE
50	120	80	P	MTA16	70	160	112	p	MSA16,PPD
51	121	81	Q	MTA17	71	161	113	q	MSA17,PPD
52	122	82	R	MTA18	72	162	114	r	MSA18,PPD
53	123	83	S	MTA19	73	163	115	s	MSA19,PPD
54	124	84	T	MTA20	74	164	116	t	MSA20,PPD
55	125	85	U	MTA21	75	165	117	u	MSA21,PPD
56	126	86	V	MTA22	76	166	118	v	MSA22,PPD
57	127	87	W	MTA23	77	167	119	w	MSA23,PPD
58	130	88	X	MTA24	78	170	120	x	MSA24,PPD
59	131	89	Y	MTA25	79	171	121	y	MSA25,PPD
5A	132	90	Z	MTA26	7A	172	122	z	MSA26,PPD
5B	133	91	[	MTA27	7B	173	123	{	MSA27,PPD
5C	134	92	\	MTA28	7C	174	124	|	MSA28,PPD
5D	135	93	]	MTA29	7D	175	125	}	MSA29,PPD
5E	136	94	^	MTA30	7E	176	126	~	MSA30,PPD
5F	137	95	_	UNT	7F	177	127	DEL	

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Title: **GPIB11V-2 Operating and Service Manual**

Edition Date: **October 1988**

Part Number: **320006-01**

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