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NI 6583R User Guide and Specifications

The NI 6583R is a single-ended and differential signaling device designed to work in conjunction with your NI FlexRIO™ FPGA module. The NI 6583 is available in two versions: one with low-voltage differential signals (LVDS) and another with multipoint low-voltage differential signals (MLVDS). The term, *differential*, in this document refers to both LVDS and MLVDS signals unless otherwise specified.

This document contains signal information and specifications for the NI 6583R, which is composed of an NI FlexRIO FPGA module and the NI 6583. This document also contains tutorial sections that demonstrate how to acquire data using a LabVIEW FPGA example VI and how to create and run your own LabVIEW project with the NI 6583R.

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Note Before configuring your NI 6583R, you must install the appropriate software and hardware. Refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications* for installation instructions. Figure 1 shows an example of a properly connected NI FlexRIO device.

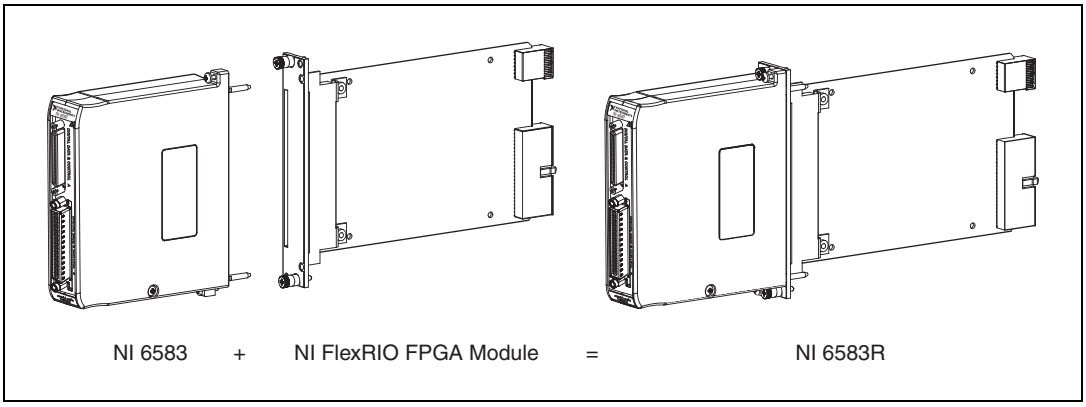


Figure 1. NI 6583R

Note *NI 6583R* refers to the combination of your NI 6583 adapter module and your NI FlexRIO FPGA module. *NI 6583* refers only to your NI 6583 adapter module.

How to Use Your NI FlexRIO Documentation Set

Refer to Figure 2 and Table 1 for information about how to use your NI FlexRIO documentation set.

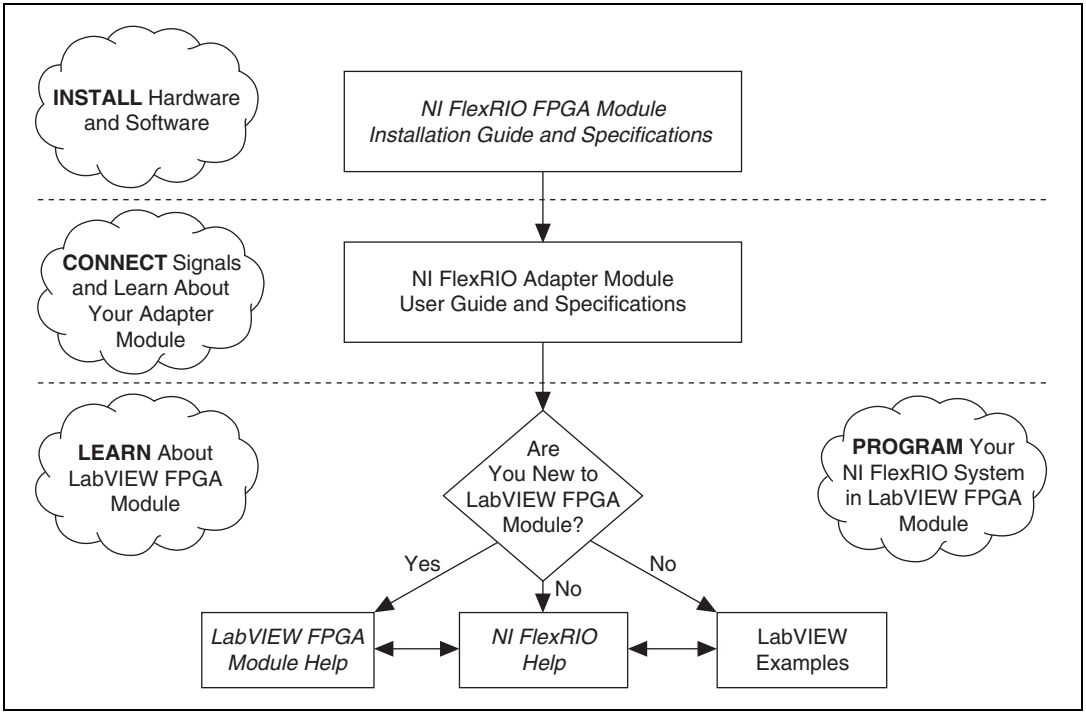


Figure 2. How to Use Your NI FlexRIO Documentation Set

Table 1. NI FlexRIO Documentation Locations and Descriptions

Document	Location	Description
NI FlexRIO FPGA Module Installation Guide and Specifications[*]	Available in your FPGA module hardware kit and from the Start Menu.	Contains installation instructions for your NI FlexRIO system and specifications for your FPGA module.
NI Adapter Module User Guide and Specifications[*]	Available in your adapter module hardware kit and from the Start Menu.	Contains signal information, examples, and specifications for your adapter module.
LabVIEW FPGA Module Help[*]	Embedded in *LabVIEW Help*.	Contains information about the basic functionality of LabVIEW FPGA Module.
NI FlexRIO Help[*]	Embedded in *LabVIEW FPGA Module Help*.	Contains FPGA module, adapter module, and CLIP configuration information.
LabVIEW Examples	Available in NI Example Finder.	Contains examples of how to run FPGA VIs and Host VIs on your device.
Other useful information on `ni.com`		
`ni.com/ipnet`	Contains LabVIEW FPGA functions and intellectual property to share.	
`ni.com/flexrio`	Contains product information and data sheets for NI FlexRIO devices.	
[*] These documents are also available at `ni.com/manuals`.		

Figure 3 shows the digital data and control (DDC) connector pin assignments for the NI 6583. DDC A contains the single-ended lines and DDC B contains the differential lines.

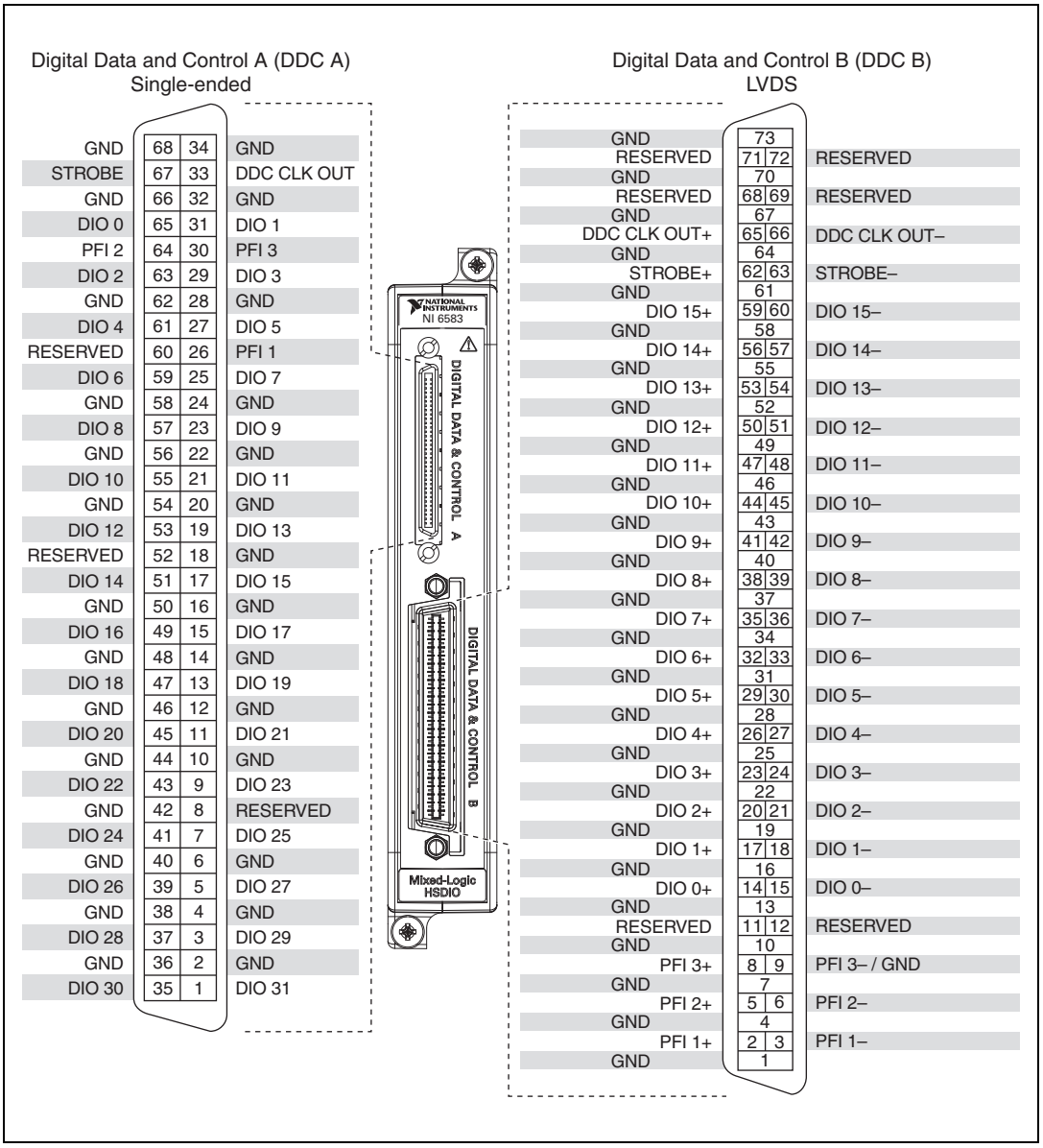


Figure 3. NI 6583 Connector Pin Assignments

Caution Connections that exceed any of the maximum ratings of input or output signals on the NI 6583R can damage the device and the chassis. NI is *not* liable for any damage resulting from such signal connections. For the maximum input and output ratings for each signal, refer to the *Specifications* section of this document.

Note If you design a custom cabling solution with the DDC B differential connector (779157-01) and NI SHB12X-B12X cable (192344-01), the NI 6583 pinout is reversed at the end connector. For example, the signal shown on pin 1 shown in Figure 3 maps to pin 73 at the end connector.

Pin and Signal Tables

Table 2 contains pin location and single-ended signal information for DDC A on the NI 6583.

Table 2. NI 6583 DDC A Connector Pins

Signal Name	Pin(s)	Signal Type	Signal Description
DDC CLK OUT	33	Clock	Terminal for the single-ended exported Sample clock.
STROBE	67	Clock	External Sample clock source that can be used for source synchronous acquisition.
DIO <0..31>	1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 35, 37, 39, 41, 43, 45, 47, 49, 51, 53, 55, 57, 59, 61, 63, 65	Data	Bidirectional single-ended digital I/O data channels 0 through 31.
PFI <1..3>	26, 30, 64	Control/Data	Bidirectional single-ended digital I/O trigger channels 1 through 3.
GND	2, 4, 6, 10, 12, 14, 16, 18, 20, 22, 24, 28, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 54, 56, 58, 62, 66, 68	Ground	Ground reference for signals.
RESERVED	8, 52, 60	—	These terminals are reserved for future use. Do not connect to these pins.

Table 3 contains pin location and differential signal information for DDC B on the NI 6583.

Table 3. NI 6583 DDC B Connector Pins

Signal Name	Pin(s)	Signal Type	Signal Description
DDC CLK OUT+	65	Clock	Positive terminal for the differential exported Sample clock.
DDC CLK OUT–	66	Clock	Negative terminal for the differential exported Sample clock.
STROBE+	62	Clock	Positive external Sample clock source that can be used for dynamic acquisition.
STROBE–	63	Clock	Negative external Sample clock source that can be used for dynamic acquisition.
DIO <0..15>+	14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 53, 56, 59	Data	Positive bidirectional digital I/O data channels 0 through 15.
DIO <0..15>–	15, 18, 21, 24, 27, 30, 33, 36, 39, 42, 45, 48, 51, 54, 57, 60	Data	Negative bidirectional digital I/O data channels 0 through 15
PFI <1..3>+	2, 5, 8	Control	Positive bidirectional digital I/O trigger channels 1 through 3.
PFI <1..3>–	3, 6, 9	Control	Negative bidirectional digital I/O trigger channels 1 through 3.
GND	1, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31, 34, 37, 40, 43, 46, 49, 52, 55, 58, 61, 64, 67, 70, 73	Ground	Ground reference for signals.
RESERVED	11, 12, 68, 69, 71, 72	—	These terminals are reserved for future use. Do not connect to these pins.

Block Diagrams

Figures 4 through 7 show the data flow through the NI 6583R. Single-ended data lines use standardized voltage levels to interpret data as either a binary zero or a one in high-speed digital data transfers. Differential data lines provide a low-noise, low-power, low-amplitude differential method for high-speed digital data transfer.

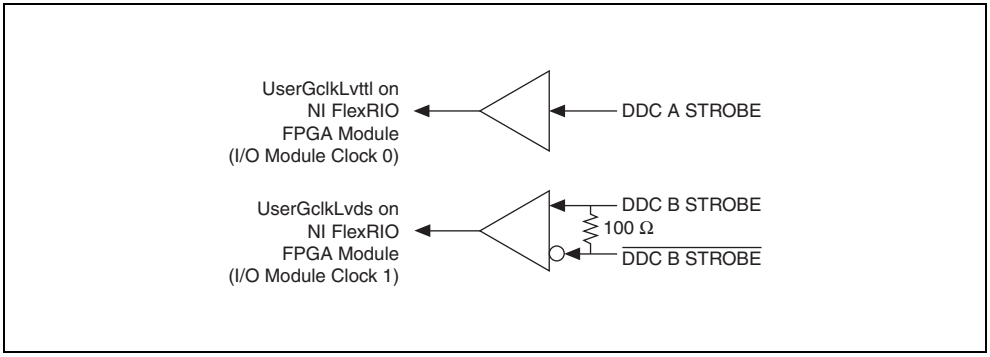


Figure 4. Clock Input Signals

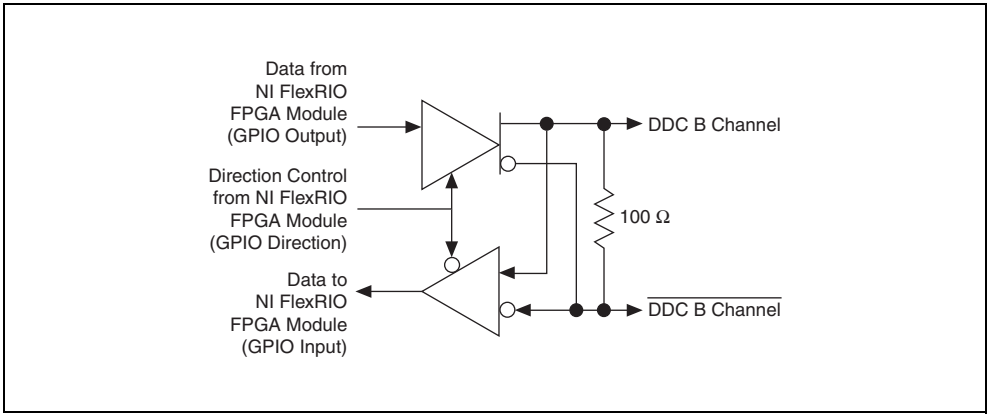


Figure 5. Differential Data and PFI Lines

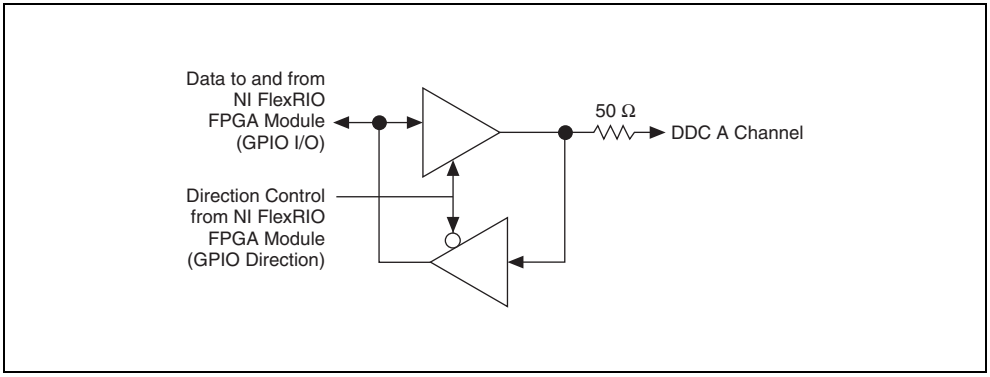


Figure 6. Single-Ended Data and PFI Lines

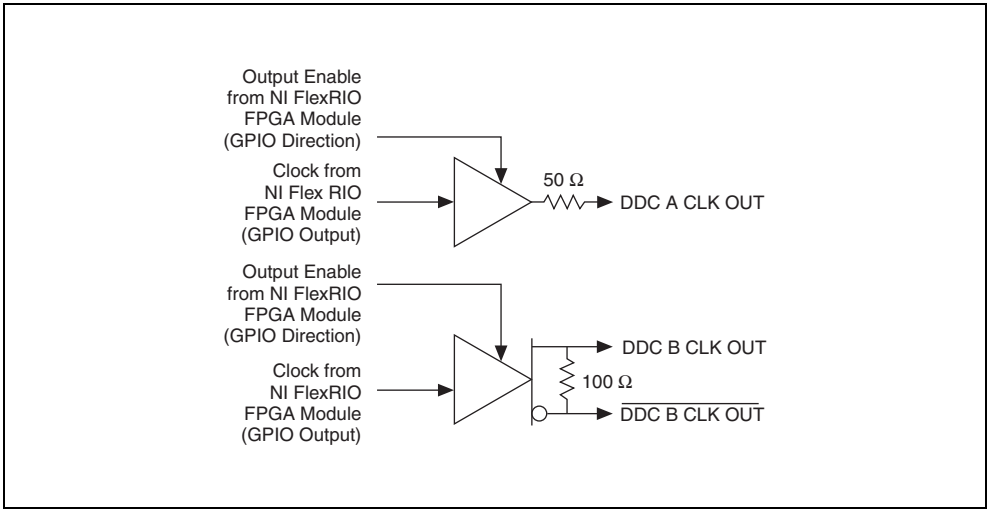


Figure 7. Clock Output Signals

Tables 4 and 5 list the NI 6583 connector signals and corresponding NI FlexRIO FPGA module signals necessary for designing custom component-level IP (CLIP). The *_CC* suffix on the single-ended and differential signals identifies channels that are capable of receiving a regional clock. Refer to the *Block Diagrams* section of this document for more information about connecting signals from the NI 6583 to the FPGA module.

Table 4. NI 6583 Single-Ended Signals and NI FlexRIO FPGA Module Signals

NI 6583		NI FlexRIO FPGA Module	
Connector	**Signal Name**	**GPIO I/O**	**GPIO Direction**
DDC A (Single-ended I/O)	DIO 0	GPIO_16_n	GPIO_16
	DIO 1	GPIO_2_n	GPIO_2
	DIO 2	GPIO_19_n	GPIO_19
	DIO 3	GPIO_5_n_CC	GPIO_5_CC
	DIO 4	GPIO_20_n	GPIO_20
	DIO 5	GPIO_4_n_CC	GPIO_4_CC
	DIO 6	GPIO_7_n_CC	GPIO_7_CC
	DIO 7	GPIO_3_n	GPIO_3
	DIO 8	GPIO_23_n_CC	GPIO_23_CC
	DIO 9	GPIO_6_n_CC	GPIO_6_CC
	DIO 10	GPIO_22_n	GPIO_22
	DIO 11	GPIO_21_n	GPIO_21
	DIO 12	GPIO_25_n_CC	GPIO_25_CC
	DIO 13	GPIO_10_n	GPIO_10
	DIO 14	GPIO_24_n_CC	GPIO_24_CC
	DIO 15	GPIO_9_n	GPIO_9
	DIO 16	GPIO_12_n	GPIO_12
	DIO 17	GPIO_8_n	GPIO_8
	DIO 18	GPIO_27_n	GPIO_27
	DIO 19	GPIO_28_n	GPIO_28
	DIO 20	GPIO_11_n	GPIO_11
	DIO 21	GPIO_26_n_CC	GPIO_26_CC
	DIO22	GPIO_30_n	GPIO_30
	DIO 23	GPIO_15_n	GPIO_15
	DIO 24	GPIO_29_n	GPIO_29
	DIO 25	GPIO_14_n	GPIO_14

Table 4. NI 6583 Single-Ended Signals and NI FlexRIO FPGA Module Signals (Continued)

NI 6583		NI FlexRIO FPGA Module	
Connector	**Signal Name**	**GPIO I/O**	**GPIO Direction**
DDC A (Single-ended I/O)	DIO 26	GPIO_50_n	GPIO_50
	DIO 27	GPIO_13_n	GPIO_13
	DIO 28	GPIO_32_n	GPIO_32
	DIO 29	GPIO_31_n	GPIO_31
	DIO 30	GPIO_49_n	GPIO_49
	DIO 31	GPIO_33_n	GPIO_33
	PFI 1	GPIO_0_n	GPIO_0
	PFI 2	GPIO_18_n	GPIO_18
	PFI 3	GPIO_1_n	GPIO_1
	STROBE	GClk_SE	—
	CLK OUT	GPIO_17_n	GPIO_17 (as enable)

Note For the DIO and PFI lines, drive the GPIO Direction high for output and low for input. For CLK OUT, drive the GPIO Direction high for enable and low for disable.

Table 5. NI 6583 Differential Signals and NI FlexRIO FPGA Module Signals

NI 6583		NI FlexRIO FPGA Module		
Connector	**Signal Name**	**GPIO Input**	**GPIO Output**	**GPIO Direction**
DDC B (Differential I/O)	DIO 0+/–	GPIO_48	GPIO_47_n	GPIO_48_n
	DIO 1+/–	GPIO_44_n	GPIO_45	GPIO_45_n
	DIO 2+/–	GPIO_41	GPIO_40_n_CC	GPIO_40_CC
	DIO 3+/–	GPIO_61	GPIO_60_n	GPIO_60
	DIO 4+/–	GPIO_62	GPIO_61_n	GPIO_62_n
	DIO 5+/–	GPIO_64	GPIO_63_n	GPIO_63
	DIO 6+/–	GPIO_42	GPIO_42_n	GPIO_41_n
	DIO 7+/–	GPIO_56_CC	GPIO_55_n	GPIO_56_n_CC
	DIO 8+/–	GPIO_54_n	GPIO_54	GPIO_55
	DIO 9+/–	GPIO_39_n_CC	GPIO_39_CC	GPIO_38_n_CC
	DIO 10+/–	GPIO_58_CC	GPIO_57_n_CC	GPIO_57_CC
	DIO 11+/–	GPIO_59_CC	GPIO_58_n_CC	GPIO_59_n_CC
	DIO 12+/–	GPIO_51_n	GPIO_51	GPIO_52
	DIO 13+/–	GPIO_36	GPIO_35_n	GPIO_35
	DIO 14+/–	GPIO_53_n	GPIO_53	GPIO_52_n
	DIO 15+/–	GPIO_37_CC	GPIO_36_n	GPIO_37_n_CC
	PFI 1+/–	GPIO_43_n	GPIO_43	GPIO_44
	PFI 2+/–	GPIO_47	GPIO_46_n	GPIO_46
	PFI 3+/–	GPIO_65_n	GPIO_65	GPIO_64_n
	STROBE+/–	GClk_LVDS	—	—
	CLK OUT+/–	—	GPIO_34_n	GPIO_34 (as enable)

Connecting Cables and Accessories

Use an NI SHC68-C68-D4 shielded cable (NI part number 781013-01) for connections to the DDC A connector. The NI SHC68-C68-D4 is designed for single-ended, high-speed digital signal transmission. The cable is shielded, with individual microcoaxial 50 Ω lines for each signal.

Use an SHB12X-B12X shielded cable (NI part number 192344-01) for connections to the DDC B connector. This cable is designed for differential, high-speed digital signal transmission.

Caution The NI 6583R must be operated with shielded cables and shielded accessories to ensure compliance with the Electromagnetic Compatibility (EMC) requirements defined in the *Specifications* section of this document. Do not use unshielded cables or accessories unless they are installed in a shielded enclosure with properly designed and shielded input/output ports and connected to the NI 6583R using a shielded cable. If unshielded cables or accessories are not properly installed and shielded, the EMC specifications for the NI 6583R are no longer guaranteed.

The following NI cables and accessories are *not* properly shielded for EMC-compliant use with the NI 6583:

- NI CB-2162 single-ended digital I/O accessory
- NI SHC68-H1X38 high-speed digital flying-leads cable accessory
- NI SMA-2164 prototyping accessory for NI 656X
- NI SHB12X-H3X24 differential flying-lead/LA cable for HSDIO

Using Accessories

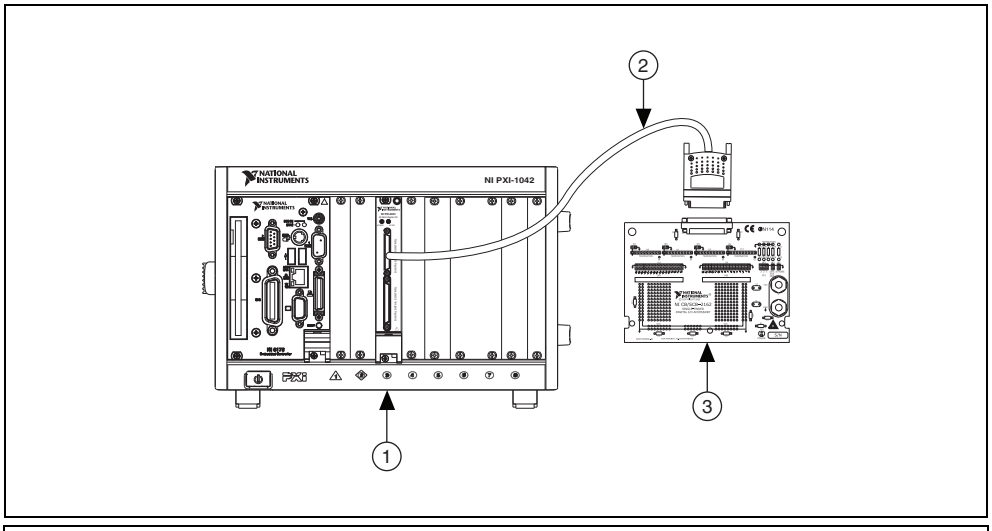
Note Whether you use NI cables and accessories or design your own, you should properly terminate cables to avoid improper measurements caused by signal reflections, overshoot, and undershoot.

Single-Ended Accessories

NI recommends using the NI CB-2162 single-ended digital I/O accessory to access the signals on the 68-pin DDC A connector and to terminate the DIO channels. The NI CB-2162 also provides a platform for circuit prototyping and DUT testing. The NI CB-2162 is specifically designed for use with single-ended devices. For more information about the NI CB-2162, refer to the *NI CB-2162 User Guide*.

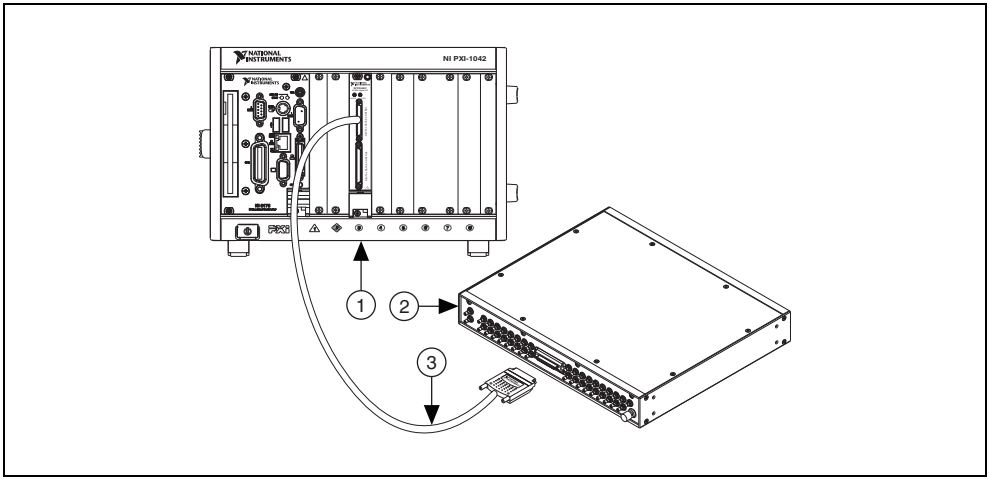
NI also offers the NI SMB-2163 breakout box for National Instruments single-ended digital waveform generator/analyzers. The NI SMB-2163 offers coaxial SMB connectors for each channel on the DDC A connector, providing an easy way to connect to other devices for testing and debugging. For more information about the NI SMB-2163, refer to the *NI SMB-2163 User Guide*.

Figures 8 and 9 show how to connect the single-ended DDC A connector and the NI CB-2162 and NI SMB-2163, respectively, using the NI SHC68-C68-D4 cable.



1	PXI/PXI Express Chassis with NI 6583R	3	NI CB-2162 Accessory
2	NI SHC68-C68-D4 Cable		

Figure 8. Connecting the NI CB-2162 Accessory

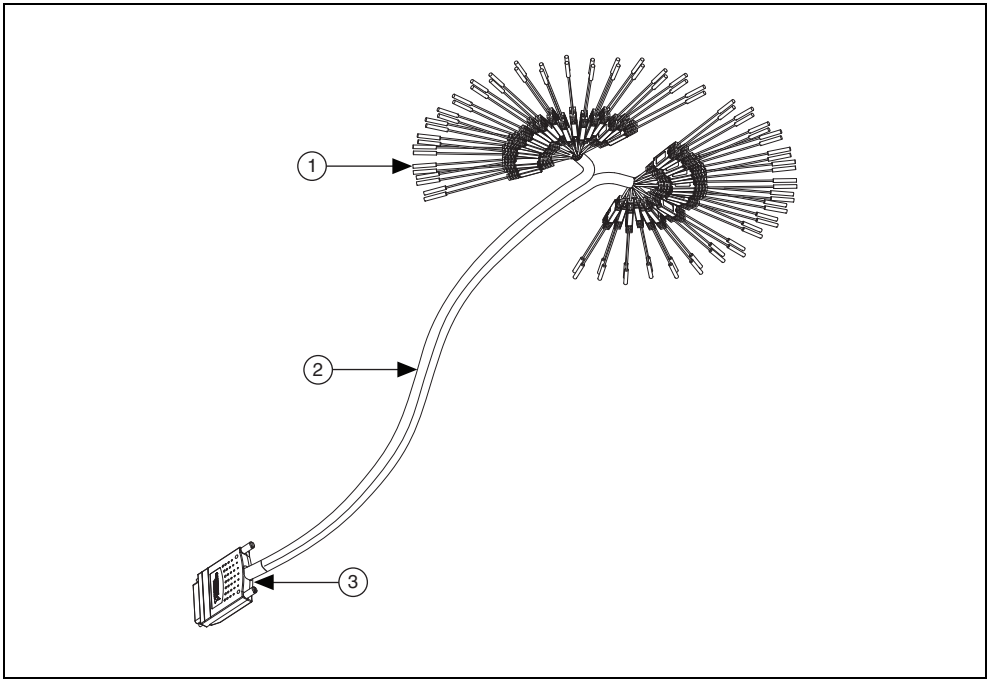


1	PXI/PXI Express Chassis with NI 6583R	3	NI SHC68-C68-D4 Cable
2	NI SMB-2163 Accessory		

Figure 9. Connecting the NI SMB-2163 Accessory

The NI SHC68-H1X38 cable is a single-ended cable that breaks out each single-ended signal into two 0.1 inch header receptacles, one receptacle each for the signal and ground. The NI SHC68-H1X38 cable provides an easy way to connect NI single-ended high-speed digital signals to various types of devices and circuits for interfacing, testing, or analysis.

This cable offers connectivity similar to that found on a typical logic analyzer, so you can use it in logic analyzer-type applications. Unlike a typical logic analyzer, however, this cable also allows for simultaneous pattern generation and acquisition so that you can use it in stimulus/response applications as well. The following figure shows the single-ended digital flying lead cable.



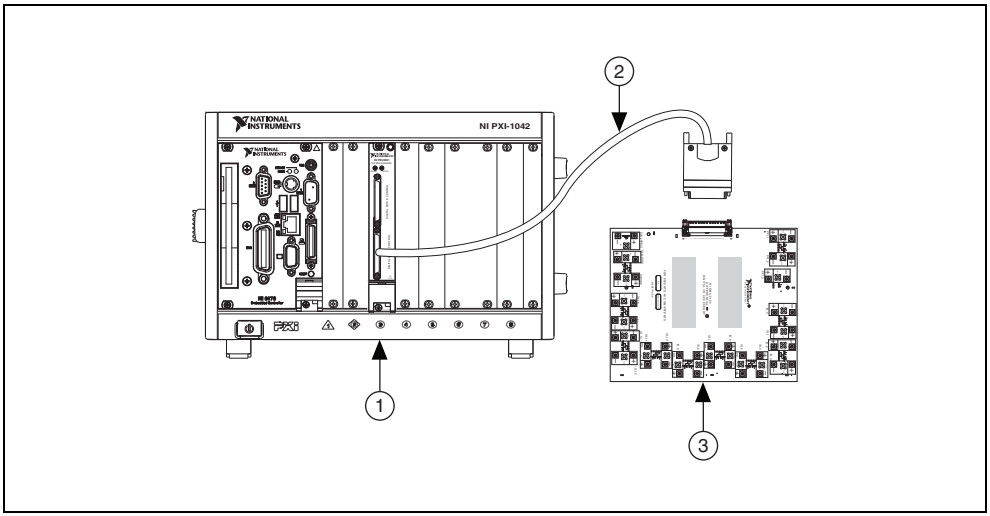
1	Lead Pairs	2	Removable Sleeving	3	68-Pin DDC A Connector

Figure 10. Single-Ended Flying Lead Cable Parts Locator Diagram

Differential Accessories

The NI SMA-2164 test fixture is a breakout box for differential signals. This fixture provides an easy way to connect to other devices for testing and debugging. For more information about using the NI SMA-2164, refer to the *NI SMA-2164 User Guide*.

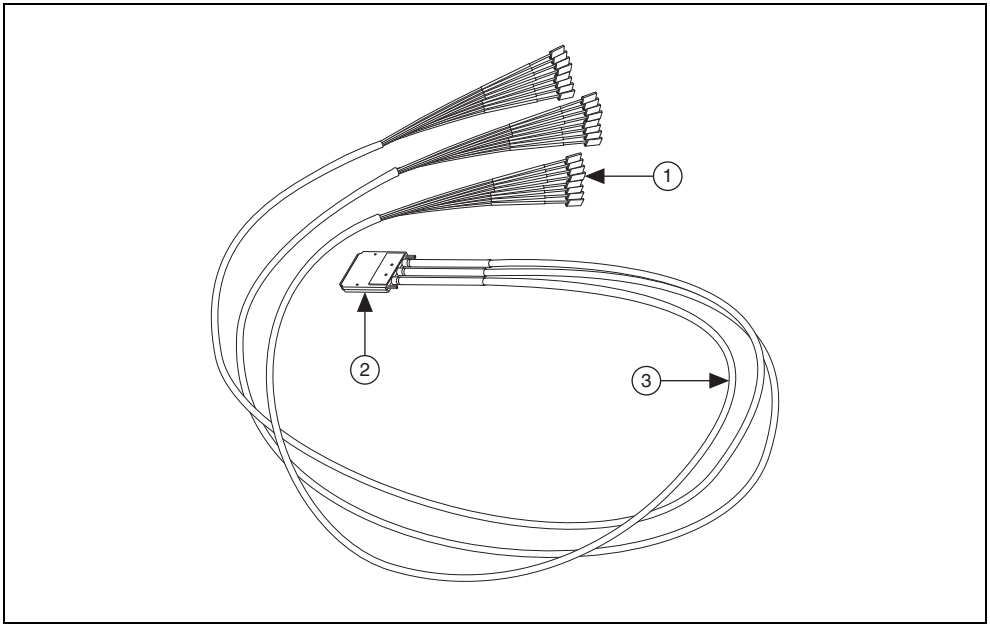
Figure 11 shows how to connect the differential DDC B connector to the NI SMA-2164 using the NI SHB12X-B12X cable.



1	PXI/PXI Express Chassis with an NI 6583R	3	NI SMA-2164
2	NI SHB12-B12X Cable		

Figure 11. Connecting the NI SMA-2164 Accessory

A flying lead cable, the NI SHB12X-H3X24, is also available for differential signals. This cable offers connectivity similar to that found on a typical logic analyzer, so you can use it in logic analyzer-type applications. This cable is shown in Figure 12.



1	Leads (1 × 3 Header Receptacle)	3	Removeable Sleeving
2	DDC B Connector		

Figure 12. NI SHB12X-H3X24 Flying Lead Cable

Creating a Custom Accessory

Many common applications may require you to create a custom accessory to easily access the signals of your device under test (DUT). If you are creating a custom accessory to use with a device with a VHDCI DDC connector, you can purchase the mating connector for the VHDCI cable from NI. For more information about creating these custom accessories, refer to the *Interfacing to the NI Digital Waveform Generator/Analyzer using the VHDCI Connector* application note, available by entering `rdinwa` in the text field at `ni.com/info`. If you are designing a custom accessory to use with a device that uses an InfiniBand connector, you can also purchase this connector.

Note If you design a custom cabling solution with the DDC B differential connector (779157-01) and SHB12X-B12X shielded cable (192344-01), the NI 6583 pinout is reversed at the end connector. For example, the signal shown on pin 1 maps to pin 73 at the end connector. Refer to *Front Panel and Connector Pinouts* section in this document for more pinout information.

Note You must install the software before doing this example. Refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications* for more information about installing your software.

The NI FlexRIO Adapter Module Support installation software includes a variety of example projects to help get you started creating your LabVIEW FPGA program. This section demonstrates how to use an existing LabVIEW FPGA example project to generate and acquire samples with the NI 6583R. This example requires the NI SHC68-C68-D4 and the NI SHB12X-B12X shielded cables and the appropriate accessories for your device. Refer to the *Using Accessories* section of this document for more information about accessories.

Note The examples available for your device are dependent on the version of the software and driver you are using. For information about which software versions are compatible with your device, visit `ni.com/info` and enter `rdsoftwareversion` as the Info Code.

Each NI 6583 example project includes the following items:

- A LabVIEW FPGA VI that can be compiled and run on the FPGA embedded in the hardware
- A VI that runs on Windows that interacts with the LabVIEW FPGA VI

Note In the LabVIEW FPGA Module software, NI FlexRIO adapter modules are referred to as *IO Modules*.

Complete the following steps to run an example VI that generates a waveform on the even channels of your device and then acquires that waveform on the odd channels of your device.

Hardware Configuration

1. For single-ended acquisition and generation, connect one end of the NI SHC68-C68-D4 shielded cable to DDC A on the NI 6583 front panel and one end to a single-ended accessory device. For differential acquisition and generation, connect one end of the NI SHB12X-B12X shielded cable to DDC B on the NI 6583 front panel and one end to a differential accessory device. Refer to the *Using Accessories* section of this document for more information about appropriate accessories for your device.
2. On your accessory devices, connect the first eight even channels (DIO <0..14>) to the first eight odd channels (DIO <1..15>).

Software Configuration

1. Launch LabVIEW.
2. In the **Getting Started** window, click **Find Examples** to display the NI Example Finder.
3. In the **NI Example Finder** window, select **Hardware Input and Output»FlexRIO» IO Modules»NI 6583**.
4. Select **NI 6583 Finite Acquisition and Generation - Simple.lvproj**.
5. In the **Project Explorer** window, open **NI 6583 Acquisition and Generation Simple (Host).vi** under **My Computer**. The host VI opens. The VI uses the NI PXI-7952R as the FPGA target. If you are not using an NI PXI-7952R, complete the following steps to change the FPGA target.

Note All example projects are configured for RIO0. If your device is not RIO0, you must update the target device name by right-clicking your device in the **Project Explorer** window, selecting **Properties**, and entering the correct target device name in the **Resource** box.

a. Select **Window»Show Block Diagram** to open the VI block diagram.

b. On the block diagram, right-click the Open FPGA VI Reference (NI PXI-7952R) function and select **Configure Open FPGA VI Reference**.

c. In the **Configure Open FPGA VI Reference** window, click the **Browse Project** button in the Open VI section.

d. In the **Select VI** window that opens, expand the tree view for your device, select the VI under your device and click **OK**.

e. Click **OK** in the **Configure Open FPGA VI Reference** window.

f. Save the VI.

6. On the front panel, select appropriate values in the **Num Samples**, **Generation Mode**, **Generation Constant**, and **DDC A Voltage Level** controls.

7. Click the **Run** button to run the VI. The NI 6583R generates a waveform on the even channels of your device and then acquires that waveform on the odd channels of your device. The front panel of the host VI displays both the generated and acquired waveforms, as shown in Figure 13. Use the **DDC A** and **DDC B** tabs on the left side of the front panel to toggle between connectors. If the generated and acquired waveforms match, then the **DDC *x* Verified?** indicator illuminates.

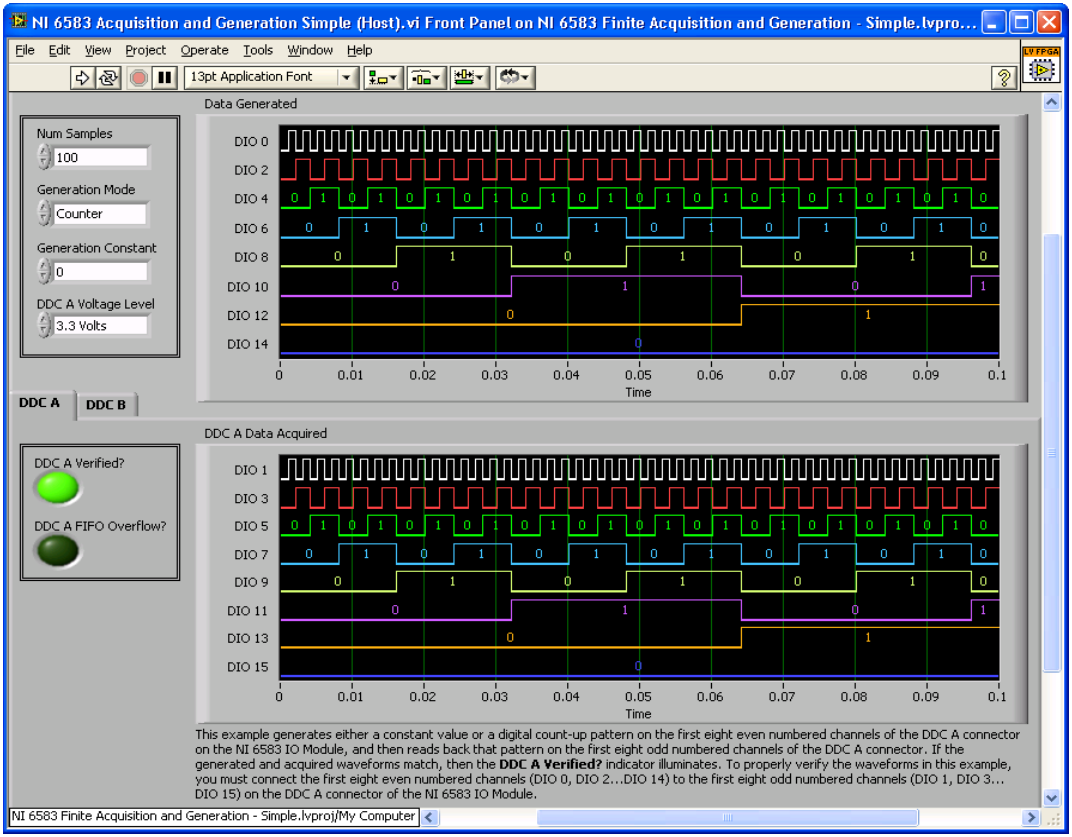


Figure 13. NI 6583 Acquisition and Generation Simple (Host) VI Front Panel

8. Close the VI.

Creating a LabVIEW Project and Running a VI on an FPGA Target

This section demonstrates how to create a LabVIEW project, an FPGA VI, and a host VI that acquires and generates single-ended data on the NI 6583R. This exercise also demonstrates how to compile the FPGA VI on your target and run a VI on the host machine.

Note Disconnect all signals from the NI 6583R connectors before running this VI.

Creating a Project

1. Launch LabVIEW, or if LabVIEW is already running, select **File»New**.
2. In the **New** dialog box, select **Project»Empty Project**. Click **OK**. The new project opens in the **Project Explorer** window.
3. Save the project as `Static RW with Voltage.lvproj`.

Creating an FPGA Target VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»Targets and Devices**.
2. In the **Add Targets and Devices on My Computer** window, select the **Existing Target or Device** button and expand the FPGA Target. The target is displayed.
3. Select your device and click **OK**. The target and target properties are loaded into the project tree.
4. In the **Project Explorer** window, right-click the FPGA target and select **New»VI**. A blank VI opens.
5. Select **Window»Show Block Diagram** to open the block diagram window.
6. In the **Project Explorer** window, select **FPGA Target (RIO*x*, PXI-79*xx*R)**.
7. Right-click **IO Module** and select **Properties**. In the General category, select **National Instruments: NI 6583**, and you can see the available component-level IP (CLIP) for the NI 6583 in the Component Level IP pane. If the category information is dimmed, select the **Enable IO Module** checkbox.

Note For more information about CLIP items for the NI 6583, refer to the *NI 6583 Component-Level Intellectual Property (CLIP)* section of this document.

8. Select **NI 6583 Basic Connector** to use the connector-based CLIP. Click **OK**.
9. In the **Project Explorer** window, expand the **IO Module (NI 6583 : NI 6583 Basic Connector)** tree view.
10. Select **SE_Data_Dir**, **SE_Data_Rd**, **SE_Data_Wr**, **Voltage_Family**, **Set_Voltage_Family**, and **Set_Voltage_Done**, and drag them onto the block diagram.

Tip If you hold down the <Ctrl> key, you can select multiple options at one time.

11. Add a While Loop around all six data nodes, as shown in Figure 14.
12. Wire a False constant to the stop condition of the While Loop.
13. Wire indicators from the output terminals of the **IO Module\SE_Data_Rd** and **IO Module\Set_Voltage_Done** nodes.
14. Wire controls from the input terminals of the **IO Module\Set_Voltage_Family**, **IO Module\SE_Data_Dir**, and **IO Module\SE_Data_Wr** nodes.
15. On the Functions palette, choose **Select a VI**.
16. In the **Select the VI to Open** window, navigate to `Program Files\National Instruments\<LabVIEW x>\examples\FlexRIO\IO Modules\NI 6583\FiniteAcqGenSimple`.

17. Select **NI 6583 Voltage Level**. Click **OK** to drag and place the file on your block diagram.
18. Right-click the Voltage Level control and select **Change to Control**.
19. Wire the Voltage Level control to the **IO Module\Voltage_Family** node, as shown in Figure 14.
20. Add a case structure around the **IO Module\SE_Data_Dir**, **IO Module\SE_Data_Rd**, and **IO Module\SE_Data_Wr** nodes driven by **IO Module\Set_Voltage_Done** to prevent input and output access while the voltage is changing.

    Your block diagram should now resemble the block diagram in Figure 14.

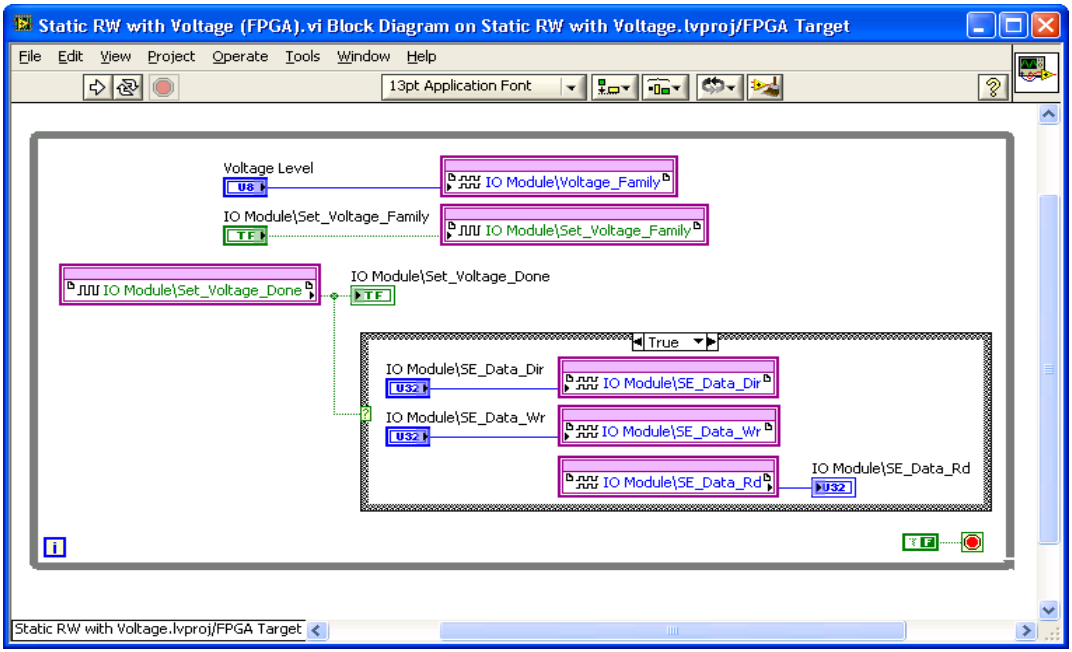


Figure 14. Static RW with Voltage (FPGA).vi Block Diagram

21. Save the VI as `Static RW with Voltage (FPGA).vi`.
22. Close the VI.
23. In the Project Explorer window under **My Computer**, expand the tree view for your device, right-click the **Static RW with Voltage (FPGA).vi** and select **Compile** to compile the files for your target.

    The **Generating Intermediate Files** window opens and displays the compilation progress. The **LabVIEW FPGA Compile Server** window opens and runs. The compilation takes several minutes.
24. When the compilation finishes, click the **Stop Server** button.
25. Click **OK** in the **Successful Compile Report** window. Close the VI without saving changes.

Creating a Host VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»VI**. A blank VI opens.
2. Select **Window»Show Block Diagram** to open the block diagram window.
3. Place the Open FPGA VI Reference function (from the FPGA Interface palette) on the block diagram.
4. Right-click the Open FPGA VI Reference function and select **Configure Open FPGA VI Reference**.
5. In the **Configure Open FPGA VI Reference** window, select the **VI** button.
6. In the **Select VI** window that opens, select the **Static RW with Voltage (FPGA).vi** under your device, and click **OK**.
7. Select the **Run the FPGA VI** checkbox if it is not already selected.
8. Click **OK** in the **Configure Open FPGA VI Reference** window. The new target name appears under the Open FPGA VI Reference function on the block diagram.
9. Add a While Loop to the block diagram, as shown in Figure 15.
10. Add the Read/Write Control function (from the FPGA Interface palette) inside the While Loop.
11. Wire the Open FPGA VI Reference function **FPGA VI Reference Out** indicator to the **FPGA VI Reference In** control on the Read/Write Control function.
12. Wire the Open FPGA VI Reference function **error out** indicator to the Read/Write Control function **error in** control.
13. Click the **Unselected** input of Read/Write Control function and select **Voltage Level**.
14. Wire a control to the **Voltage Level** FPGA input terminal.
15. Expand the bottom of the Read/Write Control function to expose five more nodes. Click the new nodes and select each of the remaining items.
16. Wire indicators from the **IO Module\SE_Data_Rd** and **IO Module\Set_Voltage_Done** output terminals.
17. Wire controls to the **IO Module\SE_Data_Dir**, **IO Module\SE_Data_Wr**, and **IO Module\Set_Voltage_Family** input terminals.
18. Add the Close FPGA VI Reference function (from the FPGA Interface palette) outside the While Loop.
19. Wire the Read/Write Control function **FPGA VI Reference Out** indicator to the Close FPGA VI Reference function **FPGA VI Reference In** control.
20. Wire the Read/Write Control **error out** parameter to the Close FPGA VI Reference **error in** parameter.

21. Right-click the stop condition of the While Loop and add an control. Label this control `Stop`. Your block diagram should now resemble the block diagram in Figure 15.

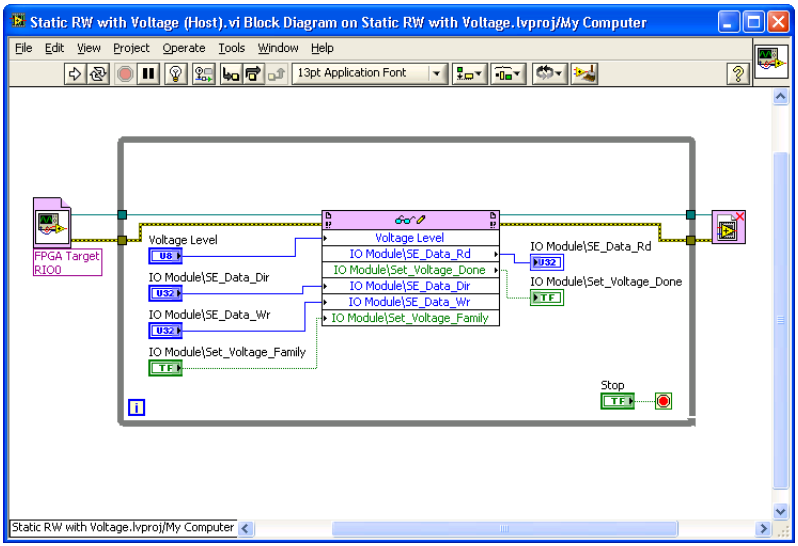


Figure 15. Data RW (Host).vi Block Diagram

22. Save the VI as `Static RW with Voltage (Host).vi`.

Running the Host VI

1. Select **Window»Show Front Panel** to open the front panel of the VI.
2. Click the **Run** button to run the VI.
3. Enter a number in the **IO Module\SE_Data_Dir** control to set the direction of the channels. A logic 0 indicates that the channel is an input, and a logic 1 indicates that the channel is an output. Each of the 32 bits corresponds directly with each of the 32 channels. Bit 0 corresponds with channel 0, and so on.
4. Connect an output channel to an input channel or to a digital multimeter (DMM).
5. Change the logic state of the output channel and ensure that the corresponding logic state on an input channel or on the DMM also changes.
6. Change the voltage on the output channel using the **IO Module\Voltage_Level** control and ensure that the voltage changes on the corresponding input channel or the DMM. Use Table 6 to set the **IO Module\Voltage_Level** control to the desired I/O voltage.
7. Click the **Stop** button on the front panel and close the VI.

Table 6. IO Module\Set Voltage Control

IO Module\Set Voltage Control	I/O Voltage
0	1.2 V
1	1.5 V
2	1.8 V
3	2.5 V
4	3.3 V

The LabVIEW FPGA Module includes a feature for HDL IP integration called CLIP. NI FlexRIO devices support two types of CLIP: user-defined and socketed.

- *User-defined CLIP* allows users to insert HDL IP into an FPGA target, enabling VHDL code to communicate directly with an FPGA VI.
- *Socketed CLIP* provides the same IP integration functionality of the user-defined CLIP, but also allows the CLIP to communicate directly with circuitry external to the FPGA. Adapter module socketed CLIP allows your IP to communicate directly with both the FPGA VI and the external adapter module connector interface.

Figure 16 shows the relationship between an FPGA VI and CLIP.

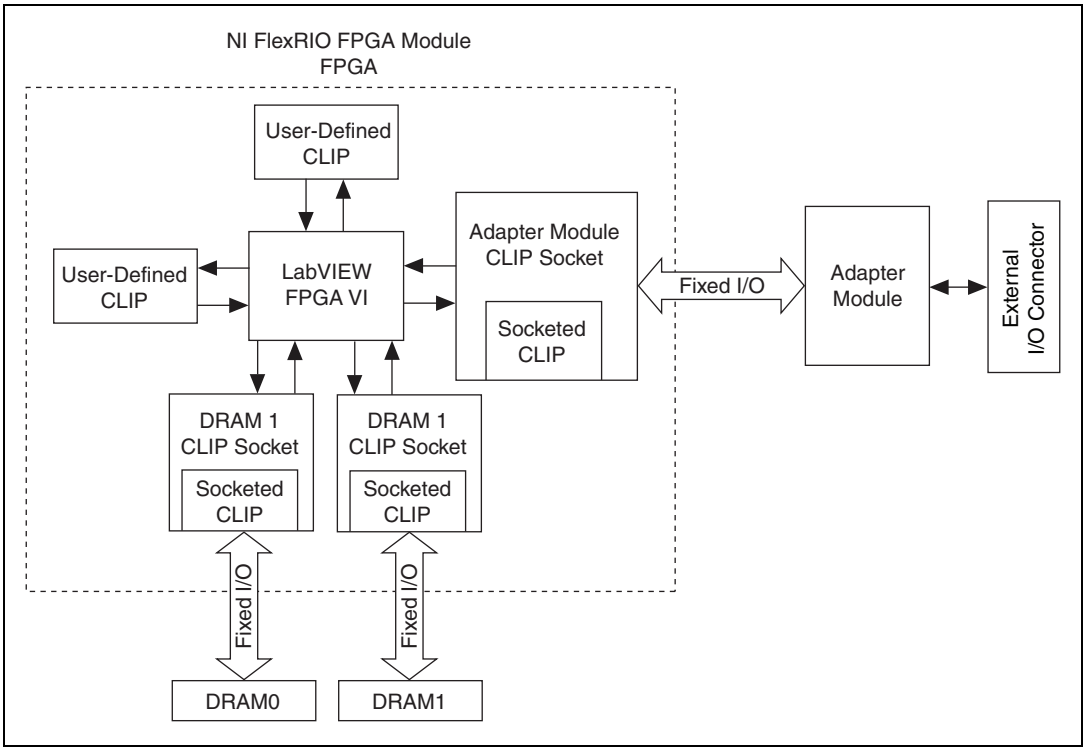


Figure 16. CLIP and FPGA VI Relationship

The NI 6583 ships with socketed CLIP options that you can use to add module I/O to the LabVIEW project. The NI 6583 has the following compatible CLIP options:

- **NI 6583 Basic Channel CLIP**—Provides read/write access to all single-ended lines on DDC A and all differential lines on DDC B using a simple channel-based interface. Each I/O line has a direction control signal. This CLIP provides a clock signal for export on each connector. The clock input data from the NI 6583 is passed to LabVIEW FPGA for use in the FPGA VI. This CLIP also allows for individual clock output inversion.
- **NI 6583 Basic Connector CLIP**—Provides read/write access to all single-ended lines on DDC A and all differential lines on DDC B. The individual data lines for DDC A are accessed using a U32 data type and the individual data lines on DDC B are accessed using a U16 data type in LabVIEW FPGA. Each I/O line has a direction signal. This CLIP also allows for individual clock output inversion.
- **NI 6583 DDR Connector CLIP**—Provides read/write access to all single-ended lines on DDC A and all differential lines on DDC B. The individual data lines for DDC A are accessed using a U32 data type and the individual data lines on DDC B are accessed using a U16 data type in LabVIEW FPGA. Data from each edge of the clock is presented as “rising” and “falling.” Each I/O line has a direction control signal. This CLIP also allows for individual clock output inversion.

Caution All CLIP options include intellectual property for voltage and direction control. The voltage is controlled with a 10-bit DAC code or with an enumerated data type. You must use this intellectual property to prevent damage to your NI 6583 and to your system.

Refer to the *NI FlexRIO Help* for more information about NI FlexRIO CLIP items, configuring the NI 6583 with a socketed CLIP, and a list of available socketed CLIP signals.

Specifications

This section lists the specifications of the NI FlexRIO adapter module (NI 6583). Pair these specifications with the specifications listed in the *NI FlexRIO FPGA Module Installation Guide and Specifications*. For more information about safety and electromagnetic compatibility, refer to the *Read Me First: Safety and Electromagnetic Compatibility* document included in your hardware kit or available at `ni.com/manuals`.

These specifications are nominal at 25 °C unless otherwise noted.

Channel Specifications

Number of connectors.....One VHDCI (DDC A for single-ended I/O)
One InfiniBand (DDC B for differential I/O)

Number of digital I/O channels .....35 total on DDC A
(32 single-ended data, 3 single-ended PFI);
19 total on DDC B
(16 differential data, 3 differential PFI)

Direction control of digital I/O channels .....Per channel

Minimum required direction change latency .....9 ns, for single-ended signals only

Number of clock input terminals .....2, STROBE on DDC A and STROBE on DDC B

Number of clock output terminals .....2, CLK OUT on DDC A and CLK OUT on DDC B

Single-ended Channels (DDC A)

(Consistent with TI part number SN74AVC2T245)

Number of programmable I/O voltage levels .....1 V_{CC}

Note The provided CLIP items have the ability to program the voltage level by logic families (1.2V, 1.5V, 1.8V, 2.5V, and 3.3V) or by DAC code (10-bit). The voltage level is shared for single-ended input and output signals.

Voltage range .....1.2 V to 3.3 V

Resolution .....10-bit, nominal

Gain.....–2.69 mV / DAC code, nominal

Offset.....3.63 V, nominal

Power up state .....Drivers disabled, 50 kΩ impedance to ground,
V_{CC} = 3.63 V

Note You must set the voltage after every power cycle prior to performing any operations.

Typical data rate

1.8 V, 2.5 V, 3.3 V.....300 Mb/s

1.5 V.....280 Mb/s

1.2 V.....240 Mb/s

Generation (Data, Clock, and PFI Channels)

Table 7. Generation Voltage Levels (100 µA load)

Generation Voltage Levels	Low Voltage Levels		High Voltage Levels	
	Characteristic	Maximum	Minimum	Characteristic
V_{CC} 1.2 V to 3.3 V	0 V	200 mV	V_{CC} – 200 mV	V_{CC}

Output impedance.....50 Ω, nominal

Maximum per channel DC drive strength

V_{CC} 1.2 V.....±6 mA
V_{CC} 1.4 V to 1.6 V.....±12 mA
V_{CC} 1.65 V to 1.95 V.....±16 mA
V_{CC} 2.3 V to 3.3 V.....±18 mA

Output protection.....Single-ended I/O can indefinitely sustain a short to any voltage between –0.5 V and V_{CC} + 0.5 V with a current not exceeding 30 mA.

Acquisition (Data, STROBE, and PFI Channels)

Table 8. Acquisition Voltage Threshold

Acquisition Voltage Levels	Low Voltage Threshold	High Voltage Threshold
	Minimum	Maximum
V_{CC} 1.2 V to 1.95 V	$0.35 \times V_{CC}$	$0.65 \times V_{CC}$
V_{CC} 1.95 V to 2.7 V	0.7 V	1.6 V
V_{CC} 2.7 V to 3.3 V	0.8 V	2.0 V

Input impedance.....50 kΩ, nominal

Input protection.....–0.5 V to 4.6 V

Note Internal diode clamps may begin conducting outside the 0 V to V_{CC} range.

LVDS Channels (DDC B)

(Consistent with TI part number SN65LVDM180)

Number of programmable I/O voltage levels .....None

Power-up state.....Drivers disabled, 100 Ω differential impedance with 300 kΩ to 3.3 V

Typical data rate.....300 Mb/s

Generation (Data, Clock, and PFI Channels)

Table 9. Generation Voltage Levels (50 Ω total load)

Offset Voltage			Differential Voltage		
Minimum	**Typical**	**Maximum**	**Minimum**	**Typical**	**Maximum**
1.125 V	1.2 V	1.375 V	247 mV	340 mV	454 mV

Output impedance ..... 100 Ω differential, nominal

Output protection ..... Each channel can indefinitely sustain a short to any voltage between –0.5 V and 4.0 V.

Note Internal diode clamps may begin conducting outside the 0 V to 3.3 V range.

Acquisition (Data, STROBE, and PFI Channels)

Table 10. Acquisition Voltage Levels

Voltage Threshold	Voltage Range	
Maximum	**Minimum**	**Maximum**
±50 mV	0 V	2.4 V

Input impedance ..... 100 Ω differential, nominal

Input protection ..... Each channel can indefinitely sustain a short to any voltage between –0.5 V and 4.0 V.

Note Internal diode clamps may begin conducting outside the 0 V to 3.3 V range.

MLVDS Channels (DDC B)

(Consistent with TI part number SN65MLVD207)

Number of programmable I/O voltage levels ..... None

Power up state ..... Drivers disabled, 100 Ω differential impedance

Fault protection ..... Type 2

Typical data rate ..... 200 Mb/s

Generation (Data, Clock, and PFI Channels)

Table 11. Generation Voltage Levels (50 Ω total load)

Offset Voltage		Differential Voltage	
Minimum	**Maximum**	**Minimum**	**Maximum**
0.8 V	1.2 V	480 mV	650 mV

Output impedance ..... 100 Ω differential, nominal

Output protection ..... Each channel can indefinitely sustain a short to any voltage between –1.4 V and 3.8 V.

Acquisition (Data, STROBE, and PFI Channels)

Magnitude of differential input voltage .....0.05 V to 3.3 V

Positive-going differential threshold.....150 mV

Negative-going differential threshold .....50 mV

Input impedance.....100 Ω differential, nominal

Input range .....–1.4 V to +3.8 V.

Power

Maximum power requirements when toggling half of the data channels at 100% data rate and half at 50% data rate. +12 V is maximized when generating, and +3.3 V is maximized when acquiring.

+12 V .....215 mA, 2.6 W

+3.3 V .....850 mA, 2.8 W

V_{ccoB}.....275 mA, 690 mW

Physical

Dimensions .....12.9 × 2.0 × 12.1 cm (5.1 × 0.8 × 4.7 in.)

Weight.....284 g (10 oz)

Front panel connectors.....One 68-pin VHDCI connector, and one 73-pin InfiniBand connector

Environmental

The NI 6583 is intended for indoor use only.

Operating environment .....0 °C to 55 °C.
Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.

Relative humidity range.....10% to 90%, noncondensing.
Tested in accordance with IEC 60068-2-56.

Altitude .....2,000 m at 25 °C ambient temperature

Pollution Degree 2

Storage environment

- Ambient temperature range .....–20 °C to 70 °C.
  Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.
- Relative humidity range.....5% to 95%, noncondensing.
  Tested in accordance with IEC 60068-2-56.

Note Clean the device with a soft, non-metallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Glossary

Maximum and *minimum* specifications are warranted not to exceed these values within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

Typical specifications are unwarranted values that are representative of a majority (3σ) of units within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

Characteristic specifications are unwarranted values that are representative of an average unit operating at room temperature.

Nominal specifications are unwarranted values that are relevant to the use of the product and convey the expected performance of the product.

Compliance and Certifications

Safety

This product meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note For the standards applied to assess the EMC of this product, refer to the *Online Product Certification* section.

Note For EMC compliance, operate this device according to the device documentation and only with the NI SHC68-C68-D4 (1 m) shielded cable, the NI SHB12X-B12X (1 m) shielded cable, and shielded accessories.

Caution To ensure the specified EMC performance, when using the MLVDS version of the NI 6583, you must attach EMI gaskets (NI part number 746228-01) to both sides of your NI 6583 before use.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)



EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit `ni.com/environment/weee`.

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Where to Go for Support

The National Instruments Web site is your complete resource for technical support. At `ni.com/support` you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from NI Application Engineers.

National Instruments corporate headquarters is located at 11500 North Mopac Expressway, Austin, Texas, 78759-3504. National Instruments also has offices located around the world to help address your support needs. For telephone support in the United States, create your service request at `ni.com/support` and follow the calling instructions or dial 512 795 8248. For telephone support outside the United States, visit the Worldwide Offices section of `ni.com/niglobal` to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

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