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Technical Sales
United States
(866) 531-6285
info@ni.com

Requirements and Compatibility | Ordering Information | Detailed Specifications
For user manuals and dimensional drawings, visit the product page resources tab on ni.com.

Last Revised: 2010-04-07 11:50:44.0

NI PXI-6541, NI PCI-6541, NI PXI-6542, NI PCI-6542





- 100 MHz maximum clock rate
- Compatible with 5.0, 3.3, 2.5, and 1.8 V (software-selectable)
- 32 channels with per-channel direction control
- Interactive waveform and script editor software
- NI Synchronization and Memory Core (SMC) device
- 1, 8, or 64 Mbit/channel onboard memory

Overview

NI 6542 and NI 6541 devices are 100 and 50 MHz digital waveform generator/analyzers, respectively, for interfacing to digital electronics. These modules feature 32 channels with per-channel direction control and deep onboard memory with triggering and pattern sequencing. Through the NI-HSDIO driver, you can interface with 5.0, 3.3, 2.5, or 1.8 V logic. You can also use these devices with the NI Digital Waveform Editor, an interactive software tool for creating and editing digital waveforms. With the SMC, you can create mixed-signal test systems with digitizers, arbitrary waveform generators, and other digital waveform generator/analyzers, or you can synchronize multiple digital devices to build low-skew multichannel systems for interfacing to high-pin-count digital ICs and electronics.

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Requirements and Compatibility

OS Information

- Windows Vista x64/x86
- Windows 7
- Windows 7 64 bit
- Windows XP x64
- Windows XP

Driver Information

- NI-HSDIO

Software Compatibility

- ANSI C/C++
- LabVIEW
- Measurement Studio
- Visual C#
- LabVIEW Base Development System

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Application and Technology

Design High-Performance Tests

NI 6541 and NI 6542 devices are ideal instruments for low-cost digital test because of features such as the following:

- Data delay at or above 25 MHz with a data delay resolution of 0.4 percent of the clock period
- Internal or external sample or reference clock sources
- ±600 ps channel-to-channel skew
- Multidevice synchronization for channel expansion or for tight synchronization with other SMC-based modular instruments

Create Digital Waveforms Interactively with the NI Digital Waveform Editor

With the NI Digital Waveform Editor, an interactive software tool for creating and editing digital waveforms, you can import existing test patterns from popular spreadsheet and VHDL simulation packages in ASCII or value change dump (VCD) formats. Once imported, you can view the waveforms graphically and edit them interactively for new devices or new test conditions. You can also build new waveforms with built-in fill patterns such as pseudorandom bit sequences (PRBS) and count up/down patterns. When ready to test

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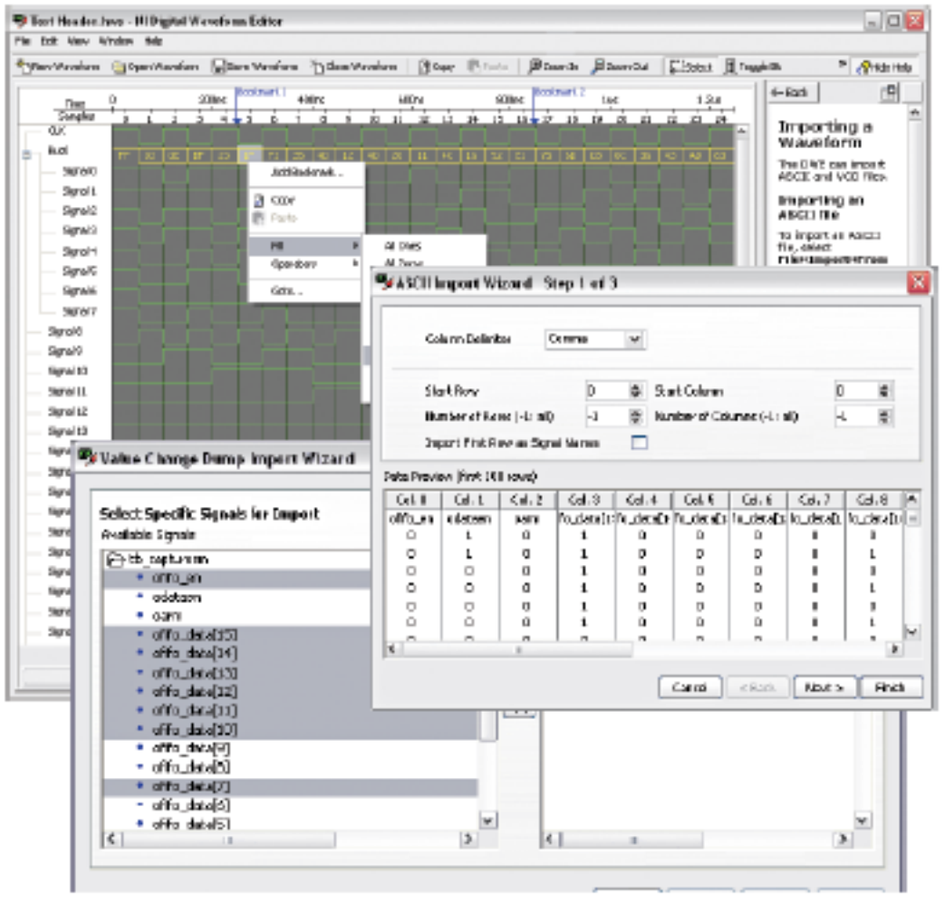
your device, the waveforms import seamlessly into NI LabVIEW, LabVIEW SignalExpress, and C. The Digital Waveform Editor is included with the 8 and 64 Mbit/channel memory models, and is a separate add-on for use with the 1 Mbit/channel model.

Build Tightly Synchronized Mixed-Signal Test Systems

NI 655x devices use the same SMC architecture as the NI 5122 high-resolution digitizers and NI 5441 arbitrary waveform generators, so you can combine these devices to build tightly synchronized mixed-signal prototyping and test systems. For tight timing requirements, these PXI modules phase-lock to the 10 MHz reference clock on the PXI backplane. If you have an external precision reference, you can import it through the front panel SMB connector.

Driver Software

NI 655x devices include the NI-HSDIO driver with an intuitive, powerful API based on IVI guidelines. The Windows-compatible NI-HSDIO driver provides an API for NI LabVIEW, LabVIEW SignalExpress, and LabWindows™/CVI, as well as other text-based development environments.



Digital Waveform Editor with ASCII and VCD Import Wizards

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Ordering Information

For a complete list of accessories, visit the product page on ni.com.

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Products	Part Number	Recommended Accessories	Part Number
NI PCI-6541			
NI PCI-6541-32MBIT/PIN Each NI PCI-6541-32MBIT/PIN requires: 1 Cable, 1 Connector Block	778988-03	**Cable:** Shielded - SHC68-C68-D4 Cable (1m) ***Also available: Unshielded* **Connector Block:** High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	196275-01 778592-01
NI PCI-6541			
NI PCI-6541- 1 Mb/ch Each NI PCI-6541- 1 Mb/ch requires: 1 Cable, 1 Connector Block	778988-01	**Cable:** Shielded - SHC68-C68-D4 Cable (1m) ***Also available: Unshielded* **Connector Block:** High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	196275-01 778592-01
NI PCI-6541			
NI PCI-6541- 8 Mb/ch Each NI PCI-6541- 8 Mb/ch requires: 1 Cable, 1 Connector Block	778988-02	**Cable:** Shielded - SHC68-C68-D4 Cable (1m) ***Also available: Unshielded* **Connector Block:** High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	196275-01 778592-01
NI PCI-6542			
NI PCI-6542- 1 Mb/ch Each NI PCI-6542- 1 Mb/ch requires: 1 Cable, 1 Connector Block	778989-01	**Cable:** Shielded - SHC68-C68-D4 Cable (1m) ***Also available: Unshielded* **Connector Block:** High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	196275-01 778592-01
NI PCI-6542			
NI PCI-6542- 32 Mb/ch Each NI PCI-6542- 32 Mb/ch requires: 1 Cable, 1 Connector Block	778989-03	**Cable:** Shielded - SHC68-C68-D4 Cable (1m) ***Also available: Unshielded* **Connector Block:** High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	196275-01 778592-01
NI PCI-6542			
NI PCI-6542- 8 Mb/ch Each NI PCI-6542- 8 Mb/ch requires: 1 Cable, 1 Connector Block	778989-02	**Cable:** Shielded - SHC68-C68-D4 Cable (1m) ***Also available: Unshielded* **Connector Block:** High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	196275-01 778592-01
NI PXI-6541			

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NI PXI-6541-1 Mb/ch Each NI PXI-6541-1 Mb/ch requires: 1 Cable, 1 Connector Block	778952-01	**Cable:** Shielded - SHC68-C68-D4 Cable (1m) ***Also available: Unshielded* **Connector Block:** High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	196275-01 778592-01
NI PXI-6541			
NI PXI-6541-64 Mb/ch Each NI PXI-6541-64 Mb/ch requires: 1 Cable, 1 Connector Block	778952-03	**Cable:** Shielded - SHC68-C68-D4 Cable (1m) ***Also available: Unshielded* **Connector Block:** High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	196275-01 778592-01
NI PXI-6541			
NI PXI-6541-8 Mb/ch Each NI PXI-6541-8 Mb/ch requires: 1 Cable, 1 Connector Block	778952-02	**Cable:** Shielded - SHC68-C68-D4 Cable (1m) ***Also available: Unshielded* **Connector Block:** High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	196275-01 778592-01
NI PXI-6542			
NI PXI-6542-1 Mb/ch Each NI PXI-6542-1 Mb/ch requires: 1 Cable, 1 Connector Block	778953-01	**Cable:** Shielded - SHC68-C68-D4 Cable (1m) ***Also available: Unshielded* **Connector Block:** High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	196275-01 778592-01
NI PXI-6542-8 Mb/ch Each NI PXI-6542-8 Mb/ch requires: 1 Cable, 1 Connector Block	778953-02	**Cable:** Shielded - SHC68-C68-D4 Cable (1m) ***Also available: Unshielded* **Connector Block:** High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	196275-01 778592-01
NI PXI-6542-64 Mb/ch Each NI PXI-6542-64 Mb/ch requires: 1 Cable, 1 Connector Block	778953-03	**Cable:** Shielded - SHC68-C68-D4 Cable (1m) ***Also available: Unshielded* **Connector Block:** High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	196275-01 778592-01

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Support and Services

System Assurance Programs

NI system assurance programs are designed to make it even easier for you to own an NI system. These programs include configuration and deployment services for your NI PXI, CompactRIO, or Compact FieldPoint system. The NI Basic System Assurance Program provides a simple integration test and ensures that your system is delivered completely assembled in one box. When you configure your system with the NI Standard System Assurance Program, you can select from available NI system driver sets and application development environments to create customized, reorderable software configurations. Your system arrives fully assembled and tested in one box with your software preinstalled. When you order your system with the standard program, you also receive system-specific documentation including a bill of materials, an integration test report, a recommended maintenance plan, and frequently asked question documents. Finally, the standard program reduces the total cost of owning an NI system by providing three years of warranty coverage and calibration service. Use the online product advisors at ni.com/advisor to find a system assurance program to meet your needs.

Technical Support

Get answers to your technical questions using the following National Instruments resources.

- **Support** - Visit ni.com/support to access the NI KnowledgeBase, example programs, and tutorials or to contact our applications engineers who are located in NI sales offices around the world and speak the local language.
- **Discussion Forums** - Visit forums.ni.com for a diverse set of discussion boards on topics you care about.
- **Online Community** - Visit community.ni.com to find, contribute, or collaborate on customer-contributed technical content with users like you.

Repair

While you may never need your hardware repaired, NI understands that unexpected events may lead to necessary repairs. NI offers repair services performed by highly trained technicians who quickly return your device with the guarantee that it will perform to factory specifications. For more information, visit ni.com/repair.

Training and Certifications

The NI training and certification program delivers the fastest, most certain route to increased proficiency and productivity using NI software and hardware. Training builds the skills to more efficiently develop robust, maintainable applications, while certification validates your knowledge and ability.

- **Classroom training in cities worldwide** - the most comprehensive hands-on training taught by engineers.
- **On-site training at your facility** - an excellent option to train multiple employees at the same time.
- **Online instructor-led training** - lower-cost, remote training if classroom or on-site courses are not possible.
- **Course kits** - lowest-cost, self-paced training that you can use as reference guides.
- **Training memberships** and training credits - to buy now and schedule training later.

Visit ni.com/training for more information.

Extended Warranty

NI offers options for extending the standard product warranty to meet the life-cycle requirements of your project. In addition, because NI understands that your requirements may change, the extended warranty is flexible in length and easily renewed. For more information, visit ni.com/warranty.

OEM

NI offers design-in consulting and product integration assistance if you need NI products for OEM applications. For information about special pricing and services for OEM customers, visit ni.com/oem.

Alliance

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Detailed Specifications

This document provides the specifications for the NI PXI/PCI-6541 (NI 6541) and the NI PXI/PCI-6542 (NI 6542).

Typical values are representative of an average unit operating at room temperature. Specifications are subject to change without notice. For the most recent NI 6541/6542 specifications, visit NI.com/manuals .

To access the NI 6541/6542 documentation, including the
NI Digital Waveform Generator/Analyzer Getting Started Guide
, which contains functional descriptions of the NI 6541/6542 signals, navigate to **Start » Programs » National Instruments » NI-HSDIO » Documentation**.

Hot Surface Allow time to cool before extracting an NI 654*X* PXI module from the PXI chassis to reduce risk of burns. Exercise caution when handling, as recently used NI 654*X* modules may exceed safe handling temperatures.

Channel Specifications

Specification	Value	Comments
Number of data channels	32	—
Direction control of data channels	Per channel	—
Number of Programmable Function Interface (PFI) channels	4	Refer to the Waveform Specifications section for more details.
Direction control of PFI channels	Per channel	—
Number of clock terminals	3 input 2 output	Refer to the Timing Specifications section for more details.

Generation Channels (Data, DDC CLK OUT, and PFI <0..3>)

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Specification	Value				Comments
Generation voltage families	1.8 V, 2.5 V, 3.3 V TTL (5 V TTL compatible)				Into 1 MΩ
Generation signal type	Single-ended				—
Generation voltage levels	**Low Voltage Levels**		**High Voltage Levels**		—
	Typical	**Maximum**	**Minimum**	**Typical**	
1.8 V	0 V	0.1 V	1.7 V	1.8 V	I = 100 µA
2.5 V	0 V	0.1 V	2.4 V	2.5 V	
3.3 V	0 V	0.1 V	3.2 V	3.3 V	
5.0 V	0 V	0.1 V	3.2 V	3.3 V	
Output impedance	50 Ω nominal				—
Maximum DC drive strength	±8 mA at 1.8 V ±16 mA at 2.5 V ±32 mA at 3.3 V				—
Data channel driver enable/disable control	Per channel				Software-selectable
Channel power-up state	Drivers disabled, 10 kΩ input impedance				—
Output protection	The device can indefinitely sustain a short to any voltage between 0 V and 5 V.				—

Acquisition Channels (Data, STROBE, and PFI <0..3>)

Specification	Value		Comments
Acquisition voltage families	1.8 V, 2.5 V, 3.3 V TTL (5 V TTL compatible)		—
Acquisition voltage levels	**Low Voltage Threshold**	**High Voltage Threshold**	—
	Maximum	**Minimum**	
1.8 V	0.45 V	1.35 V	—
2.5 V	0.75 V	1.75 V	—
3.3 V	1.00 V	2.30 V	—
5.0 V	1.00 V	2.30 V	—
Input impedance	High-impedance (10 kΩ)		—
Input protection	–1 V to 6 V		Diode clamps in the design may provide additional protection outside this range.

Timing Specifications

Sample Clock

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Specification	Value		Comments
Sample clock sources	1. On Board Clock (internal voltage-controlled crystal oscillator (VCXO) with divider) 2. CLK IN (SMB jack connector) 3. PXI_STAR (PXI backplane—PXI only) 4. STROBE (Digital Data & Control (DDC) connector; acquisition only)		—
On Board Clock frequency range	**NI 6541:** 48 Hz to 50 MHz Configurable to 200 MHz / *N*; 4 ≤ *N* ≤ 4,194,304 **NI 6542:** 48 Hz to 100 MHz Configurable to 200 MHz / *N*; 2 ≤ *N* ≤ 4,194,304		—
CLK IN frequency range	**NI 6541:** 20 kHz to 50 MHz **NI 6542:** 20 kHz to 100 MHz		Refer to the CLK IN (SMB Jack Connector) section for restrictions based on waveform type.
PXI_STAR frequency range (PXI only)	**NI 6541:** 48 Hz to 50 MHz **NI 6542**: 48 Hz to 100 MHz		Refer to the PXI_STAR (PXI Backplane) section.
STROBE frequency range	**NI 6541:** 48 Hz to 50 MHz **NI 6542:** 48 Hz to 100 MHz		Refer to the STROBE (DDC Connector) section.
Sample clock relative delay adjustment range	0 to 1 Sample clock period		You can apply a delay or phase adjustment to the On Board Clock to align multiple devices.
Sample clock relative delay adjustment resolution	10 ps		
Exported Sample clock destinations	1. DDC CLK OUT (DDC connector) 2. CLK OUT (SMB jack connector)		Sample clocks with sources other than STROBE can be exported.
Exported Sample clock delay range (δ_C)	0 to 1 Sample clock periods		For clock frequencies ≥ 25 MHz
Exported Sample clock delay resolution (δ_C)	1/256 of Sample clock period		For clock frequencies ≥ 25 MHz
Exported Sample clock jitter	**Period Jitter**	**Cycle-to-Cycle Jitter**	Typical; using On Board Clock
	20 ps_{rms}	35 ps_{rms}	

Generation Timing (Data, DDC CLK OUT, and PFI <0..3> Channels)

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Specification	Value	Comments
Data channel-to-channel skew	±600 ps	Typical skew across all data channels
Maximum data channel toggle rate	**NI 6541:** 25 MHz **NI 6542:** 50 MHz	—
Data position modes	Rising edge, Falling edge, or Delayed	Relative to Sample clock
Generation data delay range (δ_G)	0 to 1 Sample clock period	For clock frequencies ≥ 25 MHz
Generation data delay resolution (δ_G)	1/256 of Sample clock period	For clock frequencies ≥ 25 MHz
Exported Sample clock offset (t_{CO})	0 ns or 2.5 ns (default)	Software-selectable
Time delay from Sample clock (internal) to DDC connector (t_{SCDDC})	15 ns	Typical

Generation Provided Setup and Hold Times

Exported Sample Clock Mode and Offset	Voltage Family	Time from Rising Clock Edge to Data Transition (t_{PCO})	Minimum Provided Setup Time (t_{PSU})	Minimum Provided Hold Time (t_{PH})
Noninverted, 2.5 ns	1.8V	2.5 ns typical	t_P – 5.5 ns	0.5 ns
	2.5V		t_P – 4.5 ns	0.9 ns
	3.3V/5.0V		t_P – 4.5 ns	1 ns
Inverted, 0 ns	1.8V	$t_P/2$	$t_P/2$ – 3.5 ns	$t_P/2$ – 1.5ns
	2.5V		$t_P/2$ – 2.5 ns	
	3.3V/5.0V		$t_P/2$ – 2 ns	

To determine the appropriate exported Sample clock mode and offset for your NI 654*X* generation session, compare the setup and hold times from the datasheet of your device under test (DUT) to the values in this table. Select the exported Sample clock mode and offset such that the NI 654*X* provided setup and hold times are greater than the setup and hold times required for the DUT.

Refer to Figure 1 for a diagram illustrating the relationship between the exported Sample clock mode and the provided setup and hold times.

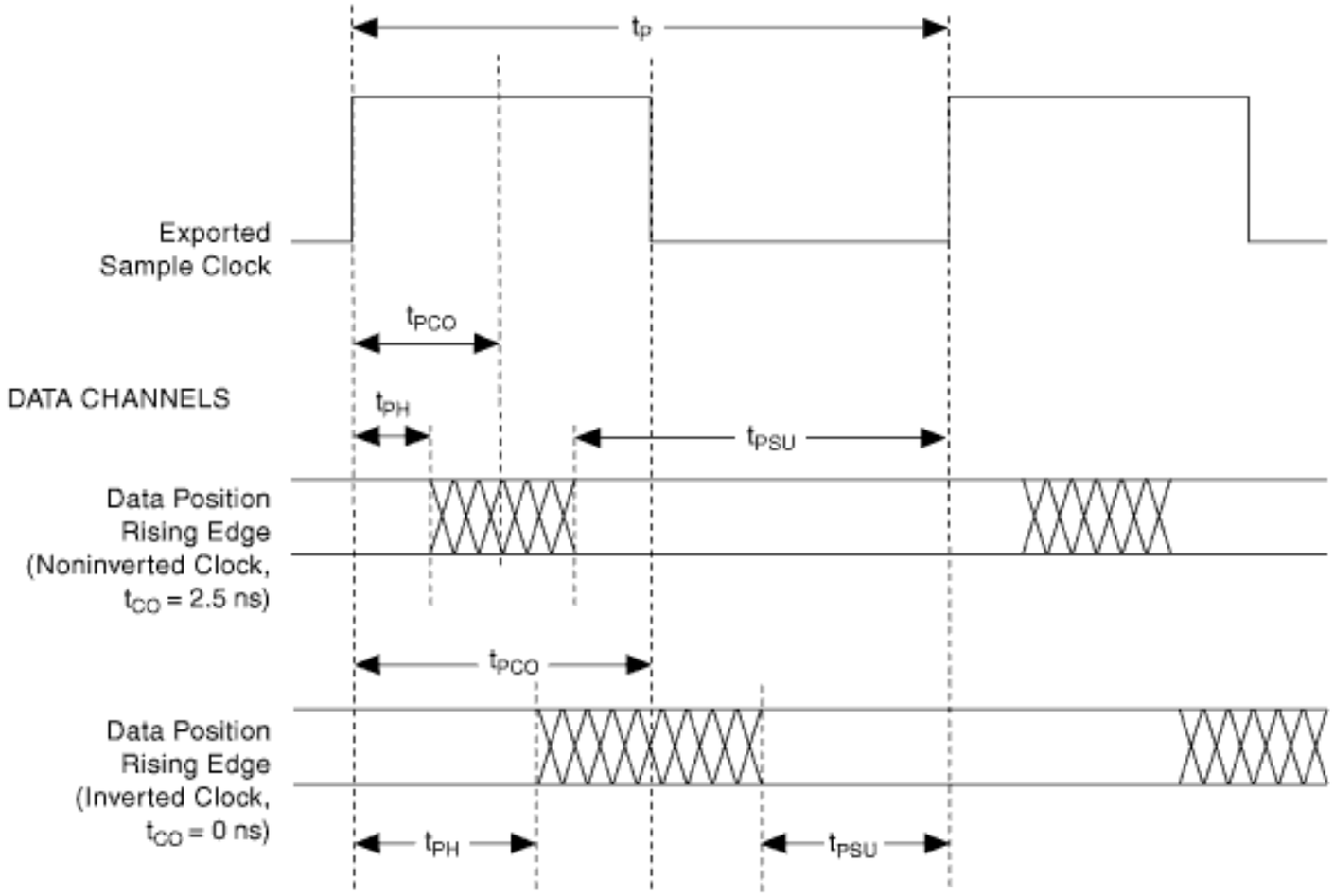
Note This table assumes the Data Position is set to the rising edge of the Sample clock and the Sample clock is exported to the DDC connector.

Note This table includes worst-case effects of channel-to-channel skew, inter-symbol interference, and jitter.

Note Other combinations of exported Sample clock mode and offset are also allowed. The preceding table only presents the values for the default case (noninverted clock with 2.5 ns offset) and the case for providing balanced setup and hold times (inverted clock with 0 ns offset).

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Generation Provided Setup and Hold Times Timing Diagram



$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{PH} = Minimum Provided Hold Time

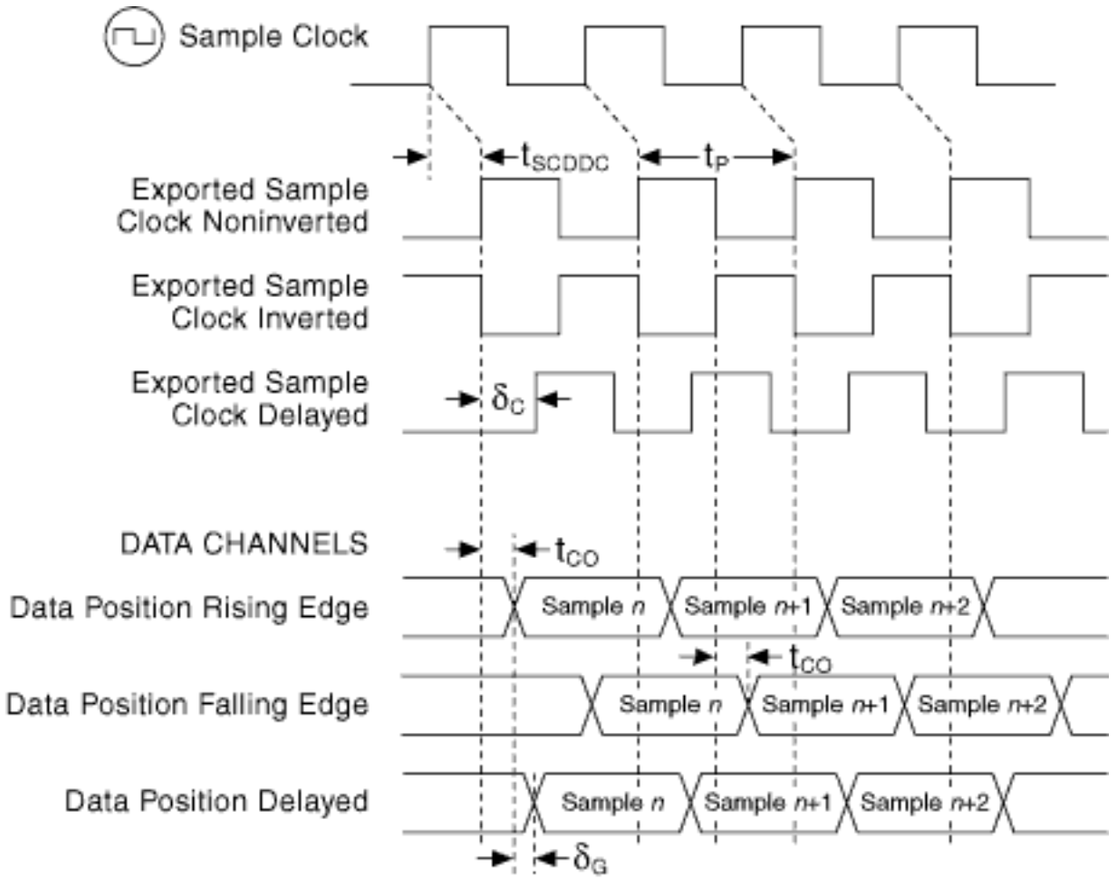
t_{PSU} = Minimum Provided Setup Time

t_{PCO} = Time from Rising Clock Edge to Data Transition (Provided Clock to Out Time)

t_{CO} = Exported Sample Clock Offset

Generation Timing Diagram

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t_{SCDDC} : Time delay from Sample Clock (internal) to DDC Connector

$0 \le \delta_C \le 1$: Exported Sample Clock Delay (fraction of t_P)

$0 \le \delta_G \le 1$: Pattern Generation Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

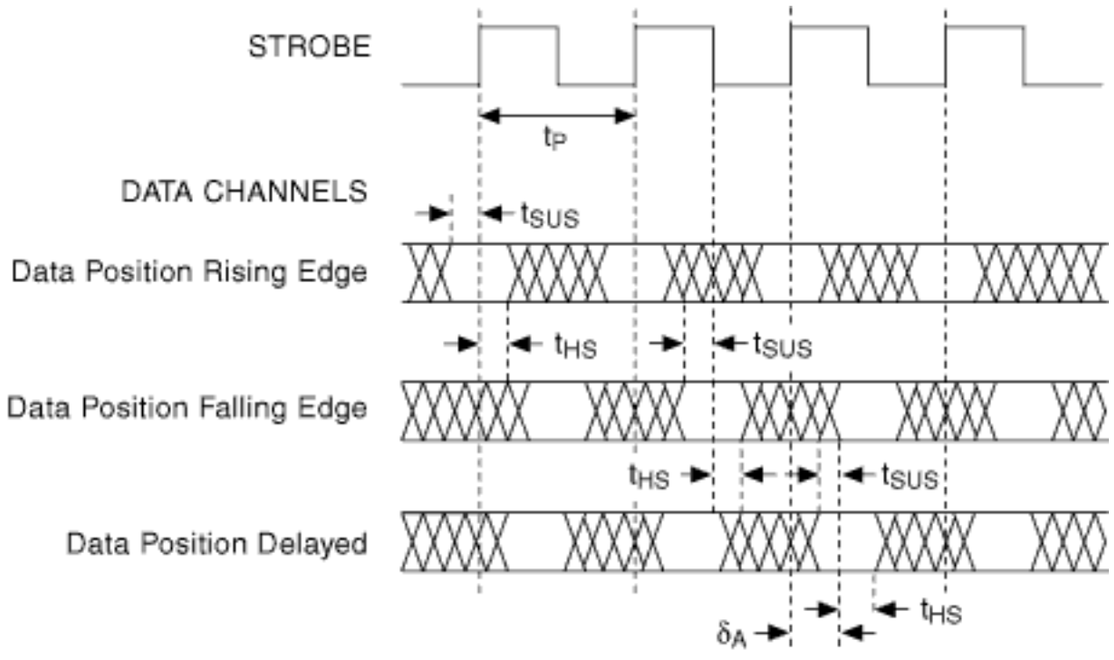
t_{CO} = Exported Sample Clock Offset; 0 or 2.5 ns, software-selectable

Acquisition Timing (Data, STROBE, and PFI <0..3> Channels)

Specification	Value	Comments
Channel-to-channel skew	±600 ps	Typical skew across all data channels
Set-up time to STROBE (t_{SUS})	3.1 ns	Maximum; includes maximum data channel-to-channel skew
Hold time to STROBE (t_{HS})	2.7 ns	Maximum; includes maximum data channel-to-channel skew
Time delay from DDC connector to internal Sample clock (t_{DDCSC})	10 ns	Typical
Set-up time to Sample clock (t_{SUSC})	0.4 ns	Does not include data channel-to-channel skew, t_{DDCSC}, or t_{SCDDC}
Hold time to Sample clock (t_{HSC})	0 ns	Does not include data channel-to-channel skew, t_{DDCSC}, or t_{SCDDC}
Acquisition data delay range (δ_A)	0 to 1 Sample clock periods	For clock frequencies ≥ 25 MHz
Acquisition data delay resolution (δ_A)	1/256 of Sample clock period	For clock frequencies ≥ 25 MHz

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Acquisition Timing Diagram Using STROBE as the Sample Clock



t_{SUS} = Set-up Time to STROBE

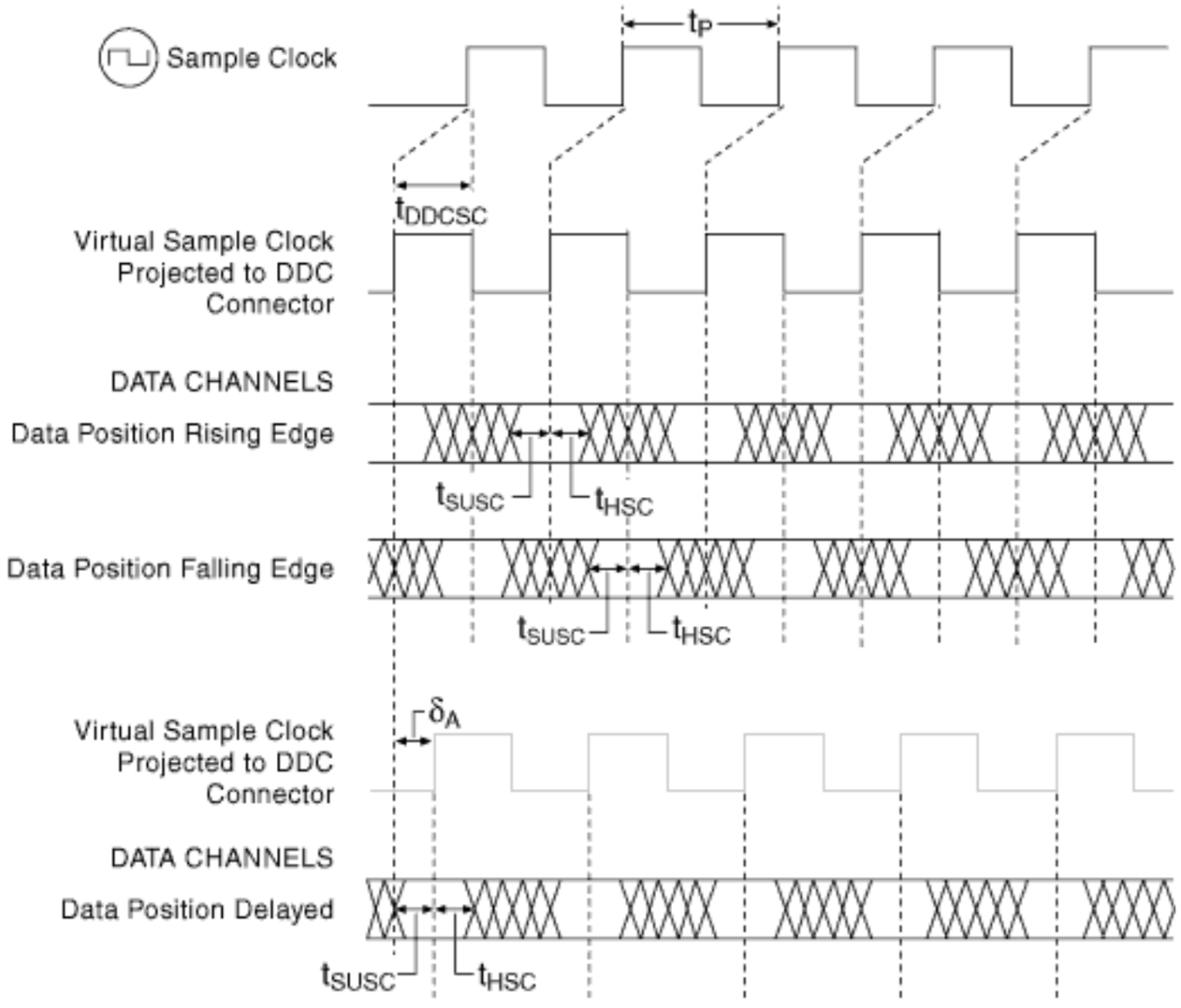
t_{HS} = Hold Time from STROBE

$0 \le \delta_A \le 1$: Pattern Acquisition Data Delay (percentage of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

Acquisition Timing Diagram with Sample Clock Sources Other than STROBE

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t_{DDCSC} : Time Delay from DDC Connector to Internal Sample Clock

$0 \leq \delta_A \leq 1$: Pattern Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{SUSC} = Set-Up Time to Sample Clock

t_{HSC} = Hold Time to Sample Clock

CLK IN (SMB Jack Connector)

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Specification	Value		
Direction	Input into device		
Destinations	1. Reference clock (for the phase lock loop (PLL)) 2. Sample clock		
Input coupling	AC		
Input protection	±10 VDC		
Input impedance	50 Ω (default) or 1 kΩ		
Minimum detectable pulse width	4 ns		
Clock requirements	Clock must be continuous and free-running		
As Sample Clock			
External Sample clock range	**Square Waves**		
	Voltage range	0.65 V_{pp} to 5.0 V_{pp}	
	Frequency range	**NI 6541:** 20 kHz to 50 MHz	
		NI 6542: 20 kHz to 100 MHz	
	Duty cycle range	f < 50 MHz: 25% to 75%, f ≥ 50 MHz: 40% to 60%	
	Sine Waves		
	Voltage range	0.65 V_{pp} to 5.0 V_{pp}	1.0 V_{pp} to 5.0 V_{pp}	2.0 V_{pp} to 5.0 V_{pp}
	Frequency range	**NI 6541:** 5.5 MHz to 50 MHz	**NI 6541:** 3.5 MHz to 50 MHz	**NI 6541:** 1.8 MHz to 50 MHz
		NI 6542: 5.5 MHz to 100 MHz	**NI 6542:** 3.5 MHz to 100 MHz	**NI 6542:** 1.8 MHz to 100 MHz
As Reference Clock			
Reference clock frequency range	10 MHz ±50 ppm		
Reference clock voltage range	0.65 V_{pp} to 5.0 V_{pp}		
Reference clock duty cycle	25% to 75%		

STROBE (DDC Connector)

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Specification	Value	Comments
Direction	Input into device	—
Destinations	Sample clock (acquisition only)	—
STROBE frequency range	**NI 6541:** 48 Hz to 50 MHz **NI 6542:** 48 Hz to 100 MHz	—
STROBE duty cycle range	**NI 6541:** 25% to 75% for clock frequencies <50 MHz **NI 6542:** 40% to 60% for clock frequencies ≥50 MHz 25% to 75% for clock frequencies <50 MHz	At the programmed threshold
Minimum detectable pulse width	4 ns	Required at both acquisition voltage thresholds
Voltage thresholds	Refer to the Acquisition Timing (Data, STROBE, and PFI <0..3> Channels) specifications in the Channel Specifications section.	—
Clock requirements	Clock must be continuous and free-running	—
Input impedance	10 kΩ	—

PXI_STAR (PXI Backplane)

Specification	Value	Comments
Direction	Input into device	—
Destinations	1. Sample clock 2. Start trigger 3. Pause trigger (generation sessions only) 4. Script trigger <0..3> (generation sessions only) 5. Reference trigger (acquisition sessions only)	—
PXI_STAR frequency range	**NI 6541:** 48 Hz to 50 MHz **NI 6542:** 48 Hz to 100 MHz	—
Clock requirements	Clock must be continuous and free-running	—

CLK OUT (SMB Jack Connector)

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Specification	Value	Comments
Direction	Output from device	—
Sources	1. Sample clock (excluding STROBE) 2. Reference clock (PLL)	—
Output impedance	50 Ω nominal	—
Electrical characteristics	Refer to the Generation Timing (Data, DDC CLK OUT, and PFI <0..3> Channels) specifications in the Channel Specifications section.	—
Maximum drive current	8 mA at 1.8V, 16 mA at 2.5V, 32 mA at 3.3V	—
Logic type	Generation logic family setting (3.3V, 2.5V, 1.8V)	—

DDC CLK OUT (DDC Connector)

Specification	Value	Comments
Direction	Output from device	—
Sources	Sample clock	STROBE cannot be routed to DDC CLK OUT
Electrical characteristics	Refer to the Generation Timing (Data, DDC CLK OUT, and PFI <0..3> Channels) specifications in the Channel Specifications section.	—

Reference Clock (PPL)

Specification	Value	Comments
Reference Clock sources	1. PXI_CLK10(PXI backplane-PXI only) 2. RTSI 7 (PCI only) 3. CLK IN (SMB jack connector) 4. None (on board clock source not locked to a reference)	Provides the reference frequency for the phase lock loop
Lock time	400ms	—
Reference clock frequencies	10 MHz ±50ppm	—
Reference clock duty cycle range	25% to 75%	—
Reference clock destinations	CLK OUT (SMB jack connector)	—

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Waveform Specifications

Memory and Scripting

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td>Memory architecture</td><td colspan="3">The NI 654X uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters such as number of script instructions, maximum number of waveforms in memory, and number of samples (S) available for waveform storage are flexible and user-defined.</td><td>Refer to the Onboard Memory section in the NI Digital Waveform Generator/Analyzer Help for more information.</td></tr>
<tr><td>Onboard memory size</td><td>1 Mbit/channel (for generation sessions)
1 Mbit/channel (for acquisition sessions)</td><td>8 Mbit/channel (for generation sessions)
8 Mbit/channel (for acquisition sessions)</td><td>64 Mbit/channel (for generation sessions)
64 Mbit/channel (for acquisition sessions)</td><td>Maximum limit for generation sessions assumes no scripting instructions.</td></tr>
<tr><td rowspan="2">Generation modes</td><td colspan="3">Single-waveform mode: Generate a single waveform once, n times, or continuously.</td><td rowspan="2">—</td></tr>
<tr><td colspan="3">Scripted mode: Generate a simple or complex sequence of waveforms. Use scripts to describe the waveforms to be generated, the order in which the waveforms are generated, how many times the waveforms are generated, and how the device responds to Script triggers.</td></tr>
<tr><td rowspan="5">Generation minimum waveform size (Samples)</td><td rowspan="2">Configuration</td><td colspan="2">Sample Rate</td><td rowspan="5">Sample rate dependent. Increasing sample rate increases minimum waveform size requirement.
For information on these configurations, refer to Common Scripting Use Cases in the NI Digital Waveform Generator/Analyzer Help .</td></tr>
<tr><td>100 MHz (NI 6542 only)</td><td>50 MHz</td></tr>
<tr><td>Single waveform</td><td>2</td><td>2</td></tr>
<tr><td>Continuous waveform</td><td>32</td><td>16</td></tr>
<tr><td>Stepped sequence</td><td>128</td><td>64</td></tr>
<tr><td></td><td>Burst sequence</td><td>512</td><td>256</td></tr>
<tr><td>Generation finite repeat count</td><td colspan="3">1 to 16,777, 216</td><td>—</td></tr>
<tr><td>Generation waveform quantum</td><td colspan="3">Waveform size must be an integer multiple of two samples (S).</td><td>Regardless of waveform size, NI-HSDIO allocates waveforms into block sizes of 32 S of physical memory.</td></tr>
<tr><td>Acquisition minimum record size</td><td colspan="3">1 S</td><td>Regardless of waveform size, NI-HSDIO allocates at least 128 bytes for a record.</td></tr>
<tr><td>Acquisition record quantum</td><td colspan="3">1 S</td><td>—</td></tr>
<tr><td>Acquisition maximum number of records</td><td colspan="3">1 record</td><td>—</td></tr>
<tr><td>Acquisition number of pre-Reference trigger samples</td><td colspan="3">0 up to full record</td><td>—</td></tr>
<tr><td>Acquisition number of post-Reference trigger samples</td><td colspan="3">0 up to full record</td><td>—</td></tr>
</table>

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Triggers (Inputs to the NI 654*X*)

Specification	Value		Comments
Trigger types	1. Start trigger 2. Pause trigger 3. Script trigger <0..3> (generation sessions only) 4. Reference trigger (acquisition sessions only)		—
Sources	1. PFI 0 (SMB jack connector) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..7> (PXI backplane—PXI only)/ RTSI <0..7> (RTSI bus—PCI only) 4. PXI_STAR (PXI backplane—PXI only) 5. Pattern match (acquisition sessions only) 6. Software (user function call) 7. Disabled (do not wait for a trigger)		—
Trigger detection	1. Start trigger (edge detection: rising or falling) 2. Pause trigger (level detection: high or low) 3. Script trigger <0..3> (edge detection: rising or falling; level detection: high or low) 4. Reference trigger (edge detection: rising or falling)		—
Minimum required trigger pulse width	40 ns		—
Destinations	1. PFI 0 (SMB jack connectors) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..6> (PXI backplane—PXI only)/ RTSI <0..6> (RTSI bus—PCI only)		Each trigger can be routed to any destination except the Pause trigger. The Pause trigger cannot be exported for acquisition sessions.
Delay from Pause trigger to Pause state	**Generation Sessions**	**Acquisition Sessions**	—
	32 Sample clock periods + 150 ns	Synchronous with the data	Use the Data Active event during generation to determine when the NI 654*X* enters the Pause state.
Delay from trigger to digital data output	32 Sample clock periods + 160 ns		—

Events (Generated from the NI 654*X*)

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Specification	Value	Comments
Event type	1. Marker <0..3> (generation sessions only) 2. Data Active event (generation sessions only) 3. Ready for Start event	—
Destinations	1. PFI 0 (SMB jack connectors) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..6> (PXI backplane—PXI only)/ RTSI <0..6> (RTSI bus—PCI only)	Each event can be routed to any destination, except the Data Active event. The Data Active event can only be routed to the PFI channels.
Marker time resolution (placement)	Markers must be placed at an integer multiple of two samples.	—

Miscellaneous

Specification	Value	Comments
Warm-up time	15 minutes	—
On Board Clock characteristics (valid when PLL reference source is set to None)		
Frequency accuracy	±100 ppm	Typical
Temperature stability	±30 ppm	Typical
Aging	±5 ppm first year	Typical

Power

Specification	Value		Comments
	Typical	**Maximum**	—
+3.3 VDC	1.6 A	1.8 A	—
+5 VDC	1.2 A	1.7 A	—
+12 VDC	0.25 A	0.40 A	—
–12 VDC	0.06 A	0.10 A	—
Total power	15 W	20.5 W	—

Software

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Specification	Value	Comments
Driver software	NI-HSDIO driver software 1.2 or later. NI-HSDIO allows you to configure and control the NI 654*X*. NI-HSDIO provides application interfaces for many development environments. NI-HSDIO follows IVI application programming interface (API) guidelines.	—
Application software	NI-HSDIO provides programming interfaces for the following application development environments: National Instruments LabVIEW 7.0 or later National Instruments LabWindows™/CVI™ 6.0 or later Microsoft Visual C/C++ 6.0 or later	—
Test panel	National Instruments Measurement & Automation Explorer (MAX) provides test panels with basic acquisition and generation functionality for the NI 654*X*. MAX is included on the NI-HSDIO driver CD.	—

Environment

Note To ensure that the NI 654 *X* cools effectively, follow the guidelines in the Maintain Forced Air Cooling Note to Users included with the NI 654*X*. The NI 654*X* is intended for indoor use only.

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Specification	Value	Comments
Operating temperature	**PXI:** 0 °C to +55 °C in all NI PXI chassis except the following: 0 °C to +45 °C when installed in an NI PXI-1000/B and NI PXI-101*X* chassis (Meets IEC-60068-2-1 and IEC-60068-2-2.) **PCI:** 0 °C to +45 °C	—
Storage temperature	–20 °C to 70 °C	—
Operating relative humidity	10% to 90% relative humidity, noncondensing (Meets IEC-60068-2-56)	—
Storage relative humidity	5% to 95% relative humidity, noncondensing (Meets IEC-60068-2-56)	—
Operating shock	30 g, half-sine, 11 ms pulse (Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	—
Storage shock	50 g, half-size, 11 ms pulse (Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	—
Operating vibration	5 Hz to 500 Hz, 0.31 g_{rms} (Meets IEC-60068-2-64.)	—
Storage vibration	5 Hz to 500 Hz, 2.46 g_{rms} (Meets 60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.)	—
Altitude	0 m to 2,000 m above sea level (at 25 °C ambient temperature)	—
Pollution Degree	2	—

Safety, Electromagnetic Compatibility, and CE Compliance

Specification	Value	Comments
Safety	The NI 654*X* meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use: • IEC 61010-1, EN 61010-1 • UL 61010-1 • CAN/CSA C22.2 No. 61010-1	For UL and other safety certifications, refer to the product label or to NI.com .
Emissions	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz	—
Immunity	EN 61326:1997 + A2:2001, Table 1	—
EMC/EMI	CE, C-Tick, and FCC Part 15 (Class A) Compliant.	—
This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:		
Low-Voltage Directive (safety)	73/23/EEC	—
Electro-magnetic Compatibility Directive (EMC)	89/336/EEC	—
For EMC compliance, operate this device with shielded cabling. In addition, filler panels must be installed. Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit NI.com/certification , search by model number or product line, and click the appropriate link in the Certification column.		

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Physical Specifications

Specification	Value		Comments
Dimensions	**PXI:** 18.6 cm × 13.1 cm (7.32 in. × 5.16 in.) Single 3U CompactPCI slot; PXI compatible **PCI:** 12.6 cm × 35.5 cm (4.95 in. × 13.9 in.)		—
Weight	**PXI:** 343.03 g (12.1 oz) **PCI:** 410 g (14.5 oz)		—
Front Panel Connectors			
Label	**Function(s)**	**Connector Type**	—
CLK IN	External Sample clock, external PLL reference input	SMB jack connector	—
PFI 0	Events, triggers	SMB jack connector	—
CLK OUT	Exported Sample clock, exported Reference clock	SMB jack connector	—
DIGITAL DATA & CONTROL	Digital data channels, exported Sample clock, STROBE, events, triggers	68-pin VHDCI connector	—

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