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USER MANUAL

NI PCIe-1437

Base, Medium, Full, and Extended Configuration Camera Link Frame Grabber

The NI PCIe-1437 is an image acquisition device with a PCIe 2.0 x8 host interface. It supports many Lite, Base, Medium, Full, 72-bit, and 80-bit configuration Camera Link-compatible cameras at up to 85 MHz. Power over Camera Link (PoCL) is supported for simplified system connectivity. A variety of auxiliary IO is provided for triggering and control via a digital I/O connector, an I/O extension connector, and RTSI. This document describes the NI PCIe-1437 features and capabilities.

Hardware Overview

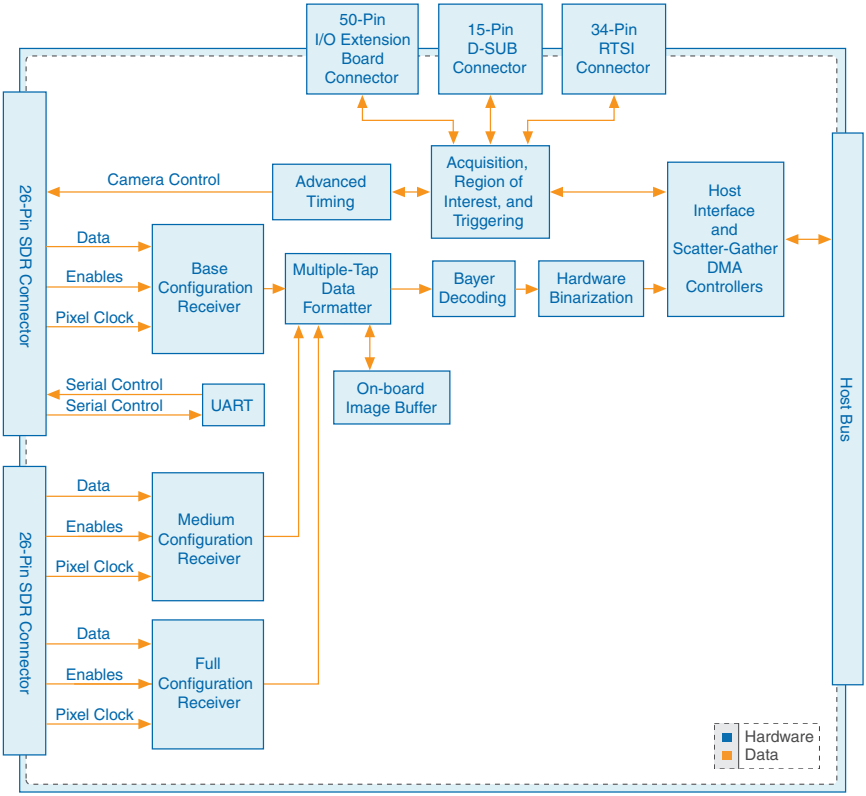
This chapter provides an overview of NI PCIe-1437 hardware functionality and explains the operations of the functional units on the device.

Functional Overview

The NI PCIe-1437 features a flexible, high-speed data path optimized for receiving and formatting video data from Camera Link cameras.

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Figure 1. NI PCIe-1437 Block Diagram



Camera Link and the NI PCIe-1437

The NI PCIe-1437 supports Camera Link Lite, Base, Medium, Full, 72-bit, and 80-bit configurations.

The Camera Link specification includes up to 80 data bits, enable signals, and asynchronous serial transmission, as well as four digital camera control lines. The four camera control lines can be configured to generate precise timing signals for controlling exposure time, frame rates, and other digital camera acquisition control signals.

The Camera Link standard defines physical connections between image acquisition devices and cameras, and it allows for flexibility of image format and data transfer protocols. The camera manufacturer defines image parameters, such as image resolution and the number of bits per pixel, and camera control parameters, such as frame-on-demand and exposure control signals.

These variable parameters are defined on a per-camera basis in a camera file (`camera_model.icd`) supplied by National Instruments. NI-IMAQ uses the information in this camera file to program the NI PCIe-1437 to acquire images from a specific camera.

Without this camera file, the driver does not have the information necessary to configure the device to recognize the image format of the particular camera you are using.

The NI PCIe-1437 supports the following number of taps for the given Camera Link configurations and bit allocations:

Table 1. Supported Camera Bit Configurations

Bits	Number of Taps					
	Lite	Base	Medium	Full	72-bit	80-bit
8	1	1, 2, or 3	4, 5, or 6	7 or 8	9	10
10	1	1 or 2	3 or 4	5		8
12		1 or 2	3 or 4	5		
14		1	2 or 3	4	5	
16		1	2 or 3	4		5
24 (RGB)		1	2	3		
30 (RGB)			1			
36 (RGB)			1			
42 (RGB)			1			
48 (RGB)			1			

Medium, Full, 72-bit, and 80-bit configurations require using two Camera Link connectors. These configurations allow for more data throughput by offering multiple synchronized data channels between the camera and the NI PCIe-1437.

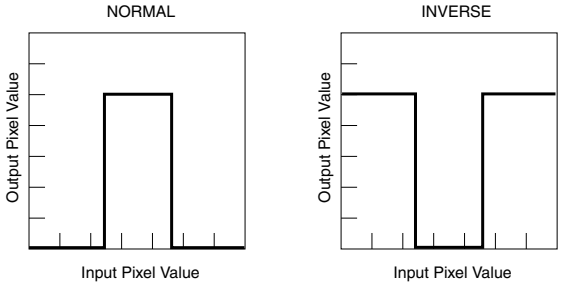
Hardware Binarization (Lookup Table)

The NI PCIe-1437 supports binarization and inverse binarization. Binarization and inverse binarization segment an image into two regions: a particle region and a background region. Use binarization and inverse binarization to isolate objects of interest in an image.

To separate objects under consideration from the background, select a pixel value range. This pixel value range is known as the gray-level interval, or the threshold interval. Binarization works by setting all image pixels that fall within the threshold interval to the image white value and setting all other image pixels to 0. Pixels inside the threshold interval are considered part of the particle region. Pixels outside the threshold interval are considered part of the background region.

Inverse binarization flips the assigned bit numbers of the particle region and the background region. Thus, all pixels that belong in the threshold interval, or the particle region, are set to 0, and all pixels outside the threshold interval, or the background region, are set to the image white value.

Figure 2. Binarization and Inverse Binarization



Multiple-Tap Data Formatter

Many digital cameras transfer multiple taps, or pixels, of data simultaneously to increase the frame rate of the camera. However, the data in each tap may not be transferred in the traditional top-left to bottom-right direction. Also, the taps may not transfer data in the same direction.

The multiple-tap data formatting circuitry on the NI PCIe-1437 can reorder the data from multiple taps. The data from each tap can be independently scanned either from left-to-right or right-to-left and top-to-bottom or bottom-to-top.

Table 2. Tap Geometry Supported by NI PCIe-1437

Number of Taps	Tap Geometry	Bits									
		8	10	12	14	16	24 (RGB)	30 (RGB)	36 (RGB)	42 (RGB)	48 (RGB)
1	1X-1Y	●	●	●	●	●	●	●	●	●	●
2	1X2-1Y	●	●	●	●	●	●				
	2X-1Y	●	●	●	●	●	●				
	2XE-1Y	●	●	●	●	●	●				
	1X-1Y2	●	●	●	●	●					
	1X-2Y	●	●	●	●	●					
	1X-2YE	●	●	●	●	●					
3	1X3-1Y	●	●	●	●	●	●				

Table 2. Tap Geometry Supported by NI PCIe-1437 (Continued)

Number of Taps	Tap Geometry	Bits									
		8	10	12	14	16	24 (RGB)	30 (RGB)	36 (RGB)	42 (RGB)	48 (RGB)
4	1X4-1Y	●	●	●	●	●					
	4X-1Y	●	●	●	●	●					
	4XE-1Y	●	●	●	●	●					
	2X2-1Y	●	●	●	●	●					
	2X2E-1Y	●	●	●	●	●					
	1X-1Y4	●	●	●	●	●					
	1X-4Y	●	●	●	●	●					
	1X2-2YE	●	●	●	●	●					
	2X-2YE	●	●	●	●	●					
	2XE-2YE	●	●	●	●	●					
5	1X5-1Y	●	●	●	●	●					
6	1X6-1Y	●									
7	1X7-1Y	●									
8	1X8-1Y	●	●								
	8X-1Y	●									
	8XE-1Y	●									
	2X4-1Y	●									
	2X4E-1Y	●									
	4X2-1Y	●									
	4X2E-1Y	●									
	1X-1Y8	●									
	1X-8Y	●									
	2X2-2YE	●									
	2X2E-2YE	●									
9	1X9-1Y	●									
10	1X10-1Y	●									

Note Data reformatting instructions for cameras have been preprogrammed into the camera files.

Bayer Decoding

The NI PCIe-1437 includes on-board hardware for Bayer decoding. The Bayer decoding hardware supports the conversion of monochrome Bayer pattern camera pixels to RGB color images, offloading the process from software running on the host CPU. Both 32-bit and 64-bit RGB output formats are supported.

On-board Image Buffer

The NI PCIe-1437 includes 512 MB of DDR3 SDRAM on-board to support the buffering of images. During a normal image acquisition, the image data is written directly to the host computer's memory by the NI PCIe-1437. Some host computer systems may not be able to keep up with peak data rates for brief periods of time due to system loading and other operations that may be occurring simultaneously. The on-board DRAM buffer automatically buffers image data in the event of a system slowdown. This significantly reduces the likelihood that an image will be dropped by the system.

Power over Camera Link (PoCL)

The NI PCIe-1437 supports Power over Camera Link with SafePower, in accordance with the Camera Link specification. This feature allows PoCL-capable cameras to be powered directly by the frame grabber, without the need for an additional power connection to the camera. Both Camera Link ports on the NI PCIe-1437 can supply power to the camera, allowing cameras to draw up to 4 W per port (8 W total).

When the driver is loaded, PoCL is enabled on the frame grabber. The NI-IMAQ camera file (*.icd file) for a given camera has a setting in the **InterfaceInfo** section for a given board called **EnablePoCL**. This can be set to either **Yes** or **No**. If **EnablePoCL** is set to **Yes**, then the driver will enable the PoCL circuitry when a session is opened to the device.

- In Measurement & Automation Explorer (MAX), a session is opened by clicking on the camera item nested under the board item in the tree.
- In LabVIEW, a session is opened by calling **IMAQ Init.vi**.

The PoCL circuitry will remain in whatever state is specified by the **EnablePoCL** setting in the NI-IMAQ camera file even after the session is closed. To change the PoCL circuitry state, the **EnablePoCL** setting must be changed in the NI-IMAQ camera file and a new session must be opened. If only NI-IMAQ is installed, the NI-IMAQ camera file must be edited in a text editor. If NI-IMAQdx is also installed, then the setting may be changed in MAX by changing the value of the **FrameGrabberAttributes::DeviceControls::DevicePoCLEnable** attribute. The setting will not take effect until a new session is opened. Switching the active NI-IMAQ camera file to a camera file with a different setting for **EnablePoCL** will also cause the state of the PoCL circuitry on the frame grabber to change.

The enabled PoCL circuitry on the frame grabber is fully compatible with both PoCL and non-PoCL camera.

In order for the NI PCIe-1437 to power a camera, it must be used with a PoCL-compatible camera and PoCL-compatible Camera Link cables. No additional configuration is needed on the NI PCIe-1437 to switch between PoCL and non-PoCL cameras.

Trigger Control and Mapping Circuitry

The trigger control and mapping circuitry routes and monitors the TTL, RTSI, and isolated inputs, and drives the TTL and RTSI outputs. You can configure each input line to perform a supported action, such as starting an acquisition, on a rising edge or a falling edge. The input lines can be read and the output lines can be driven high or low, allowing them to be used as general-purpose I/O. You can map pulses from the high-speed timing circuitry or the status signals of the NI PCIe-1437 to the output lines.

Six external TTL, eight RTSI, and two isolated input lines are available for simultaneous use. The TTL and RTSI lines are bidirectional and have a programmable direction. All the outputs have a programmable polarity. Additional I/O is available with the NI Camera Link I/O Extension Board (e.g., part number 780869-01 for PCIe or 779352-01 for PCI).

Noise Filtering

Noise filtering is available for all TTL inputs and RTSI inputs. Refer to the *NI-IMAQ VI Reference Help or the NI-IMAQ Function Reference Help* for more information about noise filtering.

Quadrature Encoder Support

The NI PCIe-1437 supports RS-422 and single-ended phase signal decoding from a quadrature encoder. The Phase A and Phase B outputs from the quadrature encoder can be interfaced with the device through the D-SUB connector on the NI PCIe-1437 or through the NI Camera Link I/O Extension Board.

Note The quadrature inputs on the NI PCIe-1437 D-SUB and the NI Camera Link I/O Extension Board cannot be used simultaneously.

The `IMG_ATTR_ENCODER_USE_IO_BOARD_INPUT` attribute must be set to 1 in order to switch the source of the encoder lines to the NI Camera Link I/O Extension Board.

- In LabVIEW if you are using the IMAQ API, you set the **Encoder»Use IO Board Input** property in the property node. This setting does not get persisted to the camera file, so you must programmatically set it in your application.
- If you are using IMAQdx, then you can set the attribute in MAX in the **Camera Attributes** tree using the attribute **FrameGrabberAttributes::EncoderControls::EncoderUseIOBoardInput**. Saving this in IMAQdx will persist the setting when using the IMAQdx API for the application.

Refer to the *Connecting to a Quadrature Encoder* section of the *NI Camera Link I/O Extension Board User Guide* for more information on connecting to and using onboard quadrature counters.

The NI PCIe-1437 provides a 64-bit counter to maintain a precise record of an absolute position determined by the encoder inputs. To generate a pulse train that is based on positional ticks, you can set a unique divide down factor. This pulse train is commonly used as a trigger for a line scan camera when performing a web inspection. The device also supports querying absolute position counter value.

Noise Filtering

Noise filtering is available for the Phase A and Phase B encoder inputs. Refer to the *NI-IMAQ VI Reference Help or the NI-IMAQ Function Reference Help* or the *NI-IMAQ Function Reference Help* for more information about noise filtering.

High-Speed Timing

Built from high-speed counters, the timing circuitry on the device can generate precise real-time control signals for your camera. Map the output of this circuitry to a digital I/O line to provide accurate pulses and pulse trains. Use these control signals to control exposure time and frame rate.

Note The external control for cameras has been preprogrammed into the camera file. You can use Measurement & Automation Explorer (MAX) to specify the frequency and duration of these signals in easy-to-use units.

Acquisition Window Control

The NI PCIe-1437 allows you to specify a particular region of active pixels and active lines within the incoming video data. The active pixel region selects the starting pixel and number of pixels to be acquired relative to the assertion edge of the horizontal (or line) enable signal from the camera. The active line region selects the starting line and number of lines to be acquired relative to the assertion edge of the vertical (or frame) enable signal.

Start Conditions

The NI PCIe-1437 can start acquisitions in the following ways:

- Software control—The device supports software control of acquisition start. You can configure the device to capture a fixed number of frames. Use this configuration for capturing a single frame or a sequence of frames.
- Trigger control—You can start an acquisition by enabling external TTL, RTSI, or isolated input lines. Each of these inputs can start a video acquisition on a rising edge or a falling edge.

Serial Interface

The NI PCIe-1437 provides serial communication to and from the camera through two LVDS pairs in the Camera Link cable. All Camera Link serial communication uses one start bit, one stop bit, no parity, and no hardware handshaking.

The NI PCIe-1437 supports all baud rates specified by the Camera Link specification. Refer to the Specifications for a list of baud rates that the NI PCIe-1437 supports.

You can use the serial interface interactively with MAX, `clsercon.exe`, or a manufacturer supplied camera control utility, or programmatically with LabVIEW, C, or .NET.

Interactively:

- MAX—Use MAX with a camera file containing preprogrammed commands. When an acquisition is initiated, the commands are sent to the camera.
- `clsercon.exe`—Use the National Instruments terminal emulator for Camera Link, `clsercon.exe`, if a camera file with preprogrammed serial commands does not exist for your camera. With `clsercon.exe`, you can still communicate serially with your

camera. Access `clsercon.exe` from the `<NI-IMAQ>\bin` directory, where `<NI-IMAQ>` is the location where NI-IMAQ is installed. This is typically in the same location where other National Instruments software is installed (e.g., `C:\Program Files (x86)\National Instruments\NI-IMAQ` or `C:\Program Files\National Instruments\NI-IMAQ`)

- Manufacturer Supplied Camera Control Utility—Camera manufacturers who are compliant with the Camera Link 1.1 or later specification provide a camera control utility which sends the appropriate serial commands for configuring your camera through the device serial port.

Programmatically:

- LabVIEW—Use the serial interface programmatically, through calls to the NI-IMAQ driver using the IMAQ Serial Write VI and IMAQ Serial Read VI.
- C—Use the serial interface programmatically, through calls to the NI-IMAQ driver using the `imgSessionSerialRead` and `imgSessionSerialWrite` functions.
- .NET—Use the serial interface programmatically, through calls to the NI-IMAQ driver using the `ImaqSerialConnection` class.

Note `clsercon.exe` and all programmatic connection methods provide direct manual access of the NI PCIe-1437 serial port, and are not required for most users.

National Instruments also fully supports the recommended serial API described in the Camera Link Specification. This specification is available on the Automated Imaging Association (AIA) website at *www.visiononline.org*.

Software Overview

Programming the NI PCIe-1437 requires the NI-IMAQdx or NI-IMAQ driver software to control the hardware. National Instruments also offers the following application software packages for analyzing and processing your acquired images.

- NI Vision Builder for Automated Inspection—Allows you to configure solutions to common inspection tasks.
- NI Vision Development Module—Provides customized control over hardware and algorithms.

The following sections provide an overview of the driver and application software. For detailed information about individual software packages, refer to the documentation specific to each software package.

NI-IMAQdx and NI-IMAQ Driver Software[1]

The NI PCIe-1437 ships with NI Vision Acquisition Software, which includes the NI-IMAQdx and NI-IMAQ driver software. Both NI-IMAQdx and NI-IMAQ have an extensive library of functions—such as routines for video configuration, continuous and single shot image

[1] NI recommends the use of NI-IMAQdx as the driver for interfacing with the NI PCIe-1437. NI-IMAQ only includes support for the NI PCIe-1437 to maintain backwards compatibility.

acquisition, memory buffer allocation, trigger control, and device configuration—you can call from the application development environment (ADE).

NI-IMAQdx and NI-IMAQ perform all functions required for acquiring and saving images but does not perform image analysis. Refer to the *National Instruments Application Software* section for image analysis functionality.

NI-IMAQ also provides the interface between the NI PCIe-1437 and LabVIEW, LabWindows™/CVI™, or a text-based programming environment. In addition to the ADEs supported by NI-IMAQ, NI-IMAQdx also provides support for LabVIEW NXG 2.1 and later.

National Instruments Application Software

This section describes the National Instruments application software packages you can use to analyze and process the images you acquire with the NI PCIe-1437.

Vision Builder for Automated Inspection

NI Vision Builder for Automated Inspection (Vision Builder AI) is configurable machine vision software that you can use to prototype, benchmark, and deploy applications. Vision Builder AI does not require programming, but is scalable to powerful programming environments.

Vision Builder AI allows you to easily configure and benchmark a sequence of visual inspection steps, as well as deploy the visual inspection system for automated inspection. You also can migrate the configured inspection to LabVIEW, extending the capabilities of the applications if necessary.

Vision Development Module

NI Vision Development Module, which consists of NI Vision and NI Vision Assistant, is an image acquisition, processing, and analysis library for common machine vision tasks, such as:

- Pattern matching
- Particle analysis
- Gauging
- Taking measurements
- Grayscale, color, and binary image display

You can use the Vision Development Module functions individually or in combination. With the Vision Development Module, you can acquire, display, and store images, as well as perform image analysis and processing.

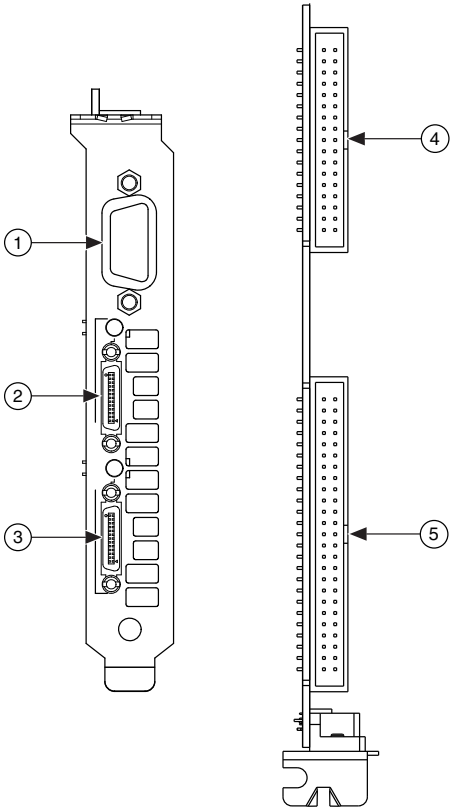
As part of the Vision Development Module, NI Vision Assistant is an interactive prototyping tool for machine vision and scientific imaging developers.

Vision Assistant generates a Builder file, which is a text description containing a recipe of the machine vision and image processing functions. This Builder file provides a guide you can use for developing applications in any ADE, such as LabWindows/CVI or Visual Basic, using the Vision Assistant machine vision and image processing libaries. Using the LabVIEW VI creation wizard, Vision Assistant can create LabVIEW VIs that perform the prototype you created in Vision Assistant. You can then use LabVIEW to add functionality to the generated VI.

Signal Connections

This section describes the connectors on the NI PCIe-1437. The following figure shows the connectors.

Figure 3. NI PCIe-1437 Connectors



1. Digital I/O Connector
2. Base Camera Link Connector
3. Medium/Full Camera Link Connector
4. RTSI Connector
5. I/O Extension Connector

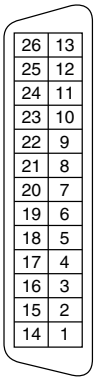
SDR Connectors

The Base and Medium/Full connectors 26-pin SDR connectors that provide reliable high-frequency transfer rates between the camera and the NI PCIe-1437.

- For Lite and Base configuration cameras, connect one 26-pin SDR Camera Link cable to the Base port on the NI PCIe-1437.
- For Medium, Full, 72-bit, or 80-bit configuration cameras, connect one 26-pin SDR Camera Link cable to the Base port and one 26-pin SDR cable to the Medium/Full port on the NI PCIe-1437.

The following figure shows the NI PCIe-1437 26-pin SDR connector.

Figure 4. 26-pin SDR Connector



The following tables list the pin descriptions for the Base connector and the Medium/Full connector.

Table 3. NI PCIe-1437 Base Connector Signal Descriptions

Pin Number	Signal Name	Description
1	DGND/12 V	Digital Ground when connected to non-PoCL cameras and 12 V power supply when connected to PoCL cameras.
2	CC(4)-	LVDS, defined as camera inputs and device outputs, reserved for camera control. On some cameras, the camera controls allow the device to control exposure time and frame rate.
3	CC(3)+	LVDS, defined as camera inputs and device outputs, reserved for camera control. On some cameras, the camera controls allow the device to control exposure time and frame rate.
4	CC(2)-	LVDS, defined as camera inputs and device outputs, reserved for camera control. On some cameras, the camera controls allow the device to control exposure time and frame rate.
5	CC(1)+	LVDS, defined as camera inputs and device outputs, reserved for camera control. On some cameras, the camera controls allow the device to control exposure time and frame rate.
6	SerTFG+	Serial transmission to the NI PCIe-1437 from the camera.

Table 3. NI PCIe-1437 Base Connector Signal Descriptions (Continued)

Pin Number	Signal Name	Description
7	SerTC-	Serial transmission to the camera from the NI PCIe-1437.
8	X(3)+	Base configuration data and enable signal from the camera to the NI PCIe-1437.
9	XCLK+	Transmission clock on the Base configuration chip for Camera Link communication between the NI PCIe-1437 and the camera.
10	X(2)+	Base configuration data and enable signal from the camera to the NI PCIe-1437.
11	X(1)+	Base configuration data and enable signal from the camera to the NI PCIe-1437.
12	X(0)+	Base configuration data and enable signal from the camera to the NI PCIe-1437.
13	DGND	Digital ground
14	DGND	Digital ground
15	CC(4)+	LVDS, defined as camera inputs and device outputs, reserved for camera control. On some cameras, the camera controls allow the device to control exposure time and frame rate.
16	CC(3)-	LVDS, defined as camera inputs and device outputs, reserved for camera control. On some cameras, the camera controls allow the device to control exposure time and frame rate.
17	CC(2)+	LVDS, defined as camera inputs and device outputs, reserved for camera control. On some cameras, the camera controls allow the device to control exposure time and frame rate.
18	CC(1)-	LVDS, defined as camera inputs and device outputs, reserved for camera control. On some cameras, the camera controls allow the device to control exposure time and frame rate.
19	SerTFG-	Serial transmission to the NI PCIe-1437 from the camera.
20	SerTC+	Serial transmission to the camera from the NI PCIe-1437.
21	X(3)-	Base configuration data and enable signal from the camera to the NI PCIe-1437.
22	XCLK-	Transmission clock on the Base configuration chip for Camera Link communication between the NI PCIe-1437 and the camera.

Table 3. NI PCIe-1437 Base Connector Signal Descriptions (Continued)

Pin Number	Signal Name	Description
23	X(2)-	Base configuration data and enable signal from the camera to the NI PCIe-1437.
24	X(1)-	Base configuration data and enable signal from the camera to the NI PCIe-1437.
25	X(0)-	Base configuration data and enable signal from the camera to the NI PCIe-1437.
26	DGND/12 V	Digital Ground when connected to non-PoCL cameras and 12 V power supply when connected to PoCL cameras.

Table 4. NI PCIe-1437 Medium/Full Connector Signal Descriptions

Pin Number	Signal Name	Description
1	DGND/12 V	Digital Ground when connected to non-PoCL cameras and 12 V power supply when connected to PoCL cameras.
2	Z(3)+	Full configuration data and enable signal from the camera to the NI PCIe-1437.
3	ZCLK+	Transmission clock on the Full configuration chip for Camera Link communication between the NI PCIe-1437 and the camera.
4	Z(2)+	Full configuration data and enable signal from the camera to the NI PCIe-1437.
5	Z(1)+	Full configuration data and enable signal from the camera to the NI PCIe-1437.
6	Z(0)+	Full configuration data and enable signal from the camera to the NI PCIe-1437.
7	-	100 Ω differential termination with pin 20.
8	Y(3)+	Medium configuration data and enable signal from the camera to the NI PCIe-1437.
9	YCLK+	Transmission clock on the Medium configuration chip for Camera Link communication between the NI PCIe-1437 and the camera.
10	Y(2)+	Medium configuration data and enable signal from the camera to the NI PCIe-1437.
11	Y(1)+	Medium configuration data and enable signal from the camera to the NI PCIe-1437.

Table 4. NI PCIe-1437 Medium/Full Connector Signal Descriptions (Continued)

Pin Number	Signal Name	Description
12	Y(0)+	Medium configuration data and enable signal from the camera to the NI PCIe-1437.
13	DGND	Digital ground
14	DGND	Digital ground
15	Z(3)-	Full configuration data and enable signal from the camera to the NI PCIe-1437.
16	ZCLK-	Transmission clock on the Full configuration chip for Camera Link communication between the NI PCIe-1437 and the camera.
17	Z(2)-	Full configuration data and enable signal from the camera to the NI PCIe-1437.
18	Z(1)-	Full configuration data and enable signal from the camera to the NI PCIe-1437.
19	Z(0)-	Full configuration data and enable signal from the camera to the NI PCIe-1437.
20	-	100 Ω differential termination with pin 7.
21	Y(3)-	Base configuration data and enable signal from the camera to the NI PCIe-1437.
22	YCLK-	Transmission clock on the Medium configuration chip for Camera Link communication between the NI PCIe-1437 and the camera.
23	Y(2)-	Base configuration data and enable signal from the camera to the NI PCIe-1437.
24	Y(1)-	Base configuration data and enable signal from the camera to the NI PCIe-1437.
25	Y(0)-	Base configuration data and enable signal from the camera to the NI PCIe-1437.
26	DGND/12 V	Digital Ground when connected to non-PoCL cameras and 12 V power supply when connected to PoCL cameras.

D-SUB Connector

The 15-pin female high-density D-SUB connector connects to general purpose digital I/O, which includes six TTL I/O lines, two optically isolated inputs, and one RS-422 quadrature encoder input. The following table shows the connector assignments and descriptions.

Figure 5. 15-pin D-SUB Connector

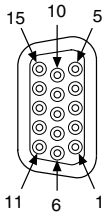


Table 5. NI PCIe-1437 15-pin D-SUB Connector Pin Descriptions

Pin Number	Signal Name	Description
1	TTL I/O 0	TTL-compatible Digital I/O or external trigger
2	Iso Input 0+	24 V-compatible isolated current-sinking digital input
3	Phase A+	Quadrature encoder phase A positive connection for single-ended or differential signal
4	Phase B-	Quadrature encoder Phase B negative connection for differential signal
5	TTL I/O 4	TTL-compatible Digital I/O or external trigger
6	TTL I/O 1	TTL-compatible Digital I/O or external trigger
7	TTL I/O 2	TTL-compatible Digital I/O or external trigger
8	Iso Input 1+	24 V-compatible isolated current-sinking digital input
9	Phase B+	Quadrature encoder Phase B positive connection for single-ended or differential signal
10	TTL I/O 3	TTL-compatible Digital I/O or external trigger
11	Digital Ground	Digital Ground reference for quadrature encoder inputs and TTL I/O
12	Iso Input 0- Iso Input 1-	Common Ground reference for isolated digital inputs
13	Phase A-	Quadrature encoder Phase A negative connection for differential signal
14	Digital Ground	Digital Ground reference for quadrature encoder inputs and TTL I/O
15	TTL I/O 5	TTL-compatible Digital I/O or external trigger

RTSI Connector

The Real-Time System Integration (RTSI) connector allows connection to one or more NI DAQ devices. This allows I/O and trigger expansion beyond that normally available to the NI PCIe-1437. The RTSI bus should only be used with NI devices compatible with the RTSI bus.

Notice The RTSI connector is designed to work only with the NI products that have a RTSI connector. Each RTSI I/O is a bidirectional pin that is compatible with both 3.3 V (LVTTL/LVCMOS) and 5 V I/O (TTL/CMOS). No over-voltage protection, reverse voltage protection, or isolation is provided on this connector. Improper use of this connector will result in damage to the NI PCIe-1437. Use of a RTSI-compatible NI product is recommended.

Figure 6. RTSI Connector

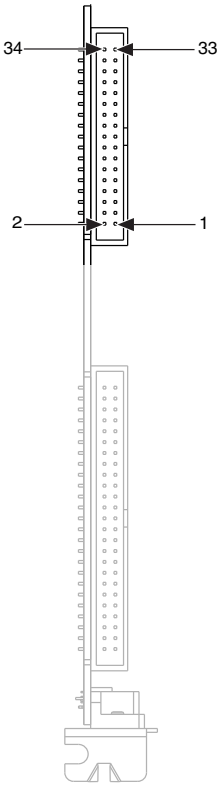


Table 6. NI PCIe-1437 RTSI Connector Pin Descriptions

Pin Number	Description
1 to 18	No connection
19	Digital Ground
20	RTSI 0
21	Digital Ground
22	RTSI 1
23	Digital Ground
24	RTSI 2
25	Digital Ground
26	RTSI 3
27	Digital Ground
28	RTSI 4
29	Digital Ground
30	RTSI 5
31	Digital Ground
32	RTSI 6
33	Digital Ground
34	RTSI 7 / RTSI Clock

I/O Extension Connector

The I/O extension connector is designed to work only with the NI Camera Link I/O Extension Board, which is available in both PCIe and PCI form factors (NI part numbers 780869-01 and 779352-01). See the corresponding user manual for details and specifications for the external I/O of the extension board. This following table describes the pinout of the internal extension connector on the NI PCIe-1437, which controls the NI Camera Link I/O Extension Board.

Notice The I/O extension connector is designed to work only with the NI Camera Link I/O Extension Board. All the I/O on the extension connector is compatible only with 3.3 V (LVTTL/LVCMOS) I/O. No over-voltage protection, reverse voltage protection, or isolation is provided on this connector. Improper use of this connector will result in damage to the NI PCIe-1437. Use of the NI Camera Link I/O Extension Board is recommended.

Figure 7. I/O Extension Connector

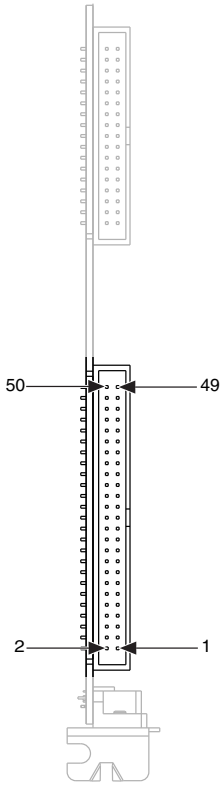


Table 7. NI PCIe-1437 I/O Extension Connector Pin Descriptions

Pin Number	Signal Name	Direction	Description
1	Phase A	Input	Single-ended version of the extension board's quadrature encoder phase A input
2	Phase B	Input	Single-ended version of the extension board's quadrature encoder phase B input
3	Digital Ground	N/A	Ground reference for all I/O on extension connector
4	Iso In 2	Input	Non-isolated version of the extension board's isolated input
5	Iso Out 2 #	Output	Inverted, non-isolated version of the extension board's isolated output

Table 7. NI PCIe-1437 I/O Extension Connector Pin Descriptions (Continued)

Pin Number	Signal Name	Direction	Description
6	Digital Ground	N/A	Ground reference for all I/O on extension connector
7	TTL In 1 #	Input	Inverted version of the extension board's TTL input
8	TTL In 2 #	Input	Inverted version of the extension board's TTL input
9	Digital Ground	N/A	Ground reference for all I/O on extension connector
10	TTL In 3 #	Input	Inverted version of the extension board's TTL input
11	TTL In 4 #	Input	Inverted version of the extension board's TTL input
12	TTL In 5 #	Input	Inverted version of the extension board's TTL input
13	Digital Ground	N/A	Ground reference for all I/O on extension connector
14	TTL In 6 #	Input	Inverted version of the extension board's TTL input
15	TTL In 7 #	Input	Inverted version of the extension board's TTL input
16	TTL In 8 #	Input	Inverted version of the extension board's TTL input
17	Digital Ground	N/A	Ground reference for all I/O on extension connector
18	TTL Out 1	Output	Signal to be output to by the extension board's TTL output
19	TTL Out Enable 1	Output	Output enable (tristate disable) for the corresponding TTL
20	TTL Out 2	Output	Signal to be output to by the extension board's TTL output
21	Digital Ground	N/A	Ground reference for all I/O on extension connector
22	TTL Out Enable 2	Output	Output enable (tristate disable) for the corresponding TTL

Table 7. NI PCIe-1437 I/O Extension Connector Pin Descriptions (Continued)

Pin Number	Signal Name	Direction	Description
23	TTL Out 3	Output	Signal to be output to by the extension board's TTL output
24	TTL Out Enable 3	Output	Output enable (tristate disable) for the corresponding TTL
25	Digital Ground	N/A	Ground reference for all I/O on extension connector
26	TTL Out 4	Output	Signal to be output to by the extension board's TTL output
27	TTL Out Enable 4	Output	Output enable (tristate disable) for the corresponding TTL
28	Digital Ground	N/A	Ground reference for all I/O on extension connector
29	TTL Out 5	Output	Signal to be output to by the extension board's TTL output
30	TTL Out Enable 5	Output	Output enable (tristate disable) for the corresponding TTL
31	TTL Out 6	Output	Signal to be output to by the extension board's TTL output
32	Digital Ground	N/A	Ground reference for all I/O on extension connector
33	TTL Out Enable 6	Output	Output enable (tristate disable) for the corresponding TTL
34	TTL Out 7	Output	Signal to be output to by the extension board's TTL output
35	TTL Out Enable 7	Output	Output enable (tristate disable) for the corresponding TTL
36	Digital Ground	N/A	Ground reference for all I/O on extension connector
37	TTL Out 8	Output	Signal to be output to by the extension board's TTL output
38	TTL Out Enable 8	Output	Output enable (tristate disable) for the corresponding TTL
39	Digital Ground	N/A	Ground reference for all I/O on extension connector

Table 7. NI PCIe-1437 I/O Extension Connector Pin Descriptions (Continued)

Pin Number	Signal Name	Direction	Description
40	Iso In 0	Input	Non-isolated version of the extension board's isolated input
41	Iso In 1	Input	Non-isolated version of the extension board's isolated input
42	Digital Ground	N/A	Ground reference for all I/O on extension connector
43	Iso Out 0 #	Output	Inverted, non-isolated version of the extension board's isolated output
44	Iso Out 1 #	Output	Inverted, non-isolated version of the extension board's isolated output
45	Board Present	Input	Indicates if the extension board is present
46	Reserved	N/A	Reserved
47	Digital Ground	N/A	Ground reference for all I/O on extension connector
48	Reserved	N/A	Reserved
49	Reserved	N/A	Reserved
50	Board Power Enable	Output	Signal to enable extension board power

Connecting Signals

The following diagrams show how different signals are connected to the NI PCIe-1437. Use shielded cables for all applications. Unshielded cables are more susceptible to noise and can corrupt the signals.

Figure 8. Connecting an Isolated Input to a Sourcing Output Device

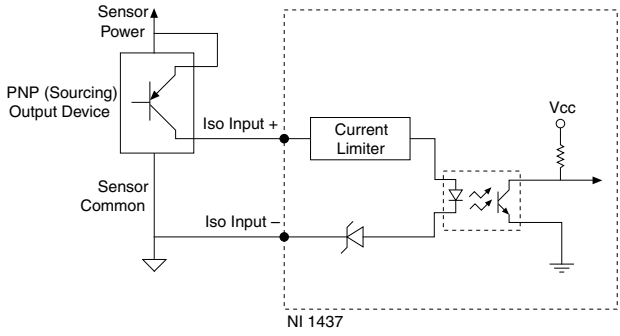


Figure 9. NI PCIe-1437 Quadrature Encoder/RS-422 Inputs Circuit

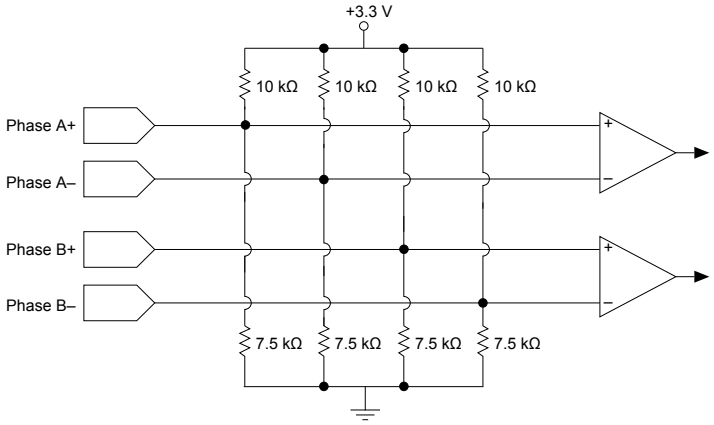


Figure 10. Connecting Differential Line Drivers to Quadrature Encoder Input

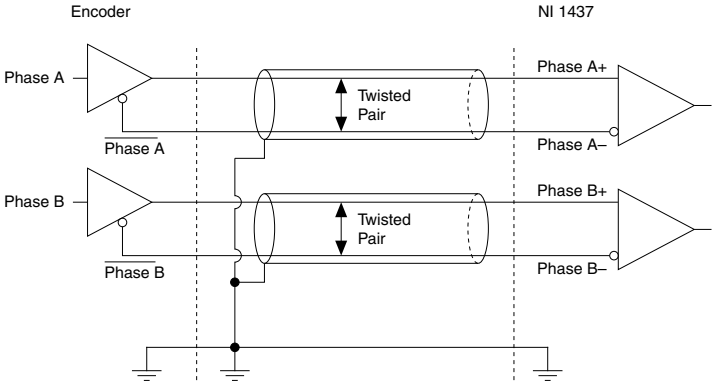


Figure 11. Connecting Single-Ended Line Drivers to Quadrature Encoder Input

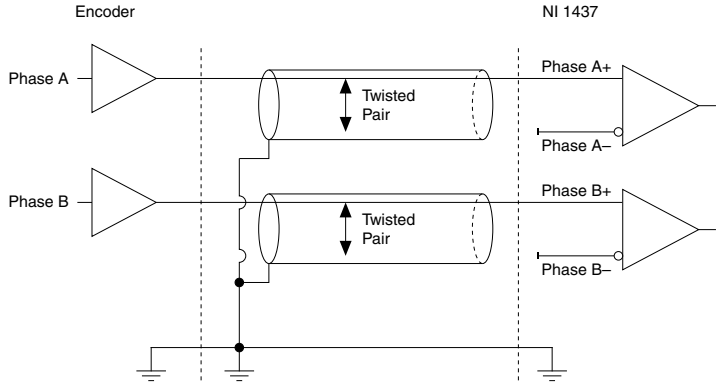
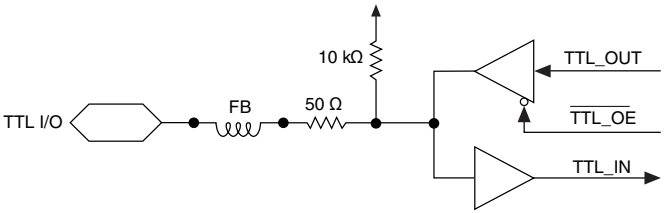


Figure 12. NI PCIe-1437 TTL Input/Output Circuit



Cabling

Use a standard Camera Link cable to connect your camera to the 26-pin SDR connector on the NI PCIe-1437. Camera Link cables consist of two SDR-26 male plugs linked with a twin-axial shielded cable and are available in two shell configurations.

NI recommends that you use the following cables to connect your camera to the 26-pin SDR connectors on the NI PCIe-1437:

- SDR to SDR Camera Link cable (part number 199746-05)
- MDR to SDR Camera Link cable (part number 199745-05)
- 15-pin D-SUB Male to Female, 5 m cable (part number 147791-05)
- 15-pin D-SUB Male to Female, 2 m cable (part number 147791-02)
- 15-pin D-SUB to Pigtail, 5 m cable (part number 147792-05)

Note To ensure the quality of the high-speed signaling of the Camera Link interface, NI recommends that you purchase high-quality Camera Link cables that are rated for the expected pixel clock frequencies rather than build a custom cable.

Refer to the Camera Link Specification for more information about Camera Link cables. This specification is available on the Automated Imaging Association (AIA) website at *www.visiononline.org*.

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