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PCIe-1473R

Camera Link Frame Grabber With FPGA Image Processing



- Places FPGA in image path for on-board pre-pocessing and control applications
- Supports up to 10-tap, 80-bit acquisition at 20 MHz to 85 MHz pixel clock frequency
- 850 MB/s of available bandwidth over two Camera Link cables
- Power over Camera Link (PoCL) support; can be used with PoCL cables to power cameras or without
- Optional digital I/O expansion card for extra triggering and isolation
- Requires LabVIEW FPGA Module software for image acquisition and processing

Overview

The NI PCIe-1473R is a cost-effective Camera Link frame grabber that works well for deployment systems and features a user-programmable FPGA for image processing. It supports 80-bit, 10-tap image acquisition from Camera Link 1.2 standard cameras up to 850MB/s over to Camera Link cables.

The PCI-Express form factor of the 1473R offers a cost-effective deployment alternative to complement the NI 1483 camera link adapter module and FlexRIO prototyping platform. This product is ideal for high-throughput systems in medical imaging, food sorting, semiconductor wafer alignment, flat panel display inspection, and more.

As the highest-bandwidth accepted imaging standard, Camera Link works well for high-resolution cameras and line-scan cameras. The NI PCIe-1433 also supports Power over Camera Link (PoCL) and can be used to power cameras through PoCL-enabled cables. You can access additional digital I/O lines using optional PCI and PCI Express I/O extension boards, which expose the following digital lines: eight bidirectional TTL, three optically isolated input, three optically isolated output, and one quadrature encoder.

NI LabVIEW and the LabVIEW FPGA Module are required to program the NI PCIe-1473R.

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Requirements and Compatibility

OS Information

- Windows 7
- Windows Vista
- Windows XP

Driver Information

- NI-IMAQ
- NI-RIO

Software Compatibility

- LabVIEW Development System
- LabVIEW FPGA Module

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Application and Technology

The Benefits of LabVIEW FPGA

At the highest level, FPGAs are reprogrammable silicon chips. Using prebuilt logic blocks and programmable routing resources, you can configure these chips to implement custom hardware functionality without ever having to pick up a breadboard or soldering iron. You develop digital computing tasks in software and compile them down to a configuration file or bitstream that contains information on how the components should be wired together. In addition, FPGAs are completely reconfigurable and instantly take on a brand new “personality” when you recompile a different configuration of circuitry. In the past, FPGA technology was available only to engineers with a deep understanding of digital hardware design. The rise of high-level design tools, however, is changing the rules of FPGA programming, with new technologies that convert graphical block diagrams or even C code into digital hardware circuitry.

The LabVIEW FPGA Module can help you program an FPGA with a LabVIEW block diagram. Under the hood, the module uses code generation techniques to synthesize the graphical development environment to FPGA hardware. This block diagram approach to FPGA is well-suited for an intuitive depiction of the inherent parallelism that FPGAs provide. Use this module with commercial off-the-shelf (COTS) hardware to create FPGA-based measurement and control hardware whether or not you have worked with hardware description languages (HDLs).

Image Processing on the FPGA

FPGA image processing reduces the computational resources required for image analysis. Because the FPGA is a hardware resource, it frees the CPU to perform other operations. CPU intervention is not required to perform the analysis, so latency is significantly reduced from preprocessed input to processed output. In this case, the FPGA performs all of the image processing, which results in minimum system latency. You can send image information to the CPU for data storage or image display after processing is complete.

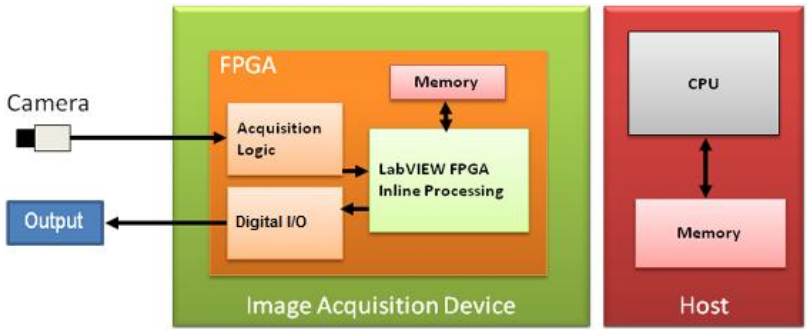


Figure 2. Image analysis is performed on the FPGA for minimal system latency.

You also can use an FPGA with a vision system's processor to perform additional processing. Figure 3 shows how to preprocess with an FPGA while the CPU performs the more advanced processing algorithms. In this case, the FPGA performs bit-level processing such as filtering or edge detection. The preprocessed image is then sent to the CPU for image-level processing such as pattern recognition. System latency is still low in this case because the CPU has fewer functions to perform than it does in a traditional vision system.

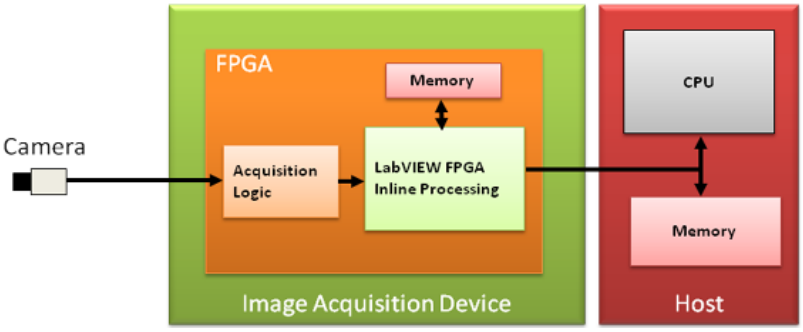


Figure 3. The image is preprocessed on the FPGA, which minimizes load on the CPU.

Many image processing algorithms are inherently parallel and hence suitable for FPGA implementations. These algorithms which involve operations on pixels, lines, and region of interest do not need high-level image information, such as patterns or objects in the image. You can perform these functions on small regions of bits as well as on multiple regions of an image simultaneously. You can pass the image data to the FPGA in parallel and, because a central processor is not required to process the data, process that data concurrently. Some examples of image processing functions that work well on an FPGA are listed below:

Preprocessing

- Image transforms
- Image operators
- Shading correction
- Bayer decoding
- Color space conversion
- 1D and 2D fast Fourier transform
- Filtering (smooth/sharpen)
- Binary morphology

Feature Extraction

- Edges, lines, and corners
- Binary objects
- Color

Measurements

- Centroid
- Area measurements

In addition to the LabVIEW graphical design environment, LabVIEW FPGA supports a feature for HDL IP integration called Component-Level IP (CLIP). With CLIP, you can insert HDL IP into an FPGA target so VHDL code can communicate directly with an FPGA VI. CLIP also facilitates communication between the FPGA and external circuitry using existing HDL IP.

The Benefits of LabVIEW FPGA

Part Number Part Description

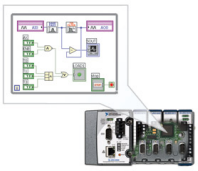
781585-01	NI PCIe-1473R, Virtex-5 LX50, Camera Link Frame Grabber
782849-01	NI PCIe-1473R, Virtex-5 LX110, Camera Link Frame Grabber
780869-01	Camera Link I/O Extension Board (PCIe)

779352-01	Camera Link I/O Extension Board (PCI)
778790-01	NI 1450, I/O Terminal Block, Horizontal Mount and Cable, used with I/O Extension Board
199744-05	Cable, Power over Camera Link (PoCL), MDR to MDR, 5M
199745-05	Cable, Power over Camera Link (PoCL), MDR to SDR, 5M
199744-02	Cable,Power over Camera Link(PoCL),MDR to MDR,2M

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Software Recommendations

NI LabVIEW FPGA Module



- Design FPGA applications for NI reconfigurable I/O (RIO) hardware targets
- Program with the same graphical environment used for desktop and real-time applications
- Execute control algorithms with loop rates up to 300 MHz
- Implement custom timing and triggering logic, digital protocols, and DSP algorithms
- Incorporate existing HDL code and third-party IP including Xilinx CORE Generator functions
- Included in the LabVIEW Embedded Control and Monitoring Suite

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Support and Services

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Get answers to your technical questions using the following National Instruments resources.

- **Support** - Visit ni.com/support to access the NI KnowledgeBase, example programs, and tutorials or to contact our applications engineers who are located in NI sales offices around the world and speak the local language.
- **Discussion Forums** - Visit forums.ni.com for a diverse set of discussion boards on topics you care about.
- **Online Community** - Visit community.ni.com to find, contribute, or collaborate on customer-contributed technical content with users like you.

Repair

While you may never need your hardware repaired, NI understands that unexpected events may lead to necessary repairs. NI offers repair services performed by highly trained technicians who quickly return your device with the guarantee that it will perform to factory specifications. For more information, visit ni.com/repair.

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Detailed Specifications

These specifications are typical at 25 °C, unless otherwise stated.

Features	
Supported camera standard	Camera Link 1.2
Supported configurations	Base, Medium, Full, 80-bit/10-tap
Camera connectors	Two 26-pin MDR
PCI Express Interface	
PCI Express compliance	1.1
Native link width	x4
Up-plugging availability	x8, x16

Note Some system devices limit data transfer rates for plug-in devices in an up-plugging configuration. Refer to the documentation provided by the computer manufacturer to determine if your computer will support a x4 plug-in device at a x4 data rate in a larger slot.

Reconfigurable FPGA	
FPGA type	Virtex-5 LX50
Number of flip-flops	19,200
Number of 6-input LUTs	19,200
Number of DSP48 slices	48 (25 × 18 multipliers)
Embedded block RAM	1,728 kbits
Trigger Characteristics	
Number of external trigger I/O lines	1
Trigger input	
Voltage range	0 to 5 V (TTL)
Input high voltage	2.0 V
Input low voltage	0.8 V
Trigger output	
Voltage range	0 to 5 V (TTL)
Output high voltage	3.06 V at 3 mA source
Output low voltage	0.55 V at 3 mA sink
Maximum pulse rate	2 MHz
Clocks	
Pixel clock frequency range	20 MHz to 85 MHz [1]

Note The Camera Link specification requires cameras to transmit at a minimum of 20 MHz.

Serial Interface	
Baud rates supported	9.6, 19.2, 38.4, 57.6, 115.2, 230.4, 460.8, or 921.6 kbps
Power Requirements	
Voltage	+3.3 V (1.5 A), +12 V (1.25 A)
Power Over Camera Link (PoCL)	

Voltage	12 V nominal
Average power output	4 W maximum
SafePower	Supported

Physical Characteristics

Dimensions	10.7 cm × 17.5 cm; (4.2 in. × 6.9 in.)
Weight	205 g (7.23 oz)

Environment

The NI 1473 is intended for indoor use only.

Operating Environment

Operating temperature	0 °C to 45°C Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.
Relative humidity range	10% to 90%, noncondensing, Tested in accordance with IEC-60068-2-56
Altitude	2,000 m at 25 °C ambient temperature
Pollution Degree	2

Storage Environment

Ambient temperature range	–20 °C to 70 °C, Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2
Relative humidity range	5% to 95%, noncondensing, Tested in accordance with IEC-60068-2-56

Note Clean the device with a soft, non-metallic brush. Make sure the device is completely dry and free from contaminants before returning it to service.

Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326 (IEC 61326): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note For the standards applied to assess the EMC of this product, refer to the *Online Product Certification* section.

Note For EMC compliance, operate this device with shielded cables and according to the documentation.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit ni.com/certification, search by module number or product line, and click the appropriate link in the Certification column.

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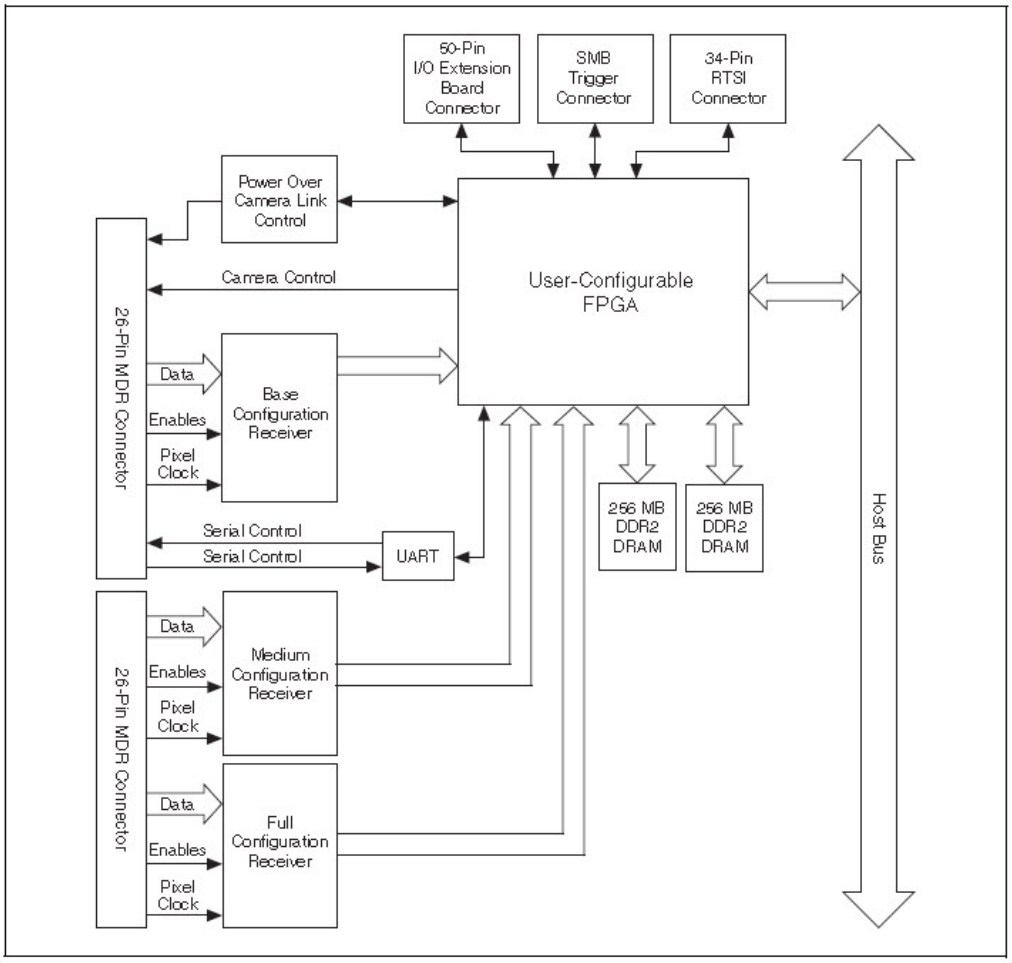
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[1] This value corresponds to the serialized Camera Link cable transmission rate of 140 to 595 MHz.

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Pinouts/Front Panel Connections



NI 1473R Block Diagram

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