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PXI

NI PXI-4204 User Manual

June 2007
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Conventions

The following conventions are used in this manual:

<> — Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, AO <3..0>.

» — The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.

 — This icon denotes a note, which alerts you to important information.

 — This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on a product, refer to the *Read Me First: Safety and Radio-Frequency Interference* for information about precautions to take.

 — When symbol is marked on a product, it denotes a warning advising you to take precautions to avoid electrical shock.

 — When symbol is marked on a product, it denotes a component that may be hot. Touching this component may result in bodily injury.

bold — Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names.

italic — Italic text denotes variables, emphasis, a cross-reference, or an introduction to a key concept. Italic text also denotes text that is a placeholder for a word or value that you must supply.

`monospace` — Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames, and extensions.

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Contents

Chapter 1
About the NI PXI-4204

What You Need to Get Started 1-2
National Instruments Documentation 1-2
Installing the Application Software, NI-DAQ, and the DAQ Device 1-3
Installing the NI PXI-4204 1-3
LED Pattern Descriptions 1-4

Chapter 2
Connecting Signals

Connecting Signals to the NI PXI-4204 2-1
Front Signal Connector 2-3
Analog Input Connections 2-5
Floating Signal Source Connection 2-6
Shielded Floating Signal Source Connection (Recommended) 2-7
Ground-Referenced Signal Connection 2-8
Shielded Ground-Referenced Signal Connection (Recommended) 2-9
Alternative Shielded Ground-Referenced Connection 2-10
High CMV Connection 2-11
Shielded High CMV Connection 2-12

Chapter 3
Using the NI PXI-4204

Theory of Operation 3-1
Signal Conditioning Functional Overview 3-3
Measurement Considerations 3-4
Differential Signals 3-4
Input Impedance 3-5
Common-Mode Rejection Ratio 3-5
Normal-Mode Rejection 3-6
Effective CMR 3-6
Timing and Control Functional Overview 3-7
Programmable Function Inputs 3-8
Device and PXI Clocks 3-9
Developing Your Application 3-11
Typical Program Flow Chart 3-11

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General Discussion of Typical Flow Chart 3-13
Creating a Task Using DAQ Assistant or Programmatically 3-13
Adjusting Timing and Triggering 3-14
Configuring Channel Properties 3-14
Acquiring, Analyzing, and Presenting 3-15
Completing the Application 3-15
Developing an Application Using LabVIEW 3-16
Using a DAQmx Channel Property Node in LabVIEW 3-17
Synchronization and Triggering 3-19
Synchronizing the NI PXI-4204 3-19
Synchronizing the NI PXI-4204 Using LabVIEW 3-21
Other Application Documentation and Material 3-22
Calibrating the NI PXI-4204 3-23
Loading Calibration Constants 3-23
Self-Calibration 3-23
External Calibration 3-24

Appendix A
Specifications

Appendix B
Timing Signal Information

Appendix C
Removing the NI PXI-4204

Appendix D
Common Questions

Glossary

Index

Figures

Figure 2-1. Installing the NI PXI-4204 Device 2-2
Figure 2-2. NI PXI-4204 Screw Terminals 2-4
Figure 2-3. NI PXI-4204 Front Label 2-5
Figure 2-4. Floating Signal Source Connection 2-6
Figure 2-5. Shielded Floating Signal Source Connection (Recommended) 2-7

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Figure 2-6. Ground-Referenced Signal Connection....2-9
Figure 2-7. Recommended Shielded Ground-Referenced Signal Connection....2-10
Figure 2-8. Alternative Shielded Ground Referenced Signal Connection....2-11
Figure 2-9. High CMV Connection....2-12
Figure 2-10. Shielded High CMV Connection....2-13

Figure 3-1. Block Diagram of NI PXI-4204....3-2
Figure 3-2. Effect of Input Impedance on Signal Measurements....3-5
Figure 3-3. AI CONV CLK Signal Routing....3-8
Figure 3-4. NI PXI-4204 PXI Trigger Bus Signal Connection....3-10
Figure 3-5. Typical Program Flowchart....3-12
Figure 3-6. LabVIEW Channel Property Node with Filtering Enabled at 10 kHz and SS/H Enabled....3-18
Figure 3-7. General Synchronizing Flowchart....3-20

Figure A-1. NI PXI-4204 Dimensions....A-6

Figure B-1. Typical Posttriggered Sequence....B-2
Figure B-2. Typical Pretriggered Sequence....B-2
Figure B-3. AI START TRIG Input Signal Timing....B-3
Figure B-4. AI START TRIG Output Signal Timing....B-3
Figure B-5. AI REF TRIG Input Signal Timing....B-4
Figure B-6. AI REF TRIG Output Signal Timing....B-5
Figure B-7. AI SAMP CLK Input Signal Timing....B-6
Figure B-8. AI SAMP CLK Output Signal Timing....B-6
Figure B-9. AI CONV CLK Input Signal Timing....B-7
Figure B-10. AI CONV CLK Output Signal Timing....B-8
Figure B-11. AI SAMPLE CLK TIMEBASE Signal Timing....B-9
Figure B-12. AI HOLD COMPLETE Signal Timing....B-10

Figure C-1. Injector/Ejector Handle Position Before Device Removal....C-2

Tables

Table 3-1. Signal Conditioning Functional Blocks....3-3
Table 3-2. PXI Trigger Bus Timing Signals....3-10
Table 3-3. NI-DAQmx Properties....3-14
Table 3-4. Programming a Task in LabVIEW....3-16
Table 3-5. Synchronizing the NI PXI-4204 Using LabVIEW....3-21

Table A-1. Maximum Sampling Rates....A-1

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1

About the NI PXI-4204

The NI PXI-4204 is part of the PXI-4200 series of data acquisition (DAQ) devices with integrated signal conditioning. The PXI-4200 series reduces measurement setup and configuration complexity by integrating signal conditioning and DAQ on the same product.

The NI PXI-4204 is a full-featured measurement device with programmable filter and gain settings per channel, ensuring maximum accuracy over the entire ±100 V input range. The NI PXI-4204 features the National Instruments (NI) programmable gain instrumentation amplifier (PGIA), an instrumentation-class amplifier that guarantees fast settling times at all gain settings.

The NI PXI-4204 is an eight-channel device for measuring voltages up to ±100 volts. The NI PXI-4204 has the following features:

- Eight differential analog input (AI) channels
- 16-bit resolution
- 200 kS/s aggregate sampling rate
- 22 kS/s per channel when simultaneously sampling all channels
- Input ranges of ±100, ±50, ±5, and ±0.5 V
- Two-pole software programmable Butterworth filters with software selectable filter settings of 6 Hz and 10 kHz per channel
- Instrumentation amplifier per channel
- Track-and-hold (T/H) circuitry providing simultaneous sample-and-hold (SS/H) capability
- Synchronization with other DAQ devices through the PXI trigger bus
- Direct connectivity through a removable COMBICON connector

You can configure most settings on a per-channel basis through software. The NI PXI-4204 is configured using Measurement & Automation Explorer (MAX) or through function calls to NI-DAQmx.

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What You Need to Get Started

To set up and use the NI PXI-4204, you need the following:

- ❑ Hardware
  - NI PXI-4204 device
  - Safety shell (provided)
  - COMBICON screw terminal connector (provided)
  - PXI or PXI/SCXI combination chassis
- ❑ Software
  - NI-DAQ 7.0 or later
  - One of the following:
    - LabVIEW
    - Measurement Studio
    - LabWindows™/CVI™
- ❑ Documentation
  - *NI PXI-4204 User Manual*
  - *Read Me First: Safety and Radio-Frequency Interference*
  - *DAQ Getting Started Guide*
  - PXI or PXI/SCXI combination chassis user manual
  - Documentation for your software
- ❑ Tools
  - 1/8 in. flathead screwdriver

You can download NI documents from `ni.com/manuals`.

National Instruments Documentation

The *NI PXI-4204 User Manual* is one piece of the documentation set for your DAQ system. You could have any of several types of manuals, depending on the hardware and software in your system. Use the documentation you have as follows:

- *DAQ Getting Started Guide*—This document describes how to install DAQ devices and the NI-DAQ driver software. Install NI-DAQ before you install the SCXI module.

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- *SCXI Quick Start Guide*—This document describes how to set up an SCXI chassis, install SCXI modules and terminal blocks, and configure the SCXI system in MAX.
- PXI or PXI/SCXI combination chassis manual—Read this manual for maintenance information about the chassis and for installation instructions.
- Accessory installation guides or manuals—If you are using accessory products, read the terminal block installation guides. It explain how to physically connect the relevant pieces of the system. Consult this guide when you are making the connections.
- Software documentation—You may have both application software and NI-DAQmx software documentation. NI application software includes LabVIEW, Measurement Studio, and LabWindows/CVI. After you set up the hardware system, use either your application software documentation or the NI-DAQmx documentation to help you write your application. If you have a large, complicated system, it is worthwhile to look through the software documentation before you configure the hardware.

Installing the Application Software, NI-DAQ, and the DAQ Device

Refer to the *DAQ Getting Started Guide*, packaged with the NI-DAQ software, to install your application software and NI-DAQ driver software.

NI-DAQ 7.0 or later is required to configure and program the NI PXI-4204 device. If you do not have NI-DAQ 7.0 or later, you can either contact an NI sales representative to request it on a CD or download the latest NI-DAQ version from `ni.com`.

Installing the NI PXI-4204

Note Refer to the *Read Me First: Safety and Radio-Frequency Interference* document before removing equipment covers or connecting or disconnecting any signal wires.

Refer to the *DAQ Getting Started Guide* to unpack, install, and configure the NI PXI-4204 in a PXI chassis and then to the *SCXI Quick Start Guide* if you are using a PXI/SCXI combination chassis.

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LED Pattern Descriptions

The following LEDs on the NI PXI-4204 front panel confirm the system is functioning properly:

- The *ACCESS* LED is normally green and blinks yellow for a minimum of 100 ms during the NI PXI-4204 configuration.
- The *ACTIVE* LED is normally green and blinks yellow for a minimum of 100 ms during data acquisition.

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2

Connecting Signals

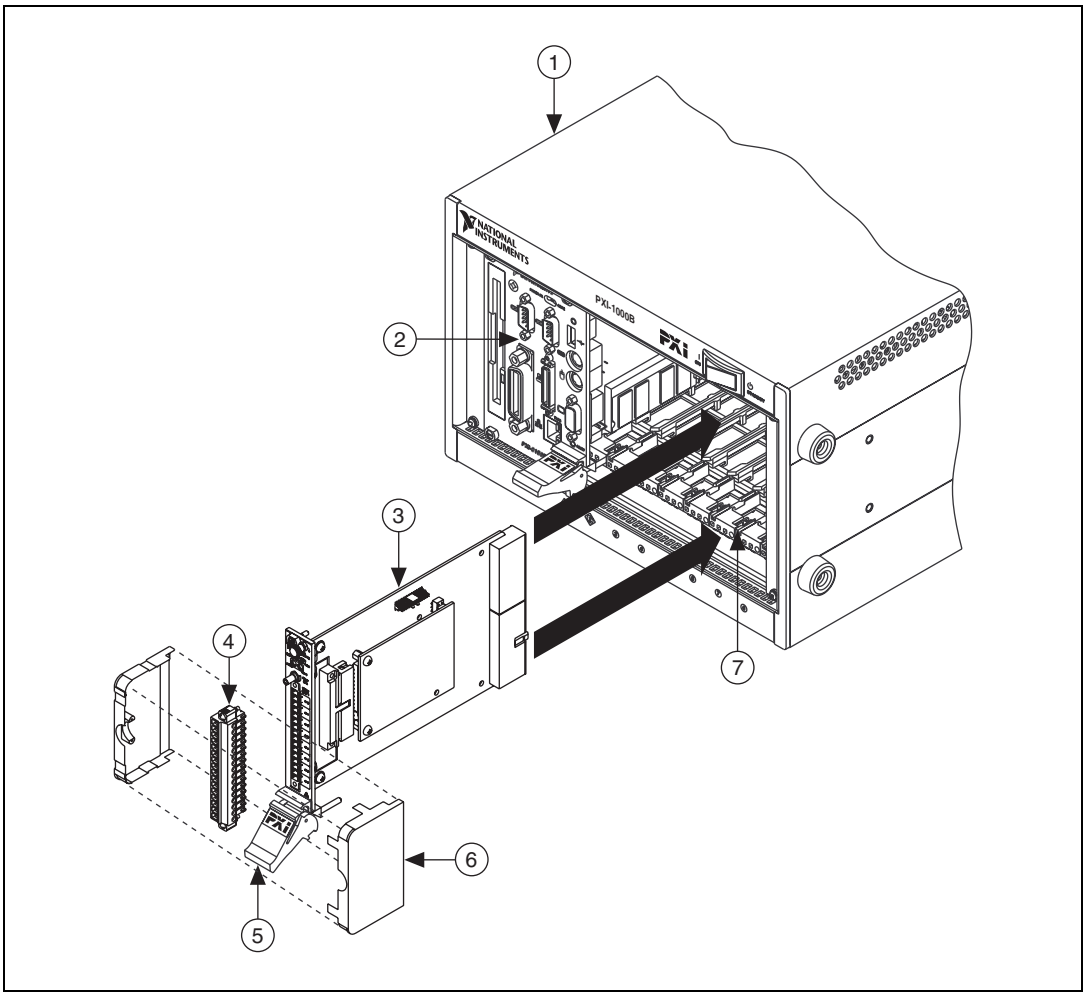
This chapter provides information about the NI PXI-4204 front signal connector and how to connect signals to the NI PXI-4204.

Connecting Signals to the NI PXI-4204

After you have verified that the NI PXI-4204 is installed correctly and self-tested the device, refer to the following sections to connect signals to the device.

Caution You *must* clamp the safety shell over the COMBICON connector to prevent accidental contact with hazardous voltages. Refer to Figure 2-1 for information about how to properly install the NI PXI-4204 and safety shell.

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1	PXI Chassis	4	COMBICON Connector	6	Safety Shell
2	PXI System Controller	5	Injector/Ejector Handle	7	Guides
3	NI PXI-4204 Device				

Figure 2-1. Installing the NI PXI-4204 Device

Caution Refer to the *Read Me First: Safety and Radio-Frequency Interference* document before removing equipment covers or connecting/disconnecting any signal wires.

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Front Signal Connector

The NI PXI-4204 is a direct-connect device. The connection interface consists of a 16-pin COMBICON connector and one SMB connector. Figure 2-2 shows the pin assignments for the signals. Figure 2-3 shows the front label of the NI PXI-4204, with each set of screw terminals labeled according to the corresponding differential input signal. To connect a signal to the NI PXI-4204, complete the following steps while referring to Figures 2-2 and 2-3:

1. Remove power from the signal lines. If this is not possible, complete the following steps while referring to Figures 2-2, and 2-3.
   a. Remove the COMBICON connector from the NI PXI-4204.
   b. Attach the signal sources according to the instructions in steps 2 through 4.
   c. Ensure the NI PXI-4204 is powered on.
   d. Reinstall the COMBICON connector.
2. Strip 7 mm (0.25 in.) of insulation from the ends of the signal wires.
3. Insert the wires into the screw terminals.
4. Tighten the screws to 0.5–0.6 N · m (4.4–5.3 lb · in.) of torque.

Connect a timing or triggering signal to the PFI0/CAL SMB connector using a cable with an SMB signal connector.

Caution The PFI0/CAL SMB connector is for low-voltage timing and calibration signals *only*. Voltages greater than ±15 V can damage the device.

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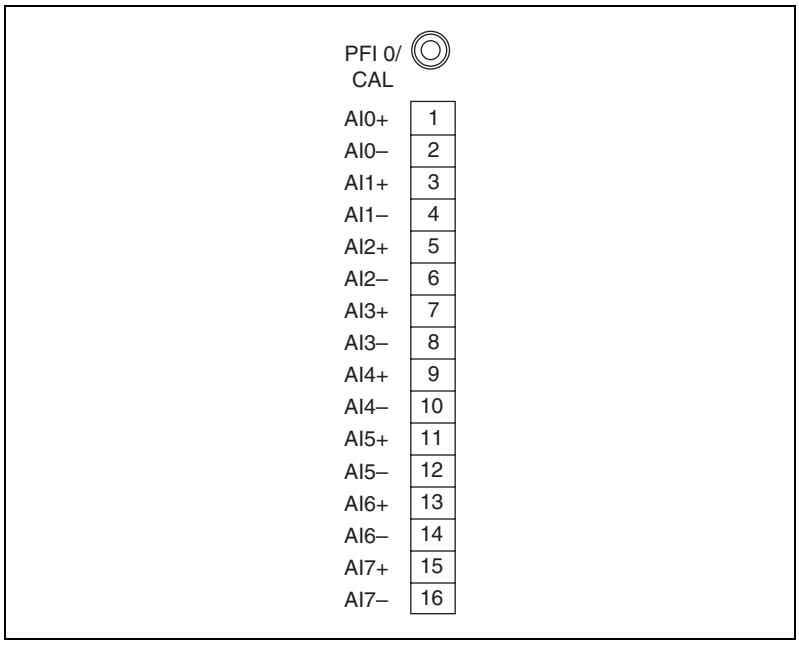


Figure 2-2. NI PXI-4204 Screw Terminals

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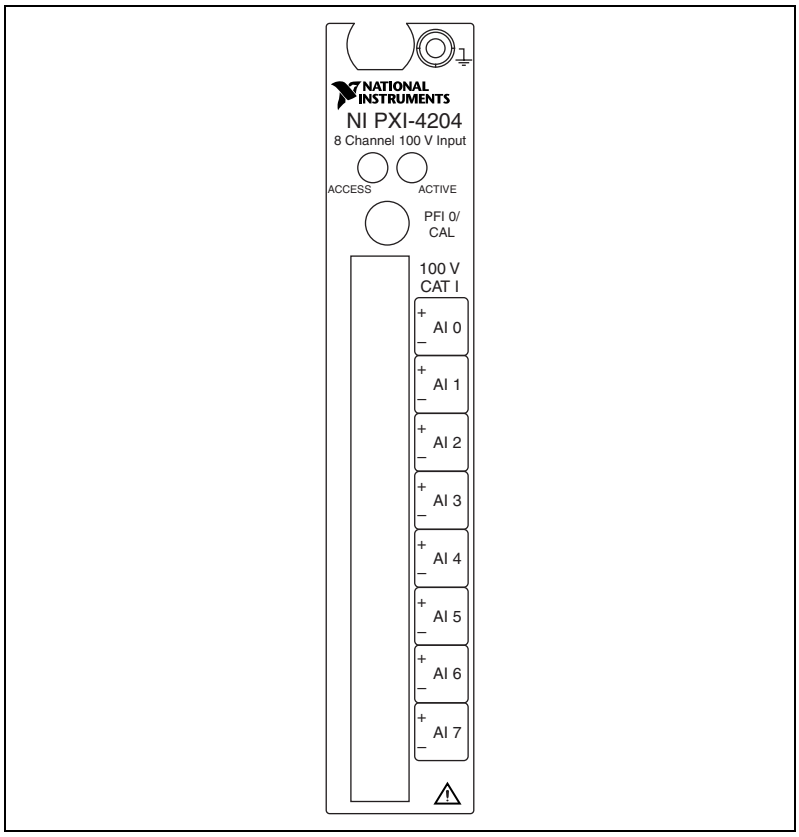


Figure 2-3. NI PXI-4204 Front Label

Analog Input Connections

The following sections provide a definition of the signal source characteristics, descriptions of various ways to connect signals to the NI PXI-4204, and electrical diagrams showing the signal source and connections. Whenever possible, use shielded twisted-pair field wiring to reduce the effects of unwanted noise sources.

In the electrical diagrams, two different ground symbols are used. These symbols indicate that you cannot assume that the indicated grounds are at the same potential. Refer to Appendix A, *Specifications*, for maximum working voltage specifications.

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Floating Signal Source Connection

Figure 2-4 illustrates the floating signal source connection. In this configuration, the signal source being measured is a floating signal source, such as a battery.

To connect a floating signal source connection to the NI PXI-4204, the signal (V_{SIG}+) is connected to the NI PXI-4204 channel (AI*X*+). The signal reference (V_{SIG}–) is connected to the channel reference (AI*X*–). The lack of shielding on the field wiring can cause this configuration to be susceptible to electrically coupled noise.

This configuration has only one ground connection—at the instrument—so there is no potential difference between grounds to introduce error in your measurements. The NI PXI-4204 input attenuators provide a ground reference for floating signal sources; therefore, external grounding bias resistors are not required.

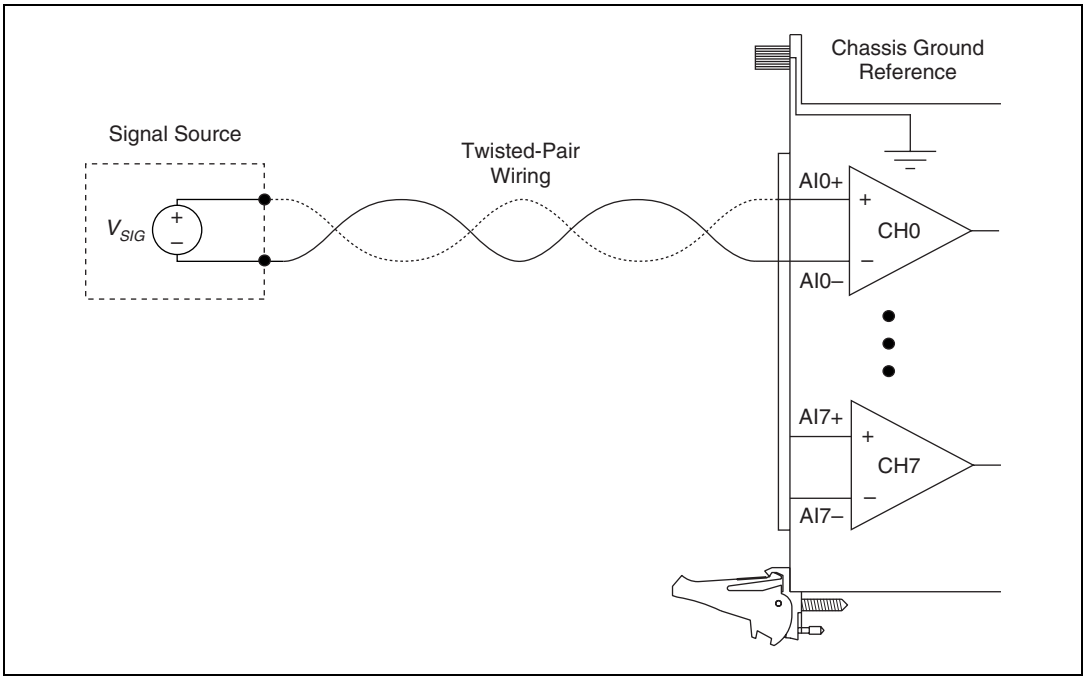


Figure 2-4. Floating Signal Source Connection

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Shielded Floating Signal Source Connection (Recommended)

The signal source shown in Figure 2-5 is identical to the one shown in Figure 2-4. The only difference is the addition of shielding around the field wiring.

You can improve the noise susceptibility of the floating signal source connection, shown in Figure 2-4, by using a shielded cable to connect the signal source to the instrument, as shown in Figure 2-5. This is the recommended shielding configuration for floating signal sources. The shielding is grounded at only one point to the NI PXI-4204 chassis ground reference. Connect the signal (V_{SIG}+) to the NI PXI-4204 channel (AI*X*+). Connect the signal reference (V_{SIG}–) to the channel reference (AI*X*–).

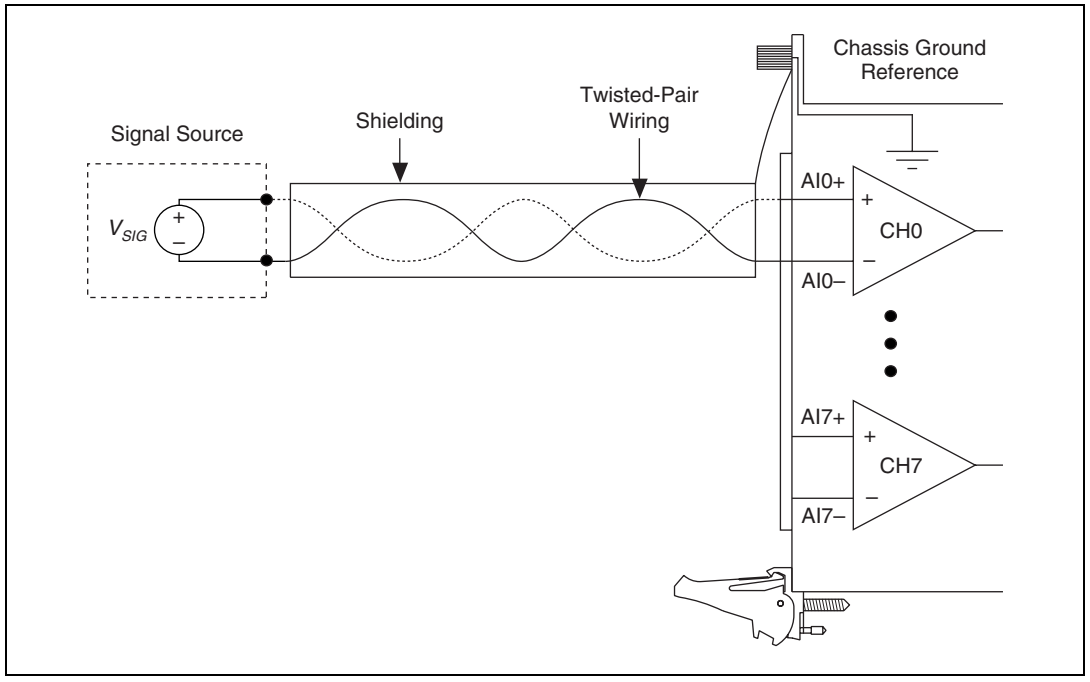


Figure 2-5. Shielded Floating Signal Source Connection (Recommended)

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Ground-Referenced Signal Connection

Figure 2-6 illustrates the ground-referenced signal connection. In this configuration, the voltage source being measured is referenced to its own ground reference that is connected through some conductive path to the instrument ground reference. For example, the path can be through a common earth ground or through the power line ground.

Note This connection is a characteristic of the signal source and no additional wiring should be added to connect the signal source ground reference to the NI PXI-4204 ground reference.

To connect a ground-reference signal source to the NI PXI-4204, the signal (V_{SIG}+) is connected to the NI PXI-4204 channel (AI*X*+). The signal reference (V_{SIG}–) is connected to the channel reference (AI*X*–). The signal ground reference (V_{SIG} Ground Reference) is referenced to the NI PXI-4204 chassis ground reference inherently through some conductive path that you do not physically connect.

This configuration is very simple to connect, but it also can be susceptible to capacitive or electrically coupled noise. Also, the difference in ground potential between the signal source ground and instrument ground creates an unwanted signal that can introduce an error into the measurement. This error is presented as a common-mode voltage (CMV) to the differential front end of the NI PXI-4204, and is reduced by the common-mode rejection (CMR) of the differential instrumentation amplifier. The effectiveness of the CMR is affected by the source resistance of the signal being measured. For more information about the effect of source resistance on CMR, refer to the *Measurement Considerations* section of Chapter 3, *Using the NI PXI-4204*.

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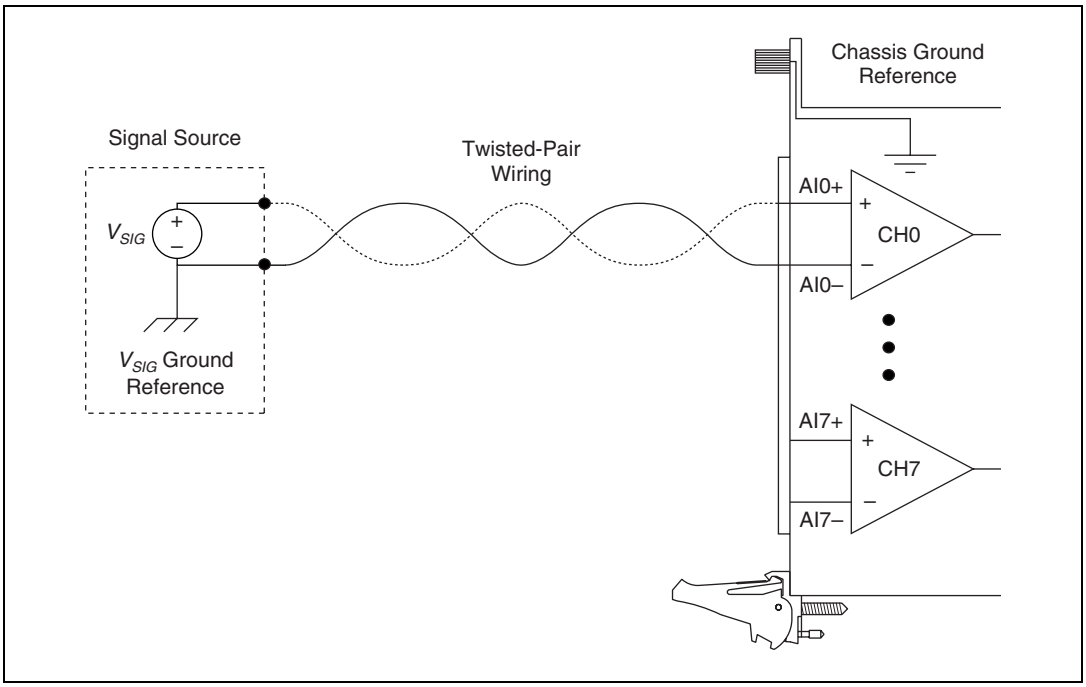


Figure 2-6. Ground-Referenced Signal Connection

Shielded Ground-Referenced Signal Connection (Recommended)

Figure 2-7 illustrates a shielded ground-referenced signal connection. The connection to this signal source is identical to the ground-referenced signal connection with the addition of shielding around the field wiring. The ground-referenced signal source in Figure 2-7 is identical to the signal source in Figure 2-6.

The shielding is grounded at only one point to the signal source ground (V_{SIG} Ground Reference). Connect the signal (V_{SIG}+) to the NI PXI-4204 channel (AI*X*+). Connect the signal reference (V_{SIG}–) to the channel reference (AI*X*–).

This shielding scheme is effective at reducing capacitive or electrically coupled noise. The same concerns regarding the difference in ground potentials, discussed in the *Ground-Referenced Signal Connection* section, also apply to this configuration.

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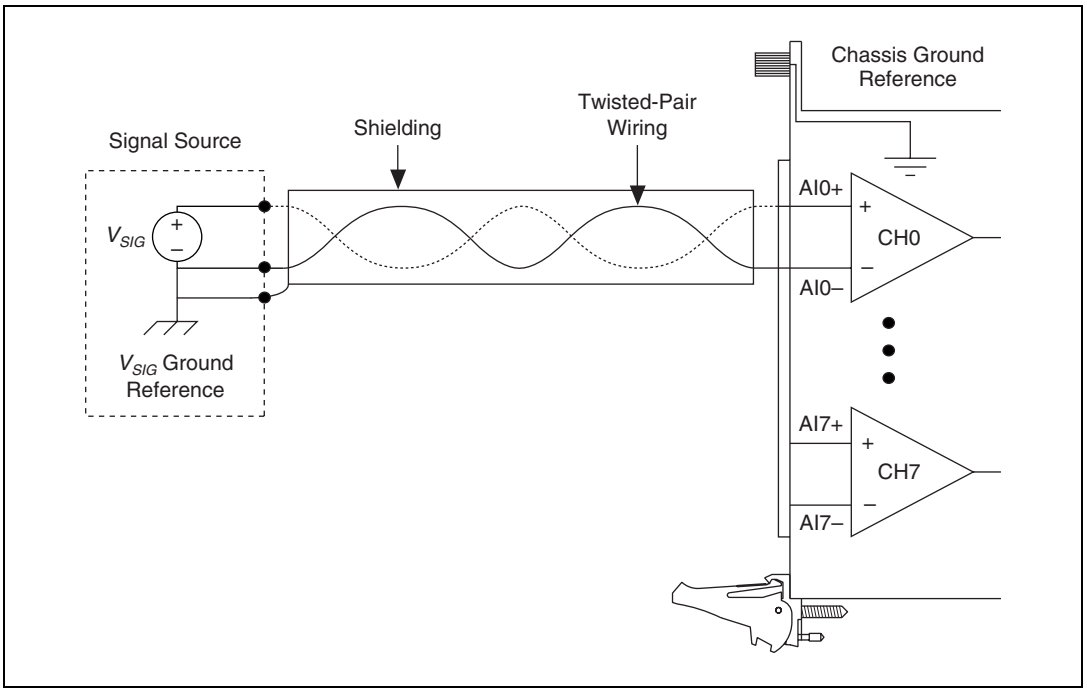


Figure 2-7. Recommended Shielded Ground-Referenced Signal Connection

Alternative Shielded Ground-Referenced Connection

Figure 2-8 illustrates an alternative shielded ground-referenced signal connection. The ground-referenced signal source in Figure 2-8 is identical to the signal source in Figure 2-7. The only difference is where you wire the shielded ground connection.

The shielded ground connection in Figure 2-7 is the most effective configuration for reducing electrically induced noise in a ground-referenced measurement. However, if connecting the shielding to the signal source ground is cumbersome or inconvenient, use the connection shown in Figure 2-8 to reduce electrically coupled noise. The shielding is grounded at only one point to the NI PXI-4204 chassis ground reference. Connect the signal (V_{SIG}+) to the NI PXI-4204 channel (AI*X*+). Connect the signal reference (V_{SIG}–) to the channel reference (AI*X*–).

The same concerns regarding the difference in ground potentials, discussed in the *Ground-Referenced Signal Connection* section, also apply to this configuration.

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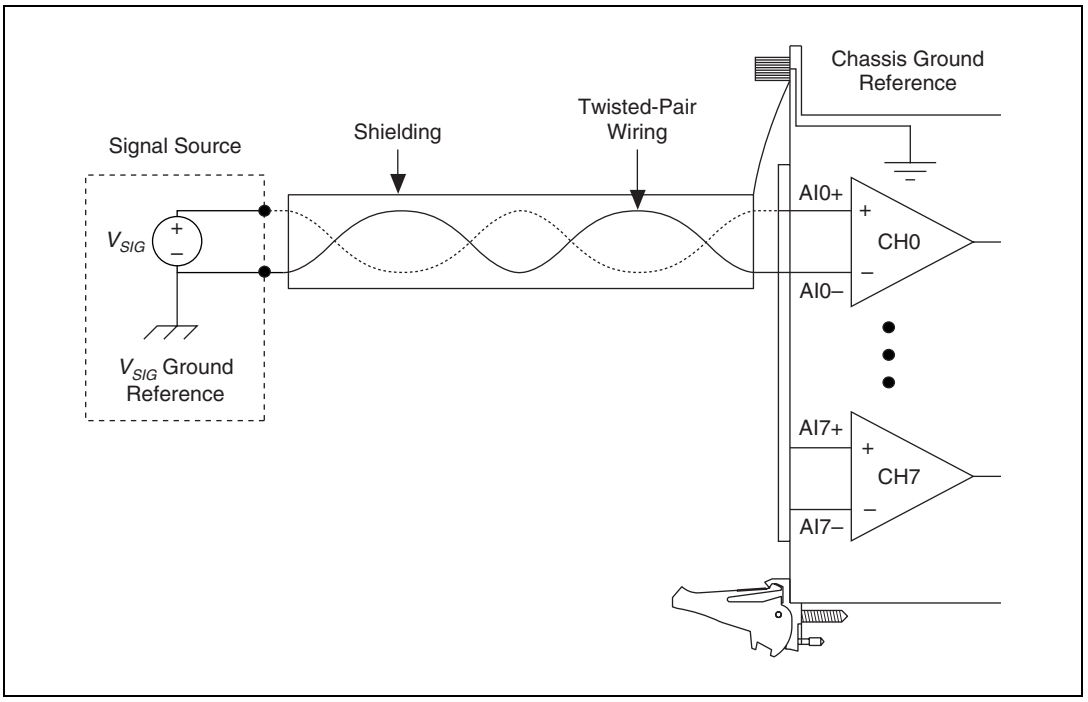


Figure 2-8. Alternative Shielded Ground Referenced Signal Connection

High CMV Connection

Figure 2-9 shows a signal source with a high CMV present. With this configuration, the signal rides on an offset voltage called the CMV. The CMV is not of interest to the measurement and can appear as an error in the voltage measurement. This type of connection can be treated as a ground-referenced signal source with a large difference between the signal source reference and the NI PXI-4204 chassis ground reference.

To connect a signal source with high CMV to the NI PXI-4204, connect the signal (V_{SIG}+) to the NI PXI-4204 channel (AI*X*+). Connect the signal reference (V_{SIG}–) to the channel reference (AI*X*–).

The balanced front end of the NI PXI-4204 rejects CMV, making it possible to measure signal sources in the presence of a large CMV. The only constraint for the NI PXI-4204 is that the combined signal and CMV must not exceed ±100 V. The maximum allowed combination of signal voltage and CMV is specified as the maximum working voltage.

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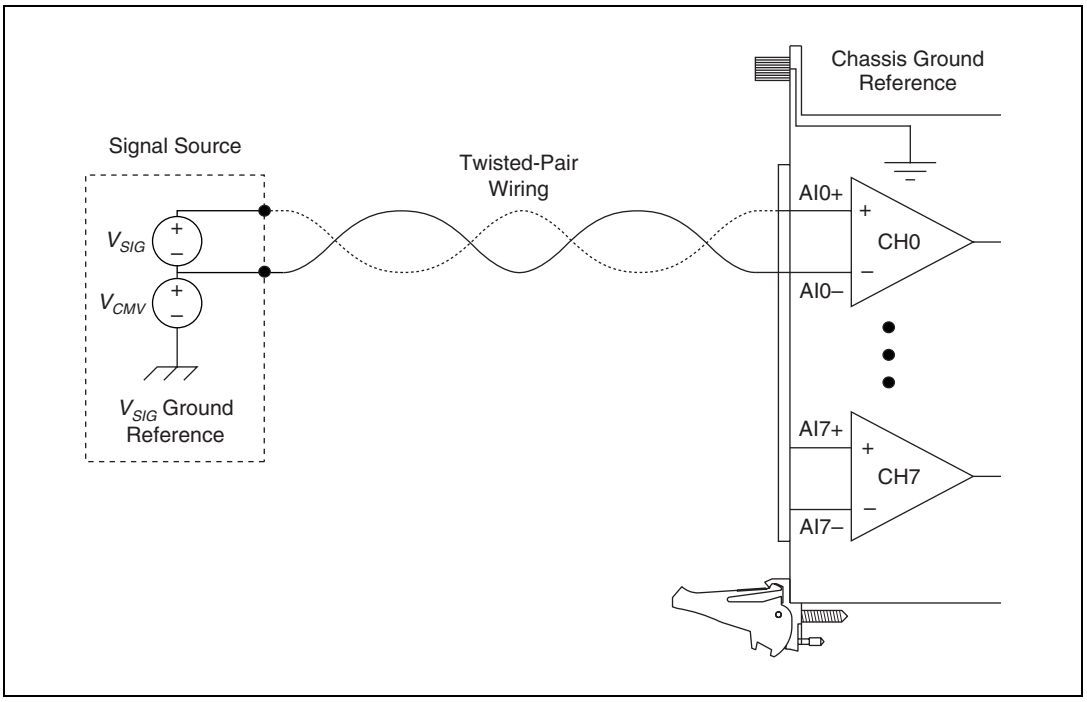


Figure 2-9. High CMV Connection

Shielded High CMV Connection

The signal source with a high CMV in Figure 2-10 is identical to the signal source in Figure 2-9. The only difference is the addition of shielding around the field wiring.

To connect a signal source with high CMV to the NI PXI-4204, connect the signal (V_{SIG}+) to the NI PXI-4204 channel (AI*X*+). Connect the signal reference (V_{SIG}–) to the channel reference (AI*X*–). The shielding is grounded at only one point to the NI PXI-4204 chassis ground reference.

This shielding scheme is effective at reducing capacitive or electrically coupled noise.

Caution If possible, ground the shielding at the NI PXI-4204, and *not* at the signal source. Grounding the shielding at the signal source in the presence of a high CMV can create a safety hazard by energizing the shield.

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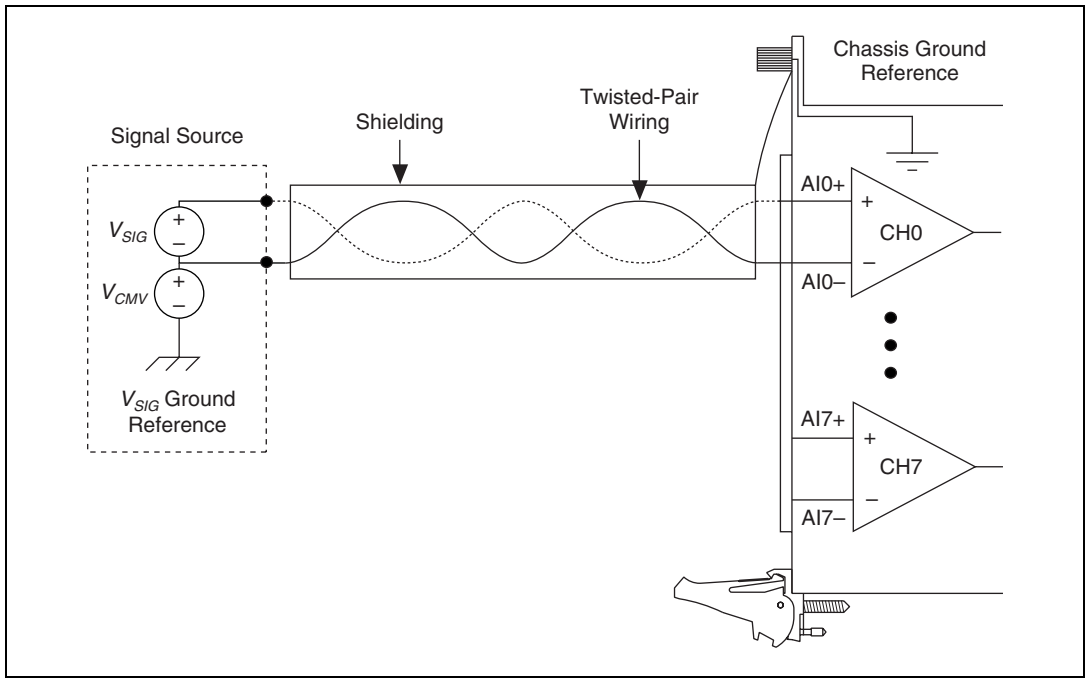


Figure 2-10. Shielded High CMV Connection

For more information about the function of the NI PXI-4204 and other measurement considerations, refer to Chapter 3, *Using the NI PXI-4204*.

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3

Using the NI PXI-4204

This chapter describes the theory of operation, measurement considerations, timing information, programming, creating program applications in LabVIEW, and calibration.

Theory of Operation

Figure 3-1 illustrates the key functional components of the NI PXI-4204, including the DAQ and integrated signal conditioning circuitry.

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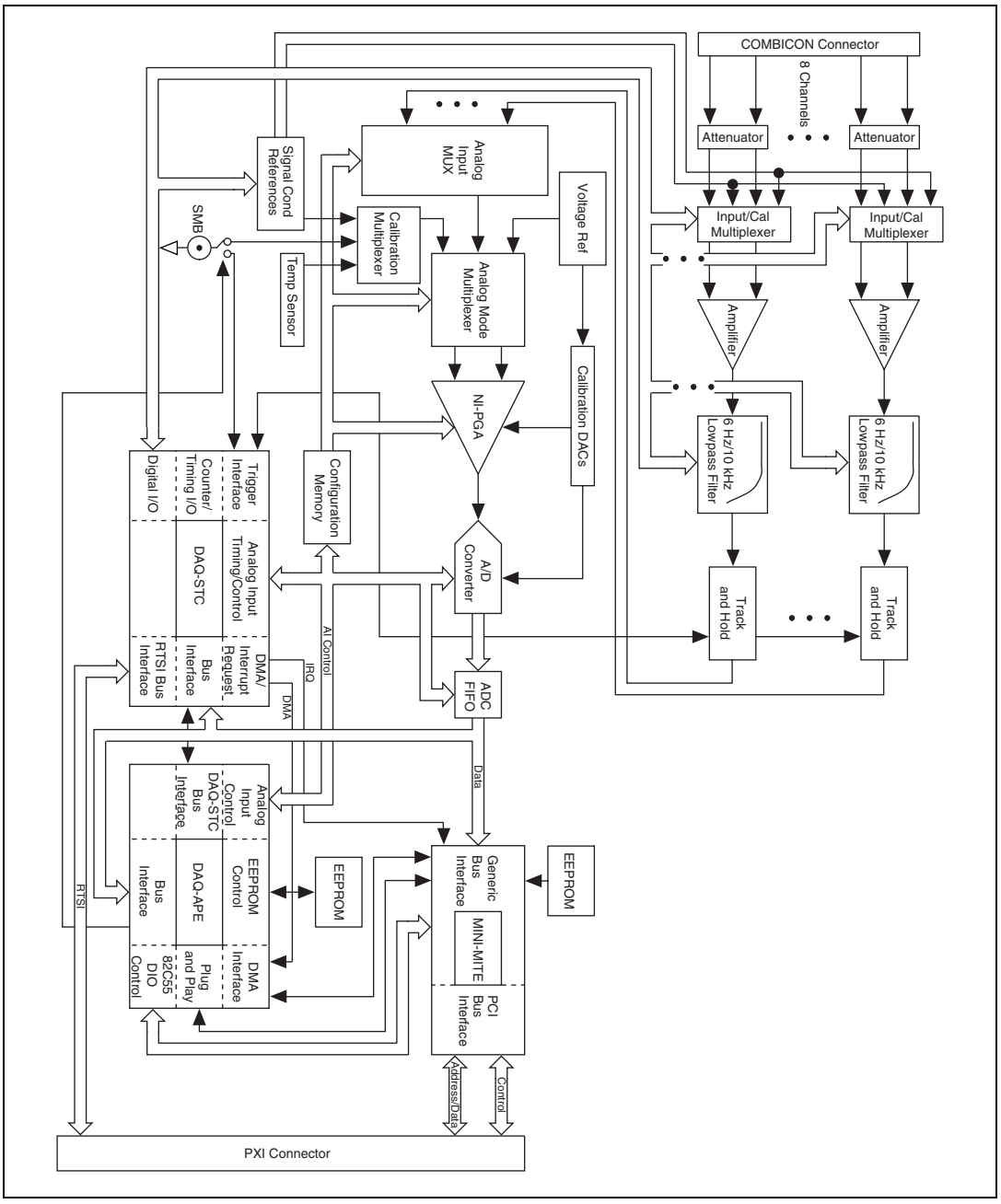


Figure 3-1. Block Diagram of NI PXI-4204

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Signal Conditioning Functional Overview

The NI PXI-4204 is part of the NI PXI-4200 series of DAQ devices designed to provide application-specific signal conditioning, DAQ, and integrated field wiring connectivity on the same product. The NI PXI-4204 signal conditioning circuitry is designed to provide attenuation, amplification, filtering, and SS/H capability as described in Table 3-1.

Table 3-1. Signal Conditioning Functional Blocks

Signal Conditioning Component	Description
Divide-by-Ten Attenuator	Each NI PXI-4204 channel front end has a balanced divide-by-ten attenuator. The attenuation is provided by a resistor-divider network that provides 1 MΩ input impedance. The balanced attenuator followed by an instrumentation amplifier provides rejection of common-mode signals and enables the NI PXI-4204 to measure voltages up to ±100 V.
Input Multiplexer	Each channel of the NI PXI-4204 includes an analog multiplexer. You can use this multiplexer to programmatically route internal test signals to the NI PXI-4204 instrumentation amplifiers for self-calibration and self-test.
Instrumentation Amplifier	The instrumentation amplifier following the attenuation stage of the NI PXI-4204 provides a very high-load impedance to the previous stage, rejection of common-mode signals, and converts differential signals to single-ended signals that are then fed to the filter stage.

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Table 3-1. Signal Conditioning Functional Blocks (Continued)

Signal Conditioning Component	Description
Lowpass Filter	The NI PXI-4204 includes a 2-pole Butterworth filter per channel with two software-selectable cutoff frequencies to reduce signal noise and improve accuracy. You can programmatically configure the filter bandwidths on a per channel basis for cutoff frequencies of 6 Hz or 10 kHz. The 6 Hz filter setting attenuates differentially connected 60 Hz signals by 40 dB.
T/H Circuitry	You can enable the NI PXI-4204 track-and-hold circuitry to enable SS/H. This allows you to acquire synchronized measurements across multiple channels. You cannot enable or disable SS/H on a per channel basis. It is disabled by default. Enabling SS/H results in slower maximum sample rates and slightly degraded accuracy. With SS/H disabled, the NI PXI-4204 uses a multiplexed architecture that enables the measurement of multiple channels using a single analog-to-digital converter (ADC). The multiplexing architecture of the NI PXI-4204 results in measurements between channels that are separated in time. The time delay between channels is determined by the sample rate at which you acquire measurements. For most low-frequency measurement applications, this time delay or phase delay is not significant.

Measurement Considerations

This section provides more information about the type of signal connection made to the NI PXI-4204 and important factors that can affect your measurement.

Differential Signals

All of the analog inputs of the NI PXI-4204 are differential. In general, a differential measurement system is preferable because it rejects not only ground loop-induced errors and common-mode voltages, but also the noise picked up in the environment to a certain degree.

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Input Impedance

Figure 3-2 illustrates the input impedance of an NI PXI-4204 and its effect on the measurement of a circuit under test. If you know the source impedance of the circuit under test, you can correct for the attenuation caused by the NI PXI-4204 in software. Since R_{IN} is relatively large, 1 MΩ, it requires a large source impedance, R_S, to cause a significant change in the measured voltage, V_{MEAS}. In general, a source impedance of less than 200 Ω does not interfere with the accuracy of the measurement. For example, a 200 Ω source impedance results in a 0.02% gain error.

$$V_{MEAS} = \frac{V_{SIG} R_{IN}}{R_S + R_{IN}}$$

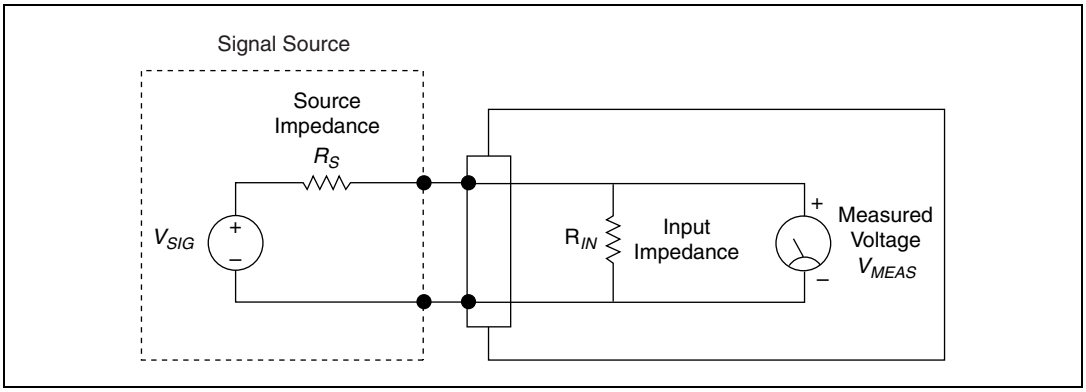


Figure 3-2. Effect of Input Impedance on Signal Measurements

Common-Mode Rejection Ratio

The ability of a measurement device to reject voltages that are common to both input terminals is referred to as the common-mode rejection ratio (CMRR) and is usually stated in decibels at a given frequency or over a given frequency band of interest. Common-mode signals can arise from a variety of sources and can be induced through conductive or radiated means. One of the most common sources of common-mode interference is due to 50 or 60 Hz powerline noise.

The minimum NI PXI-4204 CMRR is 60 dB. This results in a reduction of CMV by a factor of 1000. The measured signal source impedance can reduce the NI PXI-4204 CMR. Specifically, if the signal source has an imbalanced source impedance like the one in Figure 3-2, then an imbalance is introduced into the NI PXI-4204 front-end. This imbalance causes a reduction in the CMRR. The reduction in CMRR due to source impedance

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can be approximated by taking the ratio of the source impedance and the NI PXI-4204 input impedance, and combining it with the minimum CMRR of the NI PXI-4204.

For example, consider the following ratio of signal source and input impedance:

$$\frac{1\ \text{k}\Omega}{1\ \text{M}\Omega} = 0.001$$

Converting the NI PXI-4204 60 db CMRR specification from decibels to a ratio yields:

$$\frac{1}{10^{\frac{60}{20}}} = 0.001$$

The two terms are then added together to yield 0.002. Expressing this result in decibels yields:

$$20\log_{10}(0.002) = -54\text{dB}$$

Normal-Mode Rejection

Normal-mode rejection (NMR) refers to the ability of the NI PXI-4204 to reject a differentially (normally) applied signal when the NI PXI-4204 filters are set to 6 Hz. The NMR is a function of the lowpass filter characteristics and is quantified in the normal-mode rejection ratio (NMRR) specification, which specifies the capability of the NI PXI-4204 to reject a differentially applied unwanted 60 Hz signal. In the case of the NI PXI-4204, this specification is 40 db at 60 Hz with a 6 Hz filter setting. This NMR is usually only applicable when taking DC measurements. The NMRR is specified at the powerline frequency because this is typically where most measurement noise arises.

Effective CMR

When the frequency of a common-mode signal is known and outside of the measurement frequency band of interest, you can use an analog or digital filter, or both, to further reduce the residual error left from the finite CMRR of the instrument. The combined CMR of the instrument and the filter attenuation results in an effective CMR. When expressed in decibels, the effective CMR is equal to the sum of the CMRR and the attenuation due to the filter at a specified frequency.

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Timing and Control Functional Overview

The NI PXI-4204 is based on the NI E Series DAQ device architecture. This architecture uses the NI data acquisition system timing controller (DAQ-STC) for time-related functions. The DAQ-STC consists of two timing groups that control AI and general-purpose counter/timer functions. These groups include a total of seven 24-bit and three 16-bit counters and a maximum timing resolution of 50 ns. The DAQ-STC makes possible applications such as equivalent time sampling, and seamless changing of the sampling rate.

The NI PXI-4204 uses the PXI trigger bus to easily synchronize several measurement functions to a common trigger or timing event. The PXI trigger bus is connected through the rear signal connector to the PXI chassis backplane. The DAQ-STC provides a flexible interface for connecting timing signals to other devices or external circuitry. The NI PXI-4204 uses the PXI trigger bus to interconnect timing signals between PXI devices and the programmable function input (PFI) pin on the front SMB connector to connect the device to external circuitry. These connections are designed to enable the device to both control and be controlled by other devices and circuits.

The DAQ-STC has internal timing signals you can control by an external source. These timing signals also can be controlled by signals internally generated to the DAQ-STC, and these selections are software configurable. Figure 3-3 shows an example of the signal routing multiplexer controlling the AI CONV CLK signal.

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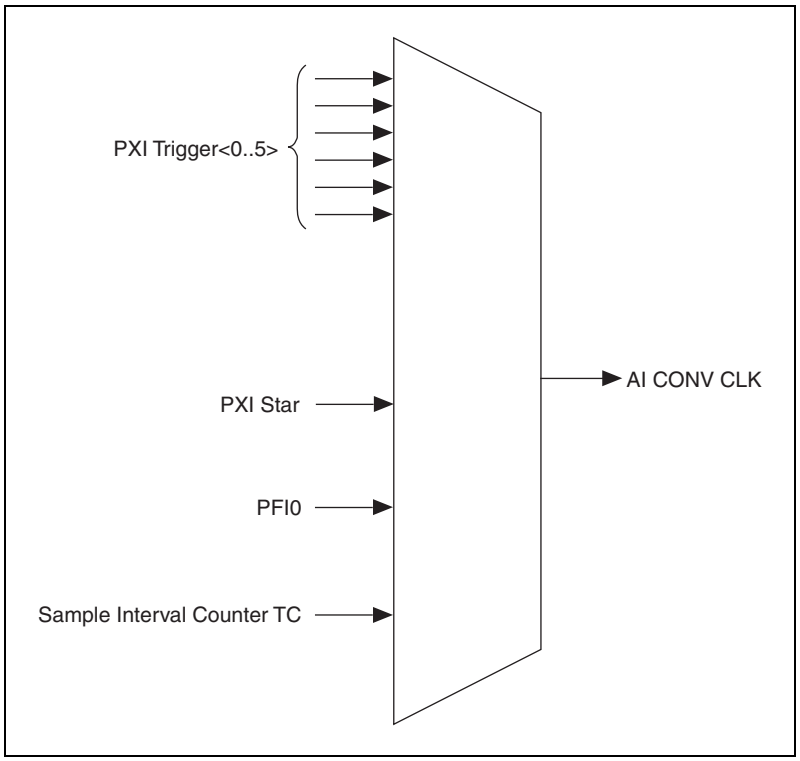


Figure 3-3. AI CONV CLK Signal Routing

Figure 3-3 shows that AI CONV CLK can be generated from a number of sources, such as the external signals PFI0, PXI_Trig<0..5>, and PXI Star, and the internal signals sample interval (SI2) counter TC.

Programmable Function Inputs

PFI0 is connected to the front SMB connector of the NI PXI-4204. Software can select PFI0 as the external source for a given timing signal. Any timing signal can use the PFI0 pin as an input, and multiple timing signals can simultaneously use the same PFI. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications. You can enable PFI0 to output the AI START TRIG signal.

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Device and PXI Clocks

Many functions performed by the NI PXI-4204 require a frequency timebase to generate the necessary timing signals for controlling A/D conversions, digital-to-analog converter (DAC) updates, or general-purpose signals at the I/O connector.

The NI PXI-4204 can use either its internal 20 MHz master timebase or a timebase received over the PXI trigger bus on the PXI clock line. This timebase is software configurable. If you configure the device to use the internal timebase, you can program the device to drive its internal timebase over the PXI trigger bus to another device programmed to receive this timebase signal. This clock source, whether local or from the PXI trigger bus, is used directly by the device as the primary frequency source. The default configuration is to use the internal timebase without driving the PXI trigger bus timebase signal. The NI PXI-4204 can use the PXI_Trig 7 line to synchronize `Master Timebase` with other devices.

For the NI PXI-4204, PXI Trig<0..5> and PXI Star connect through the NI PXI-4204 backplane. The PXI Star Trigger line allows the NI PXI-4204 to receive triggers from any Star Trigger controller plugged into slot 2 of the chassis. The NI PXI-4204 can only receive signals on the PXI Star Trigger line. For more information about the Star Trigger, refer to the *PXI Hardware Specification, Revision 2.1* and *PXI Software Specification, Revision 2.1*.

Figure 3-4 shows this signal connection scheme.

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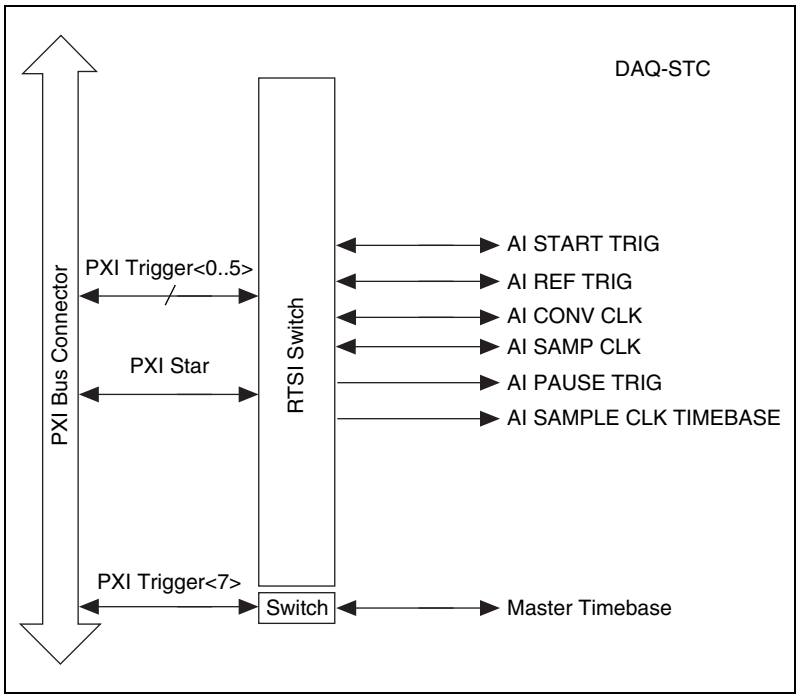


Figure 3-4. NI PXI-4204 PXI Trigger Bus Signal Connection

Table 3-2 provides more information about each of the timing signals available on the PXI trigger bus. For more detailed timing signal information, refer to Appendix B, *Timing Signal Information*.

Table 3-2. PXI Trigger Bus Timing Signals

Signal	Direction	Description	Availability on PFI0 SMB	Availability on PXI Trigger Bus
AI START TRIG	Input	This is the source for the analog input digital start trigger, the trigger that begins an acquisition.	Input	Input
	Output	This sends out the actual analog input start trigger.	Output	Output
AI REF TRIG	Input	This is the trigger that creates the reference point between the pretrigger samples and the posttrigger samples.	Input	Input
	Output			Output

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Table 3-2. PXI Trigger Bus Timing Signals (Continued)

Signal	Direction	Description	Availability on PFI0 SMB	Availability on PXI Trigger Bus
AI SAMP CLK	Input Output	This clock controls the time interval between samples. Each time the sample clock produces a pulse, one sample per channel is acquired.	Input	Input Output
AI CONV CLK	Input Output	This clock directly causes analog-to-digital conversions.	Input	Input Output
AI PAUSE TRIG	Input	This signal can pause and resume acquisition.	Input	Input
AI SAMPLE CLK TIMEBASE	Input	This timebase provides the master clock from which the sample clocks are derived.	Input	Input

Developing Your Application

This section describes the software and programming steps necessary to use the NI PXI-4204. For more information about a particular software or programming process, refer to your ADE documentation.

Typical Program Flow Chart

Figure 3-5 shows a typical program flow chart for creating an AI voltage channel, taking a measurement, and clearing the data.

Note Many example programs ship with NI-DAQmx. For more information about how to create tasks and channels, refer to the example programs.

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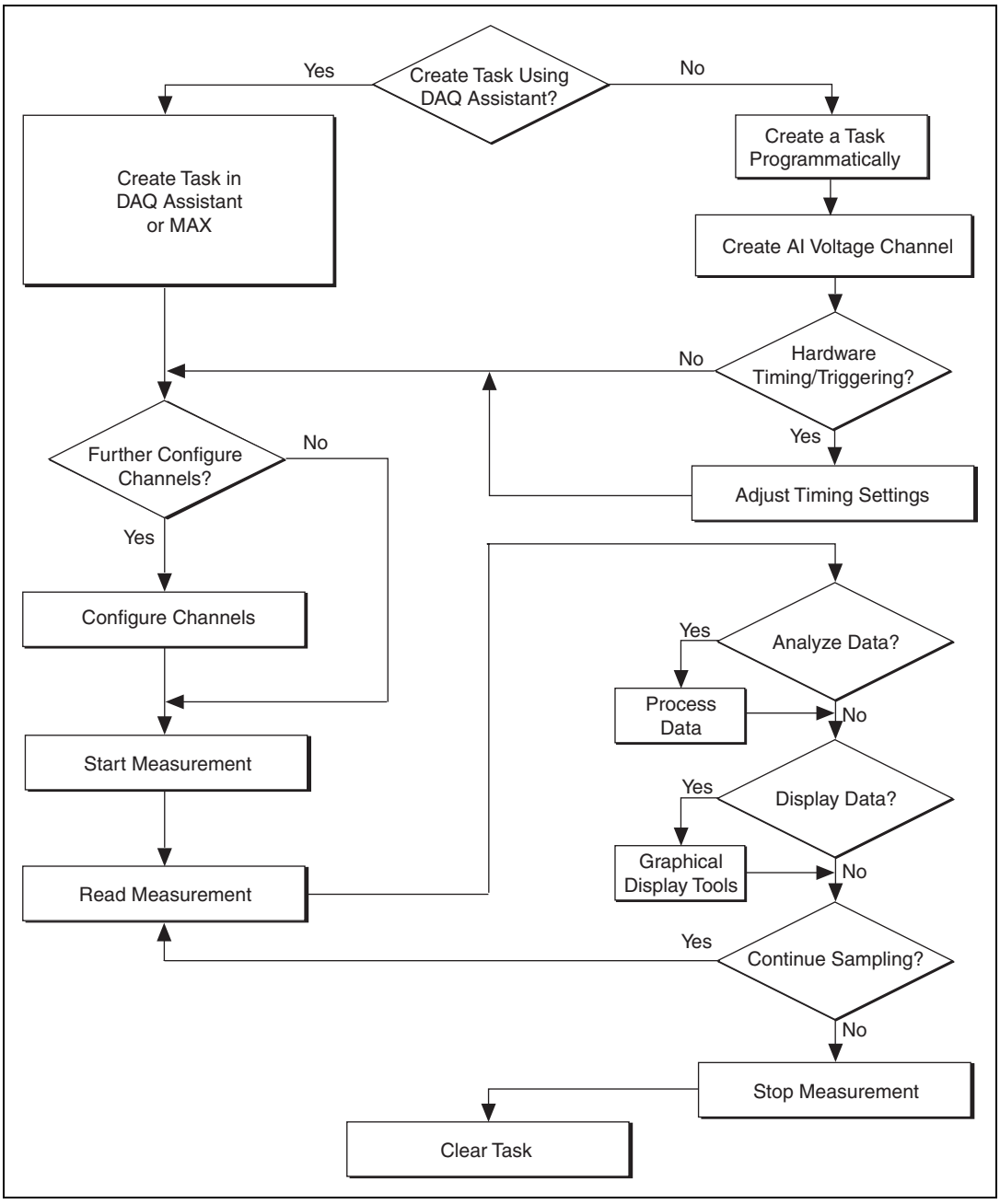


Figure 3-5. Typical Program Flowchart

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General Discussion of Typical Flow Chart

The following sections briefly discuss some considerations for a few of the steps in Figure 3-5. The purpose of these sections is to provide an overview of some of the options and features available when programming with NI-DAQmx.

Creating a Task Using DAQ Assistant or Programmatically

When creating an application, you must first decide whether to create the appropriate task using the DAQ Assistant or programmatically in the ADE.

Developing your application using NI-DAQmx gives you the ability to configure most settings, such as measurement type, selection of channels, input limits, task timing, and task triggering using the DAQ Assistant tool. You can access the DAQ Assistant either through MAX or through your NI ADE. Choosing to use the DAQ Assistant can simplify the development of your application. NI recommends creating tasks using the DAQ Assistant for ease of use, when using a sensor that requires complex scaling, or when many properties differ between channels in the same task.

If you are using an ADE other than an NI ADE, or if you want to explicitly create and configure a task for a certain type of acquisition, you can programmatically create the task from your ADE using function or VI calls. If you create a task using the DAQ Assistant, you can still further configure the individual properties of the task programmatically using function calls or property nodes in your ADE. NI recommends creating a task programmatically if you need explicit control of programmatically adjustable properties of the DAQ system. Programmatically creating tasks is also recommended if you are synchronizing multiple devices using master and slave tasks. Refer to the *Synchronizing the NI PXI-4204* section for more information about synchronizing multiple NI PXI-4204 devices.

Programmatically adjusting properties for a task created in the DAQ Assistant overrides the original settings only for that session. The changes are *not* saved to the task configuration. The next time you load the task, the task uses the settings originally configured in the DAQ Assistant.

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Adjusting Timing and Triggering

There are several timing properties that you can configure either through the DAQ Assistant or programmatically using function calls or property nodes in your application. If you create a task in the DAQ Assistant, you still can modify the timing properties of the task programmatically in your application.

When programmatically adjusting timing settings, you can set the task to acquire continuously, acquire a buffer of samples, or acquire one point at a time. For continuous and buffered acquisitions, you can set the acquisition rate and the number of samples to read. By default, the clock settings are automatically set by an internal clock based on the requested sample rate. You also can select advanced features, such as clock settings, that specify an external clock source, internal routing of the clock source, or select the active edge of the clock signal.

Configuring Channel Properties

All of the different ADEs used to configure the NI PXI-4204 access an underlying set of NI-DAQmx properties. Table 3-3 lists some of the properties that configure the NI PXI-4204. You can use this list to determine what kinds of properties you need to set to configure the device for your application. If you created the task and channels using the DAQ Assistant, you can still modify the channel properties programmatically. For a complete list of NI-DAQmx properties, refer to your ADE help file.

Table 3-3. NI-DAQmx Properties

Property	Short Name	Description
Analog Input» General Properties» Input Configuration» Coupling Property	`AI.Coupling`	DC—Allows NI-DAQmx to measure the input signal. GND—Removes the signal source from the measurement and measures only ground.
Analog Input»General Properties»Filter»Analog Lowpass»Cutoff Frequency	`AI.Lowpass.CutoffFreq`	Specifies in hertz the frequency corresponding to the –3 dB cutoff of the filter. You can specify either 6.0 or 10000.0.

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Table 3-3. NI-DAQmx Properties (Continued)

Property	Short Name	Description
Analog Input»General Properties»Advanced» Sample and Hold Enable	`AI.SampAndHold.Enable`	Specifies whether to enable the sample and hold circuitry of the device.
Analog Input»General Properties»Advanced» High Accuracy Settings» Auto Zero Mode	`AI.AutoZeroMode`	Specifies when to measure ground. NI-DAQmx subtracts the measured ground voltage from every sample.

Note This is *not* a complete list of NI-DAQmx properties. It is a representative sample of important properties you can adjust in analog input measurements with the NI PXI-4204. For a complete list of NI-DAQmx properties and more information about NI-DAQmx properties, refer to your ADE help file.

Acquiring, Analyzing, and Presenting

After configuring the task and channels, you can start your acquisition, read measurements, analyze the data returned, and display it according to the needs of your application. Typical methods of analysis include digital filtering, averaging data, performing harmonic analysis, applying a custom scale, or adjusting measurements mathematically.

NI provides powerful analysis toolsets for each NI ADE to help you perform advanced analysis on the data without requiring a programming background. After you acquire the data and perform any required analysis, it is useful to display the data in a graphical form or log it to a file. NI ADEs provide easy-to-use tools for graphical display, such as charts, graphs, slide rules, and gauge indicators. NI ADEs have tools that allow you to save the data to files such as spread sheets for easy viewing, ASCII files for universality, or binary files for smaller file sizes.

Completing the Application

After you have completed the measurement, analysis, and presentation of the data, it is important to stop and clear the task. This releases any memory used by the task and frees up the DAQ hardware for use in another task.

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Developing an Application Using LabVIEW

This section describes in more detail the steps shown in the typical program flowchart in Figure 3-5, such as how to create a task in LabVIEW and configure the channels of the NI PXI-4204. For more information or further instructions, select **Help»VI, Function, & How-To Help** from the LabVIEW menu bar.

Note Except where otherwise stated, the VIs in Table 3-4 are located on the **Functions» All Functions»NI Measurements»DAQmx - Data Acquisition** subpalette and accompanying subpalettes in the default LabVIEW palette view.

Table 3-4. Programming a Task in LabVIEW

Flowchart Step	VI or Program Step
Create Task in DAQ Assistant	Create a `DAQmx Task Name Constant` located on the **Controls»All Controls»I/O»DAQmx Name Controls** subpalette, right-click it, and select `New Task (DAQ Assistant)`.
Create a Task Programmatically (optional)	`DAQmx Create Task.vi`—This VI is optional if you created and configured your task using the DAQ Assistant. However, if you use it in LabVIEW, any changes you make to the task will not be saved to a task in MAX.
Create AI Voltage Channel (optional)	`DAQmx Create Virtual Channel.vi` (AI Voltage by default)—This VI is optional if you created and configured your task and channels using the DAQ Assistant.
Adjust Timing Settings (optional)	`DAQmx Timing.vi` (Sample Clock by default)—This VI is optional if you created and configured your task using the DAQ Assistant.
Configure Channels (optional)	DAQmx Channel Property Node—Refer to the *Using a DAQmx Channel Property Node in LabVIEW* section for more information. This step is optional if you created and fully configured the channels in your task using the DAQ Assistant.
Start Measurement	`DAQmx Start Task.vi`
Read Measurement	`DAQmx Read.vi`

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Table 3-4. Programming a Task in LabVIEW (Continued)

Flowchart Step	VI or Program Step
Analyze Data	Some examples of data analysis include filtering, scaling, harmonic analysis, and level checking. Some data analysis tools are located on the **Functions»Signal Analysis** subpalette and on the **Functions»All Functions»Analyze** subpalette.
Display Data	You can use graphical tools, such as charts, gauges, and graphs to display your data. Some display tools are located on the **Controls»Numeric Indicators** subpalette and **Controls» All Controls»Graph** subpalette.
Continue Sampling	For continuous sampling, use a While Loop. If you are using hardware timing, you also need to set the `DAQmx Timing.vi` sample mode to Continuous Samples. To do this, right-click the terminal of the `DAQmx Timing.vi` labeled **sample mode** and click **Create»Constant**. Click the box that appears and select **Continuous Samples**.
Stop Measurement	`DAQmx Stop Task.vi`—This VI is optional. Clearing the task will automatically stop the task.
Clear Task	`DAQmx Clear Task.vi`

Using a DAQmx Channel Property Node in LabVIEW

Note With the NI PXI-4204, you must use property nodes to change filter settings and to enable SS/H.

You can use property nodes in LabVIEW to manually configure your channels. To create a LabVIEW property node, complete the following steps:

1. Launch LabVIEW.
2. You can create the property node in a new VI or in an existing VI.
3. Open the block diagram view.
4. From the **All Functions** toolbox, select **All Functions» NI Measurements»DAQmx - Data Acquisition**, and select `DAQmx Channel Property Node`.

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5. Left-click inside the box labeled **Property** and select **Active Channels**. This allows you to specify exactly what channel(s) you want to configure. If you want to configure several channels with different properties, separate the lists of properties with another **Active Channels** box and assign the appropriate channel to each list of properties.

Note If you do not use Active Channels, the properties will be set on all of the channels in the task.

6. Right-click **ActiveChan** and select **Add Element**. Left-click the new **ActiveChan** box and select **Properties**. Navigate through the menus and select the property you wish to define.
7. To either get the property or write a new value, you must change the property to read or write. Right-click the property, select **Change To**, and select **Write**, **Read**, or **Default Value**.
8. Once you have added the property to the property node, right-click the terminal to change the attributes of the property, or to add a control, constant, or indicator.

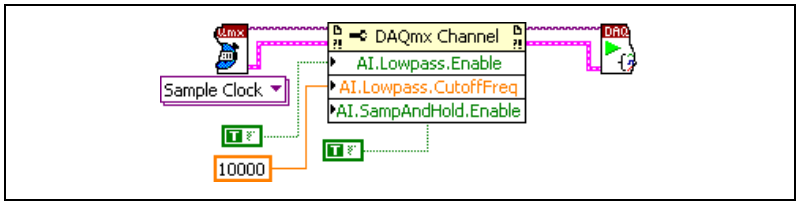


Figure 3-6. LabVIEW Channel Property Node with Filtering Enabled at 10 kHz and SS/H Enabled

9. To add another property to the property node, right-click an existing property and left-click **Add Element**. To change the new property, left-click it and select the property you wish to define.

Note Refer to the *LabVIEW Help* for information about property nodes and specific NI-DAQmx properties.

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Synchronization and Triggering

If you have multiple NI PXI-4204 devices, you can synchronize them to acquire samples at the same time and at the same rate. With SS/H enabled, and each device synchronized, you can use multiple NI PXI-4204 devices to acquire and analyze complex signals.

Note The phase difference is lower between channels on the same device with SS/H than between channels on different devices.

For multiple NI PXI-4204 devices to start an acquisition simultaneously, they all must reference a common start trigger. To prevent drift over the course of the acquisition, they must share a common timebase or sample clock.

The NI PXI-4204 that generates the start trigger and the timebase for all of the synchronized devices is called the master. The master NI PXI-4204 exports the shared timing signals through the PXI bus to the slave devices.

Each NI PXI-4204 contains a DAQ-STC chip and is capable of generating a hardware sample clock based on its timebase clock and start trigger. When using a shared timebase and start trigger, each slave NI PXI-4204 still generates a hardware sample clock, but it generates the clock using the timebase and start trigger of the master NI PXI-4204. This causes the slave device to acquire samples at the same time as the master.

The preferred method of synchronization is to use a shared timebase, but it is also possible to synchronize multiple NI PXI-4204 devices by sharing the sample clock between them. This manual only discusses the shared timebase method.

Synchronizing the NI PXI-4204

Figure 3-7 shows a typical program flow chart for synchronizing the sample clocks and start triggers of two devices, taking a measurement, and clearing the data.

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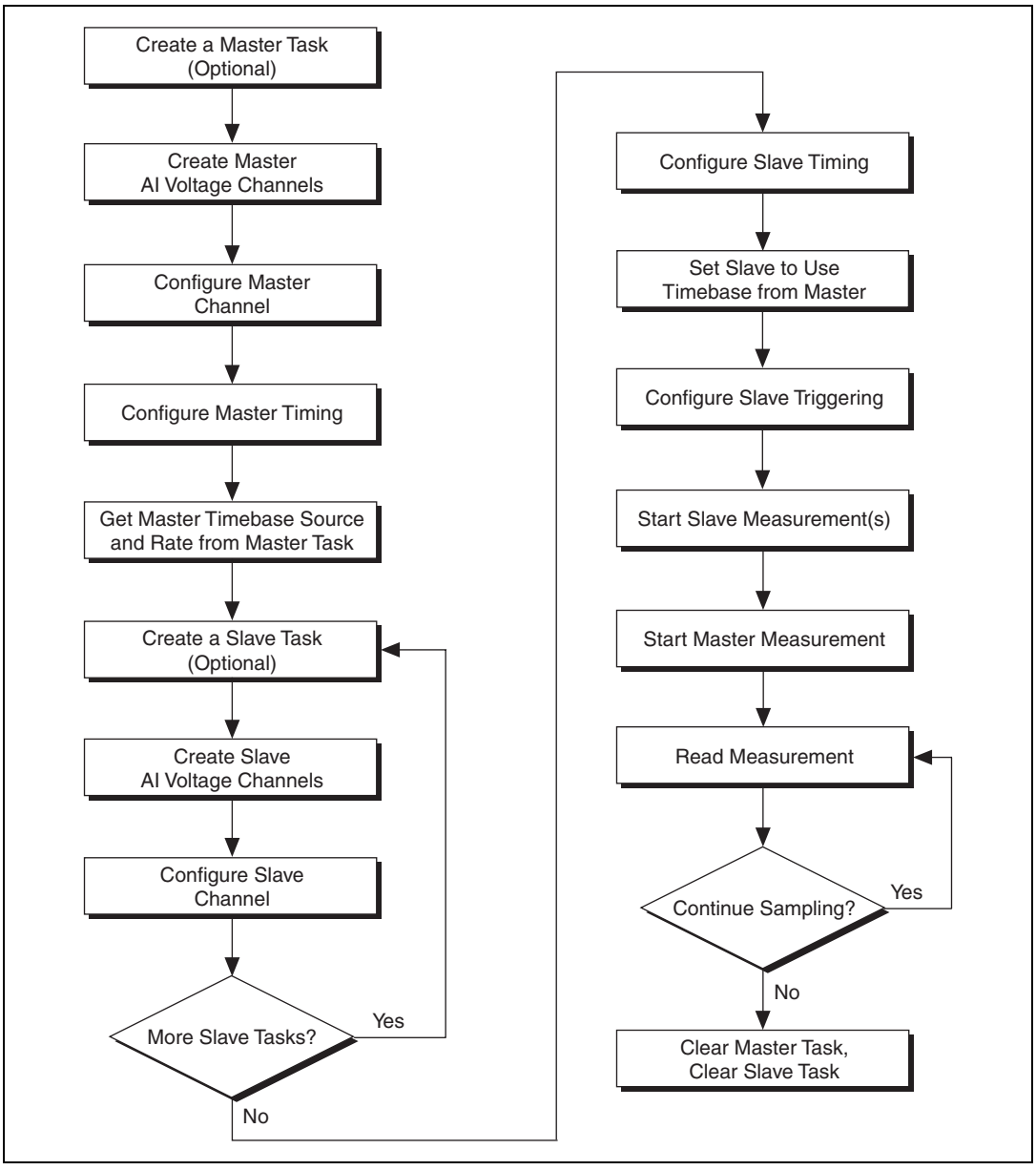


Figure 3-7. General Synchronizing Flowchart

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Synchronizing the NI PXI-4204 Using LabVIEW

This section describes in more detail the steps shown in the general synchronizing flowchart in Figure 3-7. For more information, or for further instructions, select **Help»VI, Function, & How-To Help** from the LabVIEW menu bar.

Note Except where otherwise stated, the VIs in Table 3-5 are located on the **Functions» All Functions»NI Measurements»DAQmx - Data Acquisition** subpalette and accompanying subpalettes in LabVIEW.

Table 3-5. Synchronizing the NI PXI-4204 Using LabVIEW

Flowchart Step	VI or Program Step
Create a Master Task (optional)	`DAQmx Create Task.vi`
Create Master AI Voltage Channels	`DAQmx Create Virtual Channel.vi` (AI Voltage by default)
Configure Master Channels	Use a DAQmx Channel Property Node, refer to the *Using a DAQmx Channel Property Node in LabVIEW* section for more information.
Configure Master Timing	`DAQmx Timing.vi` (Sample Clock by default)
Get Master Timebase Source and Rate from Master Task	Use a DAQmx Timing Property Node to get `MasterTimebase.Src` and `MasterTimebase.Rate`.
Create a Slave Task (optional)	`DAQmx CreateTask.vi` This VI is optional if you created and configured your task using the DAQ Assistant. However, if you use it in LabVIEW any changes you make to the task will not be saved to a task in MAX.
Create Slave AI Voltage Channels	`DAQmx Create Virtual Channel.vi` (AI Voltage by default)
Configure Slave Channels	DAQmx Channel Property Node, refer to the *Using a DAQmx Channel Property Node in LabVIEW* section for more information.
Configure Slave Timing	`DAQmx Timing.vi` (Sample Clock by default)
Set Slave to Use Timebase from Master	Use a DAQmx Timing Property Node to set `MasterTimebase.Src` and `MasterTimebase.Rate` to the values retrieved from the master task in the *Get Master Timebase Source and Rate from Master Task* step.

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Table 3-5. Synchronizing the NI PXI-4204 Using LabVIEW (Continued)

Flowchart Step	VI or Program Step
Configure Slave Triggering	`DAQmx Trigger.vi` (Start Digital Edge) use `/MasterDevice/ai/StartTrigger` as the source, substituting the master device identifier for `MasterDevice`.
Start Slave Measurement(s)	`DAQmx Start Task.vi`
Start Master Measurement	`DAQmx Start Task.vi`
Read Measurement	`DAQmx Read.vi`
Continue Sampling	For continuous sampling, use a While Loop. You also need to have set the sample mode to **Continuous Samples** in the *Configure Master Timing* and *Configure Slave Timing* steps. To do this, right-click the terminal of the `DAQmx Timing.vi` labeled **sample mode** and click **Create»Constant**. Click the box that appears and select **Continuous Samples**.
Clear Master Task	`DAQmx Clear Task.vi`
Clear Slave Task	`DAQmx Clear Task.vi`

Other Application Documentation and Material

The following locations provide more information that you may find useful when setting up or connecting signal sources or programming your application.

- LabVIEW Example Programs, available by selecting **Open» Examples** from the opening screen. Most of the examples applicable to the NI PXI-4204 are located in **Hardware Input and Output» DAQmx»Analog Measurements** and **Hardware Input and Output»DAQmx»Synchronization»Multi-Device**.
- *PXI-4204 Supported Properties* in the LabVIEW *VI, Function, & How-To Help*.
- Application Note 025: *Field Wiring and Noise Considerations for Analog Signals* available at `ni.com`. Go to `ni.com/info` and enter the info code `rdfwn3`.

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Calibrating the NI PXI-4204

Calibration refers to the process of minimizing measurement errors. On the NI PXI-4204, errors from the digitizer components of the DAQ device circuitry are corrected in the analog circuitry by onboard calibration digital-to-analog converters (CalDACs). Errors from the signal conditioning circuitry are corrected in software.

Three levels of calibration are available for the NI PXI-4204 to ensure the accuracy of its analog circuitry. The first level, loading calibration constants, is the fastest, easiest, and least accurate. The NI PXI-4204 automatically loads calibration constants stored in flash memory when powered on. The intermediate level, internal calibration, is the preferred method of assuring accuracy in your application. The last level, external calibration, is the slowest, most difficult, and most accurate.

Loading Calibration Constants

The NI PXI-4204 is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants (the values that were written to the CalDACs to achieve calibration in the factory and the remaining signal conditioning error) are stored in the onboard nonvolatile flash memory. The digitizer calibration constants are automatically read from the flash memory and loaded into the CalDACs by the NI PXI-4204 hardware the next time the device is powered on. The signal conditioning calibration constants are also read from the flash memory at this time.

Self-Calibration

The NI PXI-4204 can measure and correct for most of its calibration-related errors without any external signal connections. This calibration method is referred to as internal calibration or self-calibration. This internal calibration process, which generally takes less than two minutes, is the preferred method of assuring accuracy in your application. Initiate an internal calibration to minimize the effects of any offset and gain drifts, particularly those due to changes in temperature. During the internal calibration process, the AI channels are compared to the NI PXI-4204 onboard voltage reference. The majority of the offset and gain errors in the analog circuitry are compensated for by adjusting the CalDACs to minimize these errors. To perform a self-calibration, complete the following steps:

1. Double-click the **Measurement & Automation Explorer** icon on the desktop.

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2. Display the list of devices and interfaces by clicking the **+** next to the **Devices and Interfaces** icon.
3. Display the list of NI-DAQmx devices by clicking the **+** next to **NI-DAQmx Devices** icon.
4. Right-click the NI PXI-4204 and select **Self-Calibrate**.
5. A dialog box appears indicating that the NI PXI-4204 is self-calibrating.
6. When the dialog box disappears, the NI PXI-4204 is successfully self-calibrated.

Note The NI PXI-4204 also can be self-calibrated programmatically by using `DAQmx Self Calibrate.vi` in LabVIEW.

The results of an internal calibration are stored in the NI PXI-4204 flash memory so that the CalDACs are automatically loaded with the newly calculated calibration constants the next time the NI PXI-4204 is powered on.

Performing a self-calibration at the operating temperature of your application will ensure the NI PXI-4204 meets the specifications in Appendix A, *Specifications*.

External Calibration

The NI PXI-4204 has an onboard calibration reference for the DAQ circuitry and the signal conditioning circuitry to ensure the accuracy of self-calibration. The specifications are listed in Appendix A, *Specifications*. The reference voltages are measured at the factory and stored for subsequent internal calibrations. The voltages are stable enough for most applications, but if you are using the device at an extreme temperature or if the onboard references have not been measured for a year or more, you may want to externally calibrate the device. *NI recommends an external calibration of the NI PXI-4204 once a year.*

An external calibration refers to calibrating the device with a known external reference rather than relying on the onboard references. During the external calibration process, the onboard reference values are re-calculated. This compensates for any time or temperature drift related errors in the onboard references, which may have resulted since the last calibration. You can save the results of the external calibration process so that the new calibration constants are automatically loaded the next time the NI PXI-4204 is powered on. The NI PXI-4204 then uses the newly measured onboard references for subsequent internal calibrations.

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A

Specifications

This appendix lists the specifications for the NI PXI-4204 device. These specifications are typical at 25 °C unless otherwise noted. All specifications are with SS/H disabled unless otherwise noted.

Analog Input

Number of input channels 8

Input range ..... ±100 V

Resolution ..... 16 bits

Maximum sampling rate ..... 200 kS/s aggregate multichannel

Table A-1. Maximum Sampling Rates

Number of Channels	SS/H Disabled	SS/H Enabled
1	333 kS/s/ch	100.0 kS/s/ch
2	100.0 kS/s/ch	66.6 kS/s/ch
3	66.6 kS/s/ch	50.0 kS/s/ch
4	50.0 kS/s/ch	40.0 kS/s/ch
5	40.0 kS/s/ch	33.3 kS/s/ch
6	33.3 kS/s/ch	28.5 kS/s/ch
7	28.5 kS/s/ch	25.0 kS/s/ch
8	25.0 kS/s/ch	22.2 kS/s/ch

Input coupling ..... DC

Bandwidth ..... 6 Hz or 10 kHz 2-pole lowpass Butterworth filter response

Differential input impedance ..... 2 MΩ

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Single-ended input impedance.....1 MΩ

Offset error
temperature coefficient .....±3530 µV/°C max

Remaining offset error temperature
coefficient after self-calibration .....±385 µV/°C max

Gain error temperature coefficient.....±32 ppm/°C

Remaining gain error temperature
coefficient after self-calibration .....±25 ppm/°C

CMRR

DC to 60 Hz.....>60 dB

100 Hz to 10 kHz.....>40 dB

Normal mode 60 Hz rejection
(6 Hz filter setting) .....40 dB

Crosstalk at 1 kHz

Adjacent channels.....–75 dB

All other channels.....–90 dB

FIFO buffer size.....512 samples

Data transfers.....DMA, interrupts,
programmed I/O

DMA modes .....Scatter-gather (single transfer,
demand transfer)

Configuration memory size .....512 words

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NI PXI-4204 Accuracy Information with SS/H Disabled

Nominal Range (V)		Absolute Accuracy						Absolute Accuracy at Full Scale (mV)
		% of Reading		Offset (mV)	Noise + Quantization (mV)		Temp Drift (%/°C)	
Positive FS	Negative FS	24 Hours	1 Year		Single Pt.	Avg.		
100	–100	0.063	0.070	±16.8	±9.34	±0.92	0.0027	88
50	–50	0.031	0.038	±10.4	±4.68	±0.57	0.0025	30
5	–5	0.061	0.068	±4.7	±0.69	±0.40	0.0027	8.5
0.5	–0.5	0.061	0.068	±4.1	±0.49	±0.40	0.0027	4.8

Accuracies are valid for measurements following an internal self-calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings.

Measurement accuracies are listed for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or factory calibration temperature.

NI PXI-4204 Accuracy Information with SS/H Enabled

Nominal Range (V)		Absolute Accuracy						Absolute Accuracy at Full Scale (mV)
		% of Reading		Offset (mV)	Noise + Quantization (mV)		Temp Drift (%/°C)	
Positive FS	Negative FS	24 Hours	1 Year		Single Pt.	Avg.		
100	–100	0.085	0.090	±19.0	±9.35	±1.02	0.0027	110
50	–50	0.035	0.042	±12.6	±4.70	±0.73	0.0025	34
5	–5	0.063	0.070	±6.8	±0.82	±0.60	0.0027	11
0.5	–0.5	0.063	0.070	±6.3	±0.66	±0.60	0.0027	7.2

Accuracies are valid for measurements following an internal self-calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings.

Measurement accuracies are listed for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or factory calibration temperature.

SS/H Characteristics

Droop rate ..... <0.4 mV/ms

Hold mode settle time ..... 3 µs min

Acquisition time ..... 7 µs min

Hold step ..... 20 mV[1]

[1] The 20 mV hold step error is calibrated out during an external calibration.

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Transfer Characteristics

Nonlinearity

- ±100 V range .....0.02% typ
- Other ranges.....0.01% typ
- SS/H enabled, ±100 V range .....0.06% typ
- SS/H enabled, other ranges.....0.02% typ

DNL .....±0.5 LSB typ, ±1 LSB max

No missing codes.....16 bits, guaranteed

Calibration

Recommended warm-up time.....15 minutes

External calibration interval .....1 year

Onboard calibration reference

- Level.....5.000 V ±1 mV (actual value stored in EEPROM)
- TC.....±5 ppm/°C
- Long-term stability .....±15 ppm/ $\sqrt{1000h}$

Pre-calibration Errors[1]

Pre-calibration offset error relative to input (RTI).....865 mV max

- Signal conditioning component only .....±50mV typ, ±160 mV max

Pre-calibration gain error.....±18900 ppm max

- Signal conditioning component only .....±600 ppm typ, ±1000 ppm max

[1] The pre-calibration errors apply only for users doing register level programming. NI-DAQmx users do not see the pre-calibration errors.

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Digital Triggers

Number of triggers 2

Purpose ..... Start and stop trigger, gate, clock

Source ..... PFI0/AI START TRIG (front SMB connector), PXI_Trig<0..5> to PXI Star (PXI trigger bus)

Compatibility ..... 5 V/TTL

Response ..... Rising or falling edge

Pulse width ..... 10 ns min

Impedance ..... 10 kΩ

Coupling ..... DC

PXI Trigger Bus

Trigger lines 6

Star trigger ..... 1, input only

PCI Bus Interface

Master, slave

Power Requirements

1 A at +5 V (±5%)

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Physical

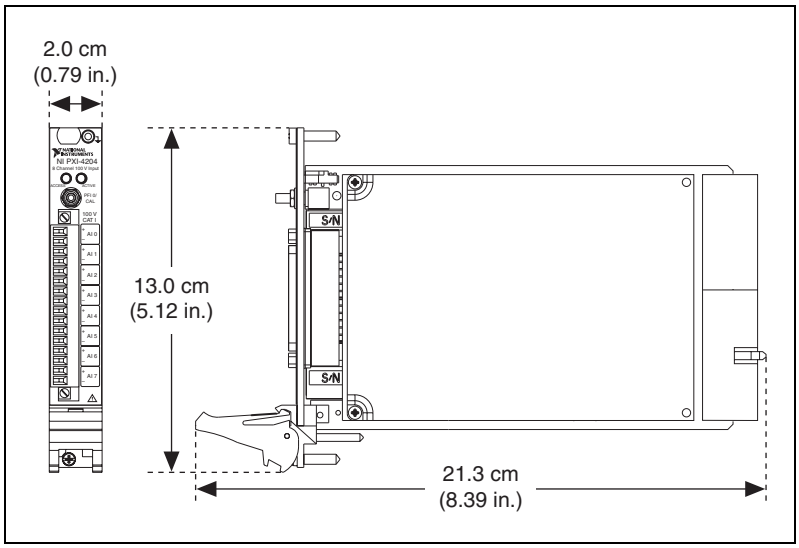


Figure A-1. NI PXI-4204 Dimensions

Weight .....207 g (7.3 oz)

Analog input signal connector .....16x1 miniature COMBICON, 3.81 mm pitch

Analog input signal mating connector .....16x1 miniature COMBICON screw-terminal connector, 3.81 mm pitch, 28–16 AWG signal wires

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Maximum Working Voltage

(Signal + common-mode) each input should remain within ±100 V of ground.

Maximum working voltage refers to the signal voltage plus the CMV.

Channel-to-earth (inputs) ..... 100 V, 70 V_{rms}, Measurement Category I

Channel-to-channel (inputs)..... 100 V, 70 V_{rms}, Measurement Category I

Cautions This device is rated for Measurement Category I and intended to carry signal voltages no greater than 100 V. This device can withstand up to 500 V impulse voltage without creating a safety hazard. Do not use this device for connection to signals or for measurements within Categories II, III, or IV. Do not connect to MAINS supply circuits, such as wall outlets, of 115 or 230 VAC.

When hazardous voltages (>42.4 V_{pk}/60 V) are present on any terminal, safety low-voltage (≤42.4 V_{pk}/60 V) cannot be connected to any other terminal.

Overvoltage Protection

AI0 to AI07 ..... ±110 V, powered on or off

SMB connector ..... ±15 V, powered on or off

Environmental

Operating temperature..... 0 to 55 °C

Storage temperature ..... –20 to 70 °C

Humidity ..... 10 to 90% RH, noncondensing

Maximum altitude ..... 2,000 m

Pollution Degree (indoor use only)..... 2

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Safety

The NI PXI-4204 is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN-61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Electromagnetic Compatibility

This product is designed to meet the requirements of the following standards of EMC for electrical equipment for measurement, control, and laboratory use:

- EN 61326 EMC requirements; Minimum Immunity
- EN 55011 Emissions; Group 1, Class A
- CE, C-Tick, ICES, and FCC Part 15 Emissions; Class A

Note For EMC compliance, operate this device according to product documentation.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

- 73/23/EEC; Low-Voltage Directive (safety)
- 89/336/EEC; Electromagnetic Compatibility Directive (EMC)

Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of their life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit `ni.com/environment/weee.htm`.

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B

Timing Signal Information

This appendix contains more information about the timing signals discussed in Chapter 3, *Using the NI PXI-4204*.

Connecting Timing Signals

Caution Exceeding the maximum input voltage ratings listed in Appendix A, *Specifications*, can damage the device and the computer. NI is *not* liable for any damage resulting from such signal connections.

Programmable Function Input Connections

You can externally control seven internal timing signals from PFI0 and the PXI trigger bus pins. The source for each of these signals is software configurable from PFI0, PXI_Trig<0..5>, or PXI Star when you want external control. This flexible routing scheme reduces the need to change the physical wiring to the device I/O connector for applications requiring alternative wiring.

Note The NI PXI-4204 cannot output the PXI Star trigger line.

As an input, each PFI signal can be individually configured for edge or level detection and polarity selection. You can use the polarity selection for any timing signal, but the edge or level detection depends on the particular timing signal being controlled. The detection requirements for each timing signal are listed in the corresponding sections.

In edge-detection mode, the minimum pulse width required is 10 ns. This requirement applies for both rising-edge and falling-edge polarity settings. There is no maximum pulse width requirement in edge-detect mode.

In level-detection mode, there are no pulse width requirements imposed by the PFIs themselves. Limits can be imposed by the particular timing signal being controlled. These requirements are listed in the sections describing the particular signals.

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DAQ Timing Connections

The timing signals are AI START TRIG, AI REF TRIG, AI SAMP CLK, AI CONV CLK, AI PAUSE TRIG, AI SAMPLE CLK TIMEBASE, and AI HOLD COMPLETE.

Posttriggered DAQ allows you to view data that is acquired after a trigger event is received. Figure B-1 shows a typical posttriggered sequence.

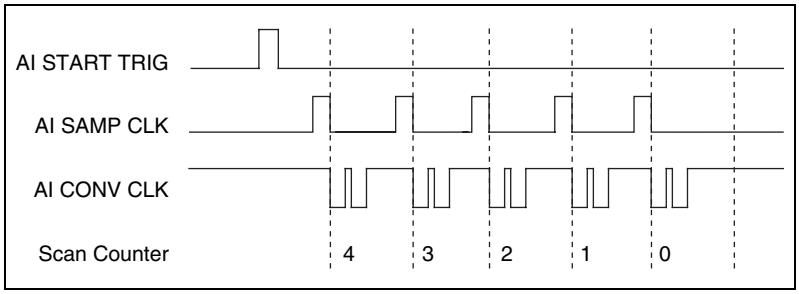


Figure B-1. Typical Posttriggered Sequence

Pretriggered DAQ allows you to view data that is acquired before the trigger of interest in addition to data acquired after the trigger. Figure B-2 shows a typical pretriggered sequence.

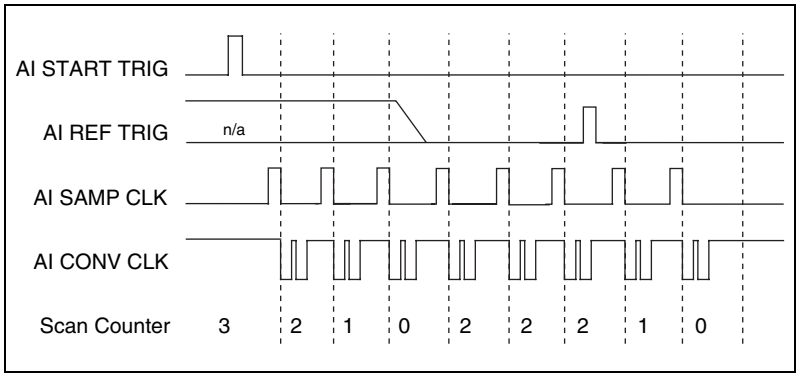


Figure B-2. Typical Pretriggered Sequence

AI START TRIG Signal

The AI START TRIG signal can be input through PFI0, PXI_Trig<0..5>, or PXI Star. The AI START TRIG signal can be output through PFI0 or PXI_Trig<0..5>.

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As an input, AI START TRIG is configured in the edge-detection mode. You can select PFI0 as the source for AI START TRIG and configure the polarity selection for either rising or falling edge. The selected edge of AI START TRIG starts the sequence for both posttriggered and pretriggered acquisitions. Refer to Figures B-1 and B-2 for the relationship of AI START TRIG to the sequence.

As an output, AI START TRIG reflects the action that initiates a sequence, even if the acquisition is externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures B-3 and B-4 show the input and output timing requirements for AI START TRIG.

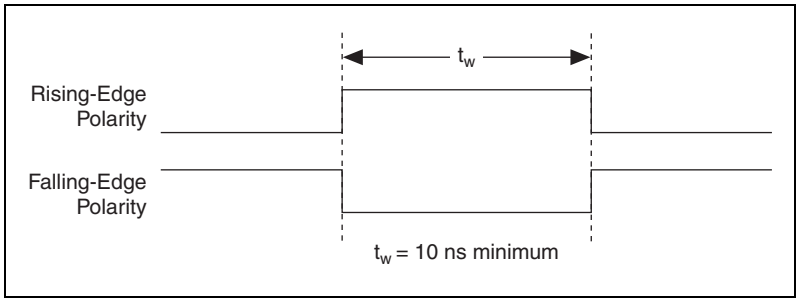


Figure B-3. AI START TRIG Input Signal Timing

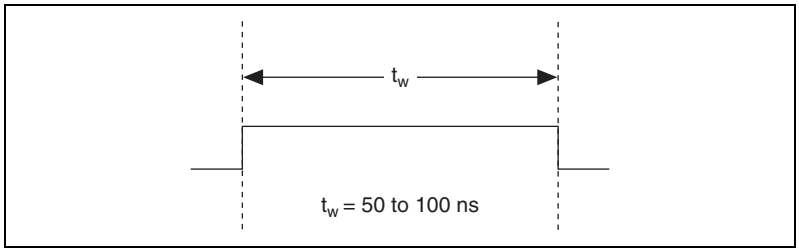


Figure B-4. AI START TRIG Output Signal Timing

The device also uses AI START TRIG to initiate pretriggered operations. In pretriggered applications, AI START TRIG is generated by a software trigger unless a PFI pin is selected as the source of AI START TRIG. Refer to the *AI REF TRIG Signal* section for a complete description of the use of AI START TRIG and AI REF TRIG in a pretriggered operation.

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AI REF TRIG Signal

The AI REF TRIG signal can be input through PFI0, PXI_Trig<0..5>, or PXI Star. Refer to Figure B-2 for the relationship of AI REF TRIG to the sequence.

As an input, AI REF TRIG is configured in edge-detection mode. You can configure the polarity selection for either rising or falling edge. The selected edge of AI REF TRIG initiates the posttriggered phase of a pretriggered sequence. In pretriggered mode, the AI START TRIG signal initiates the acquisition. The scan counter (SC) indicates the minimum number of scans before AI REF TRIG is recognized. After the SC decrements to zero, it is loaded with the number of posttrigger scans to acquire while the acquisition continues. The device ignores AI REF TRIG if it is asserted prior to the SC decrementing to zero. After the selected edge of AI REF TRIG is received, the device acquires a fixed number of scans and the acquisition stops. In pretriggered mode, the device acquires data both before and after receiving AI REF TRIG.

As an output, AI REF TRIG reflects the posttrigger in a pretriggered sequence, even if the acquisition is externally triggered by another PFI. AI REF TRIG is not used in posttriggered DAQ. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures B-5 and B-6 show the input and output timing requirements for AI REF TRIG.

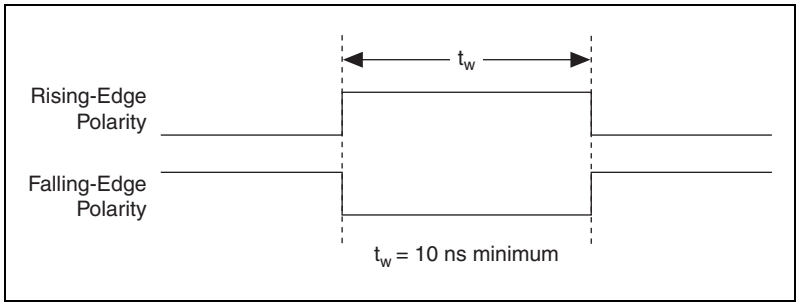


Figure B-5. AI REF TRIG Input Signal Timing

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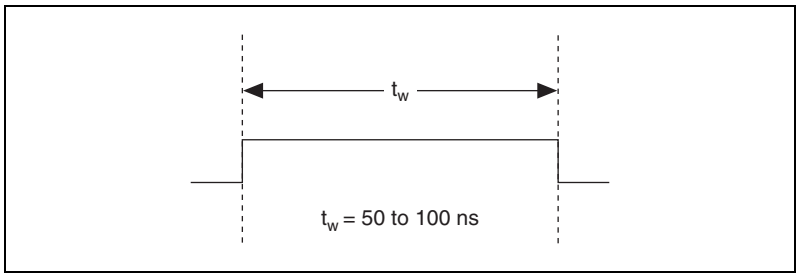


Figure B-6. AI REF TRIG Output Signal Timing

AI SAMP CLK Signal

The AI SAMP CLK signal can be externally input from PFI0, PXI_Trig<0..5>, or PXI Star. It can be output on any PXI trigger bus line. Refer to Figures B-1 and B-2 for the relationship of AI SAMP CLK to the sequence.

As an input, AI SAMP CLK is configured in edge-detection mode. You can configure the polarity selection for either rising or falling edge. The selected edge of AI SAMP CLK initiates a scan. The SI2 counter starts if you select an internally triggered AI CONV CLK.

As an output, AI SAMP CLK reflects the actual start pulse that initiates a scan, even if the starts are externally triggered by another PFI or PXI_Trig<0..5>. You have two output options. The first option is an active high pulse with a pulse width of 50 to 100 ns, which indicates the start of the scan. The second option is an active high pulse that terminates at the start of the last conversion in the scan, which indicates a scan in progress. AI SAMP CLK is deasserted, t_{off}, after the last conversion in the scan is initiated. This output is set to high-impedance at startup.

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Figures B-7 and B-8 show the input and output timing requirements for AI SAMP CLK.

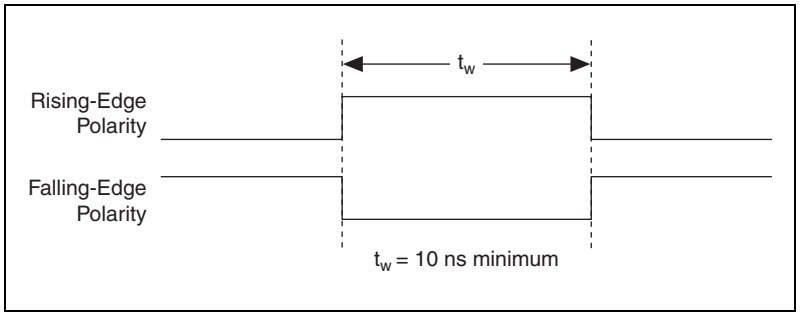


Figure B-7. AI SAMP CLK Input Signal Timing

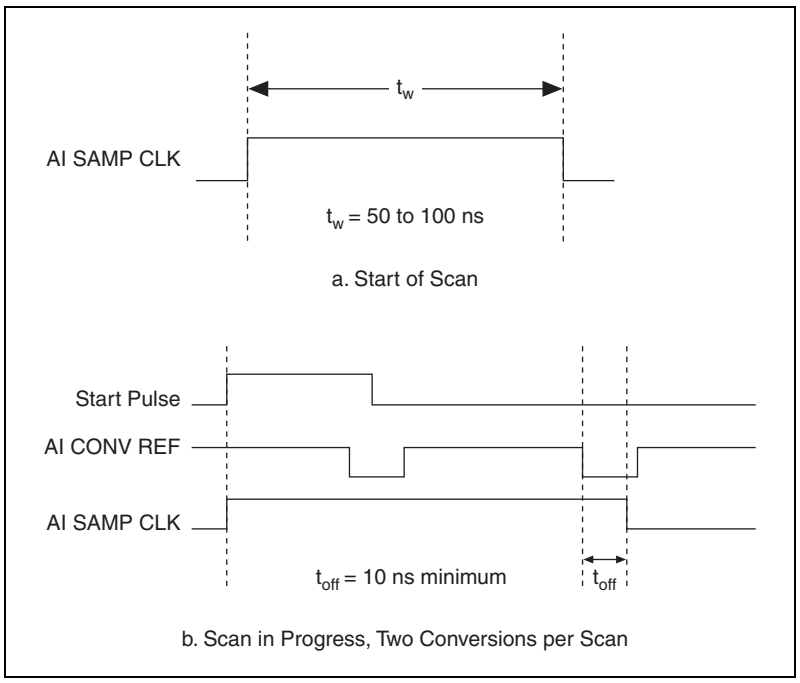


Figure B-8. AI SAMP CLK Output Signal Timing

The AI CONV CLK pulses are masked off until the device generates AI SAMP CLK. If you use internally generated conversions, the first AI CONV CLK appears when the onboard SI2 counter reaches zero. If you select an external AI CONV CLK, the first external pulse after

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AI SAMP CLK generates a conversion. Separate the AI SAMP CLK pulses by at least one scan period.

A counter on the device internally generates AI SAMP CLK unless you select some external source. The AI START TRIG signal starts this counter, and the application software or the sample counter stops it.

Scans generated by either an internal or external AI SAMP CLK are inhibited unless they occur within a sequence. Scans occurring within a sequence can be gated by either the hardware AI PAUSE TRIG signal or the software command register gate.

AI CONV CLK Signal

PFI0, PXI_Trig<0..5>, or PXI Star can externally input the AI CONV CLK signal, which is also available as an output on PXI_Trig<0..5>.

Refer to Figures B-1 and B-2 for the relationship of AI CONV CLK to the sequence.

As an input, AI CONV CLK is configured in edge-detection mode. You can configure the polarity selection for either rising or falling edge. The selected edge of AI CONV CLK initiates an A/D conversion.

As an output, AI CONV CLK reflects the actual convert pulse that connects to the ADC, even if the conversions are externally generated by another PFI. The output is an active low pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures B-9 and B-10 show the input and output timing requirements for AI CONV CLK.

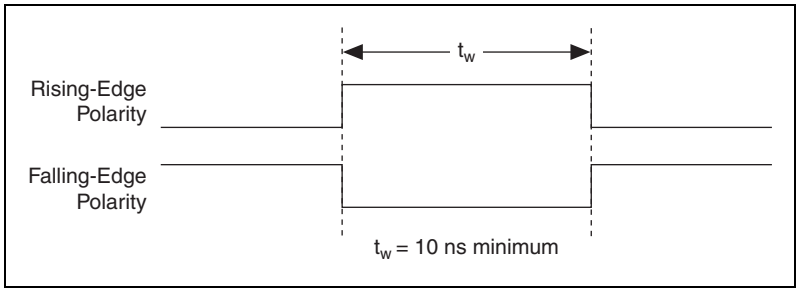


Figure B-9. AI CONV CLK Input Signal Timing

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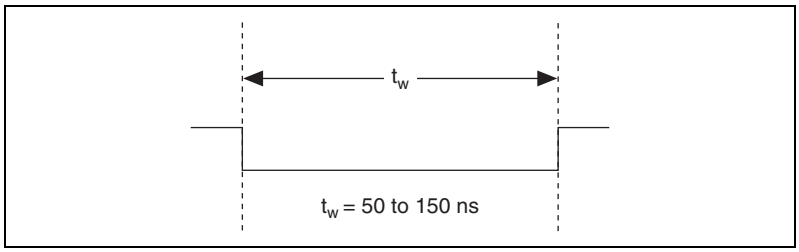


Figure B-10. AI CONV CLK Output Signal Timing

The ADC switches to hold mode within 60 ns of the selected edge. This hold-mode delay time is a function of temperature and does not vary from one conversion to the next. Separate the AI CONV CLK pulses by at least one conversion period.

The NI PXI-4204 sample interval counter generates AI CONV CLK unless you select an external source. The AI SAMP CLK signal starts the counter, which counts down and reloads itself until the scan finishes. The counter then reloads itself in preparation for the next AI SAMP CLK pulse.

A/D conversions generated by an internal or external AI CONV CLK signal are inhibited unless they occur within a sequence. Scans occurring within a sequence can be gated by either the hardware AI PAUSE TRIG signal or the software command register gate.

AI PAUSE TRIG Signal

PFI0, PXI_Trig<0..5>, or PXI Star can externally input the AI PAUSE TRIG signal, which is not available as an output on the I/O connector. AI PAUSE TRIG can mask off scans in a sequence. You can configure the pin you select as the source for AI PAUSE TRIG in level-detection mode. You can configure the polarity selection for the pin as either active high or active low.

In level-detection mode, the AI SAMP CLK signal is masked off and no scans can occur.

AI PAUSE TRIG can neither stop a scan in progress nor continue a previously gated-off scan. In other words, once a scan has started, AI PAUSE TRIG does not gate off conversions until the beginning of the next scan. Conversely, if conversions are gated off, AI PAUSE TRIG does not gate them back on until the beginning of the next scan.

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AI SAMPLE CLK TIMEBASE Signal

PFI0, PXI_Trig<0..5>, or PXI Star can externally input the AI SAMPLE CLK TIMEBASE signal, which is not available as an output on the I/O connector. The onboard scan interval (SI) counter uses AI SAMPLE CLK TIMEBASE as a clock to time the generation of the AI SAMP CLK signal. Configure the pin you select as the source for AI SAMPLE CLK TIMEBASE in level-detection mode. Configure the polarity selection for the pin for either active high or active low.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency.

Either the 20 MHz or 100 kHz internal timebase generates AI SAMPLE CLK TIMEBASE unless you select an external source. Figure B-11 shows the timing requirements for AI SAMPLE CLK TIMEBASE.

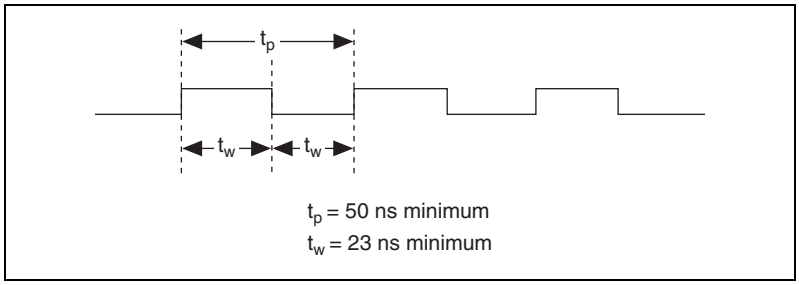


Figure B-11. AI SAMPLE CLK TIMEBASE Signal Timing

AI HOLD COMPLETE Signal

AI HOLD COMPLETE is an output-only signal that generates a pulse with the leading edge occurring approximately 50 to 100 ns after an A/D conversion begins. The polarity of this output is software configurable, but the polarity is typically configured so that a low-to-high leading edge can clock external analog input multiplexers indicating when the input signal has been sampled and can be removed. This signal has a 400 to 500 ns pulse width and is software enabled. Figure B-12 shows the timing for AI HOLD COMPLETE.

Note The polarity of AI HOLD COMPLETE is not software selectable when programmed using NI-DAQmx. It is a positive polarity pulse.

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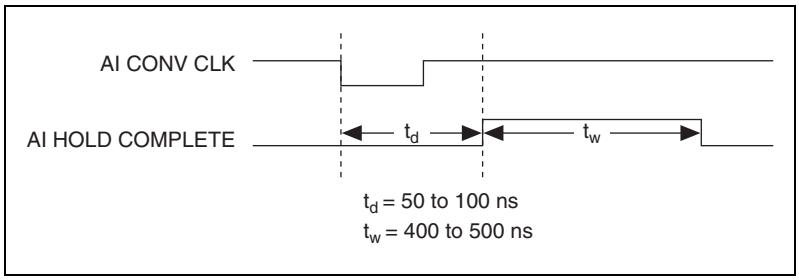


Figure B-12. AI HOLD COMPLETE Signal Timing

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C

Removing the NI PXI-4204

This section provides details about removing an NI PXI-4204 device from MAX and from a PXI chassis.

Note You must physically remove the NI PXI-4204 from the chassis before you can remove it from MAX.

Removing the NI PXI-4204 from a PXI Chassis

Consult the PXI chassis documentation for additional instructions and cautions. To remove the NI PXI-4204 device from a PXI chassis, complete the following steps while referring to Figure C-1:

1. Power off the PXI chassis. Do *not* remove the NI PXI-4204 device from a chassis that is powered on.
2. Rotate the mounting screws that secure the NI PXI-4204 to the chassis counter-clockwise until they are loose, but do not completely remove the screws.
3. Remove the NI PXI-4204 by pushing down steadily on the injector/ejector handle until the device disengages from the chassis.
4. Slide the device completely out.

The next time you restart the computer the NI PXI-4204 will have a red circle with a white **X** inside it next to the device in MAX.

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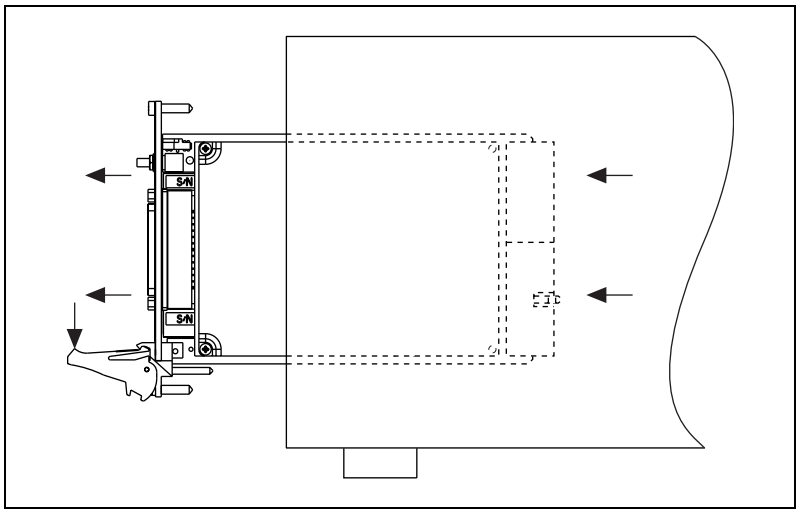


Figure C-1. Injector/Ejector Handle Position Before Device Removal

Removing the NI PXI-4204 from MAX

To remove an NI PXI-4204 device from MAX, complete the following steps after launching MAX:

1. Expand **Devices and Interfaces** to display the list of installed devices and interfaces. The NI PXI-4204 should have a red circle with a white **X** inside it next to the device to indicate it has been physically removed from the chassis.
2. Right-click the NI PXI-4204 and click **Delete**.
3. You are presented with a confirmation window. Click **Yes** to continue deleting the device or **No** to cancel this action.

The NI PXI-4204 is now removed from the list of installed devices in MAX.

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D

Common Questions

This appendix lists common questions related to the use of the NI PXI-4204.

Which version of NI-DAQ works with the NI PXI-4204 and how do I get the most current version of NI-DAQ?

You must have NI-DAQ 7.0 or later and use NI-DAQmx. Visit `ni.com` and follow the link, **Download Software»Drivers and Updates»Search Drivers and Updates**, and enter the keyword `NI-DAQ` to find the latest version of NI-DAQ for your operating system.

Does the NI PXI-4204 have hardware analog triggering?

No, the NI PXI-4204 does not support hardware analog triggering. The NI PXI-4204 does support digital triggering.

Is the NI PXI-4204 an isolated device?

No, the NI PXI-4204 is not an isolated device and should not be used in applications with working voltages larger than ±100 V. The NI PXI-4204 has only resistive isolation, which does not fit all definitions for isolation. Whereas the NI PXI-4204 has a very high input range, the maximum working voltage specification should be carefully observed. The balanced differential inputs of the NI PXI-4204 provide effective rejection of common-mode voltages resulting from ground loops. However, high CMV can damage the NI PXI-4204. Refer to Appendix A, *Specifications*, for maximum working voltage specifications. NI does offer signal conditioning devices that provide high voltage isolation. For more information about isolated NI products, visit `ni.com/sigcon`.

What is the function of the chassis ground screw?

The chassis ground screw is intended to provide a ground for shielded field wiring.

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When no signal is connected to the NI PXI-4204, what sort of behavior should I expect?

While the NI PXI-4204 may react differently due to system and condition variables, in most cases, the resistor divider network will pull the signal to ground and read approximately 0.0 V.

How do I program the NI PXI-4204?

Refer to Chapter 3, *Using the NI PXI-4204*, for application programming information or your ADE help file. There is no register-level programming manual available for the NI PXI-4204.

How do I perform an external calibration of the NI PXI-4204?

As of the NI PXI-4204 release, an external calibration document is not available. To see if an NI PXI-4204 external calibration document is currently available, click **Manual Calibration Procedures** at `ni.com/calibration`.

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Glossary

Symbol	Prefix	Value
n	nano	10^{-9}
µ	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^{3}
M	mega	10^{6}
G	giga	10^{9}

Symbols

%	percent
+	positive of, or plus
–	negative of, or minus
/	per
°	degree
Ω	ohm

A

A	amperes
A/D	analog-to-digital
AC	alternating current
ADC	analog-to-digital converter—an electronic device, often an integrated circuit, that converts an analog voltage to a digital number
ADE	application development environment

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AI	analog input
AI CONV CLK	convert signal
AI HOLD COMPLETE	scan clock signal
AI PAUSE TRIG	analog input gate signal
AI SAMP CLK	start scan signal
AISENSE	analog input sense signal

B

bandwidth	the range of frequencies present in a signal, or the range of frequencies to which a measuring device can respond
bipolar	a signal range that includes both positive and negative values (for example, –5 to +5 V)
breakdown voltage	the voltage high enough to cause breakdown of optical isolation, semiconductors, or dielectric materials. *See also* working voltage.
bus	the group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. Examples of PC buses are the ISA and PCI bus.

C

C	Celsius
CalDAC	calibration DAC
CH	channel—pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels.
channel clock	the clock controlling the time interval between individual channel sampling within a scan. Devices with SS/H do not have this clock.
CMR	common-mode rejection

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CMRR	common-mode rejection ratio—a measure of an instrument's ability to reject interference from a common-mode signal, usually expressed in decibels (dB)
common-mode signal	any voltage present at the instrumentation amplifier inputs with respect to amplifier ground
counter/timer	a circuit that counts external pulses or clock pulses (timing)

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current
DAQ	data acquisition—(1) collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing; (2) collecting and measuring the same kinds of electrical signals with A/D and/or DIO devices plugged into a computer, and possibly generating control signals with D/A and/or DIO devices in the same computer
DAQ Assistant	a configuration assistant with which you define and configure your DAQ operation
DAQ-STC	data acquisition system timing controller chip
dB	decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: $db=20\cdot\log_{10}(V1/V2)$, for signals in volts
DC	direct current
differential input	an analog input consisting of two terminals, both of which are isolated from computer ground, whose difference is measured
DIO	digital input/output
dithering	the addition of Gaussian noise to an analog input signal

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DMA	direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
DNL	differential nonlinearity—a measure in least significant bit of the worst-case deviation of code widths from their ideal value of 1 LSB
driver	software that controls a specific hardware device such as a DAQ device or a GPIB interface board

E

EEPROM	electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed
EMC	electromagnetic compatibility
EMI	electromagnetic interference—defines unwanted electromagnetic radiation from a device, which could interfere with desired signals in test or communication equipment

F

FIFO	first-in first-out memory buffer
floating signal sources	signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called nonreferenced signal sources. Some common example of floating signal sources are batteries, transformers, or thermocouples.

G

g	grams
gain	the factor by which a signal is amplified, sometimes expressed in decibels

H

Hz	hertz—the number of scans read or updates written per second

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I

I/O	input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or DAQ and control interfaces
in.	inches
input bias current	the current that flows into the inputs of a circuit
input impedance	the resistance and capacitance between the input terminals of a circuit
instrumentation amplifier	a circuit whose output voltage with respect to ground is proportional to the difference between the voltages at its two high impedance inputs

K

k	kilo—the standard metric prefix for 1,000, or 10^3, used with units of measure such as volts, hertz, and meters
kS	1,000 samples

L

LabVIEW	Laboratory Virtual Instrument Engineering Workbench—a program development application based on the programming language G and used commonly for test and measurement purposes
LED	light-emitting diode
linearity	the adherence of device response to the equation R = KS, where R = response, S = stimulus, and K = a constant
LSB	least significant bit

M

MAX	Measurement & Automation Explorer—NI software for configuring devices and channels.

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maximum working voltage	the highest voltage with respect to ground that should be applied to an input terminal during normal use, normally well under the breakdown voltage for safety margin. Includes both the signal and common-mode voltages.

N

NI	National Instruments
NI-DAQ	NI driver software for DAQ hardware
NI-DAQmx	the latest NI-DAQ driver with new VIs, functions, and development tools for controlling measurement devices
noise	an undesirable electrical signal—noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, soldering irons, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.

P

PCI	peripheral component interconnect
PFI	programmable function input
PGIA	programmable gain instrumentation amplifier
port	(1) a communications connection on a computer or a remote controller; (2) a digital port, consisting of four or eight lines of digital input and/or output
ppm	parts per million
PXI	PCI eXtensions for Instrumentation—an open specification that builds on the CompactPCI specification by adding instrumentation-specific features
PXI trigger bus	the timing bus that connects PXI DAQ devices directly, by means of connectors built into the backplane of the PXI chassis, for precise synchronization of functions. This bus is functionally equivalent to the RTSI bus for PCI DAQ devices.

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R

resolution	the smallest signal increment that can be detected by a measurement system. Resolution can be expressed in bits, in proportions, or in percent of full scale. For example, a system has 16-bit resolution, one part in 65,536 resolution, and 0.0015% of full scale.
rms	root mean square—the square root of the average value of the square of the instantaneous signal amplitude; a measure of signal amplitude
RTSI bus	real-time system integration bus—the NI timing bus that connects DAQ devices directly, for precise synchronization of functions

S

s	seconds
S	samples
S/s	samples per second—used to express the rate at which a DAQ device samples an analog signal
sample counter	the clock that counts the output of the channel clock, in other words, the number of samples taken. On devices with SS/H, this counter counts the output of the scan clock and hence the number of scans.
scan	one or more analog or digital input samples. Typically, the number of input samples in a scan is equal to the number of channels in the input group. For example, one pulse from the scan clock produces one scan which acquires one new sample from every analog input channel in the group.
scan clock	the clock controlling the time interval between scans
scan interval	controls how often a scan is initialized. The scan interval is regulated by AI SAMP CLK.
SCXI	Signal Conditioning eXtensions for Instrumentation—the NI product line for conditioning low-level signals within an external chassis near sensors so only high-level signals are sent to DAQ devices in the noisy PC environment

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self-calibrating	a property of a DAQ device that has an extremely stable onboard reference and calibrates its own A/D and D/A circuits without manual adjustments by the user
settling time	the amount of time required for a voltage to reach its final value within specified limits
signal conditioning	the manipulation of signals to prepare them for digitizing
software trigger	a programmed event that triggers an event such as DAQ
SS/H	simultaneous sample-and-hold
STC	system timing controller

T

TRIG	trigger signal
trigger	any event that causes or starts some form of data capture
TTL	transistor-transistor logic—a digital circuit composed of bipolar transistors wired in a certain manner

V

V	volts
VI	virtual instrument—(1) a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument; (2) a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program
V_{rms}	volts, root mean square

W

working voltage	the highest voltage with respect to ground that should be applied to an input terminal during normal use, normally well under the breakdown voltage for safety margin. Includes both the signal and common-mode voltages.

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Index

A

accuracy information
    with SS/H disabled, A-3
    with SS/H enabled, A-3
AI CONV CLK signal
    description, B-7
    input timing (figure), B-7
    output timing (figure), B-8
    overview (table), 3-11
    signal routing (figure), 3-8
AI HOLD COMPLETE signal
    description, B-9
AI PAUSE TRIG signal
    description, B-8
    overview (table), 3-11
AI REF TRIG signal
    description, B-4
    input signal timing (figure), B-4
    output signal timing (figure), B-5
    overview (table), 3-10
AI SAMP CLK signal
    description, B-5
    input signal timing (figure), B-6
    output signal timing (figure), B-6
    overview (table), 3-11
AI SAMPLE CLK TIMEBASE signal
    description, B-9
    overview (table), 3-11
    signal timing (figure), B-9
AI START TRIG signal
    description, B-2
    input signal timing (figure), B-3
    output signal timing (figure), B-3
    overview (table), 3-10
AI.AutoZeroMode property (table), 3-15
AI.Coupling property (table), 3-14
AI.Lowpass.CutoffFreq property (table), 3-14
AI.SampAndHold.Enable property (table), 3-15
alternative shielded ground-referenced connection, 2-10
analog input connections, 2-5
    floating signal source connection, 2-6
        shielded, 2-7
    ground-referenced signal connection, 2-8
        alternative shielded, 2-10
        shielded, 2-9
    high CMV connection, 2-11
        shielded, 2-12
analog input specifications, A-1
application development, 3-11
    acquiring data, 3-15
    adjusting timing and triggering, 3-14
    analyzing data, 3-15
    clearing tasks and memory, 3-15
    configuring channel properties, 3-14
    creating tasks
        programmatically, 3-13
        using DAQ assistant, 3-13
    documentation for, 3-22
    in application development (table), 3-14
    presenting data, 3-15
    synchronizing multiple devices, 3-19
        program flowchart (figure), 3-20
    synchronizing the NI PXI-4204, 3-19
        table, 3-21
        using LabVIEW, 3-21
    typical program flowchart (figure), 3-12
    using LabVIEW, 3-16
        DAQ channel property node, 3-17
        steps(table), 3-16

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B

block diagram of NI PXI-4204, 3-2

C

calibration, 3-23
    external calibration, 3-24
    loading calibration constants, 3-23
    pre-calibration errors, A-4
    self-calibration, 3-23
    specifications, A-4
channel properties, configuring, 3-14
    in application development (table), 3-14
    in LabVIEW, 3-17
chassis ground screw, D-1
PXI trigger bus
clocks, PXI, 3-9
    See also DAQ timing conventions
CMV. *See* high CMV connection
common questions, D-1
common-mode rejection (CMR), effective, 3-6
common-mode rejection ratio (CMRR), 3-5
configuring
    channel properties, 3-14
        in LabVIEW, 3-17
        NI-DAQmx properties (table), 3-14
conventions used in the manual, *iv*

D

DAQ Assistant, 3-13
DAQ timing conventions, B-2
    AI CONV CLK
        description, B-7
        input signal timing (figure), B-7
        output signal timing (figure), B-8
        overview (table), 3-11
    AI HOLD COMPLETE
        description, B-9
        signal timing (figure), B-10
    AI PAUSE TRIG
        description, B-8
        overview (table), 3-11
    AI REF TRIG
        description, B-4
        input signal timing (figure), B-4
        output signal timing (figure), B-5
        overview (table), 3-10
    AI SAMP CLK
        description, B-5
        input signal timing (figure), B-6
        output signal timing (figure), B-6
        overview (table), 3-11
    AI SAMPLE CLK TIMEBASE
        description, B-9
        overview (table), 3-11
        signal timing (figure), B-9
    AI START TRIG
        description, B-2
        input signal timing (figure), B-3
        overview (table), 3-10
    posttriggered sequence (figure), B-2
    pretriggered sequence (figure), B-2
DAQmx channel property node, using in LabVIEW, 3-17
DAQ-STC timing controller, 3-7
developing applications. *See* application development
device and PXI clocks, 3-9
differential signals, 3-4
digital trigger specifications, A-5
Divide-by-Ten Attenuator (table), 3-3
documentation
    application development, 3-22
    National Instruments documentation, 1-2

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E

effective CMR, 3-6
electromagnetic compatibility
  specifications, A-8
environmental specifications, A-7
external calibration, 3-24

F

floating signal source connection, 2-6
    connecting to NI PXI-4204, 2-6
    shielded, 2-7
    souce connection
        figure, 2-6
front signal connector, 2-3
    front label of NI PXI-4204 (figure), 2-5
    signal assignments (figure), 2-4
    steps for signal connection, 2-3

G

ground-referenced signal connection, 2-8
    alternative shielded, 2-10
    connecting to NI PXI-4204, 2-8
    shielded, 2-9

H

high CMV connection, 2-11
    connecting to NI PXI-4204, 2-11
    shielded, 2-12

I

injector/ejector handle position (figure), C-2
input impedance, 3-5
Input Multiplexer (table), 3-3
installation
    application software, 1-3
    NI PXI-4204, 1-3
Instrumentation Amplifier (table), 3-3
isolation, D-1

L

LabVIEW software
    application development, 3-16
        DAQmx channel property node, 3-17
        steps (table), 3-16
    synchronizing NI PXI-4204, 3-21
LabWindows/CVI software, 1-2
Lowpass Filter (table), 3-4

M

MAX. *See* Measurement & Automation
  Explorer (MAX)
maximum working voltage, A-7
Measurement & Automation Explorer
  (MAX), 1-1
    removing NI PXI-4220, C-2
measurement considerations, 3-4
    common-mode rejection ratio, 3-5
    differential signals, 3-4
    effective CMR, 3-6
    input impedance, 3-5
        effect on signal measurements
          (figure), 3-5
    normal-mode rejection, 3-6
Measurement Studio software, 1-2

N

NI PXI-4204
    See also installation, specifications
    application development, 3-11
        using LabVIEW, 3-16
    calibration, 3-23
    configuring, 3-3
    device and PXI clocks, 3-9
    documentation, 1-2, 3-22
    installing (figure), 2-2
    measurement considerations, 3-4
    overview, 1-1
    programmable function inputs, 3-8

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requirements for getting started, 1-2
signal conditioning functional blocks (table), 3-3
signal connection, 2-1
software
LabVIEW, 1-2
LabWindows/CVI, 1-2
Measurement Studio, 1-2
NI-DAQ, 1-2
synchronization and triggering, 3-19
theory of operation, 3-1
block diagram, 3-2
device and PXI clocks, 3-9
measurement considerations, 3-4
programmable function inputs, 3-8
signal conditioning functional overview, 3-3
timing and control overview, 3-7
timing and control overview, 3-7
NI-DAQ software, 1-2
NI-DAQmx
creating a task, 3-13
properties (table), 3-14
normal-mode rejection (NMR), 3-6

O

operation theory. *See* NI PXI-4204
overvoltage protection specifications, A-7

P

PCI bus interface specifications, A-5
PFIs. *See* programmable function inputs
physical specifications, A-6
posttriggered data acquisition, B-2
power requirements specifications, A-5
pretriggered acquisition, B-2
programmable function inputs
description, B-1
overview, 3-8
programming. *See* application development
PXI clocks, 3-9
PXI trigger bus
overview, 3-7
signal connection (figure), 3-10
specifications, A-5
timebase signal, 3-9
timing signals (table), 3-10

Q

questions and answers, D-1

R

regulatory compliance specifications, A-8
removing NI PXI-4220
from Measurement & Automation Explorer (MAX), C-2
from PXI chassis, C-1

S

safety specifications, A-8
self-calibration, 3-23
shielded floating signal source connection, 2-7
shielded ground-referenced signal connection, 2-9
alternative shielded connection, 2-10
shielded high CMV connection, 2-12
signal conditioning
functional blocks (table), 3-3
overview, 3-3
signal connections, 2-1
analog input connections, 2-5
floating signal source connection, 2-6
shielded, 2-7
ground-referenced signal connection, 2-8
alternative shielded, 2-10
shielded, 2-9

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high CMV connection, 2-11
shielded, 2-12
front signal connector, 2-1, 2-3
NI PXI-4204, 2-1
signal measurement. *See* measurement considerations
specifications
accuracy information
with SS/H disabled, A-3
with SS/H enabled, A-3
analog input, A-1
maximum sampling rates (table), A-1
calibration, A-4
digital triggers, A-5
electromagnetic compatibility, A-8
environmental, A-7
overvoltage protection, A-7
PCI bus interface, A-5
physical, A-6
power requirements, A-5
regulatory compliance, A-8
safety, A-8
SS/H characteristics, A-3
transfer characteristics, A-4
SS/H characteristics specifications, A-3
Star Trigger controller, 3-9
synchronization and triggering
NI PXI-4204, 3-19
overview, 3-19
program flowchart (figure), 3-20
using LabVIEW, 3-21

T

T/H (Track-and-Hold) circuitry (table), 3-4
theory of operation *See* NI PXI-4204
timing and control overview, 3-7
timing and triggering, adjusting, 3-14
timing signal routing
device and PXI clocks, 3-9
timing signals. *See* DAQ timing connections, programmable function imputs
transfer characteristics specifications, A-4
trigger bus. *See* PXI trigger bus
triggering
See also synchronization and triggering
adjusting, 3-14
digital triggering specifications, A-5
hardware analog triggering, D-1

V

voltage
maximum working voltage, A-7
overvoltage protection, A-7

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