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DAQ

NI 6624 User Manual

NI PCI-6624 and NI PXI-6624 Devices

December 2006
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All Class A products display a simple warning statement of one paragraph in length regarding interference and undesired operation. The FCC rules have restrictions regarding the locations where FCC Class A products can be operated.

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Changes or modifications not expressly approved by NI could void the user's authority to operate the equipment under the FCC Rules.

Class A

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user is required to correct the interference at their own expense.

Canadian Department of Communications

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

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* The CE marking Declaration of Conformity contains important supplementary information and instructions for the user or installer.

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About This Manual

This manual describes the electrical and mechanical aspects of the National Instruments NI 6624 device, and contains information about device operation and programming. Unless otherwise noted, text applies to both the PCI-6624 device and the PXI-6624 device. The PCI and PXI implementations are the same in functionality; their primary difference is the bus interface.

Conventions

The following conventions are used in this manual:

<> — Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, AO <3..0>.

» — The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.

 — This icon denotes a note, which alerts you to important information.

 — This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on a product, refer to the *Read Me First: Safety and Radio-Frequency Interference* document for information about precautions to take.

bold — Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names.

italic — Italic text denotes variables, emphasis, a cross-reference, or an introduction to a key concept. Italic text also denotes text that is a placeholder for a word or value that you must supply.

`monospace` — Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames, and extensions.

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Related Documentation

The following documents contain information that you might find helpful as you use this manual.

- *NI 6624 Specifications*—This document contains specifications for the NI 6624 device. It available for download at `ni.com/manuals`.
- *DAQ Getting Started Guide*—This guide describes how to install the NI-DAQ 7.*x* software and the DAQ device, and how to confirm that the device is operating properly.
- *NI-DAQmx Help*—This help file contains information about using NI-DAQmx to program National Instruments devices. NI-DAQmx is the software you use to communicate with and control your DAQ device.
- *Measurement & Automation Explorer Help for NI-DAQmx*—This help file contains information about configuring and testing DAQ devices, SCXI devices, SCC devices, and RTSI cables using Measurement & Automation Explorer (MAX) for NI-DAQmx, and information about special considerations for operating systems.
- *DAQ Assistant Help*—This help file contains information about creating and configuring channels, tasks, and scales using the DAQ Assistant.

Note You can download these documents at `ni.com/manuals`.

- *PXI Hardware Specification Revision 2.1*—This document introduces the PXI architecture and describes the electrical, mechanical, and software requirements for PXI.

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1 Introduction

This chapter describes the NI 6624 device, lists what you need to get started, and describes optional equipment. If you have not already installed the NI 6624 device, refer to the *DAQ Getting Started Guide* for installation instructions.

About NI 6624 Device

The NI 6624 is an isolated counter/timer device that uses two TIO ASICs (application-specific integrated circuits) developed by National Instruments. It has eight counters, each with three individually isolated inputs and one isolated output. It allows operation at up to 48 V, with robust protection against higher voltage transients and short circuits. There are also two additional PFI inputs.

The inputs on the NI 6624 are driven referenced to either the supply or ground and protected by current-limiting circuits. Outputs are open-drain, low-side switches that are protected against short circuits at all speeds of operation. All inputs and outputs are protected against reverse polarity connection.

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Figure 1-1 illustrates the key functional components of the NI 6624 device.

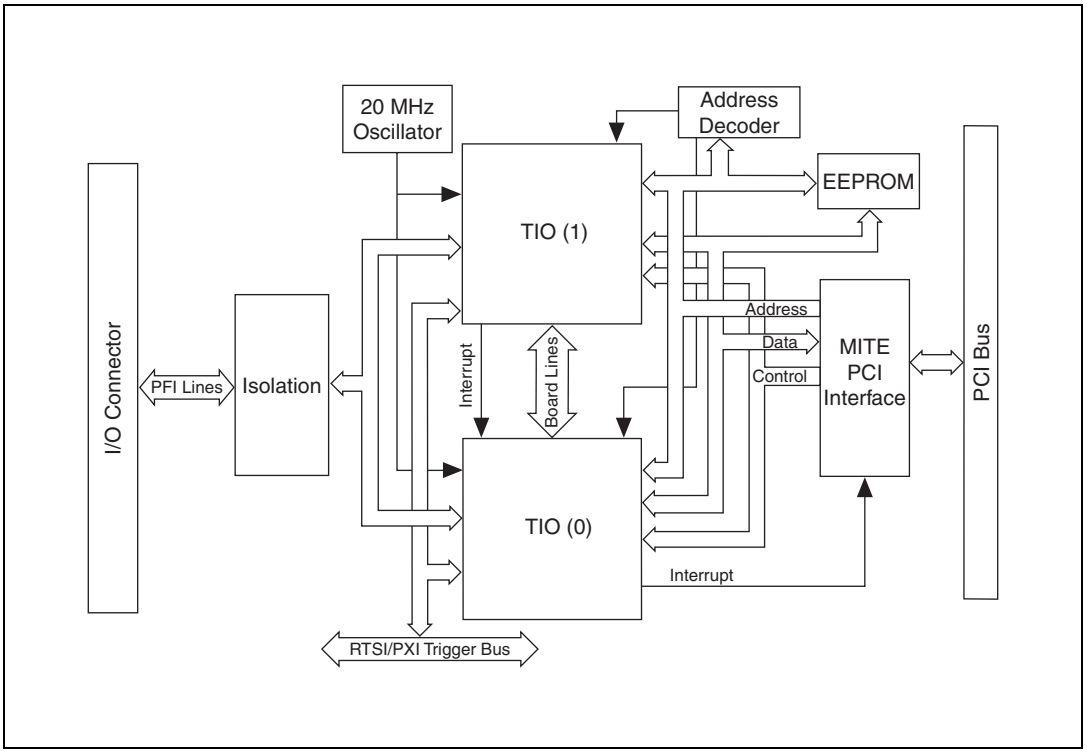


Figure 1-1. NI 6624 Block Diagram

Using PXI with CompactPCI

Using PXI-compatible products with standard products is an important feature provided by *PXI Hardware Specification Revision 2.1*. If you use a PXI-compatible plug-in module in a standard chassis, you cannot use PXI-specific functions, but you can still use the basic plug-in device functions. For example, the RTSI bus on a PXI TIO Series device is available in a PXI chassis, but not in a CompactPCI chassis.

The specification permits vendors to develop sub-buses that coexist with the basic PCI interface on the bus. Compatible operation is not guaranteed between devices with different sub-buses nor between devices with sub-buses and PXI. The standard implementation for does not include these sub-buses. The PXI TIO Series device works in any standard chassis adhering to the *PICMG 2.0 R3.0* core specification.

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PXI-specific features are implemented on the J2 connector of the bus. The PXI device is compatible with any chassis with a sub-bus that does not drive the lines used by that device. Even if the sub-bus is capable of driving these lines, the PXI device is still compatible as long as those pins on the sub-bus are disabled by default and never enabled.

Caution Damage can result if these lines are driven by the sub-bus. NI is *not* liable for any damage resulting from improper signal connections.

Getting Started

Before installing your DAQ device, you must install the software you plan to use with the device.

Installing NI-DAQ 7.*x*

If you are using NI-DAQ 7.1 or later, refer to the *DAQ Getting Started Guide*, which you can download at `ni.com/manuals`. The *DAQ Getting Started Guide* offers NI-DAQ users step-by-step instructions for installing software and hardware, configuring channels and tasks, and getting started developing an application.

Installing Other Software

If you are using other software, refer to the installation instructions that accompany your software.

Installing Hardware

The *DAQ Getting Started Guide* contains non-software-specific information about how to install PCI, PXI, PCMCIA, and USB/IEEE 1394 devices, as well as accessories and cables.

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Accessories and Cables

Table 1-1 lists the accessories and cables available for use with the NI 6624 device.

Table 1-1. Accessories and Cables

Accessory	Description
SH100-100-F	100-pin shielded cable, 2 m
R1005050	Ribbon cable with a 100-pin connector to two 50-pin connectors, 1 m or 2 m
RTSI cable	Cable that connects to the RTSI bus
CB-50	50-pin connector block
CB-50LP	Low-cost 50-pin connector block
SCB-100	100-pin connector block

Note The R1005050 requires two 50-pin connector blocks to enable connection to all NI 6624 lines. The CB-100 kit contains two CB-50 connector blocks and a R1005050 1 m cable. Go to `ni.com` for more information about this kit and other optional equipment available from National Instruments.

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2

Device Overview

This chapter provides information about NI 6624 device functionality.

Duplicate Count Prevention

Duplicate count prevention (or synchronous counting mode) ensures that a counter returns correct data in applications that are a slow or non-periodic external source. Duplicate count prevention applies only to buffered counter applications such as measuring frequency or period.

For such buffered applications, the counter should store the number of times an external source pulses between rising edges on the Gate signal.

Example Application That Works Correctly (No Duplicate Counting)

Figure 2-1 shows an external buffered signal as the period measurement Source.

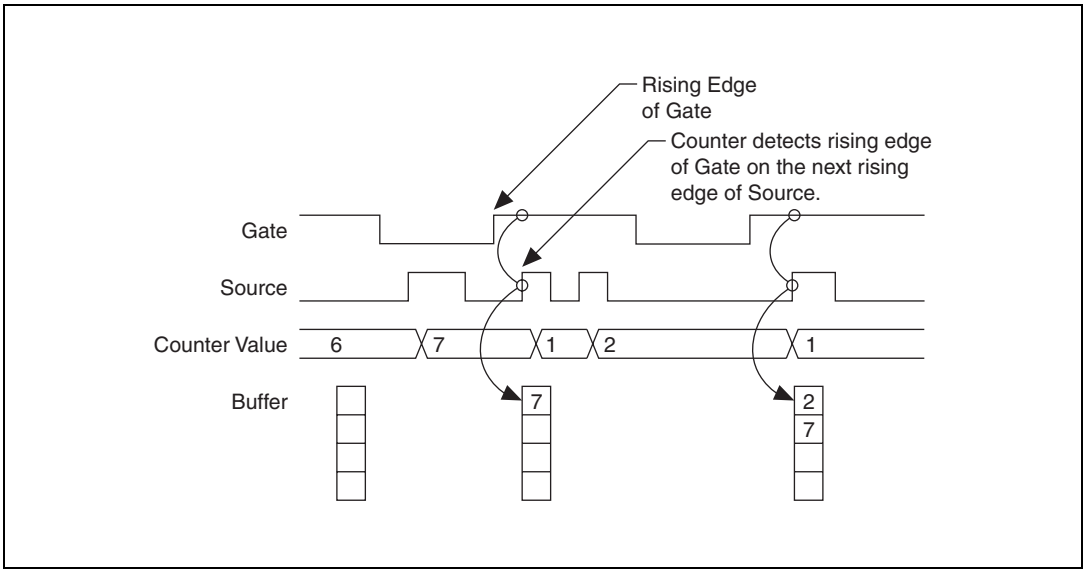


Figure 2-1. Example Application That Works Correctly

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On the first rising edge of the Gate, the current count of 7 is stored. On the next rising edge of the Gate, the counter stores a 2 because two Source pulses occurred after the previous rising edge of Gate.

The counter synchronizes or samples the Gate signal with the Source signal. So the counter does not detect a rising edge in the Gate until the next Source pulse. In this example, the counter stores the values in the buffer on the first rising Source edge after the rising edge of Gate.

Example Application That Works Incorrectly (Duplicate Counting)

In Figure 2-2, after the first rising edge of Gate, no Source pulses occur, so the counter does not write the correct data to the buffer.

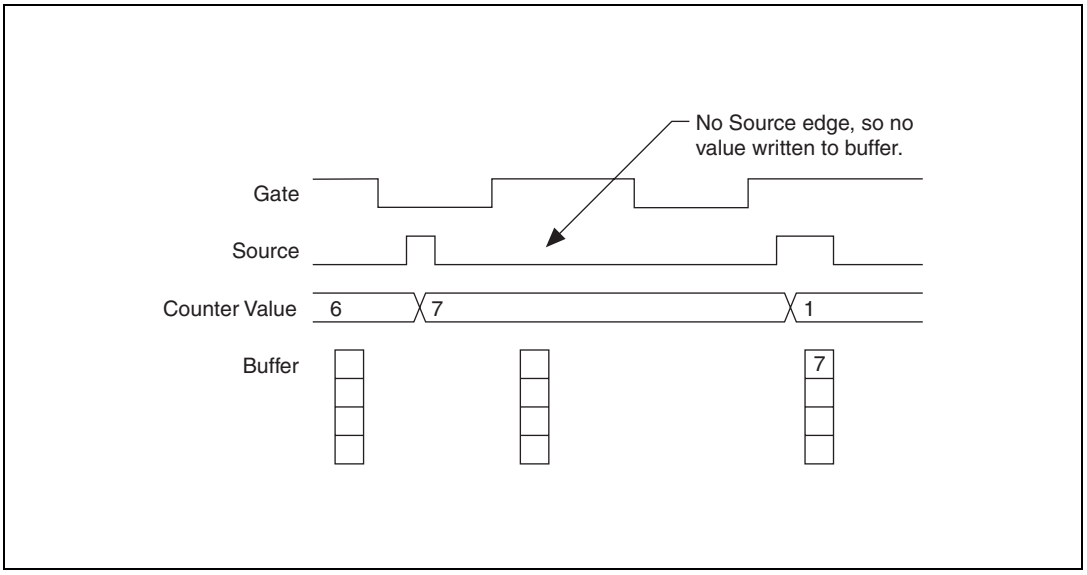


Figure 2-2. Example Application That Works Incorrectly

Example Application That Prevents Duplicate Counting

With duplicate count prevention enabled, the counter synchronizes both the Source and Gate signals to the maximum onboard timebase. By synchronizing to the timebase, the counter detects edges on the Gate even if the Source does not pulse. This enables the correct current count to be

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stored in the buffer even if no Source edges occur between Gate signals. Figure 2-3 shows an example application that prevents duplicate counting.

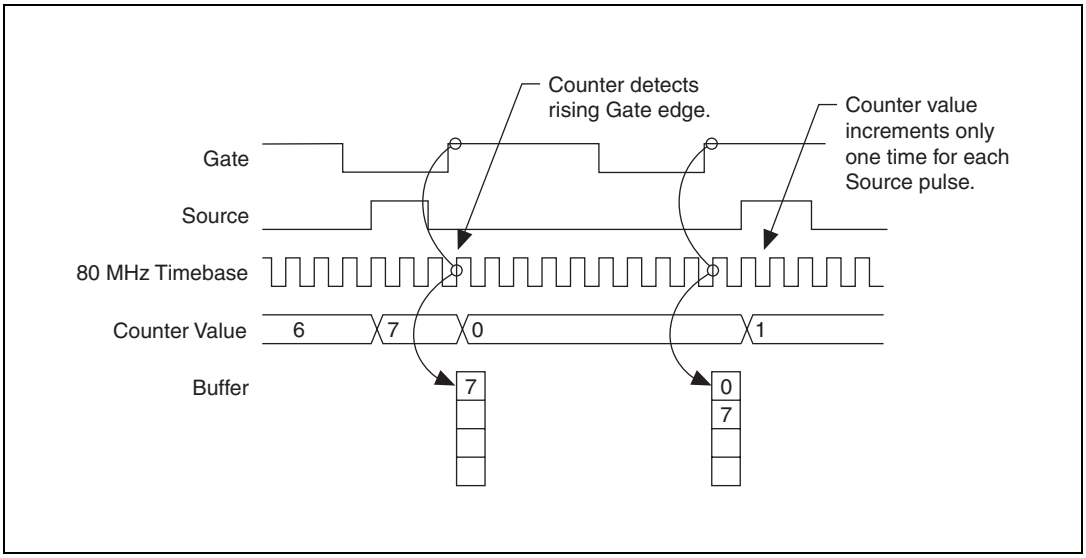


Figure 2-3. Example Application That Prevents Duplicate Counting

Even if the Source pulses are long, the counter increments only once for each source pulse.

Normally, the counter and Counter *n* Internal Output signals change synchronously to the Source signal. With duplicate count prevention, the counter value and Counter *n* Internal Output signals change synchronously to the maximum onboard timebase.

Notice that duplicate count prevention should only be used if the frequency of the Source signal is one-fourth of the maximum onboard timebase.

Enabling Duplicate Count Prevention in NI-DAQmx

You can enable duplicate count prevention in NI-DAQmx by setting the **Enable Duplicate Count Prevention** attribute/property. For specific information on finding the **Enable Duplicate Count Prevention** attribute/property, refer to the help file for the API you are using. Refer to the *NI-DAQmx Help* for more information.

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When to Use Duplicate Count Prevention

Use duplicate count prevention for buffered measurements that use an external Ctr*n*Source signal and the frequency of the signal is less than or equal to one-fourth of the maximum onboard timebase. Use this mode if you are using a low frequency or you expect zero Ctr*n*Source edges between successive edges of the Ctr*n*Gate signal.

You should use duplicate count prevention if the following conditions are true:

- You are making a buffered counter input measurement
- You are using an external signal (such as PFI *x*) as the counter Source
- The frequency of the external source is one-fourth of the maximum onboard timebase
- You can have the counter value and output to change synchronously with the maximum onboard timebase

In all other cases, do *not* enable duplicate count prevention.

When Not to Use Duplicate Count Prevention

Use duplicate counter prevention only for buffered measurements with an external Ctr*n*Source signal. Do not use it when the Ctr*n*Source signal is greater than one-fourth of the maximum timebase.

Transfer Rates

The maximum sustainable transfer rate the NI 6624 device can achieve for a buffered acquisition depends on the following factors:

- Amount of available bus bandwidth
- Processor speed and operating system
- Application software

To reduce the amount of bus activity, limit the number of devices generating bus cycles. Because direct-memory access (DMA) transfers are faster than interrupt-driven transfers, NI-DAQmx uses DMA by default for buffered acquisitions.

Note The maximum sustainable transfer rate is always lower than the peak transfer rate.

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Table 2-1 lists the maximum transfer rates for the NI 6624 device.

Table 2-1. Maximum Transfer Rates

DMA		Interrupt	
Finite Operation			
Buffer Size (Samples)	**Rate (kS/s)**	**Buffer Size (Samples)**	**Rate (kS/s)**
100	5,000	100	77
1,000	2,150	1,000	77
10,000	1,600	10,000	77
100,000	1,350	100,000	77
Continuous Operation			
Buffer Size (Samples)	**Rate (kS/s)**	**Buffer Size (Samples)**	**Rate (kS/s)**
100	44	100	7
1,000	202	1,000	46
10,000	212	10,000	75
100,000	245	100,000	76
default	212	default	75

Note Transfer rates may vary depending on your computer hardware, operating system and system activity. This benchmark data was determined on an AMD Athlon XP 1800 computer with 128 MB of PC-2100 DDR RAM running Windows XP and LabVIEW using one counter of the TIO device. For continuous measurements, the transfer rate is the maximum sustained rate for 30 seconds on one counter. The maximum sustainable transfer rates for the NI 6624 were found using internal signals to provide the stimulus for the measurement. The numbers do not reflect the transfer rates through the optical isolation.

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3

Signal Connections

This chapter describes how to make input and output signal connections to the NI 6624 device by way of the device I/O connector and the RTSI connector.

Programmable Function Interfaces (PFIs)

The NI 6624 has 34 PFI lines, with 26 inputs and eight outputs. The PFI lines are unidirectional. They are set either as inputs or outputs. An input cannot be configured as an output and an output cannot be configured as an input through software.

Digital Filtering

Each PFI line coming from the I/O connector can be passed through a simple digital debouncing filter. The filter operates off a filter clock and a fast internal sampling clock. The filter circuit samples the signal on the PFI line on each rising edge of the sampling clock. A change in the signal is propagated only if it maintains its new state for at least the duration between two consecutive rising edges of the filter clock timebase. The frequency of the filter clock timebase determines whether a transition in the signal may propagate or not. The function of the internal sampling clock is to increase the sampling rate and prevent aliasing.

Figure 3-1 demonstrates the function of this filter.

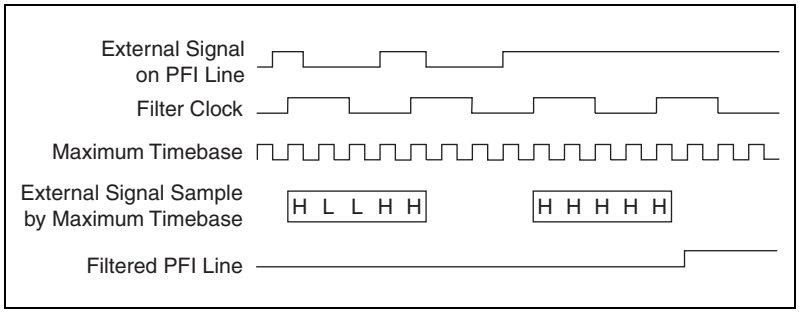


Figure 3-1. Digital Filtering

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In Figure 3-1, the low-to-high transition is guaranteed to be passed through only if the signal remains high for at least two periods of the filter clock timebase and is sampled high at each sampling clock rising edge during this time. Although the low-to-high transition is shown in this example, the same is true for high-to-low transitions.

Note The effect of filtering is that the signal transition is shifted by two filter clock timebase periods.

The figure shows that if sampling was done at each rising edge of the filter clock timebase alone, the first two pulses would have been seen as one continuous transition. However, using the faster sampling clock detects the glitch; thus, the two short pulses are ignored.

The intent of the filter is to eliminate glitches that may appear on a signal. The filter is sensitive to the duration for which a digital signal transitions from one state to another. If a square wave is applied to the filter, its propagation will depend on its frequency and duty cycle.

There are four filter settings available in the TIO devices: 5 µs, 1 µs, 500 ns, and 100 ns. The 5 µs filter will pass all pulse widths (high and low) that are 5 µs or longer. It will block all pulse widths that are 2.5 µs (one-half of 5 µs) or shorter. Pulse widths between 2.5 µs and 5 µs may or may not pass, depending on the phase of the pulse with respect to the filter clock timebase. The same relationship extends to all other filter clocks.

In addition to these hard-wired filter clocks, you can use any PFI, RTSI, or internal signal as the source for the filter clock timebase. Use signals with a duty cycle as close to 50 percent as possible.

If the period of the filter clock timebase is $t_{fltrclk}$, this filter guarantees to pass pulse widths that are $2*t_{fltrclk}$ or longer and to block pulse widths that are $t_{fltrclk}$ or shorter. A pulse with a width between these two ranges may or may not pass, depending on the phase of the pulse with respect to the filter clock timebase.

Table 3-1 summarizes the properties of the different filter settings.

Table 3-1. Filter Settings

Filter Setting	Pulse Width Passed	Pulse Width Blocked
5 µs	5 µs	2.5 µs
1 µs	1 µs	500 ns

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Table 3-1. Filter Settings (Continued)

Filter Setting	Pulse Width Passed	Pulse Width Blocked
500 ns	500 ns	250 ns
100 ns	100 ns	50 ns
Programmable setting with period of clock = $t_{fltrclk}$	$2*t_{fltrclk}$	$t_{fltrclk}$

You individually configure the filter setting for each PFI line. The filters are useful to maintain signal integrity. They can prevent measurement errors caused by noise, crosstalk, or transmission line effects.

Note The NI 6624 has 1 µs digital filters enabled on all PFI lines by default.

For more information about using the digital filters on your device, refer to *Digital Filtering for Counters* in the *NI-DAQmx Help*.

Power-On State

When the NI 6624 is powered on, the lines are in the following states:

- **Initial input state**—At power-on, all input lines are pulled low if nothing is driving them externally, for example, through the I/O connector.
- **Initial output state**—At power-on, all output lines are off.
- **Initial RTSI state**—At power-on, all RTSI lines are at high impedance. The voltage levels of the RTSI lines are pulled high.
- **Initial PFI state**—At power-on, all PFI lines are active high unless configured otherwise by software. An active level (1) corresponds to a high voltage, and an inactive level (0) corresponds to a low voltage.

Note After an output is used, its default state as determined by the driver becomes LOW, the output MOSFET being ON. If such a behavior is undesirable—because of continuous power dissipation in the load, for example—you can change this default state to HIGH, switching the output MOSFET to OFF, through software.

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Pin Assignments

Table 3-2 lists the NI 6624 I/O connector pin assignments.

Table 3-2. NI 6624 Connector Pin Assignments

Signal Name	Motion Encoder Context	Counter Context (Default)	Pin Number	Pin Number	Counter Context (Default)	Motion Encoder Context	Signal Name
PFI 39+	channel A(0)+	CTR 0 SRC+	1	51	CTR 4 SRC+	channel A(4)+	PFI 23+
PFI 39–	channel A(0)–	CTR 0 SRC–	2	52	CTR 4 SRC–	channel A(4)–	PFI 23–
PFI 38+	index/z(0)+	CTR 0 GATE+	3	53	CTR 4 GATE+	index/z(4)+	PFI 22+
PFI 38–	index/z(0)–	CTR 0 GATE–	4	54	CTR 4 GATE–	index/z(4)–	PFI 22–
PFI 37+	channel B(0)+	CTR 0 AUX+	5	55	CTR 4 AUX+	channel B(4)+	PFI 21+
PFI 37–	channel B(0)–	CTR 0 AUX–	6	56	CTR 4 AUX–	channel B(4)–	PFI 21–
PFI 36 Vdd	—	CTR 0 Vdd	7	57	CTR 4 Vdd	—	PFI 20 Vdd
PFI 36 Vss	—	CTR 0 Vss	8	58	CTR 4 Vss	—	PFI 20 Vss
PFI 36	—	CTR 0 OUT	9	59	CTR 4 OUT	—	PFI 20
PFI 36 Vss	—	CTR 0 Vss	10	60	CTR 4 Vss	—	PFI 20 Vss
PFI 35+	channel A(1)+	CTR 1 SRC+	11	61	CTR 5 SRC+	channel A(5)+	PFI 19+
PFI 35–	channel A(1)–	CTR 1 SRC–	12	62	CTR 5 SRC–	channel A(5)–	PFI 19–
PFI 34+	index/z (1)+	CTR 1 GATE+	13	63	CTR 5 GATE+	index/z(5)+	PFI 18+
PFI 34–	index/z (1)–	CTR 1 GATE–	14	64	CTR 5 GATE–	index/z(5)–	PFI 18–
PFI 33+	channel B(1)+	CTR 1 AUX+	15	65	CTR 5 AUX+	channel B(5)+	PFI 17+

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Table 3-2. NI 6624 Connector Pin Assignments (Continued)

Signal Name	Motion Encoder Context	Counter Context (Default)	Pin Number	Pin Number	Counter Context (Default)	Motion Encoder Context	Signal Name
PFI 33–	channel B(1)–	CTR 1 AUX–	16	66	CTR 5 AUX–	channel B(5)–	PFI 17–
PFI 32 Vdd	—	CTR 1 Vdd	17	67	CTR 5 Vdd	—	PFI 16 Vdd
PFI 32 Vss	—	CTR 1 Vss	18	68	CTR 5 Vss	—	PFI 16 Vss
PFI 32	—	CTR 1 OUT	19	69	CTR 5 OUT	—	PFI 16
PFI 32 Vss	—	CTR 1 Vss	20	70	CTR 5 Vss	—	PFI 16 Vss
PFI 31+	channel A(2)+	CTR 2 SRC+	21	71	CTR 6 SRC+	channel A(6)+	PFI 15+
PFI 31–	channel A(2)–	CTR 2 SRC–	22	72	CTR 6 SRC+	channel A(6)–	PFI 15–
PFI 30+	index/z (2)+	CTR 2 GATE+	23	73	CTR 6 GATE+	index/z(6)+	PFI 14+
PFI 30–	index/z (2)–	CTR 2 GATE–	24	74	CTR 6 GATE–	index/z(6)–	PFI 14–
PFI 29+	channel B(2)+	CTR 2 AUX+	25	75	CTR 6 AUX+	channel B(6)+	PFI 13+
PFI 29–	channel B(2)–	CTR 2 AUX–	26	76	CTR 6 AUX–	channel B(6)–	PFI 13–
PFI 28 Vdd	—	CTR 2 Vdd	27	77	CTR 6 Vdd	—	PFI 12 Vdd
PFI 28 Vss	—	CTR 2 Vss	28	78	CTR 6 VSS	—	PFI 12 Vss
PFI 28	—	CTR 2 OUT	29	79	CTR 6 OUT	—	PFI 12
PFI 28 Vss	—	CTR 2 Vss	30	80	CTR 6 Vss	—	PFI 12 Vss
PFI 27+	channel A(3)+	CTR 3 SRC+	31	81	CTR 7 SRC+	channel A(7)+	PFI 11+
PFI 27–	channel A(3)–	CTR 3 SRC–	32	82	CTR 7 SRC–	channel A(7)–	PFI 11–

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Table 3-2. NI 6624 Connector Pin Assignments (Continued)

Signal Name	Motion Encoder Context	Counter Context (Default)	Pin Number	Pin Number	Counter Context (Default)	Motion Encoder Context	Signal Name
PFI 26+	index/z (3)+	CTR 3 GATE+	33	83	CTR 7 GATE+	index/z(7)+	PFI 10+
PFI 26–	index/z (3)–	CTR 3 GATE–	34	84	CTR 7 GATE–	index/z(7)–	PFI 10–
PFI 25+	channel B(3)+	CTR 3 AUX+	35	85	CTR 7 AUX+	channel B(7)+	PFI 9+
PFI 25–	channel B(3)–	CTR 3 AUX–	36	86	CTR 7 AUX–	channel B(7)–	PFI 9–
PFI 24 Vdd	—	CTR 3 Vdd	37	87	CTR 7 Vdd	—	PFI 8 Vdd
PFI 24 Vss	—	CTR 3 Vss	38	88	CTR 7 Vss	—	PFI 8 Vss
PFI 24	—	CTR 3 OUT	39	89	CTR 7 OUT	—	PFI 8
PFI 24 Vss	—	CTR 3 Vss	40	90	CTR 7 Vss	—	PFI 8 Vss
PFI 0+	—	—	41	91	—	—	PFI 4+
PFI 0–	—	—	42	92	—	—	PFI 4–
NC	—	—	43	93	—	—	NC
NC	—	—	44	94	—	—	NC
NC	—	—	45	95	—	—	NC
NC	—	—	46	96	—	—	NC
NC	—	—	47	97	—	—	NC
NC	—	—	48	98	—	—	NC
NC	—	—	49	99	—	—	NC
NC	—	—	50	100	—	—	NC

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I/O Connector Pinout

Figure 3-2 shows the NI 6624 I/O connector pin assignments.

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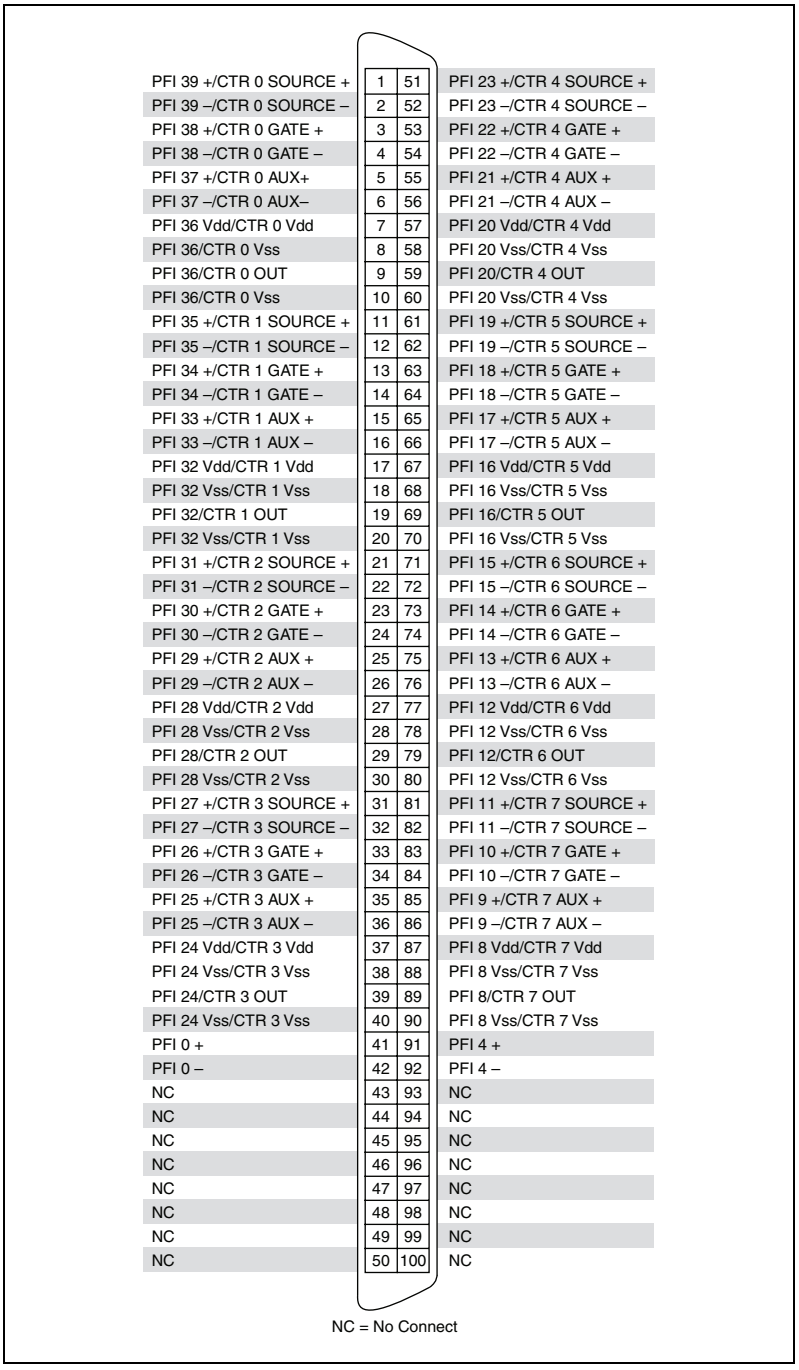


Figure 3-2. NI 6624 Connector Pinout

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Inputs

The inputs on the NI 6624 can be driven referenced to either the supply or ground of the external device connected to them. They have a current limiter that protects the optical isolator. The optical isolator transfers the externally connected signals to the TIO. A diode protects against reverse connected signals.

Figure 3-3 shows a single NI 6624 isolated input.

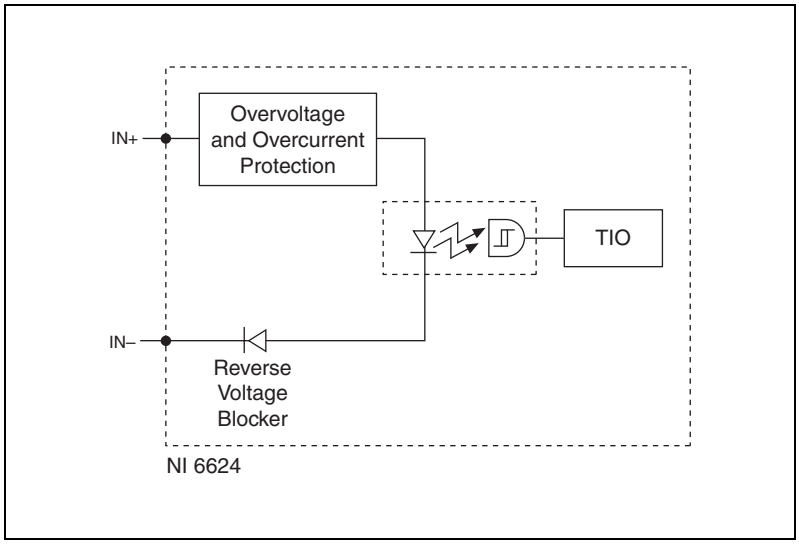


Figure 3-3. NI 6624 Isolated Input

Inputs can be connected to be referenced to either the supply or ground of the external device, depending on whether or not this device can source the amount of current required by the NI 6624 input circuitry. The minimum amount of current required by the NI 6624 inputs to guarantee a digital HIGH is 2.2 mA. The overvoltage and overcurrent protector does not allow the amount of current flowing through the input circuitry to exceed 10 mA.

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Use the following guidelines for connecting the NI 6624 to be referenced to either the supply or ground.

Connecting the NI 6624 as Referenced to Ground

Connect the external device to the IN+ pin, and connect the device ground to the IN– pin, as shown in Figure 3-4.

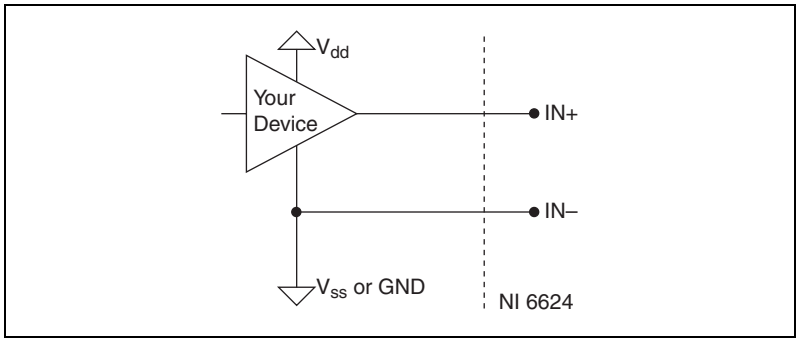


Figure 3-4. Connecting as Referenced to Ground

Connecting the NI 6624 as Referenced to the Supply

Connect the Vdd on the external device to the NI 6624 IN+, and connect the output of the external device to the IN– pin, as shown in Figure 3-5.

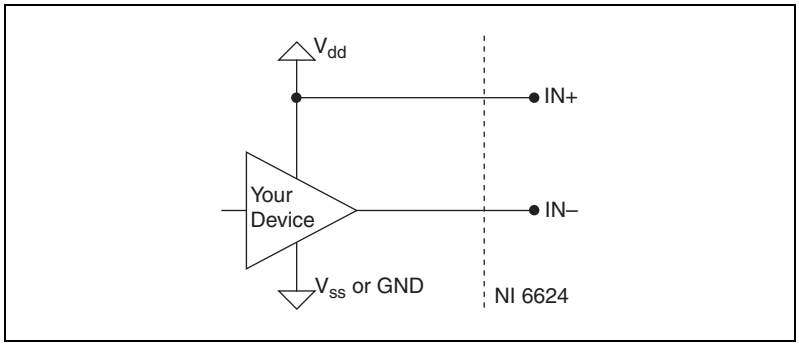


Figure 3-5. Connecting as Referenced to the Supply

Note Connecting the NI 6624 as referenced to the supply reverses the digital logic. To operate the NI 6624 with TTL devices, connect the NI 6624 as referenced to the supply.

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Outputs

The outputs on the NI 6624 consist of N-channel MOSFETs that are connected as low-side switches. A Schottky diode blocks reverse connections.

Figure 3-6 shows an example of connecting a single NI 6624 isolated output.

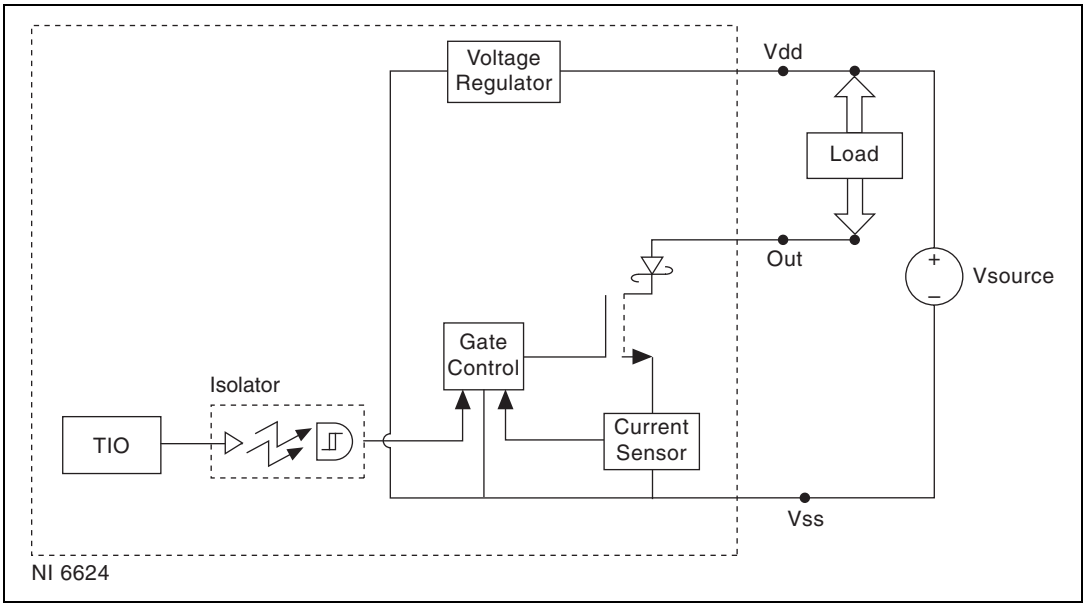


Figure 3-6. Connecting a Single NI 6624 Isolated Output

In order for the output circuit to function, you must provide and connect 5 to 48 V between Vdd and Vss. Reverse connections of Vdd and Vss do not damage the circuit as long as these connections do not exceed the 60 VDC, as listed in the *NI 6624 Specifications* document, available for download from `ni.com/manuals`.

If the amount of current the MOSFET conducts exceeds a certain level (800 mA, typical), such as when a short occurs in the load, the MOSFET turns off for 250 ms to protect itself and the load. After this period of time, the output tries to switch on. If the short still exists, it will be turned off for another 250 ms. This process continues until the overcurrent or short condition is removed, after which switching automatically resumes.

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Note Add bypass capacitor(s) between Vdd and Vss at the load to reduce the chances of ringing when the output switches on and off, especially when the connecting wires are long.

Note After you use an output, its default state as determined by the driver becomes LOW, the output MOSFET being ON. If you want to change this state, for example to eliminate continuous power dissipation in the load during the idle state, you can change the default to HIGH, switching the output MOSFET to OFF, through software.

Note NI recommends that you connect both Vss terminals at the connector block to the available reference or ground, and keep all connections as short as possible. For more information about connections to inductive loads, refer to the *Driving Inductive Loads* section of this document.

Driving Inductive Loads

When one of the outputs on the NI 6624 is driving a fairly inductive load, make sure that the high voltages that appear because of suddenly switching the current through the inductor do not cause damage to the output circuit or the load. You can avoid this problem by adding flyback diodes across your inductive load as shown in Figure 3-7.

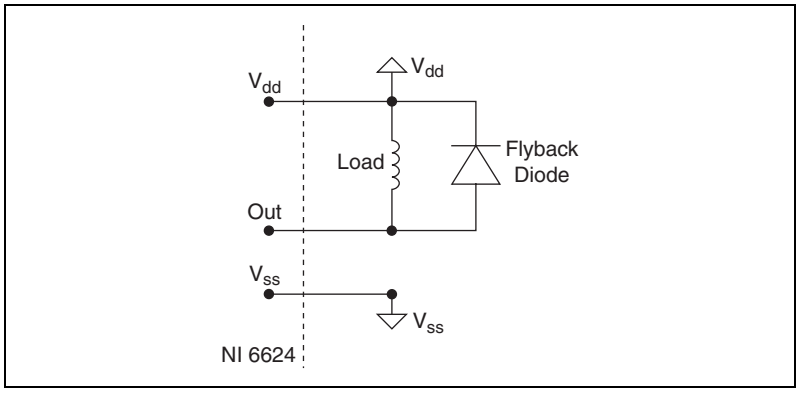


Figure 3-7. Adding Flyback Diodes across Inductive Load

Note Ensure the diode you chose is capable of handling the amount of current the load is holding when the output is ON.

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Input Threshold Voltage

When you want a threshold higher than the default (4 V max for HIGH), you can insert a zener diode in series with an input to shift its threshold by the zener breakdown voltage. You can install the zener diode in the connector block. Figure 3-8 shows the polarity of the zener diode with respect to the NI 6624 input.

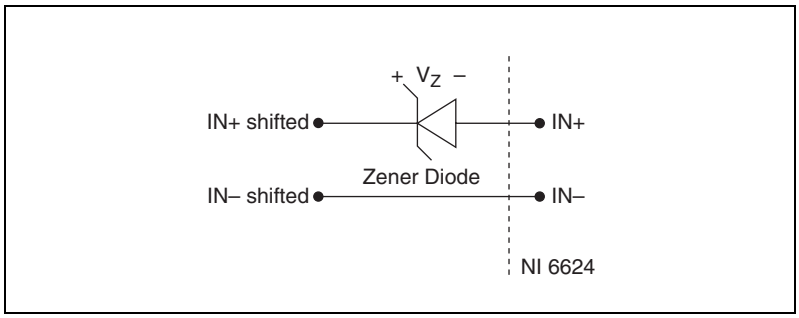


Figure 3-8. Polarity of Zener Diode with Respect to NI 6624 Input

After inserting the zener diode, the new threshold becomes 4 + V_Z. For example, if you choose the zener diode such that V_Z is approximately equal to 7.5 V when its current, I_Z, varies from 1–10 mA, the threshold voltage between IN+ shifted and IN– shifted is approximately 4 + 7.5, 11.5 V.

Counters

The counters on TIO devices are a superset of the DAQ system timing controller (DAQ-STC) general-purpose counters developed by National Instruments. These counters are backward compatible with the DAQ-STC in functionality and software programming. The same software API and functions are used to program the DAQ-STC general-purpose counters and the counters on TIO devices.

The counters on TIO devices have two internal timebases: 100 kHz and 20 MHz. Each counter has a gate, auxiliary, and source input. Each of these inputs can be an internal or external signal that connects to the I/O connector. Each counter also has an output signal.

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Counter *n* Source Signal

You can select any PFI as well as many other internal signals as the Counter *n* Source (Ctr*n*Source) signal. The Ctr*n*Source signal is configured in edge-detection mode on either the rising or falling edge. The selected edge of the Ctr*n*Source signal increments and decrements the counter value depending on the application the counter is performing.

You can export the Ctr*n*Source signal to the I/O connector's default PFI input for each Ctr*n*Source. For example, you can export the Ctr0Source signal to the PFI 39/CTR 0 SRC pin, even if another PFI is inputting the Ctr0Source signal. This output is set to high-impedance at startup.

For most applications, unless you select an external source, the 80MHzTimebase signal (if available), 20MHzTimebase signal, or 100kHzTimebase signal generates the Ctr*n*Source signal.

Figure 3-9 shows the timing requirements for the Ctr*n*Source signal.

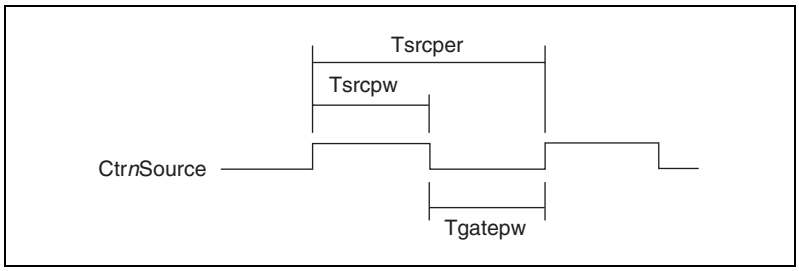


Figure 3-9. Timing Requirements for Ctr*n*Source Signal

Figure 3-9 shows the minimum period and pulse width that you must use for the Ctr*n*Source signal. This signal must satisfy both minimum criteria. If the high phase of the Ctr*n*Source signal is Tsrcpw ns, the low phase must be Tsrcper – Tsrcpw.

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The minimum pulse width and period listed in Table 3-3 is the minimum required for the internal signals. The TIO device has signal requirements in order to pass through the isolation circuitry. For more information about these signal requirements, refer to the *NI 6624 Specifications* document, which is available at `ni.com/manuals`.

Table 3-3. Minimum Pulse Width Signal for Ctr*n*Source Internal Signals

Parameter	Minimum	Minimum with RTSI Connector	Description
Tsrcpw (without prescaling)	1 µs	5 ns	Ctr*n*Source minimum pulse width (without prescaling)
Tsrcpw (with prescaling)	1 µs	3.5 ns	Ctr*n*Source minimum pulse width (with prescaling)
Tsrcper (without prescaling)	2 µs	50 ns	Ctr*n*Source minimum period (without prescaling)
Tsrcper (with prescaling)	2 µs	16.67 ns	Ctr*n*Source minimum period (with prescaling)

Counter Source to Counter Out Delay

Figure 3-10 shows the Ctr*n*Source to Ctr*n*InternalOutput delay.

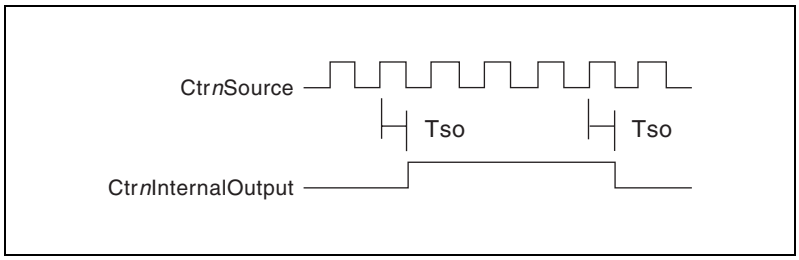


Figure 3-10. Ctr*n*Source to Ctr*n*InternalOutput Delay

Figure 3-10 shows the delay between the active edge of the Ctr*n*Source signal and the active edge of the Ctr*n*InternalOutput signal. In the figure, the Ctr*n*Source and Ctr*n*InternalOutput signals are active high. If you use the pulse output mode for the Ctr*n*InternalOutput signal, you will see the TC pulse one Ctr*n*Source period before the Ctr*n*InternalOutput toggles under the toggle output mode.

The output delay listed in Table 3-4 is for internal signals. The corresponding delay values at a connector block are larger due to cable

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delays. The TIO device's isolation circuitry delays the signals further. For more information about these signal delays, refer to the *NI 6624 Specifications* document, available for download at `ni.com/manuals`.

Table 3-4. Output Delay for Internal Signals

Parameter	Typical	Maximum	Description
Tso	16 ns	26 ns	Ctr*n*Source to Ctr*n*InternalOutput delay

Note When using duplicate count prevention mode, the minimum period of signal used as the source of the counter must be greater than or equal to four times the period of the maximum timebase. For more information, refer to the *Duplicate Count Prevention* section of Chapter 2, *Device Overview*.

Note You cannot export the Ctr*n*Source signal to the I/O connector on the NI 6624.

Counter *n* Gate Signal

You can select any PFI or RTSI, as well as many other internal signals like the Counter *n* Gate (Ctr*n*Gate) signal. The Ctr*n*Gate signal is configured in edge-detection or level-detection mode depending on the application performed by the counter. The gate signal can perform many different operations, including starting and stopping the counter, generating interrupts, and saving the counter contents.

You can export the Ctr*n*Gate signal to the I/O connector's default PFI input for each Ctr*n*Gate. For example, you can export the gate signal connected to counter 0 to the PFI 38/CTR 0 GATE pin, even if another PFI is inputting the Ctr0Gate signal. This output is set to high-impedance at startup.

Figure 3-11 shows the timing requirements for the Ctr*n*Gate signal.

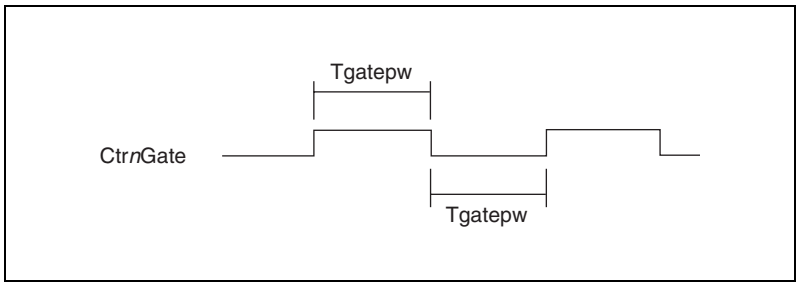


Figure 3-11. Timing Requirements for Ctr*n*Gate Signal

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The minimum pulse width and period listed in Table 3-5 is the minimum required for the internal signals. The NI 6624 has signal requirements in order to pass through the isolation circuitry. For more information about these signal requirements, refer to the *NI 6624 Specifications* document, available for download from `ni.com/manuals`.

Table 3-5. Minimum Pulse Width for Ctr*n*Gate Internal Signals

Parameter	Minimum	Minimum with RTSI Connector	Description
Tgatepw	1 µs	5 ns	Ctr*n*Gate minimum pulse width

Note For buffered measurements, the minimum period required for the Ctr*n*Gate signal is determined by how fast the system can transfer data from your device to computer memory.

Counter *n* Auxiliary Signal

You can select any PFI or RTSI, as well as many other internal signals as the Counter *n* Auxiliary (Ctr*n*Aux) signal. Much like this Ctr*n*Gate signal, the Ctr*n*Aux signal is configured in edge-detection or level-detection mode depending on the application performed by the counter. The aux signal can perform many different operations including starting and stopping the counter, generating interrupts, and saving the counter contents. You can also use this signal to control the counting direction in edge-counting applications.

Figure 3-12 shows the timing requirements for the Ctr*n*Aux signal.

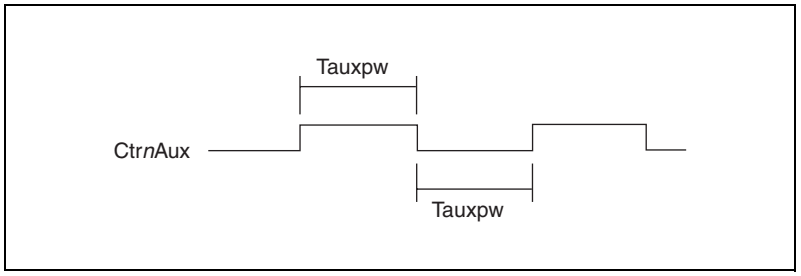


Figure 3-12. Timing Requirements for the Ctr*n*Aux Signal

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Table 3-6. Minimum Pulse Width for Ctr*n*Aux Internal Signals

Parameter	Minimum	Minimum with RTSI Connector	Description
Tauxpw	1 µs	5 ns	Ctr*n*Aux minimum pulse width

Counter *n* Internal Output Signal

The Counter *n* Internal Output (Ctr*n*InternalOutput) signal is available only as an output on the CTR *n* OUT pin, where *n* is the number of your counter. For example, the Ctr0InternalOutput signal is available as an output on the PFI 36/CTR 0 OUT pin. You can also route the Ctr*n*InternalOutput signal to other locations on the board, such as RTSI.

The Ctr*n*InternalOutput signal reflects the terminal counter (TC) of counter *n*. The counter generates a terminal count when its count value rolls over. The two software-selectable output options are pulse on TC and toggle output polarity on TC. The output polarity is software-selectable for both options. This output is set to high-impedance at startup.

Hardware Arm Start Triggers

You can arm each counter using a software command or by using the Arm Start Trigger. The Arm Start Trigger may be an internal or an external signal. By using the Arm Start Trigger, you can start more than one counter simultaneously by configuring each counter to use the same Arm Start Trigger signal.

Counter Pairs

Each counter on the NI 6624 is paired with another counter. This pairing allows some counter signals to connect to signals on the other counter. The counters are paired as shown in Table 3-7.

Table 3-7. Counter Pairs

ctr0	ctr1
ctr2	ctr3
ctr4	ctr5
ctr6	ctr7

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Ctr0InternalOutput, which you can connect to Ctr1Gate, is an example of two signals that you can connect between the ctr0/ctr1 pair. Conversely, to connect Ctr0InternalOutput to Ctr2Gate, you must use other circuitry on the NI 6624 device (such as RTSI Triggers).

Counter Applications

You can use the NI 6624 device in the following counter-based applications:

- Counting Edges
- Frequency Measurement
- Period Measurement
- Position Measurement with Linear and Angular Encoders[1]
- Pulse Width Measurement
- Semi-Period Measurement
- Two-Edge Separation Measurement
- Pulse Generation

You can perform these measurements through programmed I/O, interrupt, or DMA data transfer mechanisms. The measurements can be finite or continuous in duration. Some of the applications also use start triggers, pause triggers, and hardware arm triggers.

Note For more information about programming counter applications and triggers in software, refer to the *NI-DAQmx Help*, and/or use the examples that are available with NI-DAQmx.

Real-Time System Integration Bus

TIO devices use the National Instruments Real-Time System Integration (RTSI) bus to easily synchronize several measurement functions to a common trigger or timing event. In a PCI system, the RTSI bus consists of the RTSI bus interface and a ribbon cable. The bus can route timing and trigger signals between several functions on as many as five DAQ devices in the computer. In a PXI system, the RTSI bus consists of the RTSI bus

[1] When used with the NI 6624, the encoder should be able to drive the minimum 2.2 mA required by the NI 6624. Refer to the *Inputs* section for more information. If the encoder cannot drive but can sink that amount of current, then the NI 6624 can be connected as referenced to the supply. In this case, the signals read by the NI 6624 are inverted. The index (z) input should always be positive logic in order for the encoder input of the NI 6624 to operate properly. This means that the index (z) will not work when referenced to the supply, and as a result, should be left disconnected.

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interface and the PXI trigger signals on the PXI backplane. This bus can route timing and trigger signals between several functions on as many as seven DAQ devices in the system. For a RTSI connector pinout, go to `ni.com/info` and enter `rtsipin`.

RTSI Triggers

TIO devices require a frequency timebase for its operation. This frequency timebase must come from the onboard crystal oscillator and is required even if the device is receiving a MasterTimebase signal from the RTSI trigger bus. Any TIO device can drive its 20MHzTimebase signal onto the RTSI Trigger 7 pin. Although some TIO devices have a 80MHzTimebase, the RTSI bus cannot carry the 80MHzTimebase signal for bandwidth reasons. By default, TIO devices do not drive the RTSI Trigger 7 bus clock line.

Figure 3-13 shows the RTSI signal connection scheme for PCI TIO devices.

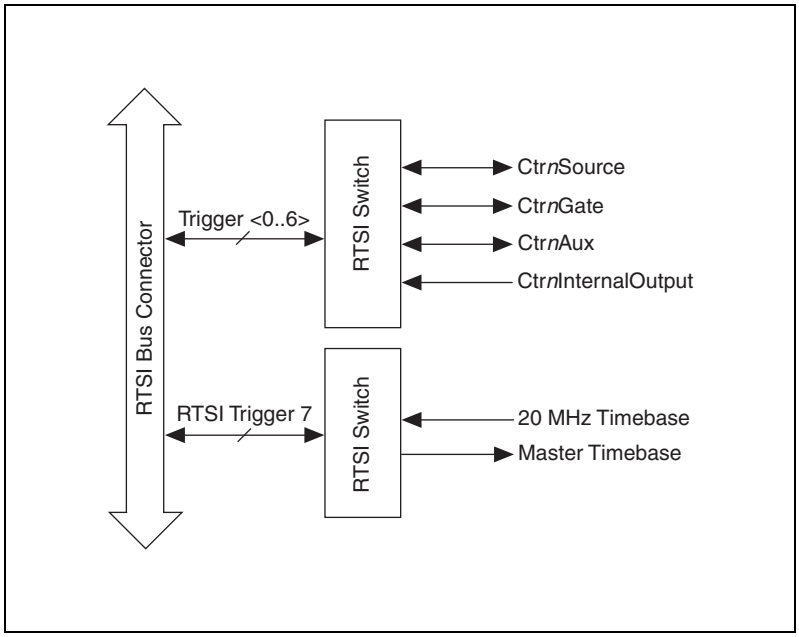


Figure 3-13. RTSI Signal Connection Scheme for PCI

PXI TIO devices use PXI trigger line 7 as their RTSI clock line. The maximum timebase provided by the PXI TIO device is phase locked to the 10 MHz PXI backplane clock. By using other PXI modules that phase lock

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their board clocks to the 10 MHz PXI backplane clock, you can better synchronize operation in a multi-module PXI system. The phase locking is enabled by default and can be disabled by way of software. If the module is used in a compact PCI chassis that does not have the 10 MHz PXI backplane clock, the phase locking is automatically disabled. Additionally, PXI trigger line 6 corresponds to PXI star trigger on PXI TIO devices.

Figure 3-14 shows the RTSI signal connection scheme for PXI TIO devices.

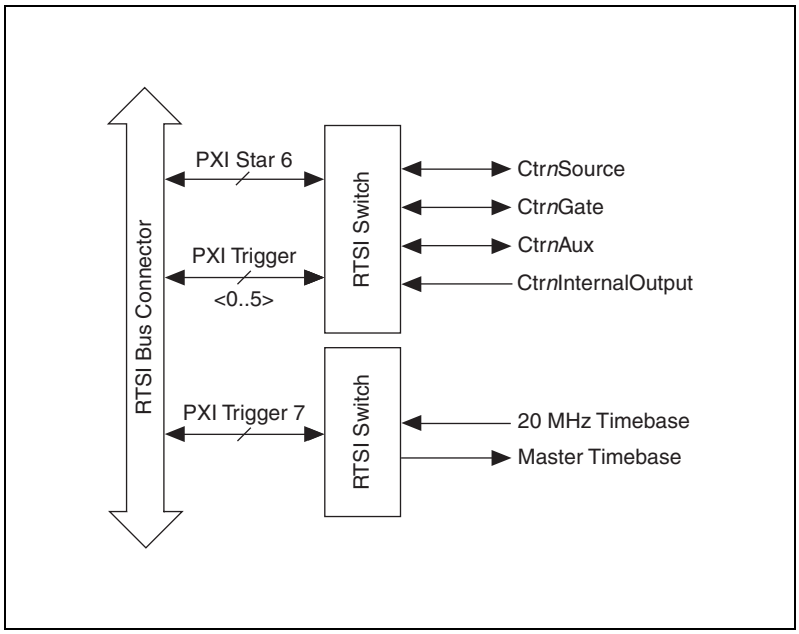


Figure 3-14. RTSI Signal Connection for PXI

I/O Signals

Field Wiring Considerations

To prevent incorrect results caused by environmental noise and crosstalk, make sure the NI 6624 and the peripheral device share a common ground reference. Connect one or more NI 6624 device D GND lines to the ground reference of your peripheral device.

You can also use the digital filters available on each PFI line to reduce errors that these problems might cause.

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Noise

For noise immunity, take the following precautions:

- When routing signals to the NI 6624 device, keep cabling away from noise sources.
- Separate the NI 6624 device signal lines from high-current or high-voltage lines. High-current or high-voltage lines that run in parallel paths at a close distance can induce currents in or voltages on the NI 6624 device signal lines. To reduce the coupling between lines, separate parallel lines by a reasonable distance or run the lines at right angles to one another.
- Do not run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic and electric fields caused by monitors, electric motors, welding equipment, breakers, transformers, or other devices by running them through special metal conduits.
- Use appropriate digital filtering to remove noise.

Crosstalk

Crosstalk mainly occurs when the capacitance between lines in a cable induces a smaller transition on another line. Figure 3-15 shows an example of crosstalk.

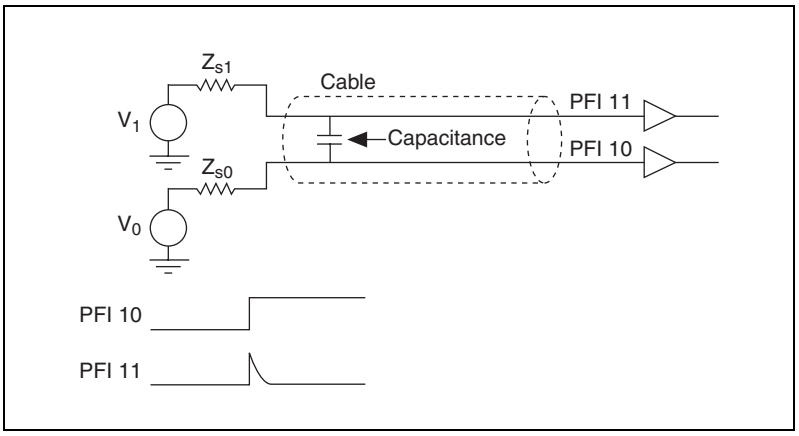


Figure 3-15. Crosstalk Example

In Figure 3-15, PFI 10 and PFI 11 are configured as inputs. V_0 drives PFI 10 and V_1 drives PFI 11. When PFI 10 (the offending line) transitions from one state to another, it induces a small transition in PFI 11 (the victim

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line). The magnitude of the transition (or crosstalk) induced in PFI 11 is proportional to the following:

- The speed of the transition on the offending line (PFI 10 in the previous example)
- The length of the cable and the proximity of the victim to the offending line
- The source impedance of the victim line (V_1 in the previous example) and the level of the offending line (V_0)

Crosstalk most often causes measurement errors when the victim line is connected to a slowly changing signal.

When any of the outputs is running at higher than 5 V, and/or when fast-edged signals are mixed with slow-edged signals at the inputs, the latter ones should be digitally filtered. You can reduce crosstalk-related problems by using a ribbon cable and separating the fast-edged and slow-edged signals on the cable. For example, when you use PFI 12 as an output, you should avoid connecting a slowly changing signal to either PFI 11 or PFI 13. As another example, if you are connecting a fast-edged signal to PFI 10, you should avoid connecting a slowly changing signal to either PFI 9 or PFI 11.

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A

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Glossary

Symbol	Prefix	Value
c	centi	10^{-2}
m	milli	10^{-3}
µ	micro	10^{-6}
n	nano	10^{-9}
k	kilo	10^{3}
M	mega	10^{6}

Symbols

°	degree
–	negative of, or minus
/	per
%	percent
±	plus or minus
+	positive of, or plus

A

A	amperes
ANSI	American National Standards Institute
API	application programming interface
arm	To enable a counter to start an operation. If the application requires a trigger, an armed counter waits for the trigger to begin the operation.
ASIC	application specific integrated circuit

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asynchronous	A property of an event that occurs at an arbitrary time, without synchronization to a reference clock.

B

b	Bit—one binary digit, either 0 or 1.
B	Byte—eight related bits of data, an eight-bit binary number. Also used to denote the amount of memory required to store one byte of data.
base address	A memory address that serves as the starting address for programmable registers. All other addresses are located by adding to the base address.
buffer	A block of memory used to store measurement results.
buffered	A type of measurement in which multiple measurements are made consecutively and measurement results are stored in a buffer.
bus	The group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. Examples of PC buses are the AT, EISA, and PCI bus.

C

C	Celsius
clock	Hardware component that provides timing for various device operations.
cm	centimeters
CMOS	complementary metal-oxide semiconductor
CompactPCI	An electrical superset of the PCI bus architecture with a mechanical form factor suited for industrial applications.
crosstalk	An unwanted signal on one channel due to activity on a different channel.
current drive capability	The amount of current a digital or analog output channel is capable of sourcing or sinking while still operating within voltage range specifications.

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current sinking	The ability of a DAQ board to dissipate current for analog or digital output signals.
current sourcing	The ability of a DAQ board to supply current for analog or digital output signals.

D

DAQ	data acquisition Collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing. Collecting and measuring the same kinds of electrical signals with A/D and/or DIO boards plugged into a computer, and possibly generating control signals with D/A and/or DIO boards in the same computer.
DAQ-STC	A custom ASIC developed by National Instruments that provides timing information and general-purpose counter/timers on National Instruments E Series boards.
DC	direct current
decode	Used in the context of motion encoders. The two channels of a motion encoder indicate information about movement and direction of movement of an external device. Decoding refers to extracting this information from the signals on these channels.
device	A plug-in data acquisition board, card, or pad that can contain multiple channels and conversion devices. Plug-in boards, PCMCIA cards, and DAQ devices that connect to your computer parallel port, are all examples of DAQ devices.
DIO	digital input/output
DLL	Dynamic link library—a software module in Microsoft Windows containing executable code and data that can be called or used by Windows applications or other DLLs. Functions and data in a DLL are loaded and linked at run time when they are referenced by a Windows application or other DLLs.

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DMA — Direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.

driver — Software that controls a specific hardware device such as a DAQ board.

E

EEPROM — Electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed.

EISA — extended industry standard architecture

encode — Used in the context of motion encoders. Motion encoders provide information about movement and direction of movement of an external device. The process of producing the pulses that contain this information is called encoding.

ETS — equivalent time sampling

F

FSK — frequency shift keying

G

GATE — The signal that controls the operation of a counter. This signal may start or stop the operation of a counter, reload the counter, or save the results of a counter.

glitch — A brief, unwanted change, or disturbance, in a signal level.

GND — ground

H

hardware — The physical components of a computer system, such as the circuit boards, plug-in boards, chassis, enclosures, peripherals, cables, and so on.

HW — hardware

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HW Save register	A register inside the NI-TIO ASIC that stores the result of a measurement.
Hz	Hertz—a unit of frequency. One hertz corresponds to one cycle or event per second.

I

I/O	Input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces.
in.	inches
interrupt	A computer signal indicating that the CPU should suspend its current task to service a designated activity.
interrupt level	The relative priority at which a device can interrupt.
IOH	current, output high
IOL	current, output low
IRQ	interrupt request signal
ISA	industry standard architecture

L

LabVIEW	Laboratory Virtual Instrument Engineering Workbench, a National Instruments graphical programming application.

M

m	meters
max	maximum
maximum timebase	The fastest internal timebase available on a device.
min	minimum

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motion encoders — Transducers that generate pulses to indicate the physical motion of a device. The most common type of motion encoders are quadrature encoders. Two-pulse encoders (also referred to as up/down encoders) are another example.

N

NI-DAQ — NI driver software for DAQ hardware.

NI-TIO — A custom ASIC developed by National Instruments that provides counter and digital I/O functionality.

noise — An undesirable electrical signal—noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, soldering irons, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.

O

OCXO — oven-controlled crystal oscillator

operating system — Base-level software that controls a computer, runs programs, interacts with users, and communicates with installed hardware or peripheral devices.

P

PCI — Peripheral component interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 Mbytes/s.

PFI — programmable function input

port — A communications connection on a computer or a remote controller.

A digital port, consisting of lines of digital input and/or output.

ppb — parts per billion

prescaling — The division of frequency of an input signal that is to be used as SOURCE of a counter.

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programmed I/O	A data transfer method in which the CPU reads or writes data as prompted by software.
PXI	Modular instrumentation standard based on CompactPCI developed by National Instruments with enhancements for instrumentation.

R

reflection	A high-speed signal transition behaves like a wave and is reflected like a wave at an inadequately terminated endpoint. This phenomenon is referred to as reflection.
RG	Reserved ground. Pins that are marked RG on the I/O connector are no-connects if you use the SH100-100-S2 shielded cable, while they are ground pins if you use the R100100 unshielded ribbon cable.
ribbon cable	A flat cable in which the conductors are side by side.
ringing	The oscillation of a signal about a high-voltage or low-voltage state immediately following a transition to that state.
RTSI Bus	Real-time system integration bus—the National Instruments timing bus that connects DAQ boards directly, by means of connectors on top of the boards, for precise synchronization of functions.

S

s	seconds
Save register	*See* HW Save register.
source	In the counter context, source refers to the signal that causes the counter to increment or decrement. In the context of signals, source refers to the device that drives a signal.
SOURCE	The signal that causes the counter to increment or decrement.
start trigger	A TTL level signal having two discrete levels, a high and a low level, that starts an operation.
synchronous	A property of an event that is synchronized to a reference clock.

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T

TC	Terminal count—a strobe that occurs when a counter reaches zero from either direction.
termination	Matching of impedances at the end of a signal path to minimize reflections.
timebase	Another term used for the SOURCE of a counter. Usually indicates an internal SOURCE provided by or derived from an onboard oscillator.
trigger	Any event that causes, starts, or stops some form of data capture.
tri-state	A third output state, other than high or low, in which the output is undriven.
TTL	transistor-transistor logic
two-pulse encoder	A motion encoder that has two channels: channels A and B. Pulses on channel A indicate movement in one direction while pulses on channel B indicate movement in the opposite direction. This type of encoder is also referred to as up down encoder.

U

unstrobed digital I/O	A type of digital input or output in which software reads or writes the digital line or port states directly, without using any handshaking or hardware-controlled timing functions. Also called immediate, nonhandshaking, or unlatched digital I/O.
UP_DOWN	The signal that determines whether a counter increments or decrements.

V

V	volts
VDC	volts direct current
Vin	volts in
VI	Virtual Instrument. A LabVIEW program; so-called because it models the appearance and function of a physical instrument.

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W

wire — Data path between nodes.

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