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PXI

NI PXI-665*x* User Manual

Timing and Synchronization Module for PXI

February 2016
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This hardware has been tested and found to comply with the applicable regulatory requirements and limits for electromagnetic compatibility (EMC) as indicated in the hardware's Declaration of Conformity (DoC)[1]. These requirements and limits are designed to provide reasonable protection against harmful interference when the hardware is operated in the intended electromagnetic environment. In special cases, for example when either highly sensitive or noisy hardware is being used in close proximity, additional mitigation measures may have to be employed to minimize the potential for electromagnetic interference.

While this hardware is compliant with the applicable regulatory EMC requirements, there is no guarantee that interference will not occur in a particular installation. To minimize the potential for the hardware to cause interference to radio and television reception or to experience unacceptable performance degradation, install and use this hardware in strict accordance with the instructions in the hardware documentation and the DoC[1].

If this hardware does cause interference with licensed radio communications services or other nearby electronics, which can be determined by turning the hardware off and on, you are encouraged to try to correct the interference by one or more of the following measures:

- Reorient the antenna of the receiver (the device suffering interference).
- Relocate the transmitter (the device generating interference) with respect to the receiver.
- Plug the transmitter into a different outlet so that the transmitter and the receiver are on different branch circuits.

Some hardware may require the use of a metal, shielded enclosure (windowless version) to meet the EMC requirements for special EMC environments such as, for marine use or in heavy industrial areas. Refer to the hardware's user documentation and the DoC[1] for product installation requirements.

When the hardware is connected to a test object or to test leads, the system may become more sensitive to disturbances or may cause interference in the local electromagnetic environment.

Operation of this hardware in a residential area is likely to cause harmful interference. Users are required to correct the interference at their own expense or cease operation of the hardware.

Changes or modifications not expressly approved by National Instruments could void the user's right to operate the hardware under the local regulatory rules.

[1] The Declaration of Conformity (DoC) contains important EMC compliance information and instructions for the user or installer. To obtain the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

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About This Manual

Thank you for purchasing the National Instruments NI PXI-665*x* Timing and Synchronization Module. The NI PXI-665x enables you to route PXI timing and trigger signals between two or more devices within a single PXI chassis or between two or more chassis. The NI PXI-665*x* can generate and route clock signals between devices in multiple chassis, providing a method to synchronize multiple devices in a multichassis PXI system.

This manual describes the electrical and mechanical aspects of the NI PXI-665*x* and contains information concerning its operation and programming.

National Instruments Documentation

The *NI PXI-665x User Manual* is one piece of the documentation set for your measurement system. You could have any of several other documents describing your hardware and software. Use the documentation you have as follows:

- Measurement hardware documentation—This documentation contains detailed information about the measurement hardware that plugs into or is connected to the computer. Use this documentation for hardware installation and configuration instructions, specifications about the measurement hardware, and application hints.
- Software documentation—Refer to the *NI-Sync User Manual*, available at `ni.com/manuals`.

You can download NI documentation from `ni.com/manuals`.

Related Documentation

The following documents contain information that you might find helpful as you read this manual:

- *PICMG 2.0 R3.0*, *CompactPCI Core Specification*, available from PICMG at `www.picmg.org`
- *PXI Specification*, Revision 2.1, available from `www.pxisa.org`
- *NI-VISA User Manual*, available from `ni.com/manuals`
- *NI-VISA Help*, included with the NI-VISA software
- *NI-Sync User Manual*, available from `ni.com/manuals`
- *NI PXI-665x Calibration Procedure*, available from `ni.com/manuals`

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1 Introduction

The NI PXI-665x enables you to route PXI timing and trigger signals between two or more devices within a single PXI chassis or between two or more chassis. The NI PXI-665*x* modules generate and route clock signals between devices in multiple chassis, providing a method for synchronizing multiple devices in a PXI system.

What You Need to Get Started

To set up and use the NI PXI-665*x*, you need the following items:

- ☐ NI PXI-665*x* Timing and Triggering Module
- ☐ *NI PXI-665x User Manual*
- ☐ NI-VISA software
- ☐ *NI-Sync* software
- ☐ One of the following software packages and documentation:
  - LabVIEW
  - LabWindows™/CVI™
  - Microsoft Visual C++ (MSVC)
- ☐ PXI chassis
- ☐ PXI embedded controller or a desktop computer connected to the PXI chassis using MXI-3 hardware

If you are using the NI PXI-665*x* in a system to synchronize NI PXI-4472, NI PXI-5112, NI PXI-5411, NI PXI-6115, or E Series DAQ modules, you can refer to the *NI-Sync User Manual*, which you can find on the *NI-Sync* CD or download from `ni.com/manuals`.

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Unpacking

The NI PXI-665*x* is shipped in an antistatic package to prevent electrostatic damage to the module. Electrostatic discharge (ESD) can damage several components on the module.

Caution *Never* touch the exposed pins of connectors.

To avoid such damage in handling the module, take the following precautions:

- Ground yourself using a grounding strap or by touching a grounded object.
- Touch the antistatic package to a metal part of the computer chassis before removing the module from the package.

Remove the module from the package and inspect the module for loose components or any sign of damage. Notify NI if the module appears damaged in any way. Do *not* install a damaged module into the computer.

Store the NI PXI-665*x* in the antistatic envelope when not in use.

Software Programming Choices

When programming the NI PXI-665*x*, you can use NI application development environment (ADE) software such as LabVIEW or LabWindows/CVI, or you can use other ADEs such as Visual C/C++.

LabVIEW features interactive graphics, a state-of-the-art interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

LabWindows/CVI is a complete ANSI C ADE that features an interactive user interface, code generation tools, and the LabWindows/CVI Data Acquisition and Easy I/O libraries.

Safety Information

The following section contains important safety information that you *must* follow when installing and using the product.

Do *not* operate the product in a manner not specified in this document. Misuse of the product can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to National Instruments for repair.

Do *not* substitute parts or modify the product except as described in this document. Use the product only with the chassis, modules, accessories, and cables specified in the installation instructions. You *must* have all covers and filler panels installed during operation of the product.

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Do *not* operate the product in an explosive atmosphere or where there may be flammable gases or fumes. If you must operate the product in such an environment, it must be in a suitably rated enclosure.

If you need to clean the product, use a soft, nonmetallic brush. The product *must* be completely dry and free from contaminants before you return it to service.

Operate the product only at or below Pollution Degree 2. Pollution is foreign matter in a solid, liquid, or gaseous state that can reduce dielectric strength or surface resistivity. The following is a description of pollution degrees:

- Pollution Degree 1 means no pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- Pollution Degree 2 means that only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- Pollution Degree 3 means that conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to condensation.

You *must* insulate signal connections for the maximum voltage for which the product is rated. Do *not* exceed the maximum ratings for the product. Do not install wiring while the product is live with electrical signals. Do not remove or add connector blocks when power is connected to the system. Avoid contact between your body and the connector block signal when hot swapping modules. Remove power from signal lines before connecting them to or disconnecting them from the product.

Operate the product at or below the measurement category[1] marked on the hardware label. Measurement circuits are subjected to working voltages[2] and transient stresses (overvoltage) from the circuit to which they are connected during measurement or test. Measurement categories establish standard impulse withstand voltage levels that commonly occur in electrical distribution systems. The following is a description of measurement categories:

- Measurement Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS[3] voltage. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special hardware, limited-energy parts of hardware, circuits powered by regulated low-voltage sources, and electronics.
- Measurement Category II is for measurements performed on circuits directly connected to the electrical distribution system (MAINS[3]). This category refers to local-level electrical distribution, such as that provided by a standard wall outlet (for example, 115 AC voltage

[1] Measurement categories, also referred to as overvoltage or installation categories, are defined in electrical safety standard IEC 61010-1 and IEC 60664-1.

[2] Working voltage is the highest rms value of an AC or DC voltage that can occur across any particular insulation.

[3] MAINS is defined as a hazardous live electrical supply system that powers hardware. Suitably rated measuring circuits may be connected to the MAINS for measuring purposes.

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for U.S. or 230 AC voltage for Europe). Examples of Measurement Category II are measurements performed on household appliances, portable tools, and similar hardware.

- Measurement Category III is for measurements performed in the building installation at the distribution level. This category refers to measurements on hard-wired hardware such as hardware in fixed installations, distribution boards, and circuit breakers. Other examples are wiring, including cables, bus bars, junction boxes, switches, socket outlets in the fixed installation, and stationary motors with permanent connections to fixed installations.
- Measurement Category IV is for measurements performed at the primary electrical supply installation typically outside buildings. Examples include electricity meters and measurements on primary overcurrent protection devices and on ripple control units.

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2

Installing and Configuring

This chapter describes how to install the NI PXI-665*x* hardware and software and how to configure the device.

Installing the Software

Refer to the `readme.htm` file that accompanies the *NI-Sync* CD for software installation directions.

Note Be sure to install the driver software *before* installing the NI PXI-665*x* hardware.

Installing the Hardware

The following are general installation instructions. Consult the chassis user manual or technical reference manual for specific instructions and warnings about installing new modules.

1. Power off and unplug the chassis.
2. Choose an available PXI slot in the PXI chassis.

Note The PXI_STAR and PXI_CLK10_IN signals are only available in the System Timing Slot (Slot 2).

3. Remove the filler panel for the PXI slot you chose in step 2.
4. Ground yourself using a grounding strap or by touching a grounded object. Follow the ESD protection precautions described in the *Unpacking* section of Chapter 1, *Introduction*.
5. Insert the NI PXI-665*x* into the PXI slot. Use the injector/ejector handle to fully insert the module into the chassis.
6. Screw the front panel of the device to the front panel mounting rail of the chassis.
7. Visually verify the installation. Make sure the module is not touching other modules or components and is fully inserted into the slot.
8. Plug in and power on the chassis.

The NI PXI-665*x* is now installed.

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Configuring the Module

The NI PXI-665*x* is completely software configurable. The system software automatically allocates all module resources.

The two LEDs on the front panel provide information about module status. The front panel description sections of Chapter 3, *Hardware Overview*, describe the LEDs in greater detail.

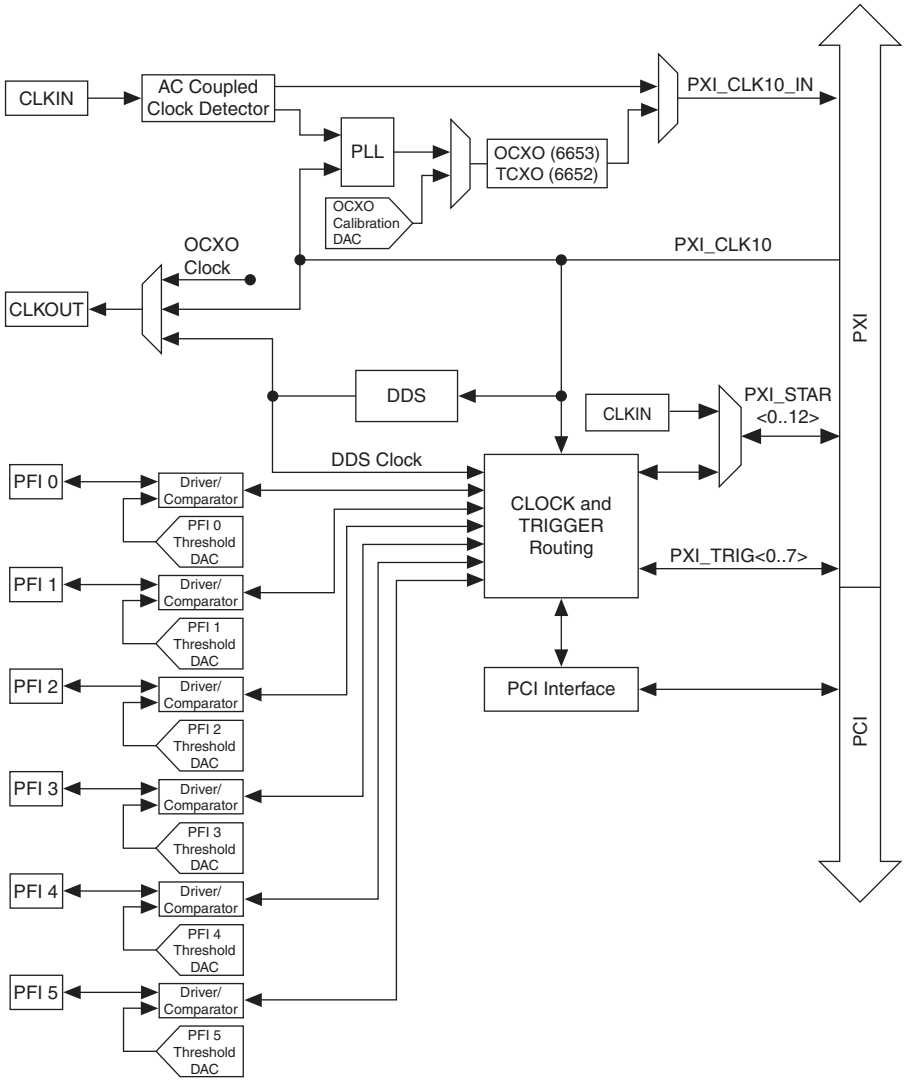
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3 Hardware Overview

This chapter presents an overview of the hardware functions of the NI PXI-6653, NI PXI-6652, and NI PXI-6651. Figure 3-1 provides a functional overview of the NI PXI-6653 and NI PXI-6652 hardware. Figure 3-2 provides a functional overview of the NI PXI-6651 hardware.

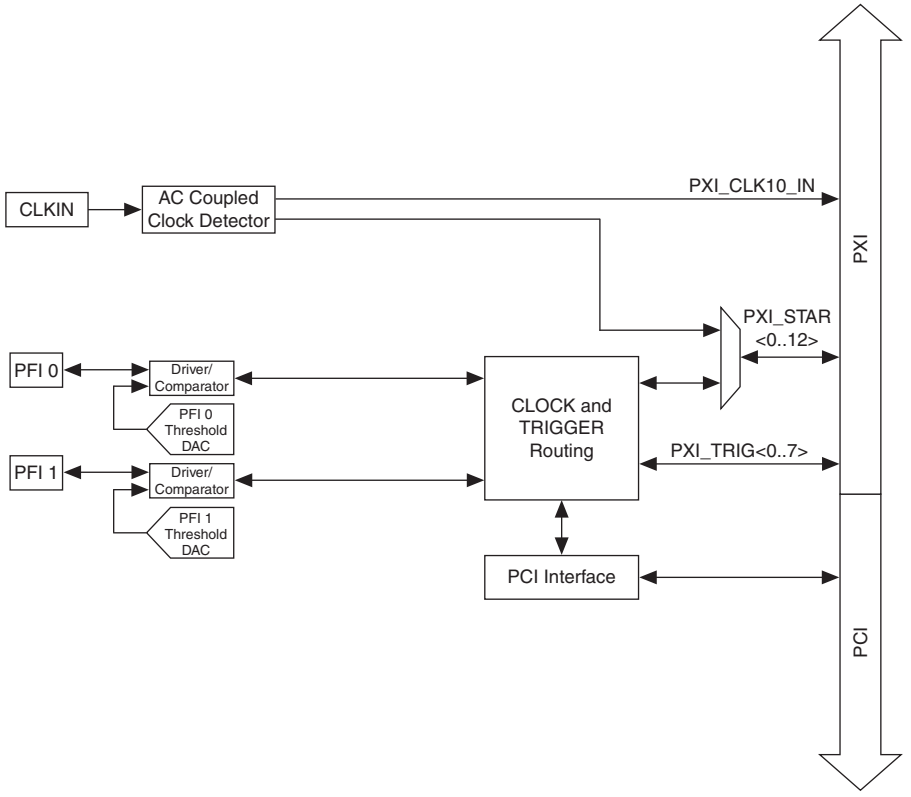
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Figure 3-1. Functional Overview of the NI PXI-6653 and NI PXI-6652



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Figure 3-2. Functional Overview of the NI PXI-6651

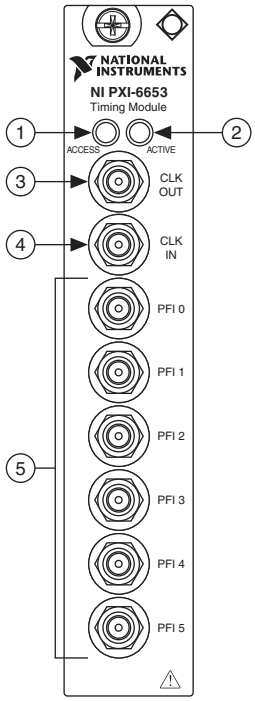


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NI PXI-6653 Front Panel

Figure 3-3 shows the connectors and LEDs on the front panel of the NI PXI-6653.

Figure 3-3. NI PXI-6653 Front Panel



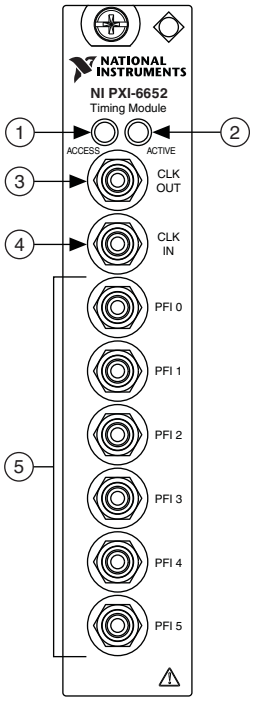
1	Access LED	4	CLKIN Connector
2	Active LED	5	PFI <0..5> Connectors
3	CLKOUT Connector		

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NI PXI-6652 Front Panel

Figure 3-4 shows the connectors and LEDs on the front panel of the NI PXI-6652.

Figure 3-4. NI PXI-6652 Front Panel



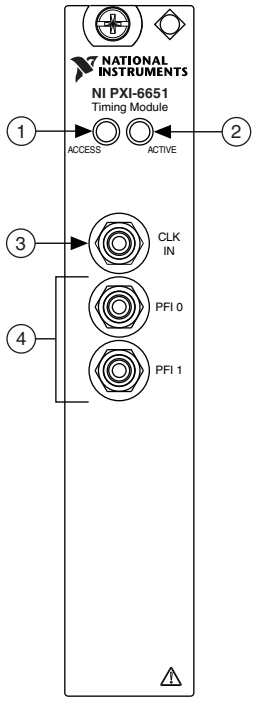
1	Access LED	4	CLKIN Connector
2	Active LED	5	PFI <0..5> Connectors
3	CLKOUT Connector		

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NI PXI-6651 Front Panel

Figure 3-5 shows the connectors and LEDs on the front panel of the NI PXI-6651.

Figure 3-5. NI PXI-6651 Front Panel



1	Access LED	3	CLKIN Connector
2	Active LED	4	PFI <0..1> Connectors

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Access LED

The Access LED indicates the communication status of the NI PXI-665*x*. Refer to Figures 3-3, 3-4, and 3-5 for the location of the Access LED.

Table 3-1 summarizes what the Access LED colors represent.

Table 3-1. Access LED Color Indication

Color	Status
Off	Module is not yet functional.
Green	Driver has initialized the module.
Amber	Module is being accessed. The Access LED flashes amber for 50 ms when the module is accessed.

Active LED

The Active LED can indicate an error or phase-locked loop (PLL) activity. You can change the Active LED to amber, unless an error overrides the selection. Refer to Figures 3-3, 3-4, and 3-5 for the location of the Active LED.

Tip Changing the Active LED color to amber is helpful when you want to identify devices in a multichassis situation or when you want an indication that your application has reached a predetermined section of the code.

Table 3-2 illustrates the meaning of each Active LED color.

Table 3-2. Active LED Color Quick Reference Table

Color	PXI_CLK10 Stopped	PLL Error	User Setting	PLL Active
Red	Yes	Yes	—	—
Amber	No	No	Yes	—
Green	No	No	No	Yes
Off	No	No	No	No

Note A red Active LED can indicate that either PXI_CLK10 has stopped or that there is a PLL error.

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Connectors

This section describes the connectors on the front panel of the NI PXI-665*x*.

- **CLKIN**— Clock Input. This connector supplies the module with a clock that can be programmatically routed to:
  - The onboard PLL for use as a reference for the oscillator to route to PXI_CLK10_IN for distribution to other modules in the chassis.
  - Directly to PXI_CLK10_IN for distribution to other modules in the chassis.
  - Any PXI_STAR line.

Note Refer to Appendix A Specifications for the frequency ranges for each one of these uses for CLKIN.

- **CLKOUT** (NI PXI-6653 and NI PXI-6652 only)—Clock Output. This connector is used to source a clock that can be routed programmatically from the oven-controlled crystal oscillator (OCXO) or temperature-compensated crystal oscillator (TCXO), direct digital synthesis (DDS), or backplane clock (PXI_CLK10).
- **PFI <0..5>**—Programmable Function Interface <0..5>. (The NI PXI-6651 supports only PFI 0..1.) These connectors can be used for either input or output. Additionally, **PFI 0** can be used as a clock input for internally synchronizing other signals. Refer to the *Synchronous Routing* section for more information about this functionality. You can program the behavior of these PFI connections individually.

Refer to Figures 3-3, 3-4, and 3-5 for diagrams showing the locations of these connections on the NI PXI-665*x* front panel.

Caution Connections that exceed any of the maximum ratings of input or output signals on the NI PXI-665*x* can damage the module and the computer. NI is *not* liable for any damage resulting from such signal connections.

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Hardware Features

The NI PXI-6653 and NI PXI-6652 perform two broad functions:

- Generating clock and trigger signals
- Routing internally or externally generated signals from one location to another

The NI PXI-6651 is primarily a slave module and can only route externally generated signals. Table 3-3 outlines the function and direction of the signals discussed in detail in the remainder of this chapter.

Table 3-3. Signal Descriptions

Signal Name	Direction	Description
PXI_CLK10_IN	Out	This is a signal that can replace the native 10 MHz oscillator on the PXI backplane. PXI_CLK10_IN may originate from the onboard OCXO or TCXO or from an external source.
PXI_CLK10	In	This signal is the PXI 10 MHz backplane clock. By default, this signal is the output of the native 10 MHz oscillator in the chassis. An NI PXI-665*x* in Slot 2 can replace this signal with PXI_CLK10_IN.
OCXO Clock (NI PXI-6653) or TCXO Clock (NI PXI-6652)	Out	This is the output of the 10 MHz OCXO or TCXO. The OCXO and TCXO are extremely stable and accurate frequency sources.
CLKIN	In	CLKIN is a signal connected to the SMB input pin of the same name. CLKIN can be routed directly to PXI_CLK10_IN, be used as a phase lock reference for the OCXO or TCXO, or be routed to a PXI_STAR line.
CLKOUT (NI PXI-6653 and NI PXI-6652 only)	Out	CLKOUT is the signal on the SMB output pin of the same name. Either the OCXO clock, TCXO clock, DDS clock, or PXI_CLK10 may be routed to this location.
DDS Clock (NI PXI-6653 and NI PXI-6652 only)	Out	This is the output of the NI PXI-6653 or NI PXI-6652 DDS. The DDS frequency can be programmed with fine granularity from 1 Hz to 105 MHz. The DDS chip automatically phase-locks to PXI_CLK10.

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Table 3-3. Signal Descriptions (Continued)

Signal Name	Direction	Description
PXI_STAR <0..12>	In/Out	The PXI star trigger bus connects Slot 2 to Slot <3..15> in a star configuration. The electrical paths of each star line are closely matched to minimize intermodule skew. An NI PXI-665*x* in Slot 2 can route signals to Slots <3..15> using the star trigger bus.
PFI <0..5>	In/Out	The Programmable Function Interface pins on the NI PXI-665*x* route timing and triggering signals between multiple PXI chassis. A wide variety of input and output signals can be routed to or from the PFI lines.
PXI_TRIG <0..7>	In/Out	The PXI trigger bus consists of eight digital lines shared among all slots in the PXI chassis. The NI PXI-665*x* can route a wide variety of signals to and from these lines. **Note**: PXI_TRIG <0..5> are also known as RTSI <0..5> in some hardware devices and APIs. However, PXI_TRIG <6..7> are *not* identical to RTSI <6..7>.

The remainder of this chapter describes how these signals are used, acquired, and generated by the NI PXI-665*x* hardware, and explains how you can route the signals between various locations to synchronize multiple measurement devices and PXI chassis.

Clock Generation

The NI PXI-6653 and NI PXI-6652 can generate two types of clock signals. The first clock is generated using the onboard DDS chip, and the second is generated with a precise 10 MHz oscillator. The following sections describe the two types of clock generation and explain the considerations for choosing either type.

Direct Digital Synthesis (DDS)

DDS is a method of generating a clock with programmable frequency. DDS consists of a frequency tuning word, an accumulator, a sine-lookup table, a D/A converter (DAC), and a comparator.

The frequency tuning word is a number that specifies the desired frequency. Each master clock cycle, the frequency tuning word is added to the accumulator, which rolls over when it gets to its maximum value. The accumulator value is used to get a point in the sine-lookup table, which is converted to an analog voltage by the DAC. For example, if the sine table is 128 points long,

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and the frequency tuning word is one, the accumulator takes 128 clock cycles to output one sine wave. If you change the frequency tuning word to 3, the accumulator steps through the sine table three times as fast, and outputs a sine wave in 128/3, or 42.6, clock cycles.

The output of the DAC is run through an analog filter to smooth the sine wave. The filtered output is then run through a comparator, which changes the output to a square wave with the specified frequency.

You can specify the programmable DDS frequency on the NI PXI-6653 and NI PXI-6652 with a precision of approximately 1 µHz within the range 1 Hz to 105 MHz. The accuracy of the frequency depends on the PXI_CLK10 reference clock, so a precise 10 MHz source improves the accuracy of the DDS output. You can replace the 10 MHz clock with the OCXO for more accurate DDS timing.

PXI_CLK10 and OCXO or TCXO

The NI PXI-6653 features a precision 10 MHz OCXO. The NI PXI-6652 features a precision 10 MHz TCXO. The frequency accuracy of this clock is several orders of magnitude greater than the frequency accuracy of the native 10 MHz PXI backplane clock (PXI_CLK10).

The main source of error in most frequency reference oscillators is temperature variation. The OCXO houses the oscillator circuit inside a sealed oven. A resistive heater and automatic feedback circuit maintain a precisely controlled operating temperature for the oscillator. This temperature-control scheme minimizes frequency error to low enough levels that other sources of error become considerable. The user can do two things to help mitigate these other error sources and achieve the best possible performance from the OCXO:

1. Use a chassis that has as little variance in the 5 V supply as possible. The OCXO has an error of 1 ppb for every 1% of inaccuracy in the voltage level of the 5 V supply. The *CompactPCI Specification* requires all chassis to regulate the 5 V supply to -3% to +5% which results in a -3 ppb to +5 ppb possible error referenced to 5 V. Improved performance can be obtained by using a chassis that specifies a tighter accuracy on the 5 V supply. NI recommends using the NI PXI-1044 or NI PXI-1045 chassis as they have tighter power supply regulation performance.
2. Avoid power-cycling the OCXO. The longer the OCXO is consistently powered, the more stable the aging rate will be.

For the tightest performance requirements, the OCXO can be calibrated by the user in the same system in which the NI PXI-6653 is normally used. Doing so will calibrate out error from the power supply variance and, if done at the normal operating temperature, reduce the error from temperature variance. Refer to the *NI PXI-665x Calibration Procedure* for more information on calibrating the OCXO.

The TCXO contains circuitry to measure the temperature of the oscillator. It uses the temperature to adjust its frequency output according to the crystal's known frequency variation across its operating temperature range.

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An NI PXI-6653 or NI PXI-6652 module in Slot 2 of a PXI chassis can replace the native PXI 10 MHz backplane frequency reference clock (PXI_CLK10) with the more stable and accurate output of the OCXO or TCXO. All other PXI modules in the chassis that reference the 10 MHz backplane clock benefit from this more accurate frequency reference. Furthermore, the DDS chip on the NI PXI-6653 or NI PXI-6652 references its output to the backplane clock and also takes advantage of the superior OCXO or TCXO accuracy. The OCXO or TCXO does not automatically replace the native 10 MHz clock; this feature must be explicitly enabled in software. The OCXO or TCXO output also can be routed out to the **CLKOUT** connector.

In addition to replacing the native backplane clock directly, the OCXO or TCXO can phase lock to an external frequency source. This operation is discussed in detail in the *Using the PXI_CLK10 PLL* section.

Routing Signals

The NI PXI-665*x* has versatile trigger routing capabilities. It can route signals to and from the front panel, the PXI star triggers, and the PXI/RTSI triggers.

The NI PXI-665*x* also can route a 10 MHz clock from **CLKIN** to the PXI 10 MHz reference clock, or a clock of a different frequency from CLKIN to any number of PXI_STAR lines. The NI PXI-6653 and NI PXI-6652 can lock the OCXO or TCXO to an external reference clock and send that to the PXI 10 MHz reference clock. The NI PXI-6653 and NI PXI-6652 can route the OCXO, TCXO, DDS, or PXI 10 MHz reference clock to **CLKOUT**.

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Figures 3-6 and 3-7 summarize the routing features of the NI PXI-6653 and NI PXI-6652. The remainder of this chapter details the capabilities and constraints of the routing architecture.

Figure 3-6. High-Level Schematic of NI PXI-6653 and NI PXI-6652 Signal Routing Architecture

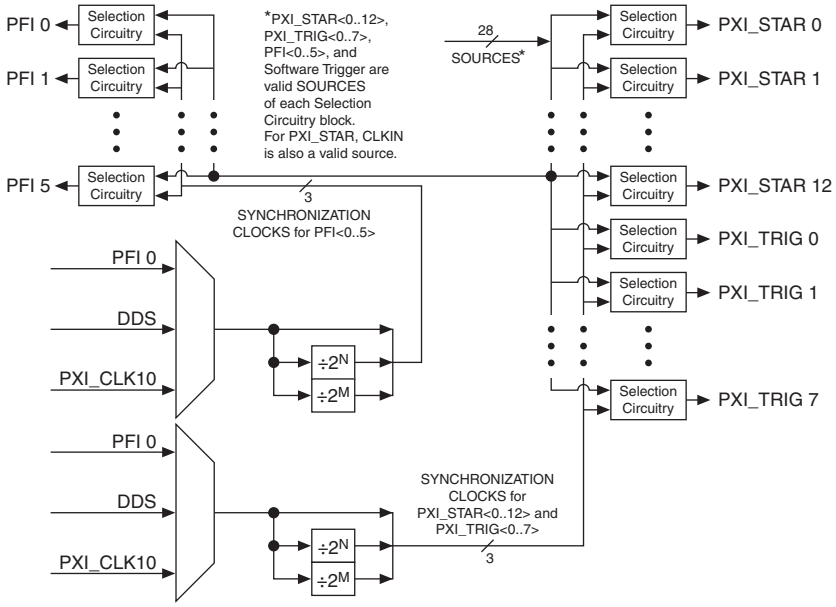
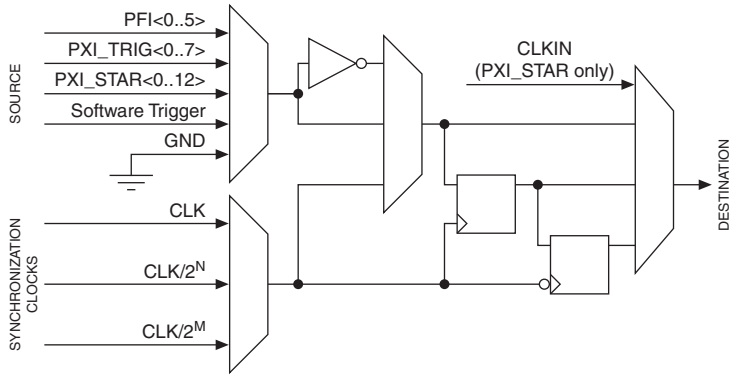


Figure 3-7 provides a more detailed view of the *Selection Circuitry* referenced in Figure 3-6.

Figure 3-7. Signal Selection Circuitry Diagram



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Determining Sources and Destinations

All signal routing operations can be characterized by a *source* (input) and a *destination*. In addition, synchronous routing operations must also define a third signal known as the *synchronization clock*. Refer to the *Choosing the Type of Routing* section for more information on synchronous versus asynchronous routing.

Table 3-4 summarizes the sources and destinations of the NI PXI-665*x*. The destinations are listed in the horizontal heading row, and the sources are listed in the column at the far left. A ✓ in a cell indicates that the source and destination combination defined by that cell is a valid routing combination.

Table 3-4. Sources and Destinations for NI PXI-665*x* Signal Routing Operations

		Destinations						
		Front Panel			**Backplane**			**Onboard**
Sources			CLKOUT	PFI <0..5>	PXI_ CLK10_IN	PXI_Star Trigger <0..12>	RTSI/PXI TRIG <0..7>	OCXO/ TCXO Reference PLL
	Front Panel	CLKIN	✓†	✓†	✓	✓	✓†	✓
		PFI <0..5> (NI PXI-6651 0..1 Only)		✓		✓	✓	
	Backplane	PXI_ CLK10	✓	✓		✓	✓	
		PXI_STAR <0..12>		✓		✓	✓	
		RTSI/PXI TRIG <0..7>		✓		✓	✓	
	Onboard	OCXO or TCXO (NI PXI-6653 and NI PXI-6652 Only)	✓	✓†	✓	✓†	✓†	
		DDS (NI PXI-6653 and NI PXI-6652 Only)	✓	✓		✓	✓	
		Global Software Trigger		✓		✓	✓	

† Can be accomplished in two stages by routing source to PXI_CLK10_IN, replacing PXI_CLK10 with PXI_CLK10_IN (occurs automatically in most chassis), and then routing PXI_CLK10 to the destination. The source must be 10 MHz.

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Using Front Panel PFIs As Inputs

The front-panel PFIs can receive external signals from 0 to +5 V. The input impedance of PFI inputs can be programmatically set to 10 kΩ or 50 Ω , to match the cable impedance and minimize reflections.

Note Terminating the signals with a 50 Ω resistance is recommended when the source is another NI PXI-665*x* or any other source with a 50 Ω output.

The voltage thresholds for the front-panel PFI inputs are programmable. The input signal is generated by comparing the input voltage on the PFI connectors to the voltage output of software-programmable DACs. The thresholds for the PFI lines are individually programmable, which is useful if you are importing signals from multiple sources with different voltage swings. The front panel PFI inputs can be routed to any PXI star triggers, PXI/RTSI triggers, or other front panel PFI outputs.

Using Front Panel PFIs As Outputs

The front panel PFI outputs are +3.3 V drivers with 50 Ω output impedance. The outputs can drive high-impedance loads or 50 Ω loads, such as a 50 Ω coaxial cable with a 50 Ω receiver. When driving a high-impedance load, the receiver sees a +3.3V signal. When driving a 50 Ω load the receiver sees a single +1.6 V step—a +3.3 V step split across the 50 Ω resistors at the source and the destination. This cable configuration is the recommended setup to minimize reflections.

You can independently select the output signal source for each PFI line from one of the following sources:

- Another PFI <0..5>
- PXI/RTSI triggers <0..7> (PXI_TRIG <0..7>)
- PXI_STAR <0..12>
- Global software trigger
- PFI synchronization clock

The PFI synchronization clock may be any of the following signals:

- DDS clock
- PXI_CLK10
- PFI 0 Input
- Any of the previously listed signals divided by the first frequency divider (2^n, up to 512)
- Any of the previously listed signals divided by the second frequency divider (2^m, up to 512)

Refer to the *Choosing the Type of Routing* section for more information on the synchronization clock.

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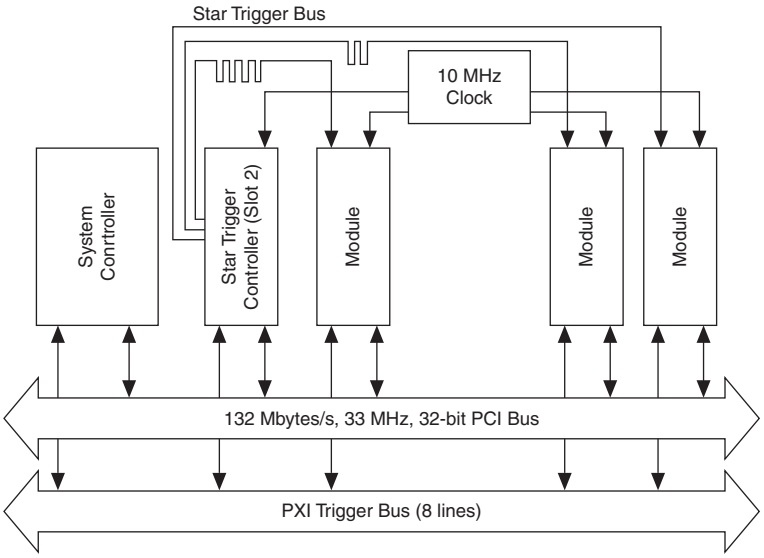
Note The PFI synchronization clock is the same for all routing operations in which PFI <0..5> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

Brief Overview of PXI Synchronization Features

PCI eXtensions for Instrumentation (PXI) is a rugged PC-based platform that offers a high-performance, low-cost deployment solution for measurement and automation systems. PXI combines the Peripheral Component Interconnect (PCI) electrical bus with the rugged, modular Eurocard mechanical packaging of CompactPCI and adds specialized synchronization buses and key software features.

Figure 3-8 provides an overview of the PXI synchronization architecture.

Figure 3-8. PXI Synchronization Architecture



The PXI trigger Bus, PXI star triggers, and PXI_CLK10 are PXI features that enhance synchronization. The PXI trigger bus is a multi-drop 8-line bus that goes to every slot. The PXI star trigger bus is a set of up to 13 point-to-point matched-length connections between the system timing slot and every slot starting with slot 3 and up to slot 15. The propagation delay between the system timing slot and each destination slot is matched to within 1ns to achieve low-skew triggering. PXI_CLK10 is a high quality 10 MHz clock that is distributed with low skew to each PXI slot. This 10 MHz signal can be sourced from the native PXI backplane oscillator or from the system timing slot Controller Module installed in the system timing slot (such as the NI PXI-665*x*).

The following sections describe in more detail the use of PXI triggers and PXI star triggers with the NI PXI-665*x* series.

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Using the PXI/RTSI Triggers

The PXI trigger bus is a set of 8 electrical lines that go to every slot in a segment of a PXI chassis (multi-drop up to 8 slots). Only one PXI module should drive a particular PXI_Trigger line at a given time. The signal is then received by modules in all other PXI slots. This feature makes the PXI triggers convenient in situations where you want, for instance, to trigger several devices, because all modules will receive the same trigger.

Given the architecture of the PXI trigger bus, triggering signals do not reach each slot at precisely the same time. A difference of several nanoseconds can occur between slots, especially in larger PXI chassis (which can have buffers between segments). This delay is not a problem for many applications. However, if your application requires tighter synchronization, use the PXI_STAR triggers (refer to next section), or use the PXI trigger bus synchronous to PXI_CLK10 as shown in Figure 3-11.

The multi-drop nature of the PXI trigger bus can introduce signal integrity issues. Therefore, National Instruments does not recommend the use of PXI_Trigger lines for clock distribution. The preferred method for clock distribution is the use of the PXI_STAR triggers. However, the NI PXI-665*x* Series does support routing of clocks to the PXI_Trigger lines, in case you must use them.

You can independently select the output signal source for each PXI/RTSI trigger line from one of the following sources:

- PFI <0..5>
- Another PXI/RTSI trigger <0..7> (PXI_TRIG <0..7>)
- PXI_STAR <0..12>
- Global software trigger
- PXI_Trig/PXI_Star synchronization clock

The PXI_Trig/PXI_Star synchronization clock may be any of the following signals:

- DDS clock
- PXI_CLK10
- PFI 0 Input
- Any of the previously listed signals divided by the first frequency divider (2^n, up to 512)
- Any of the previously listed signals divided by the second frequency divider (2^m, up to 512)

Refer to the *Choosing the Type of Routing* section for more information about the synchronization clock.

Note The PXI_Trig/PXI_Star synchronization clock is the same for all routing operations in which PXI_TRIG <0..7> or PXI_STAR <0..12> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

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Using the PXI Star Triggers

There are up to 13 PXI star triggers per chassis. Each trigger line is a dedicated connection between the System Timing Slot (Slot 2) and one other slot. The *PXI Specification*, Revision 2.1, requires that the propagation delay along each star trigger line be matched to within 1 ns. A typical upper limit for the skew in most NI PXI chassis is 500 ps. The low skew of the PXI star trigger bus is useful for applications that require triggers to arrive at several modules nearly simultaneously.

The star trigger lines are bidirectional, so signals can be sent to System Timing Slot from a module in another slot or from System Timing Slot to the other module.

You can independently select the output signal source for each PXI star trigger line from one of the following sources:

- PFI <0..5>
- PXI/RTSI triggers <0..7> (PXI_TRIG <0..7>)
- Another PXI star trigger line (PXI_STAR <0..12>)
- Global software trigger
- PXI_Trig/PXI_Star synchronization clock
- CLKIN

Refer to the *Using the PXI/RTSI Triggers* section for a list of possible sources for the synchronization clock for PXI Star trigger outputs.

Note The PXI_Trig/PXI_Star synchronization clock is the same for all routing operations in which PXI_TRIG <0..7> or PXI_STAR <0..12> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

Choosing the Type of Routing

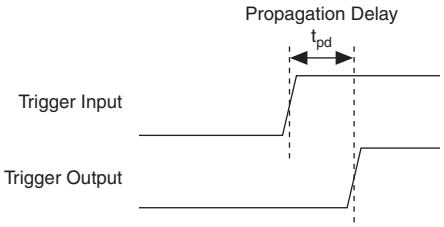
The NI PXI-665*x* routes signals in one of two ways: asynchronously or synchronously. The following sections describe the two routing types and the considerations for choosing each type.

Asynchronous Routing

Asynchronous routing is the most straightforward method of routing signals. Any asynchronous route can be defined in terms of two signal locations: a source and a destination. A digital pulse or train comes in on the source and is propagated to the destination. When the source signal goes from low to high, this rising edge is transferred to the destination after a propagation delay through the module. Figure 3-9 illustrates an asynchronous routing operation.

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Figure 3-9. Asynchronous Routing Operation



Some delay is always associated with an asynchronous route, and this delay varies among NI PXI-665*x* modules, depending on variations in temperature and chassis voltage. Typical delay times in the NI PXI-665*x* for asynchronous routes between various sources and destinations are given in Appendix A, *Specifications*.

Asynchronous routing works well if the total system delays are not too long for the application. Propagation delay could be caused by the following reasons:

- Output delay on the source
- Propagation delay of the signal across the backplane(s) and cable(s)
- Propagation delay of the signal through the NI PXI-665*x*
- Time for the receiver to recognize the signal

Both the source and the destination of an asynchronous routing operation on the NI PXI-665*x* can be any of the following lines:

- Any front panel PFI pin (PFI <0..5)
- Any PXI star trigger line (PXI_STAR <0..12>)
- Any PXI/RTSI trigger line (PXI_TRIG <0..7>)

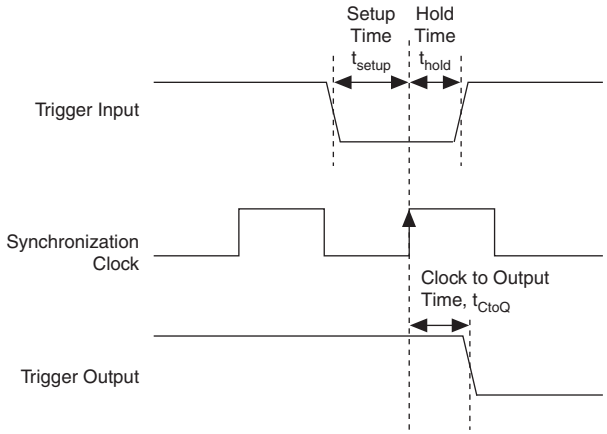
Synchronous Routing

A synchronous routing operation is defined in terms of three signals: a source, a destination, and a synchronization clock. Unlike asynchronous routing, the output of a synchronous routing operation does not directly follow the input after a propagation delay. Instead, the logic state of the input is sampled on each active edge of the synchronization clock and the output is set to that logic state after a small delay, as shown in Figure 3-10. Thus, the output is said to be *synchronous* with this clock.

The NI PXI-665*x* boards support routing synchronous to either the rising or falling edge of the synchronization clock. In addition, the polarity of the destination signal can be inverted, which is useful when handling active-low digital signals.

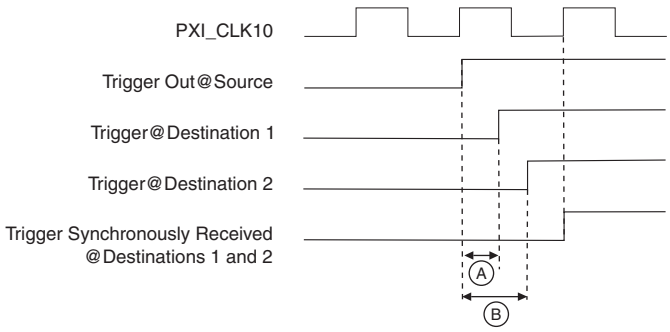
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Figure 3-10. Synchronous Routing Operation



Synchronous routing can be useful for eliminating skew when sending triggers to several destinations. For example, when sending triggers using the PXI Trigger lines, the trigger arrives at each slot at a slightly different time. However, if the trigger is sent and received synchronously using a low-skew synchronization clock, all receiving devices can act on the trigger at the same time, as shown in Figure 3-11.

Figure 3-11. Synchronous Routing to Multiple Destinations



A: Propagation delay from source to destination 1.

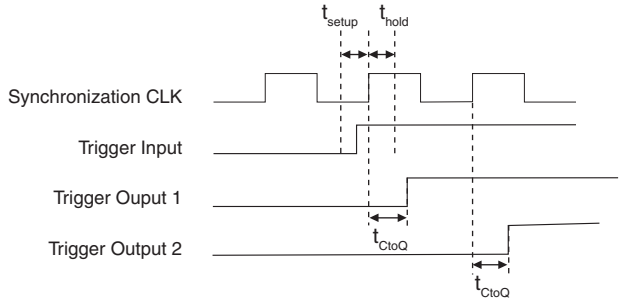
B: Propagation delay from source to destination 2.

Synchronous routing requires the input to be stable at a logic low or logic high state within a window of time around the clock edge. This window of time around the clock edge is defined by the setup time (t_{setup}) and hold time (t_{hold}). If the input signal changes within this window of time, it is undetermined whether the output of the synchronous route will go to the old or new logic state. This is important, for example, if a source is being routed synchronously to several destinations. As shown in Figure 3-12, if the source signal changes within the setup-and-hold

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window around the synchronization clock edge, one of the destinations might go to the new logic level while the other destination might remain at the old logic level and change when the next synchronization clock edge occurs.

Figure 3-12. Synchronous Routing Uncertainty with Setup-and-Hold Violation



Therefore, if your application requires that the trigger arrive at the multiple destinations simultaneously, you must ensure that the input is stable within the setup and hold window around the synchronization clock edge. For more information and possible methods to ensure this requirement is met, go to `ni.com/info` and enter Info Code `SyncTriggerRouting`.

Possible sources for synchronous routing include the following sources:

- Any front panel PFI pin
- Any PXI star trigger line (PXI_STAR <0..12>)
- Any PXI/RTSI trigger line (PXI_TRIG <0..7>)
- Global software trigger
- The synchronization clock itself

The destination of a synchronous routing operation on the NI PXI-665*x* can be any of the following lines:

- Any front panel PFI pin (PFI <0..5)
- Any PXI star trigger line (PXI_STAR <0..12>)
- Any PXI/RTSI trigger line (PXI_TRIG <0..7>)

The synchronization clock for a synchronous route can be any of the following signals:

- 10 MHz PXI backplane clock signal
- DDS clock on the NI PXI-6653 or NI PXI-6652
- Front panel PFI 0 Input
- One of two “divided copies” of any of the previously listed three signals. The NI PXI-665*x* includes two clock-divider circuits that can divide the synchronization clock signals by any power of 2 up to 512.

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Refer to Figures 3-6 and 3-7 for an illustration of how the NI PXI-665*x* performs synchronous routing operations.

Generating a Single Pulse (Global Software Trigger)

The global software trigger is a single pulse with programmable delay that is fired on a software command. This signal is always routed synchronously with a clock. Therefore, asynchronous routing is not supported when the signal source is the global software trigger.

The software trigger can be delayed by up to 15 clock cycles on a per route basis. This feature is useful if a single pulse must be sent to several destinations with significantly different propagation delays. By delaying the pulse on the routes with shorter paths, you can compensate for the propagation delay. An example of such a situation would be when a trigger pulse must arrive nearly simultaneously at the local backplane and the backplane of another chassis separated by 50 m of coaxial cable.

Using the PXI_CLK10 PLL

A module in the System Timing Slot (Slot 2) of a PXI chassis can replace the PXI_CLK10 reference clock. The NI PXI-665*x* offers three options for this replacement. This section describes each option.

- The first option is to replace PXI_CLK10 directly with the OCXO output on the NI PXI-6653 or TCXO output on the NI PXI-6652. This oscillator is a more stable and accurate reference than the native backplane clock.
- The second option is to route a 10 MHz clock directly from the front panel to PXI_CLK10_IN, which is the pin on the backplane that will replace PXI_CLK10. There is a delay through the module, as well as a distribution delay on the backplane. These delays tend to be similar for chassis of the same model, so routing the same clock to a pair of chassis usually matches PXI_CLK10 to within a few nanoseconds.
- The third option is to employ the NI PXI-6653 or NI PXI-6652 PLL circuitry for the OCXO or TCXO. As in option 1, the output of the OCXO or TCXO replaces the native 10 MHz signal. However, this scheme also requires an input signal on **CLKIN**. This signal must be a stable clock, and its frequency must be a multiple of 1 MHz (5 MHz or 13 MHz, for example). The PLL feedback circuit generates a voltage proportional to the phase difference between the reference input on PXI_CLK10 and the output of the OCXO or TCXO. This PLL voltage output then tunes the output frequency of the OCXO or TCXO. As long as the incoming signal is a stable 1 MHz frequency multiple, the PLL circuit quickly locks the OCXO or TCXO to the reference, eliminating all phase drift between the two signals.

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Using the PLL provides several advantages over the other two options for replacing the PXI backplane clock:

- CLKIN is not required to be 10 MHz. If you have a stable reference that is a multiple of 1 MHz, such as 13 or 5 MHz, you can frequency-lock the chassis to it.
- If CLKIN stops or becomes disconnected, PXI_CLK10 is still present in the chassis.
- If CLKIN is 10 MHz, the NI PXI-6653 or NI PXI-6652 can compensate for distribution delays in the backplane. The feedback in the PLL comes from PXI_CLK10. This PLL makes it possible for the NI PXI-6653 or NI PXI-6652 to align clock edges at CLKIN with the edges of PXI_CLK10 that the modules receive. If you split an external (accurate) 10 MHz reference and route it to two chassis, they can both lock to it. The result is a tighter synchronization of PXI_CLK10 on the chassis.

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4

Calibration

This chapter discusses the calibration of the NI PXI-665*x*.

Calibration consists of verifying the measurement accuracy of a device and correcting for any measurement error. The NI PXI-665*x* is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the corrections that were needed to meet specifications—are stored in the onboard nonvolatile memory (EEPROM). The driver software uses these stored values.

Factory Calibration

The factory calibration of the NI PXI-665*x* involves calculating and storing four calibration constants. These values control the accuracy of four features of the device, which are discussed in the following sections.

OCXO Frequency

The OCXO frequency can be varied over a small range. The output frequency of the OCXO is adjusted using this constant to meet the specification listed in Appendix A, *Specifications*. This calibration applies only to the NI PXI-6653.

TCXO Frequency

The TCXO frequency can be varied over a small range. The output frequency of the TCXO is adjusted using this constant to meet the specification listed in Appendix A, *Specifications*. This calibration applies only to the NI PXI-6652.

PXI_CLK10 Phase

When using the PLL to lock PXI_CLK10 to an external reference clock, the phase between the clocks can be adjusted. The time between rising edges of PXI_CLK10 and the input clock is minimized using this constant.

DDS Start Trigger Phase

To start the DDS reliably, the DDS start trigger must arrive within a certain window of time. The phase of the DDS start trigger is controlled by this constant to meet the setup and hold-time requirements of the DDS.

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DDS Initial Phase

The phase of the DDS output is adjusted using this constant so that the DDS outputs from multiple NI PXI-6653 or NI PXI-6652 modules are aligned.

Additional Information

Refer to `ni.com/calibration` for additional information on NI calibration services.

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A

Specifications

This appendix lists the system specifications for NI PXI-665*x* modules. These specifications are typical at 25 °C, unless otherwise stated.

Note Specifications are subject to change without notice.

CLKIN Characteristics

CLKIN fundamental
frequency range[1] ..... 1 MHz to 105 MHz, sine or square wave
Input impedance ..... 50 Ω, nominal
Input coupling ..... AC
Voltage range ..... 400 mVp-p to 5 Vp-p
Absolute maximum input voltage[2] ..... 6 Vp-p, max
CLKIN to PXI_CLK10_IN delay (No PLL) .... 14 ns to 14.7 ns, typical
CLKIN to PXI_CLK10
offset when using PLL ..... ±1 ns, max
CLKIN frequency accuracy requirement
- For PLL and OCXO ..... ±1.5 ppm
- For PLL and TCXO ..... ±5.0 ppm
- For replacing PXI_CLK10 (no PLL) ..... ±100 ppm[3]

Jitter added to CLKIN
- Without PLL ..... 0.5 ps_{rms}, 10 Hz to 100 kHz, typical
- With PLL ..... 0.6 ps_{rms}, 10 Hz to 100 kHz, typical

Duty cycle distortion of CLKIN to
PXI_CLK10_IN without PLL ..... ±1%, max
Required input duty cycle
when using PLL ..... 45 to 55%

---

[1] CLKIN fundamental frequency can be any multiple of 1 MHz within the range specified when the PLL is engaged and PXI_CLK10 is locking to it. The frequency must be 10 MHz when replacing PXI_CLK10 without the PLL.

[2] Stresses beyond those listed can cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods of time can affect device reliability. Functional operation of the device outside the conditions indicated in the operational parts of the specification is not implied.

[3] This is a requirement of the PXI specification.

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CLKOUT Characteristics

Output frequency

- From PXI_CLK10 ..... 10 MHz
- From OCXO/TCXO ..... 10 MHz
- From DDS[1] ..... 1 MHz to 105 MHz

Duty cycle ..... 40 to 60%

Output impedance ..... 50 Ω, nominal

Output coupling ..... AC

Amplitude, software configurable to two voltage levels (low and high drive)

Open Load	Square Wave
Low Drive	2.0 Vp-p, typical
High Drive	5.0 Vp-p, typical

50 Ω Load	Square Wave
Low Drive	1.0 Vp-p, typical
High Drive	2.5 Vp-p, typical

Square wave rise/fall time (10 to 90%)

- High or low drive ..... 0.5 - 2.5 ns

PFI <0..5>

Input Characteristics

Frequency range ..... DC to 105 MHz

Input impedance ..... 50 Ω, nominal, or 1 kΩ ±10%, || 35 pF, software-selectable

Input coupling ..... DC

Voltage level ..... 0 V to 5 V

Absolute maximum input voltage[2] ..... ±5.25 V, max

[1] The lower limit is load dependent because of the AC coupling. This limit is less than 1 MHz for high-impedance loads.

[2] Stresses beyond those listed can cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods of time can affect device reliability. Functional operation of the device outside the conditions indicated in the operational parts of the specifications is not implied.

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Input threshold
- Voltage level ..... 0 to 4.3 V, software-selectable
- Voltage resolution ..... 16.8 mV (8 bits)
- Error ..... ±40 mV

Hysteresis ..... 50 mV

Asynchronous delay, t_{pd}
- PFI <0..5> to PXI_TRIG <0..7> output ..... 15 ns to 23 ns, typical
- PFI <0..5> to PXI_STAR <0..12> output ..... 10 ns to 19 ns, typical

Synchronized trigger input setup time, t_{setup}[1] ... 11.2 ns, typical

Synchronized trigger input hold time, t_{hold}[1] ..... -10.8 ns, typical

Output Characteristics

Frequency range ..... DC to 105 MHz

Output impedance ..... 50 Ω, nominal

Output coupling ..... DC

Voltage level ..... 0 to 1.6 V into 50 Ω;
0 to 3.3 V into open circuit, typical

Absolute maximum applied voltage[2] ..... ±5.25 V, max

Output current ..... ±48 mA, max

Synchronized trigger clock to out time, t_{CtoQ}[1] ..... 8.4 ns, typical

Output-to-output skew, synchronous ..... 500 ps, typical

PXI_STAR Trigger Characteristics

PXI_STAR <0..12> to PXI_STAR <0..12> output skew at NI PXI-665*x* backplane connector[3] ..... 300 ps, typical

Asynchronous delays, t_{pd}
- PXI_STAR <0..12> to PFI <0..5> output ..... 7 to 11 ns, typical
- PXI_STAR <0..12> to PXI_TRIG <0..7> output ..... 13 to 19 ns, typical

---

[1] Relative to PXI_CLK10.

[2] Stresses beyond those listed can cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods of time can affect device reliability. Functional operation of the device outside the conditions indicated in the operational parts of the specifications is not implied.

[3] This specification applies to all synchronous routes to the PXI_Star lines, as well as asynchronous routes from the PFI inputs to the PXI_Star lines.

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PXI Trigger Characteristics

PXI_TRIG <0..7> to
PXI_TRIG <0..7> output skew
at NI PXI-665*x* backplane connector ..... 5 ns, typical

Asynchronous delay, t_{pd}

PXI_TRIG <0..7> to PFI <0..5> output .... 11 to 17 ns, typical

OCXO Characteristics

Nominal frequency ..... 10 MHz

Accuracy within 1 year of calibration
adjustment within 0 °C to 55 °C
operating temperature range[1] ..... ±80 ppb

Long-term stability ..... ±50 ppb/year

Stability vs temperature ..... <10 ppb peak-to-peak within 0 °C to 55 °C operating temperature range

Jitter

to CLKOUT ..... 2.0 ps_{rms}, 10 Hz to 100 kHz, typical

to CLK10IN ..... 1.5 ps_{rms}, 10 Hz to 100 kHz, typical

Recommended calibration interval ..... 1 year

TCXO Characteristics

Nominal frequency ..... 10 MHz

Accuracy within 1 year of calibration
adjustment within 0 °C to 55 °C
operating temperature range ..... ±3.5 ppm

Long-term stability[2] ..... ±1 ppm/year

Stability vs temperature ..... <1.6 ppm peak-to-peak within 0 °C to 55 °C operating temperature range

Recommended calibration interval ..... 1 year

DDS Characteristics

Frequency range ..... 1 Hz to 105 MHz

Frequency resolution ..... <1.1 µHz

Frequency accuracy[3] ..... Equivalent to PXI_CLK10 accuracy

---

[1] After 72 hours of continuous operation.

[2] Includes stability of TCXO and supporting circuitry.

[3] The DDS frequency inherits the relative frequency of PXI_CLK10. For example, if you route the OCXO to PXI_CLK10, the DDS output inherits the same relative frequency accuracy as the OCXO output.

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Physical

Chassis requirement ..... One 3U CompactPCI or PXI slot
(PXI system timing slot for full functionality)

Weight

- NI PXI-6651 ..... 163 g
- NI PXI-6652 ..... 184 g
- NI PXI-6653 ..... 203 g

Front panel connectors ..... SMB male, 50 Ω

Front panel indicators ..... Two tricolor LEDs (green, red, and amber)

Recommended maximum cable length

- PFI/CLKOUT, DC to 10 MHz ..... 200 m
- CLKOUT High Gain, 105 MHz[1] ..... 100 m
- PFI/CLKOUT Low Gain, 105 MHz[1] ..... 30 m

Power Requirements

+5 V ..... 2 A, max

+3.3 V ..... 600 mA, max

+12 V ..... 500 mA, max

-12 V ..... 0 A, max

Environmental

Operating Environment

Ambient temperature range ..... 0 to 55 °C
(Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)

Relative humidity range ..... 10% to 90%, noncondensing
(Tested in accordance with IEC 60068-2-56.)

Maximum altitude ..... 2,000 m (at 25 °C ambient temperature)

Pollution Degree 2

Indoor use only

[1] Maximum cable length with a direct cable connection. Loss from a signal splitter would reduce maximum cable length.

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Storage Environment

Ambient temperature range ..... -20 to 70 °C
(Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)

Relative humidity range..... 5% to 95% noncondensing
(Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Operational Shock..... 30 g peak, half-sine, 11 ms pulse
(Tested in accordance with IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)

Random Vibration

Operating ..... 5 to 500 Hz, 0.3 g_{rms}

Nonoperating ..... 5 to 500 Hz, 2.4 g_{rms}
(Tested in accordance with IEC 60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Caution Clean the NI PXI-665*x* module with a soft nonmetallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

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Electromagnetic Compatibility

This product is designed to meet the requirements of the following standards of EMC for electrical equipment for measurement, control, and laboratory use:

- EN 61326 (IEC 61326): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note For the standards applied to assess the EMC of this product, refer to the *Online Product Certification* section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

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B

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Glossary

Symbol	Prefix	Value
p	pico	10^{-12}
n	nano	10^{-9}
μ	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^{3}
M	mega	10^{6}

Symbols

%	percent
±	plus or minus
+	positive of, or plus
-	negative of, or minus
/	per
°	degree
Ω	ohm

A

accumulator	a part where numbers are totaled or stored
ADE	application development environment
asynchronous	a property of an event that occurs at an arbitrary time, without synchronization to a reference clock

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B

backplane	an assembly, typically a printed circuit board (PCB), with 96-pin connectors and signal paths that bus the connector pins. PXI systems have two connectors, called the J1 and J2 connectors.
bus	the group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. An example of a PC bus is the PCI bus.

C

C	Celsius
CLKIN	CLKIN is a signal connected to the SMB input pin of the same name. CLKIN can serve as PXI_CLK10_IN or be used as a phase lock reference for the OCXO.
CLKOUT	CLKOUT is the signal on the SMB output pin of the same name. Either the OCXO clock or PXI_CLK10 can be routed to CLKOUT.
clock	hardware component that controls timing for reading from or writing to groups
CompactPCI	a Eurocard configuration of the PCI bus for industrial applications

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device that converts a digital number into a corresponding analog voltage or current
DAQ	data acquisition—(1) collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing; (2) collecting and measuring the same kinds of electrical signals with A/D and/or DIO devices plugged into a computer, and possibly generating control signals with D/A and/or DIO devices in the same computer

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DC	direct current
DDS	direct digital synthesis—a method of creating a clock with a programmable frequency

E

EEPROM	electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed
ESD	electrostatic discharge

F

frequency	the basic unit of rate, measured in events or oscillations per second using a frequency counter or spectrum analyzer. Frequency is the reciprocal of the period of a signal.
frequency tuning word	a number that specifies the frequency
front panel	the physical front panel of an instrument or other hardware

H

Hz	hertz—the number of scans read or updates written per second

I

in.	inch or inches

J

jitter	the rapid variation of a clock or sampling frequency from an ideal constant frequency

L

LabVIEW	a graphical programming language
LED	light-emitting diode—a semiconductor light source

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M

master	the requesting or controlling device in a master/slave configuration
Measurement & Automation Explorer (MAX)	a controlled centralized configuration environment that allows you to configure all of your National Instruments DAQ, GPIB, IMAQ, IVI, Motion, VISA, and VXI devices

N

NI-DAQ	National Instruments driver software for DAQ hardware

O

OCXO	oven-controlled crystal oscillator
oscillator	a device that generates a fixed frequency signal. An oscillator most often generates signals by using oscillating crystals, but also may use tuned networks, lasers, or atomic clock sources. The most important specifications on oscillators are frequency accuracy, frequency stability, and phase noise.
output impedance	the measured resistance and capacitance between the output terminals of a circuit

P

PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 Mbytes/s.
PFI	Programmable Function Interface
PLL	phase-locked loop
precision	the measure of the stability of an instrument and its capability to give the same measurement over and over again for the same input signal
propagation delay	the amount of time required for a signal to pass through a circuit

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PXI	a rugged, open system for modular instrumentation based on CompactPCI, with special mechanical, electrical, and software features. The PXIbus standard was originally developed by National Instruments in 1997, and is now managed by the PXIbus Systems Alliance.
PXI star	a special set of trigger lines in the PXI backplane for high-accuracy device synchronization with minimal latencies on each PXI slot
PXI_Trig/PXI_Star synchronization clock	the clock signal that is used to synchronize the RTSI/PXI triggers or PXI_STAR triggers on an NI PXI-6653

R

RTSI bus	Real-Time System Integration bus—the NI timing bus that connects DAQ devices directly, by means of connectors on top of the devices, for precise synchronization of functions

S

s	seconds
skew	the actual time difference between two events that would ideally occur simultaneously. Inter-channel skew is an example of the time differences introduced by different characteristics of multiple channels. Skew can occur between channels on one module, or between channels on separate modules (intermodule skew).
slave	a computer or peripheral device controlled by another computer
slot	the place in the computer or chassis in which a card or module can be installed
Slot 2	the second slot in a PXI system which can house a master timing unit
SMB	sub miniature type B—a small coaxial signal connector that features a snap coupling for fast connection
synchronous	a property of an event that is synchronized to a reference clock

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T

t_{CtoQ}	clock to output time
t_{hold}	hold time
t_{pd}	propagation delay time
TRIG	trigger signal
trigger	a digital signal that starts or times a hardware event (for example, starting a data acquisition operation)
t_{setup}	setup time

V

V	volts
VI	virtual instrument

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