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Multifunction RIO

NI R Series Multifunction RIO User Manual

NI 781xR, NI 783xR, NI 784xR, and NI 785xR Devices

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About This Manual

This manual describes the electrical and mechanical aspects of the National Instruments 781*x*R/783*x*R/784*x*R/785*x*R devices and contains information about programming and using the devices.

Conventions

The following conventions appear in this manual:



This icon denotes a note, which alerts you to important information.



This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on a product, refer to the *Read Me First: Safety and Electromagnetic Compatibility* document for information about precautions to take.



When symbol is marked on a product, it denotes a warning advising you to take precautions to avoid electrical shock.



When symbol is marked on a product, it denotes a component that may be hot. Touching this component may result in bodily injury.

NI 78*xx*R

NI 781*x*R, 783*x*R, NI 784*x*R, and NI 785*x*R refer to all PCI, PCI Express, and PXI R Series devices.

Related Documentation

The following documents contain information that you may find helpful as you use this help file. Your documentation needs may vary depending on the hardware and software you use for your application.



Note Most R Series manuals are available as PDFs. You must have Adobe Reader with Search and Accessibility 5.0.5 or later installed to view the PDFs. Refer to the Adobe Systems Incorporated Web site at `www.adobe.com` to download Adobe Reader. Refer to `ni.com/manuals` for updated documentation resources.

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Software Documentation

- LabVIEW FPGA documentation
  - *Getting Started with LabVIEW FPGA 8.x*—This KnowledgeBase, available at `ni.com/kb`, provides links to the top resources that can be used to assist in getting started with programming in LabVIEW FPGA.
  - *FPGA Module* book in the *LabVIEW Help*—Select **Help»Search the LabVIEW Help** in LabVIEW to view the *LabVIEW Help*. Browse the **FPGA Module** book in the **Contents** tab for information about using the FPGA Module to create VIs that run on the NI 78*xx*R device.
  - *LabVIEW FPGA Module Release and Upgrade Notes*—Contains information about installing the LabVIEW FPGA Module, describes new features, and provides upgrade information. To access this document, refer to `ni.com/manuals`. In LabVIEW 8.0 or later, you can also view the LabVIEW Manuals directory that contains this document by selecting **Start» All Programs»National Instruments»LabVIEW»LabVIEW Manuals**.
- LabVIEW Real-Time documentation
  - *Getting Started with the LabVIEW Real-Time Module*—Provides exercises to teach you how to develop a real-time project and VIs, from setting up RT targets to building, debugging, and deploying real-time applications. This document provides references to the LabVIEW Help and other Real-Time Module documents for more information as you create the real-time application. To access this document, refer to `ni.com/manuals`. In LabVIEW 8.0 or later, you can also view the LabVIEW Manuals directory that contains this document by selecting **Start»All Programs»National Instruments»LabVIEW»LabVIEW Manuals**.
  - *Real-Time Module* book in the *LabVIEW Help*—Select **Help» Search the LabVIEW Help** in LabVIEW to view the *LabVIEW Help*. Browse the **Real-Time Module** book in the **Contents** tab for information about how to build deterministic applications using the LabVIEW Real-Time Module.
  - *LabVIEW Real-Time Module Release and Upgrade Notes*—Includes information about system requirements, installation, configuration, new features and changes, and compatibility issues for the LabVIEW Real-Time Module. To access this document, refer to `ni.com/manuals`. In LabVIEW 8.0 or later, you can also view the LabVIEW Manuals

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directory that contains this document by selecting **Start»All Programs»National Instruments»LabVIEW»LabVIEW Manuals**.

Device-Specific Documentation

- *Getting Started with R Series Multifunction RIO*—This document explains how to install and configure NI 781*x*R/783*x*R/784*x*R/785*x*R, and contains a tutorial that demonstrates how to begin taking a measurement using LabVIEW FPGA. This document is available at `ni.com/manuals`.
- *NI R Series Multifunction RIO Specifications*—Lists the specifications of the NI 781*x*R/783*x*R/784*x*R/785*x*R R Series devices. This document is available at `ni.com/manuals`.

Additional Resources

The following documents contain information you might find helpful:

- NI Developer Zone tutorial, *Field Wiring and Noise Considerations for Analog Signals*, at `ni.com/zone`
- *PICMG CompactPCI 2.0 R3.0*
- *PXI Hardware Specification Revision 2.1*
- *PXI Software Specification Revision 2.1*
- *National Instruments Example Finder*—LabVIEW contains an extensive library of VIs and example programs for use with R Series devices. To access the NI Example Finder, open LabVIEW and select **Help»Find Examples**, then select **Hardware Input and Output»R Series**.
- *LabVIEW FPGA IPNet*—Offers resources for browsing, understanding, and downloading LabVIEW FPGA functions or IP (Intellectual Property). Use this resource to acquire IP that you need for your application, download examples to help learn programming techniques, and explore the depth of IP offered by the LabVIEW FPGA platform. To access the LabVIEW FPGA IPNet, visit `ni.com/ipnet`.

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1 Introduction

This chapter describes the NI 781*x*R/783*x*R/784*x*R/785*x*R, the concept of the Reconfigurable I/O (RIO) device, optional software and equipment for using the NI 78*xx*R, and safety information about the NI 78*xx*R.

About the Reconfigurable I/O Device

Table 1-1 lists an overview of the NI 78*xx*R R Series Multifunction RIO devices.

Table 1-1. NI 78*xx*R R Series Multifunction RIO Device Overview

Device	I/O Channels	FPGA	AI Sample Rate
NI PCI/PXI-7811R	160 DIO	Virtex-II XC2V1000	—
NI PCI/PXI-7813R	160 DIO	Virtex-II XC2V3000	—
NI PCI/PXI-7830R	4 AI, 4 AO, 56 DIO	Virtex-II XC2V1000	200 kS/s
NI PCI/PXI-7831R	8 AI, 8 AO, 96 DIO	Virtex-II XC2V1000	200 kS/s
NI PCI/PXI-7833R	8 AI, 8 AO, 96 DIO	Virtex-II XC2V3000	200 kS/s
NI PCIe/PXI-7841R	8 AI, 8 AO, 96 DIO	Virtex-5 LX30	200 kS/s
NI PCIe/PXI-7842R	8 AI, 8 AO, 96 DIO	Virtex-5 LX50	200 kS/s
NI PCIe/PXI-7851R	8 AI, 8 AO, 96 DIO	Virtex-5 LX30	750 kS/s
NI PCIe/PXI-7852R	8 AI, 8 AO, 96 DIO	Virtex-5 LX50	750 kS/s
NI PXI-7853R	8 AI, 8 AO, 96 DIO	Virtex-5 LX85	750 kS/s
NI PXI-7854R	8 AI, 8 AO, 96 DIO	Virtex-5 LX110	750 kS/s

A user-reconfigurable FPGA (Field-Programmable Gate Array) controls the digital I/O lines on the NI 781*x*R, and the digital and analog I/O lines on the NI 783*x*R/784*x*R/785*x*R. The FPGA on the R Series device allows you to define the functionality and timing of the device. You can change the functionality of the FPGA on the R Series device in LabVIEW using the LabVIEW FPGA Module to create and download a custom virtual

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instrument (VI) to the FPGA. Using the FPGA Module, you can graphically design the timing and functionality of the R Series device. If you only have LabVIEW but not the FPGA Module, you cannot create new FPGA VIs, but you can create VIs that run on Windows or a LabVIEW Real-Time (RT) target to control existing FPGA VIs.

Some applications require tasks such as real-time, floating-point processing or datalogging while performing I/O and logic on the R Series device. You can use the LabVIEW Real-Time Module to perform these additional applications while communicating with and controlling the R Series device.

The R Series device contains Flash memory to store a startup VI for automatic loading of the FPGA when the system is powered on.

The NI 78*xx*R uses the Real-Time System Integration (RTSI) bus to easily synchronize several measurement functions to a common trigger or timing event. R Series PCI devices access the RTSI bus through a RTSI cable connected between devices. R Series PXI devices access the RTSI bus through the PXI trigger lines implemented on the PXI backplane.

Refer to the *NI R Series Multifunction RIO Specifications*, available at `ni.com/manuals`, for detailed device specifications.

Using PXI with CompactPCI

Using PXI-compatible products with standard CompactPCI products is an important feature provided by *PXI Hardware Specification Revision 2.1* and *PXI Software Specification Revision 2.1*. If you use a PXI-compatible plug-in card in a standard CompactPCI chassis, you cannot use PXI-specific functions, but you still can use the basic plug-in card functions. For example, the RTSI bus on the R Series device is available in a PXI chassis but not in a CompactPCI chassis.

The CompactPCI specification permits vendors to develop sub-buses that coexist with the basic PCI interface on the CompactPCI bus. Compatible operation is not guaranteed between CompactPCI devices with different sub-buses nor between CompactPCI devices with sub-buses and PXI. The standard implementation for CompactPCI does not include these sub-buses. The R Series device works in any standard CompactPCI chassis adhering to the *PICMG CompactPCI 2.0 R3.0* core specification.

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PXI-specific features are implemented on the J2 connector of the CompactPCI bus. Table 1-2 lists the J2 pins used by the NI PXI-78*xx*R. The NI 78*xx*R is compatible with any CompactPCI chassis with a sub-bus that does not drive these lines. Even if the sub-bus is capable of driving these lines, the R Series device is still compatible as long as those pins on the sub-bus are disabled by default and are never enabled.

Caution Damage can result if the J2 lines are driven by the sub-bus.

Table 1-2. Pins Used by the NI PXI-78*xx*R

NI PXI-78*xx*R Signal	PXI Pin Name	PXI J2 Pin Number
PXI_Trig<0..7>	PXI Trigger<0..7>	A16, A17, A18, B16, B18, C18, E16, E18
PXI_Clk10	PXI Clock 10 MHz	E17
PXI_Star	PXI Star Trigger	D17
PXI_Lbl<0..12>*	LBL<0..12>	A1, A19, C1, C19, C20, D1, D2, D15, D19, E1, E2, E19, E20
PXI_Lbr<0..12>*	LBR<0..12>	A2, A3, A20, A21, B2, B20, C3, C21, D3, D21, E3, E15, E21
* NI PXI-781*x*R/783*x*R only		

Overview of Reconfigurable I/O

This section explains reconfigurable I/O and describes how to use the LabVIEW FPGA Module to build high-level functions in hardware.

Refer to Chapter 2, *Hardware Overview of the NI 78xxR*, for descriptions of the I/O resources on the NI 78*xx*R.

Reconfigurable I/O Concept

R Series Multifunction RIO devices are based on a reconfigurable FPGA core surrounded by fixed I/O resources for analog and digital input and output. You can configure the behavior of the reconfigurable FPGA to match the requirements of the measurement and control system. You can implement this user-defined behavior as an FPGA VI to create an application-specific I/O device.

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Flexible Functionality

Flexible functionality allows the NI 78*xx*R to match individual application requirements and to mimic the functionality of fixed I/O devices. For example, you can configure an R Series device in one application for three 32-bit quadrature encoders and then reconfigure the R Series device in another application for eight 16-bit event counters.

You also can use the R Series device with the LabVIEW Real-Time Module in timing and triggering applications, such as control and hardware-in-the-loop (HIL) simulations. For example, you can configure the R Series device for a single timed loop in one application and then reconfigure the device in another application for four independent timed loops with separate I/O resources.

User-Defined I/O Resources

You can create your own custom measurements using the fixed I/O resources. For example, one application might require an event counter that increments when a rising edge appears on any of three digital input lines. With an NI 783*x*R/784*x*R/785*x*R R Series device, another application might require a digital line to be asserted after an analog input exceeds a programmable threshold. You can implement these behaviors in the hardware for fast, deterministic performance.

Device-Embedded Logic and Processing

You can implement LabVIEW logic and processing in the FPGA of the R Series device. Typical logic functions include Boolean operations, comparisons, and basic mathematical operations. You can implement multiple functions efficiently in the same design, operating sequentially or in parallel. You also can implement more complex algorithms such as control loops. You are limited only by the size of the FPGA.

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Reconfigurable I/O Architecture

Figure 1-1 shows an FPGA connected to fixed I/O resources and a bus interface. The fixed I/O resources include A/D converters (ADCs), D/A converters (DACs), and digital I/O lines.

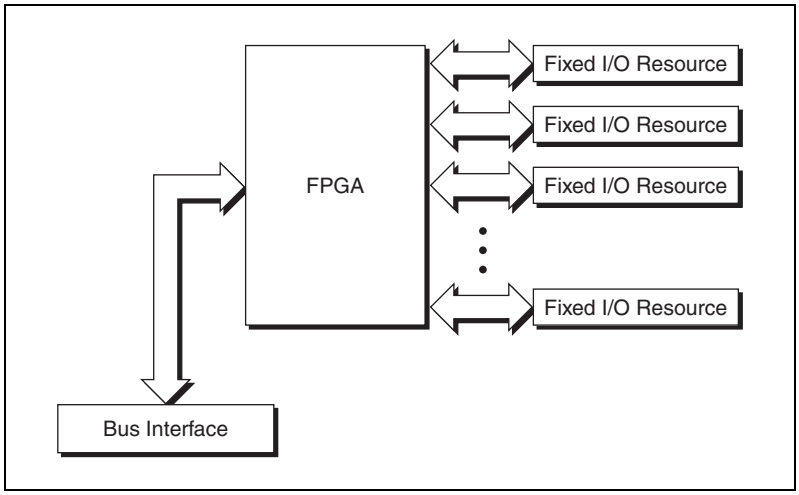


Figure 1-1. High-Level FPGA Functional Overview

Software accesses the R Series device through the bus interface, and the FPGA connects the bus interface and the fixed I/O to make possible timing, triggering, processing, and custom I/O measurements using the LabVIEW FPGA Module.

The FPGA logic provides timing, triggering, processing, and custom I/O measurements. Each fixed I/O resource used by the application uses a small portion of the FPGA logic that controls the fixed I/O resource. The bus interface also uses a small portion of the FPGA logic to provide software access to the device.

The remaining FPGA logic is available for higher-level functions such as timing, triggering, and counting. The functions use varied amounts of logic.

You can place useful applications in the FPGA. How much FPGA space your application requires depends on your need for I/O recovery, I/O, and logic algorithms.

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The FPGA does not retain the VI when the R Series device is powered off, so you must reload the VI each time you power on the device. You can load the VI from onboard Flash memory or from software over the bus interface. One advantage to using Flash memory is that the VI can start executing almost immediately after power up, instead of waiting for the computer to completely boot and load the FPGA VI. Refer to the *LabVIEW Help* for more information about how to store your VI in Flash memory.

Reconfigurable I/O Applications

You can use the LabVIEW FPGA Module to create or acquire new VIs for your application. The FPGA Module allows you to define custom functionality for the R Series device using a subset of LabVIEW functionality. Refer to the R Series examples, available in LabVIEW by selecting **Help»Find Examples**, and then selecting **Hardware Input and Output»R Series**, for examples of FPGA VIs.

Software Development

You can use LabVIEW with the LabVIEW FPGA Module to program the NI 78*xx*R. To develop real-time applications that control the NI 78*xx*R, use LabVIEW with the LabVIEW Real-Time Module.

LabVIEW FPGA Module

The LabVIEW FPGA Module enables you to use LabVIEW to create VIs that run on the FPGA of the R Series target device. Use the FPGA Module VIs and functions to control the I/O, timing, and logic of the R Series device and to generate interrupts for synchronization. Select **Help»Search the LabVIEW Help** to view the *LabVIEW Help*. In the *LabVIEW Help*, use the **Contents** tab to browse to the **FPGA Interface** book for more information about the FPGA Interface functions.

You can use Interactive Front Panel Communication to communicate directly with the FPGA VI running on the FPGA target. You can use Programmatic FPGA Interface Communication to programmatically control and communicate with FPGA VIs from host VIs.

Use the FPGA Interface functions when you target LabVIEW for Windows or an RT target to create host VIs that wait for interrupts and control the FPGA by reading and writing the FPGA VI running on the R Series device.

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Note If you use the R Series device without the FPGA Module, you can use the RIO Device Setup utility, available by selecting **Start»All Programs»National Instruments»NI-RIO»RIO Device Setup** to download precomplied FPGA VIs to the Flash memory of the R Series device. This utility installs with NI-RIO. You also can use the utility to configure the analog input mode, to synchronize the clock on the R Series device to the PXI clock (for NI PXI-78*xx*R only), and to configure when the VI loads from Flash memory. For more information about using the RIO Device Setup utility, refer to the *RIO Device Setup Help*, found at **Start»All Programs»National Instruments»NI-RIO»RIO Device Setup Help**.

LabVIEW Real-Time Module

The LabVIEW Real-Time Module extends the LabVIEW development environment to deliver deterministic, real-time performance.

You can write host VIs that run in Windows or on RT targets to communicate with FPGA VIs that run on the NI 78*xx*R. You can develop real-time VIs with LabVIEW and the LabVIEW Real-Time Module, and then download the VIs to run on a hardware target with a real-time operating system. The LabVIEW Real-Time Module allows you to use the NI 78*xx*R in RT Series PXI systems being controlled in real time by a VI.

The NI 781*x*R is designed as a single-point DIO complement to the LabVIEW Real-Time Module. The NI 783*x*R/784*x*R/785*x*R is designed as a single-point AI, AO, and DIO complement to the LabVIEW Real-Time Module. Refer to the *LabVIEW Help*, available by selecting **Help»Search the LabVIEW Help**, for more information about the LabVIEW Real-Time Module.

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Cables and Accessories

National Instruments offers a variety of products you can use with R Series devices, including cables, connector blocks, and other accessories, as shown in Table 1-3.

Table 1-3. R Series Connectivity Options

Cable	Connector		Accessory	Description
	NI 781*x*R	NI 783*x*R/ 784*x*R/785*x*R		
SHC68-68-RMIO (NI Recommended)	—	0	NI SCB-68	High-performance shielded cable wired specifically for signal connection from the RMIO connector* to the NI SCB-68 terminal block to provide higher signal integrity and noise immunity.
SHC68-68-RDIO (NI Recommended)	0, 1, 2, 3	1, 2†	NI SCB-68	High-performance shielded cable wired specifically for signal connection from the RDIO connector* to the NI SCB-68 terminal block to provide higher signal integrity and noise immunity.
SH68-C68-S	0, 1, 2, 3	1, 2†	NI SCB-68	Basic shielded cable for signal connection from the RMIO or RDIO connector to the NI SCB-68 terminal block for noise reduction.

* For a diagram of the twisted pairs in the SHC68-68-RMIO and SHC68-68-RDIO cables and the signals to which they correspond, go to `ni.com/info` and enter the info code `rdrmio`.

† NI 7830R does not have Connector 2.

Refer to Appendix A, *Connecting I/O Signals*, for more information about using these cables and accessories to connect I/O signals to the NI 78*xx*R. Refer to `ni.com/products` or contact the sales office nearest to you for the most current cabling options.

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Custom Cabling

NI offers a variety of cables for connecting signals to the NI 78*xx*R. If you need to develop a custom cable, a nonterminated shielded cable is available from NI. The SHC68-NT-S connects to the NI 78*xx*R VHDCI connectors on one end of the cable. The other end of the cable is not terminated. This cable ships with a wire list identifying the wires that correspond to each NI 78*xx*R pin. You can use this cable to quickly connect the NI 78*xx*R signals that you need to the connector of your choice. Refer to Appendix A, *Connecting I/O Signals*, for the NI 78*xx*R connector pinouts.

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2

Hardware Overview of the NI 78*xx*R

This chapter presents an overview of the hardware functions and I/O connectors on the NI 78*xx*R.

Figure 2-1 shows a block diagram for the NI 781*x*R. Figure 2-2 shows a block diagram for the NI 7830R. Figure 2-3 shows a block diagram for the NI 7831R/7833R/784*x*R/785*x*R.

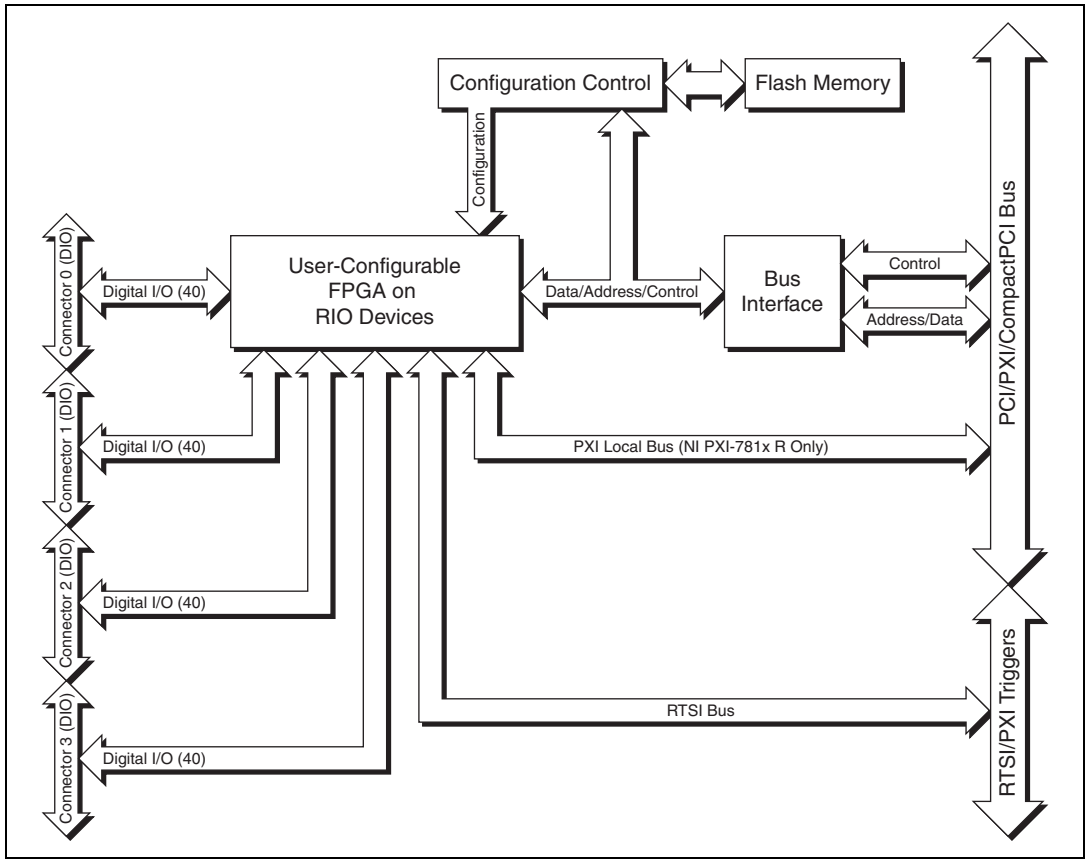


Figure 2-1. NI 781*x*R Block Diagram

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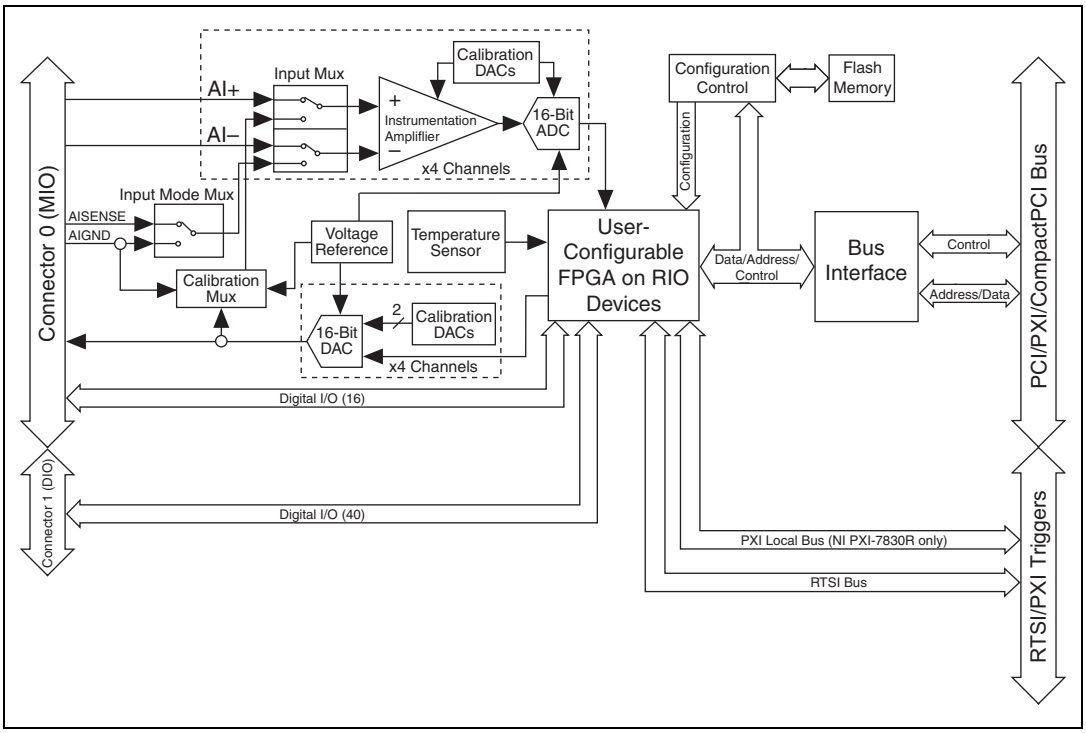


Figure 2-2. NI 7830R Block Diagram

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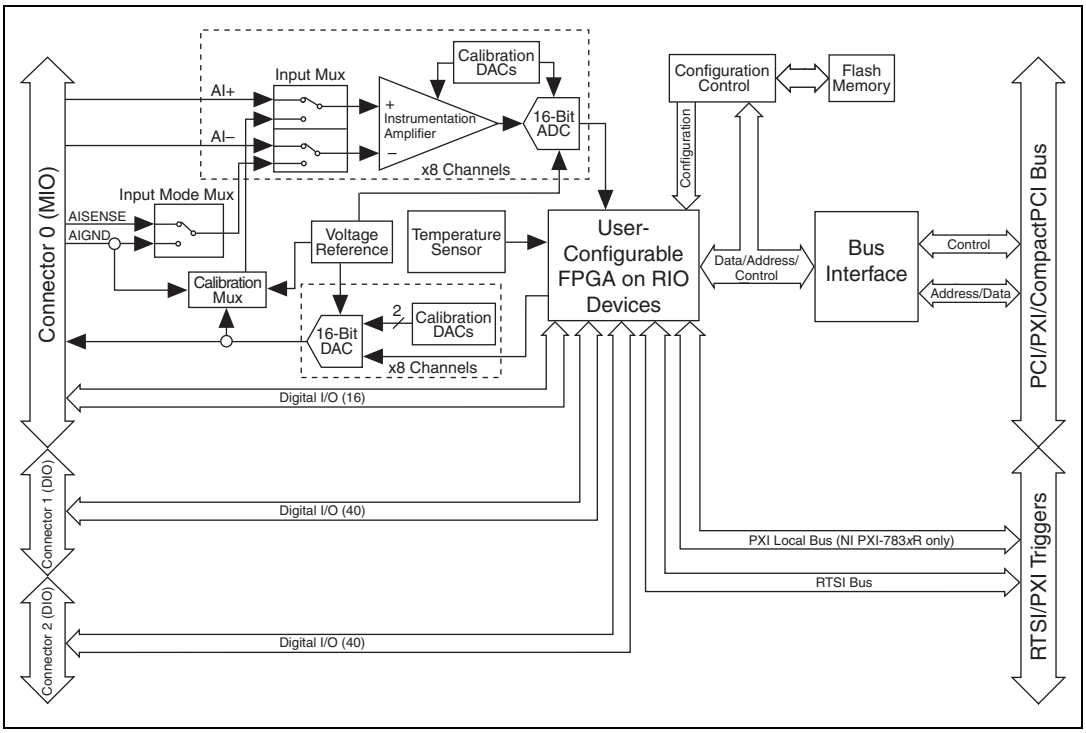


Figure 2-3. NI 7831R/7833R/784*x*R/785*x*R Block Diagram

NI 7811R Overview

The NI 7811R has 160 bidirectional DIO lines and a Virtex-II XC2V1000 FPGA.

NI 7813R Overview

The NI 7813R has 160 bidirectional DIO lines and a Virtex-II XC2V3000 FPGA.

NI 7830R Overview

The NI 7830R has four independent, 16-bit AI channels; four independent, 16-bit AO channels; 56 bidirectional DIO lines that you can configure individually for input or output; and a Virtex-II XC2V1000 FPGA.

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NI 7831R/7833R Overview

The NI 7831R/7833R each have eight independent, 16-bit AI channels; eight independent, 16-bit AO channels; 96 bidirectional DIO lines that you can configure individually for input or output; and a Virtex-II XC2V3000 FPGA.

NI 784*x*R Overview

The NI 784*x*R each have eight independent, 16-bit AI channels; eight independent, 16-bit AO channels; and 96 bidirectional DIO lines that you can configure individually for input or output. The NI PXI-7841R has a Virtex-5 LX30 FPGA, and the NI PXI-7842R has a Virtex-5 LX50 FPGA.

NI 785*x*R Overview

The NI 785*x*R each have eight independent, 16-bit AI channels; eight independent, 16-bit AO channels; and 96 bidirectional DIO lines that you can configure individually for input or output. The NI PXI-7851R has a Virtex-5 LX30 FPGA, the NI PXI-7852R has a Virtex-5 LX50 FPGA, the NI PXI-7853R has a Virtex-5 LX85 FPGA, and the NI PXI-7854R has a Virtex-5 LX110 FPGA.

Analog Input (NI 783*x*R/784*x*R/785*x*R Only)

You can sample NI 783*x*R/784*x*R/785*x*R AI channels simultaneously or at different rates. The input mode is software configurable, and the input range is fixed at ±10 V. The converters return data in two's complement format. Table 2-1 shows the ideal output code returned for a given AI voltage.

Table 2-1. Ideal Output Code and AI Voltage Mapping

Input Description	AI Voltage	Output Code (Hex) (Two's Complement)
Full-scale range –1 LSB	9.999695	7FFF
Full-scale range –2 LSB	9.999390	7FFE
Midscale	0.000000	0000

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Table 2-1. Ideal Output Code and AI Voltage Mapping (Continued)

Input Description	AI Voltage	Output Code (Hex) (Two's Complement)
Negative full-scale range +1 LSB	–9.999695	8001
Negative full-scale range	–10.000000	8000
Any input voltage	$\frac{Output\ Code}{32{,}768} \times 10.0\ \text{V}$	—

Input Modes

The NI 783*x*R/784*x*R/785*x*R input mode is software configurable. The input channels support three input modes—differential (DIFF), referenced single ended (RSE), and nonreferenced single ended (NRSE). The selected input mode applies to all the input channels. Table 2-2 describes the three input modes.

Table 2-2. Available Input Modes for the NI 783*x*R/784*x*R/785*x*R

Input Mode	Description
DIFF	When the NI 783*x*R/784*x*R/785*x*R is configured in DIFF input mode, each channel uses two AI lines. The positive input pin connects to the positive terminal of the onboard instrumentation amplifier. The negative input pin connects to the negative input of the instrumentation amplifier.
RSE	When the NI 783*x*R/784*x*R/785*x*R is configured in RSE input mode, each channel uses only its positive AI pin. This pin connects to the positive terminal of the onboard instrumentation amplifier. The negative input of the instrumentation amplifier connects internally to the AI ground (AIGND).
NRSE	When the NI 783*x*R/784*x*R/785*x*R is configured in NRSE input mode, each channel uses only its positive AI pin. This pin connects to the positive terminal of the onboard instrumentation amplifier. The negative input of the instrumentation amplifier on each AI channel connects internally to the AISENSE input pin.

Input Range

The NI 783*x*R/784*x*R/785*x*R AI range is fixed at ±10 V.

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Connecting Analog Input Signals

The AI signals for the NI 783*x*R/784*x*R/785*x*R are AI<0..*n*>+, AI<0..*n*>–, AIGND, and AISENSE. For the NI 7830R, *n*=4. For the NI 7831R/7833R/784*x*R/785*x*R, *n*=8. The AI<0..*n*>+ and AI<0..*n*>– signals are connected to the eight AI channels of the NI 783*x*R/784*x*R/785*x*R. For all input modes, the AI<0..*n*>+ signals are connected to the positive input of the instrumentation amplifier on each channel. The signal connected to the negative input of the instrumentation amplifier depends on how you configure the input mode of the device.

In differential input mode, signals connected to AI<0..*n*>– are routed to the negative input of the instrumentation amplifier for each channel. In RSE input mode, the negative input of the instrumentation amplifier for each channel is internally connected to AIGND. In NRSE input mode, the AISENSE signal is connected internally to the negative input of the instrumentation amplifier for each channel. In DIFF and RSE input modes, AISENSE is not used.

Caution Exceeding the differential and common-mode input ranges distorts the input signals. Exceeding the maximum input voltage rating can damage the NI 783*x*R/784*x*R/785*x*R and the computer. NI is *not* liable for any damage resulting from such signal connections. The maximum input voltage ratings are listed in Table A-2, *NI 78xxR I/O Signal Summary*.

AIGND is a common AI signal that is routed directly to the ground tie point on the NI 783*x*R/784*x*R/785*x*R. You can use this signal for a general analog ground tie point to the NI 783*x*R/784*x*R/785*x*R if necessary.

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Connection of AI signals to the NI 783*x*R/784*x*R/785*x*R depends on the input mode of the AI channels you are using and the type of input signal source. With different input modes, you can use the instrumentation amplifier in different ways. Figure 2-4 shows a diagram of the NI 783*x*R/784*x*R/785*x*R instrumentation amplifier.

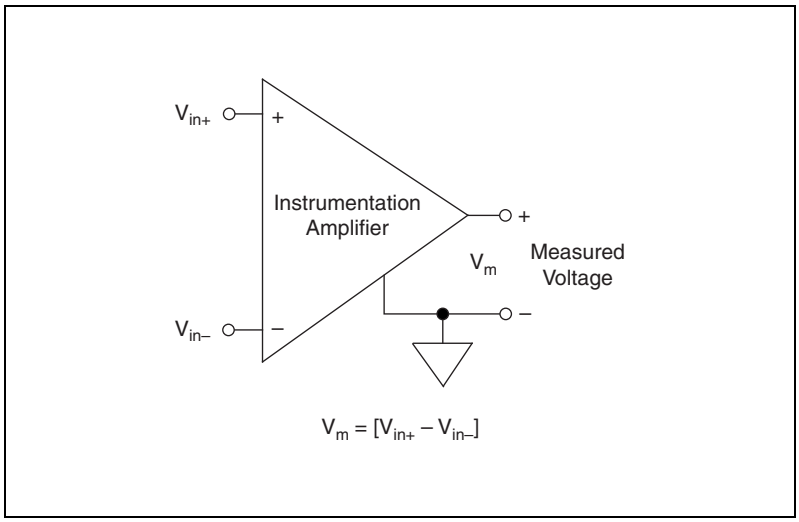


Figure 2-4. NI 783*x*R/784*x*R/785*x*R Instrumentation Amplifier

The instrumentation amplifier applies common-mode voltage rejection and presents high input impedance to the AI signals connected to the NI 783*x*R/784*x*R/785*x*R. Input multiplexers on the device route signals to the positive and negative inputs of the instrumentation amplifier. The instrumentation amplifier converts two input signals to a signal that is the difference between the two input signals. The amplifier output voltage is referenced to the device ground. The NI 783*x*R/784*x*R/785*x*R ADC measures this output voltage when it performs A/D conversions.

You must reference all signals to ground either at the source device or at the NI 783*x*R/784*x*R/785*x*R. If you have a floating source, reference the signal to ground by using RSE input mode or the DIFF input mode with bias resistors. Refer to the *Differential Connections for Nonreferenced or Floating Signal Sources* section of this chapter for more information about these input modes. If you have a grounded source, do not reference the signal to AIGND. You can avoid this reference by using DIFF or NRSE input modes.

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Types of Signal Sources

When configuring the input channels and making signal connections, you must first determine whether the signal sources are floating or ground referenced. The following sections describe these two signal types.

Floating Signal Sources

A floating signal source is not connected to the building ground system but instead has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source.
You must connect the ground reference of a floating signal to the NI 783*x*R/784*x*R/785*x*R AIGND through a bias resistor to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats out of the common-mode input range.

Ground-Referenced Signal Sources

A ground-referenced signal source is connected to the building system ground, so it is already connected to a common ground point with respect to the NI 783*x*R/784*x*R/785*x*R, assuming that the computer is plugged into the same power system. Instruments or devices with nonisolated outputs that plug into the building power system are ground referenced signal sources.

The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV. This difference can be much higher if power distribution circuits are improperly connected. If a grounded signal source is improperly measured, this difference might appear as a measurement error. The connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

Input Modes

The following sections discuss single-ended and differential measurements and considerations for measuring both floating and ground-referenced signal sources.

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Figure 2-5 summarizes the recommended input mode for both types of signal sources.

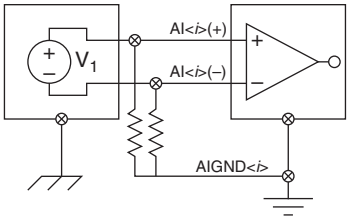
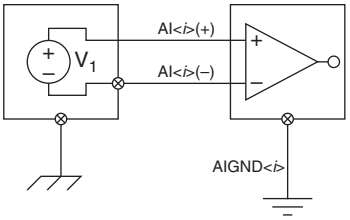
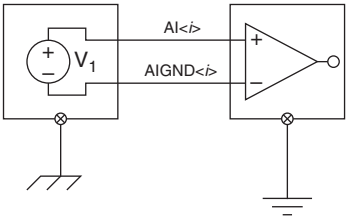
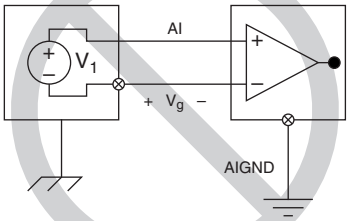
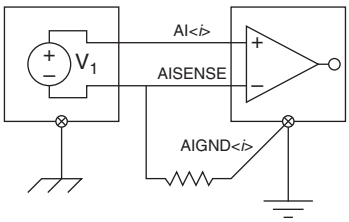
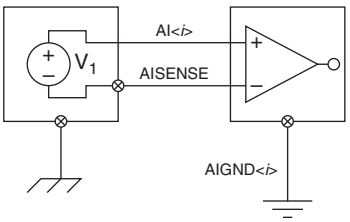
Input	Signal Source Type	
	Floating Signal Source (Not Connected to Building Ground)	**Grounded Signal Source**
	Examples • Ungrounded Thermocouples • Signal Conditioning with Isolated Outputs • Battery Devices	Examples • Plug-in Instruments with Nonisolated Outputs
Differential (DIFF)	 See text for information on bias resistors.	
Single-Ended—Ground Referenced (RSE)		NOT RECOMMENDED  Ground-loop losses, V_g, are added to measured signal.
Single-Ended—Nonreferenced (NRSE)	 See text for information on bias resistors.	

Figure 2-5. Summary of Analog Input Connections

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Differential Connection Considerations (DIFF Input Mode)

In DIFF input mode, the NI 783*x*R/784*x*R/785*x*R measures the difference between the positive and negative inputs. DIFF input mode is ideal for measuring ground-referenced signals from other devices. When using DIFF input mode, the input signal connects to the positive input of the instrumentation amplifier and its reference signal, or return, connects to the negative input of the instrumentation amplifier.

Use differential input connections for any channel that meets any of the following conditions:

- The input signal is low level (less than 1 V).
- The leads connecting the signal to the NI 783*x*R/784*x*R/785*x*R are greater than 3 m (10 ft).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce noise pickup and increase common-mode noise rejection. Differential signal connections also allow input signals to float within the common-mode limits of the instrumentation amplifier.

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Differential Connections for Ground-Referenced Signal Sources

Figure 2-6 shows how to connect a ground-referenced signal source to a channel on the NI 783*x*R/784*x*R/785*x*R configured in DIFF input mode.

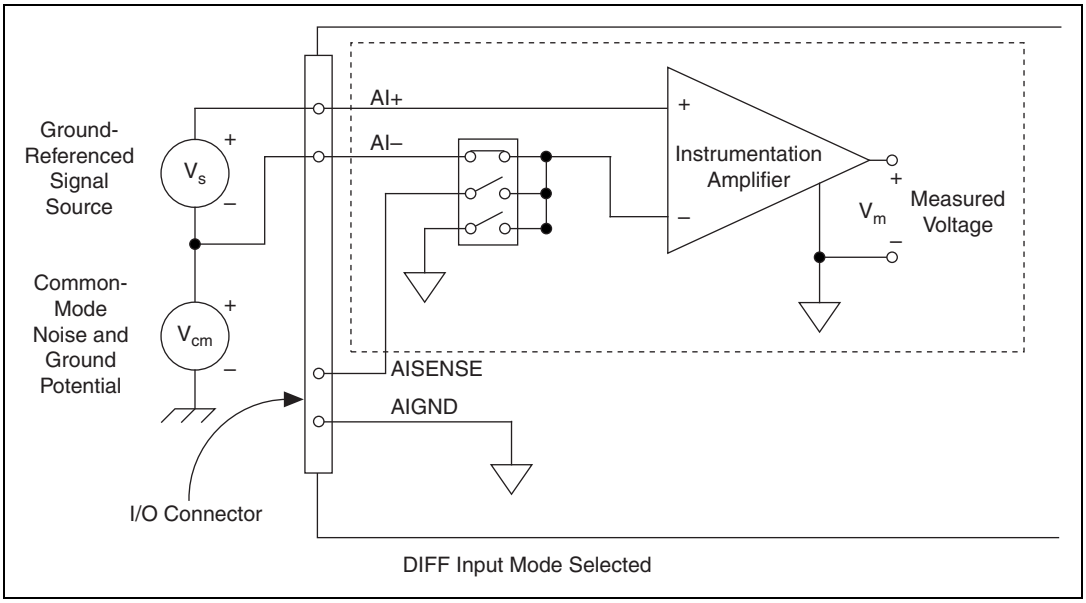


Figure 2-6. Differential Input Connections for Ground-Referenced Signals

With this connection type, the instrumentation amplifier rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the NI 783*x*R/784*x*R/785*x*R ground, shown as V_{cm} in Figure 2-6. In addition, the instrumentation amplifier can reject common-mode noise pickup in the leads connecting the signal sources to the device. The instrumentation amplifier can reject common-mode signals when $V+_{in}$ and $V-_{in}$ (input signals) are both within their specified input ranges. Refer to the *NI R Series Multifunction RIO Specifications*, available at `ni.com/manuals`, for more information about input ranges.

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Differential Connections for Nonreferenced or Floating Signal Sources

Figure 2-7 shows how to connect a floating signal source to a channel on the NI 783*x*R/784*x*R/785*x*R configured in DIFF input mode.

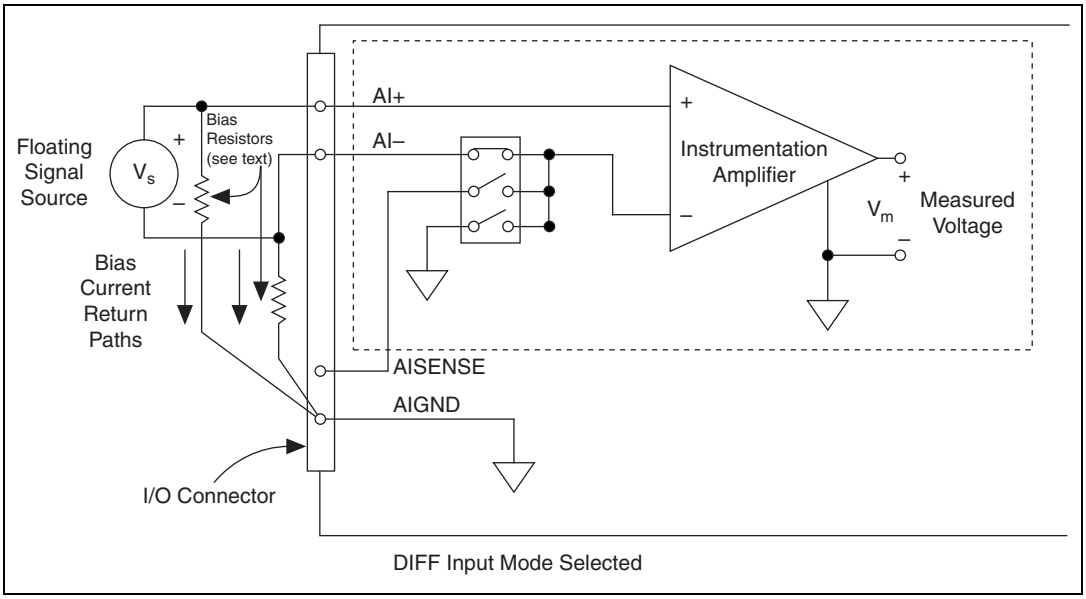


Figure 2-7. Differential Input Connections for Nonreferenced Signals

Figure 2-7 shows two bias resistors connected in parallel with the signal leads of a floating signal source. If you do not use the resistors and the source is truly floating, the source might not remain within the common-mode signal range of the instrumentation amplifier, causing erroneous readings. You must reference the source to AIGND by connecting the positive side of the signal to the positive input of the instrumentation amplifier and connecting the negative side of the signal to AIGND and to the negative input of the instrumentation amplifier without resistors. This connection works well for DC-coupled sources with low source impedance, less than 100 Ω.

For larger source impedances, this connection leaves the differential signal path significantly out of balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line because it is connected to ground. Hence, this noise appears as a differential-mode signal instead of a common-mode signal, and the instrumentation amplifier does not reject it. In this case, instead of directly connecting the negative

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line to AIGND, connect it to AIGND through a resistor that is about 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance. About the same amount of noise couples onto both connections, which yields better rejection of electrostatically coupled noise. Also, this input mode does not load down the source, other than the very high-input impedance of the instrumentation amplifier.

You can fully balance the signal path by connecting another resistor of the same value between the positive input and AIGND, as shown in Figure 2-7. This fully balanced input mode offers slightly better noise rejection but has the disadvantage of loading down the source with the series combination (sum) of the two resistors. If, for example, the source impedance is 2 kΩ and each of the two resistors is 100 kΩ, the resistors load down the source with 200 kΩ and produce a –1% gain error.

Both inputs of the instrumentation amplifier require a DC path to ground for the instrumentation amplifier to work. If the source is AC coupled (capacitively coupled), the instrumentation amplifier needs a resistor between the positive input and AIGND. If the source has low-impedance, choose a resistor that is large enough not to significantly load the source but small enough not to produce significant input offset voltage as a result of input bias current, typically 100 kΩ to 1 MΩ. In this case, connect the negative input directly to AIGND. If the source has high output impedance, balance the signal path as previously described using the same value resistor on both the positive and negative inputs. Loading down the source causes some gain error.

Single-Ended Connection Considerations

When an NI 783*x*R/784*x*R/785*x*R AI signal is referenced to a ground that can be shared with other input signals, it forms a single-ended connection. The input signal connects to the positive input of the instrumentation amplifier and the ground connects to the negative input of the instrumentation amplifier.

You can use single-ended input connections for any input signal that meets the following conditions:

- The input signal is high-level (>1 V).
- The leads connecting the signal to the NI 783*x*R/784*x*R/785*x*R are less than 3 m (10 ft).
- The input signal can share a common reference point with other signals.

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Use DIFF input connections for greater signal integrity for any input signal that does not meet the preceding conditions.

You can configure the NI 783*x*R/784*x*R/785*x*R channels in software for RSE or NRSE input modes. Use the RSE input mode for floating signal sources. In this case, the NI 783*x*R/784*x*R/785*x*R provides the reference ground point for the external signal. Use the NRSE input mode for ground-referenced signal sources. In this case, the external signal supplies its own reference ground point and the NI 783*x*R/784*x*R/785*x*R should not supply one.

In single-ended input modes, electrostatic and magnetic noise couples into the signal connections more than in differential input modes. The coupling is the result of differences in the signal path. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two conductors.

Single-Ended Connections for Floating Signal Sources (RSE Input Mode)

Figure 2-8 shows how to connect a floating signal source to a channel on the NI 783*x*R/784*x*R/785*x*R configured for RSE input mode.

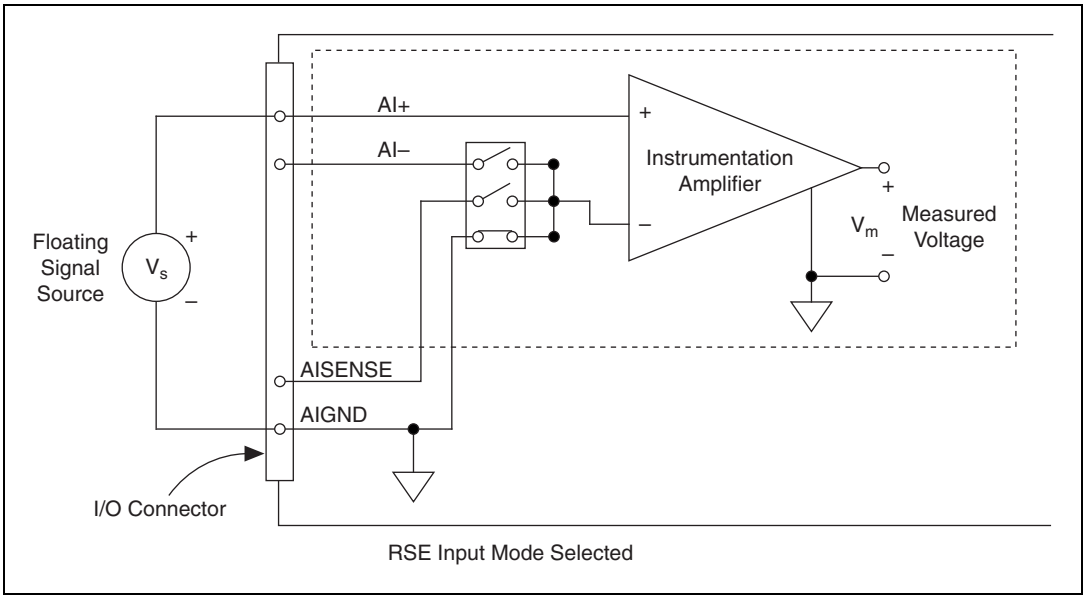


Figure 2-8. Single-Ended Input Connections for Nonreferenced or Floating Signals

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Single-Ended Connections for Grounded Signal Sources (NRSE Input Mode)

To measure a grounded signal source with a single-ended input mode, you must configure the NI 783*x*R/784*x*R/785*x*R in the NRSE input mode. Then connect the signal to the positive input of the NI 783*x*R/784*x*R/785*x*R instrumentation amplifier and connect the signal local ground reference to the negative input of the instrumentation amplifier. The ground point of the signal should be connected to AISENSE. Any potential difference between the NI 783*x*R/784*x*R/785*x*R ground and the signal ground appears as a common-mode signal at both the positive and negative inputs of the instrumentation amplifier. The instrumentation amplifier rejects this difference. If the input circuitry of a NI 783*x*R/784*x*R/785*x*R is referenced to ground in RSE input mode, this difference in ground potentials appears as an error in the measured voltage.

Figure 2-9 shows how to connect a grounded signal source to a channel on the NI 783*x*R/784*x*R/785*x*R configured for NRSE input mode.

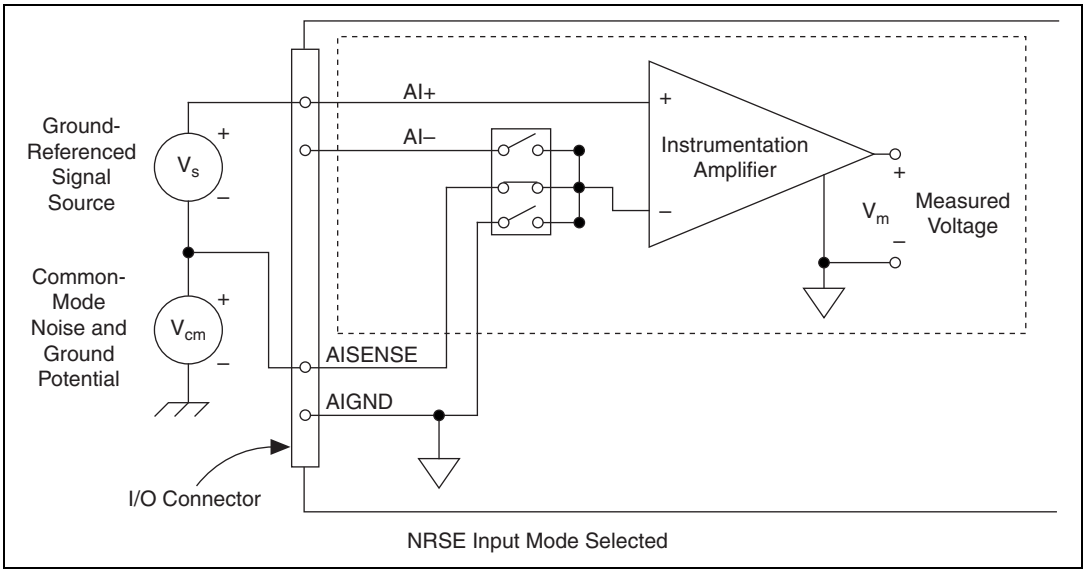


Figure 2-9. Single-Ended Input Connections for Ground-Referenced Signals

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Common-Mode Signal Rejection Considerations

Figure 2-6 and Figure 2-9 show connections for signal sources that are already referenced to some ground point with respect to the NI 783*x*R/784*x*R/785*x*R. In these cases, the instrumentation amplifier can reject any voltage caused by ground potential differences between the signal source and the device. With differential input connections, the instrumentation amplifier can reject common-mode noise pickup in the leads connecting the signal sources to the device. The instrumentation amplifier can reject common-mode signals when $V+_{in}$ and $V-_{in}$ (input signals) are both within their specified input ranges. Refer to the *NI R Series Multifunction RIO Specifications*, available at `ni.com/manuals`, for more information about input ranges.

Analog Output

The bipolar output range of the NI 783*x*R/784*x*R/785*x*R AO channels is fixed at ±10 V. Some applications require that the AO channels power on to known voltage levels. To set the power-on levels, you can configure the NI 783*x*R/784*x*R/785*x*R to load and run a VI when the system powers on. The VI can set the AO channels to the desired voltage levels. The VI interprets data written to the DAC in two's complement format. Table 2-3 shows the ideal AO voltage generated for a given input code.

Table 2-3. Ideal Output Voltage and Input Code Mapping

Output Description	AO Voltage	Input Code (Hex) (Two's Complement)
Full-scale range –1 LSB	9.999695	7FFF
Full-scale range –2 LSB	9.999390	7FFE
Midscale	0.000000	0000
Negative full-scale range, +1 LSB	–9.999695	8001
Negative full-scale range	–10.000000	8000
Any output voltage	—	$\frac{AO\ Voltage}{10.0\ V} \times 32{,}768$

Note If your VI does not set the output value for an AO channel, then the AO channel voltage output will be undefined.

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Connecting Analog Output Signals

The AO signals are AO <0..*n*> and AOGND.

AO <0..*n*> are the AO channels. AOGND is the ground reference signal for the AO channels.

Figure 2-10 shows how to make AO connections to the NI 783*x*R/784*x*R/785*x*R.

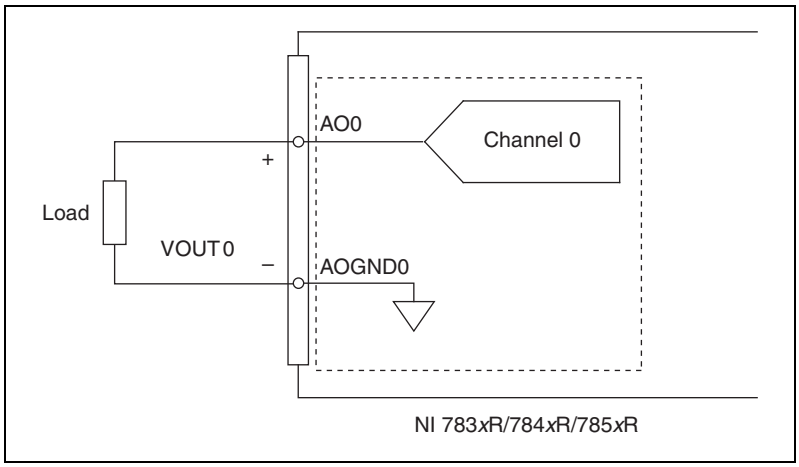


Figure 2-10. Analog Output Connections

Digital I/O

You can configure the NI 78*xx*R DIO lines individually for either input or output. When the system powers on, the DIO lines are at high impedance. To set another power-on state, you can configure the NI 78*xx*R to load a VI when the system powers on. The VI can then set the DIO lines to any power-on state.

Connecting Digital I/O Signals

The DIO signals on the NI 78*xx*R RDIO connectors are DGND and DIO<0..39>. The DIO signals on the NI 783*x*R/784*x*R/785*x*R RMIO connector are DGND and DIO<0..15>. The DIO<0..*n*> signals make up the DIO port and DGND is the ground reference signal for the DIO port. The NI 781*x*R has four RDIO connectors for a total of 160 DIO lines. The

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NI 7830R has one RMIO and one RDIO connector for a total of 56 DIO lines. The NI 7831R/7833R/784*x*R/785*x*R has one RMIO and two RDIO connectors for a total of 96 DIO lines.

Refer to Figure A-1, *NI 781xR Connector Pin Assignments and Locations*, for the connector locations and the I/O connector pin assignments on the NI 781*x*R. Refer to Figure A-2, *NI 783xR/784xR/785xR Connector Pin Assignments and Locations*, for the connector locations and the I/O connector pin assignments on the NI 783*x*R/784*x*R/785*x*R.

The DIO lines on the NI 78*xx*R are TTL-compatible. When configured as inputs, they can receive signals from 5 V TTL, 3.3 V LVTTL, 5 V CMOS, and 3.3 V LVCMOS devices. When configured as outputs, they can send signals to 5 V TTL, 3.3 V LVTTL, and 3.3 V LVCMOS devices. Because the digital outputs provide a nominal output swing of 0 to 3.3 V (3.3 V TTL), the DIO lines cannot drive 5 V CMOS logic levels. To interface to 5 V CMOS devices, you must provide an external pull-up resistor to 5 V. This resistor pulls up the 3.3 V digital output from the NI 78*xx*R to 5 V CMOS logic levels. Refer to the *NI R Series Multifunction RIO Specifications*, available at `ni.com/manuals`, for detailed DIO specifications.

Caution Exceeding the maximum input voltage ratings, listed in Table A-2, *NI 78xxR I/O Signal Summary*, can damage the NI 78*xx*R and the computer. NI is *not* liable for any damage resulting from such signal connections.

Caution Do *not* short the DIO lines of the NI 78*xx*R directly to power or to ground. Doing so can damage the NI 78*xx*R by causing excessive current to flow through the DIO lines.

You can connect multiple NI 78*xx*R digital output lines in parallel to provide higher current sourcing or sinking capability. If you connect multiple digital output lines in parallel, your application must drive all of these lines simultaneously to the same value. If you connect digital lines together and drive them to different values, excessive current can flow through the DIO lines and damage the NI 78*xx*R. Refer to the *NI R Series Multifunction RIO Specifications*, available at `ni.com/manuals`, for more information about DIO specifications. Figure 2-11 shows signal connections for three typical DIO applications.

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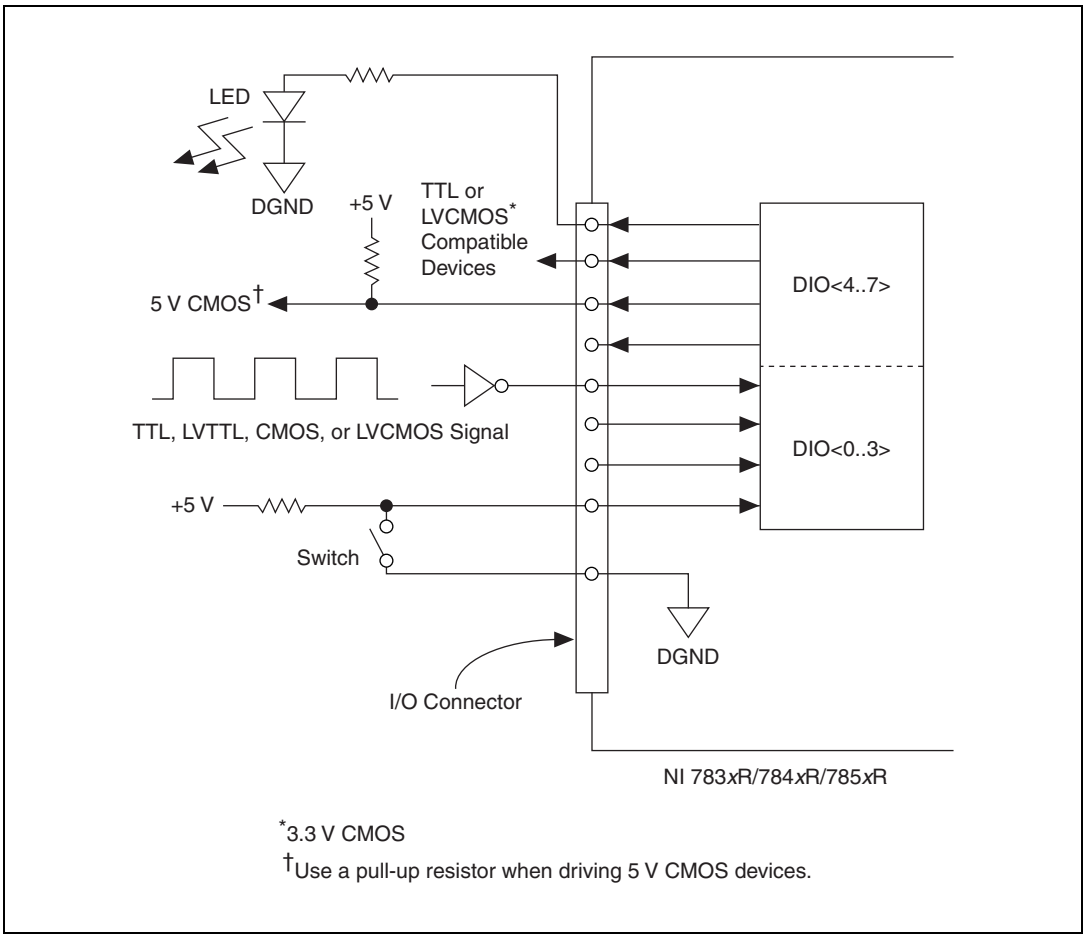


Figure 2-11. Example Digital I/O Connections

Figure 2-11 shows DIO<0..3> configured for digital input and DIO<4..7> configured for digital output. Digital input applications include receiving TTL, LVTTL, CMOS, or LVCMOS signals and sensing external device states, such as the state of the switch shown in Figure 2-11. Digital output applications include sending TTL or LVCMOS signals and driving external devices, such as the LED shown in Figure 2-11.

The NI 78*xx*R SHC68-68-RDIO cable contains individually shielded bundles that route each digital signal on an individually shielded pair of wires, and each signal is twisted with its own wire to digital ground.

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The SHC68-68-RDIO was designed specifically for R Series devices and is the NI-recommended cable for digital applications. If you are using the SH68-C68-S cable, however, please note the following considerations.

The SH68-C68-S shielded cable contains 34 twisted pairs of conductors. To maximize the digital I/O available on the NI 78*xx*R, some of the DIO lines are twisted with power or ground and some DIO lines are twisted with other DIO lines. To obtain maximum signal integrity, place edge-sensitive or high-frequency digital signals on the DIO lines that are paired with power or ground. Because the DIO lines that are twisted with other DIO lines can couple noise onto each other, use these lines for static signals or non-edge-sensitive, low-frequency digital signals. Examples of high-frequency or edge-sensitive signals include clock, trigger, pulse-width modulation (PWM), encoder, and counter signals. Examples of static signals or non-edge-sensitive, low-frequency signals include LEDs, switches, and relays. Table 2-4 summarizes these guidelines.

Table 2-4. DIO Signal Guidelines for the NI 78*xx*R

Device	Digital Lines	SH68-C68-S Shielded Cable Signal Pairing	Recommended Types of Digital Signals
NI 781*x*R	DIO<0..27>	DIO line paired with power or ground	All types—high-frequency or low-frequency signals, edge-sensitive or non-edge-sensitive signals
	DIO<28..39>	DIO line paired with another DIO line	Static signals or non-edge-sensitive, low-frequency signals
NI 783*x*R, NI 784*x*R, NI 785*x*R	Connector 0, DIO<0..7>; Connector 1, DIO<0..27>; Connector 2, DIO<0..27>	DIO line paired with power or ground	All types—high-frequency or low-frequency signals, edge-sensitive or non-edge-sensitive signals
	Connector 0, DIO<8..15>; Connector 1, DIO<28..39>; Connector 2, DIO<28..39>	DIO line paired with another DIO line	Static signals or non-edge-sensitive, low-frequency signals

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RTSI Trigger Bus

The NI 78*xx*R can send and receive triggers through the RTSI trigger bus. The RTSI bus provides eight shared trigger lines that connect to all the devices on the bus. In PXI, the trigger lines are shared between all the PXI slots in a bus segment. In PCI, the RTSI bus is implemented through a ribbon cable connected to the RTSI connector on each device that needs to access the RTSI bus.

You can use the RTSI trigger lines to synchronize the NI 78*xx*R to any other device that supports RTSI triggers. On the NI PCI-781*x*R/783*x*R and NI PCIe-784*x*R/785*x*R, the RTSI trigger lines are labeled RTSI/RTSI<0..6> and RTSI/RTSI7. On the NI PXI-78*xx*R, the RTSI trigger lines are labeled PXI/PXI_Trig<0..7>. In addition, the NI PXI-78*xx*R can use the PXI star trigger line to send or receive triggers from a device plugged into Slot 2 of the PXI chassis. The PXI star trigger line on the NI PXI-78*xx*R is PXI/PXI_Star.

The NI 78*xx*R can configure each RTSI trigger line either as an input or an output signal. Because each trigger line on the RTSI bus is connected in parallel to all the other RTSI devices on the bus, only one device should drive a particular RTSI trigger line at a time. For example, if one NI PXI-78*xx*R is configured to send out a trigger pulse on PXI/PXI_Trig0, the remaining devices on that PXI bus segment must have PXI/PXI_Trig0 configured as an input.

Caution Do *not* drive the same RTSI trigger bus line with the NI 78*xx*R and another device simultaneously. Such signal driving can damage both devices. NI is *not* liable for any damage resulting from such signal driving.

For more information on using and configuring triggers, select **Help» Search the LabVIEW Help** in LabVIEW to view the *LabVIEW Help*. Refer to the *PXI Hardware Specification Revision 2.1* and *PXI Software Specification Revision 2.1* at `www.pxisa.org` for more information about PXI triggers.

PXI Local Bus (NI PXI-781*x*R/783*x*R Only)

The NI PXI-781*x*R/783*x*R can communicate with other PXI devices using the PXI local bus. The PXI local bus is a daisy-chained bus that connects each PXI peripheral slot with its adjacent peripheral slot on either side. For example, the right local bus lines from a PXI peripheral slot connect to the left local bus lines of the adjacent slot on the right. Each local bus is 13 lines

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wide. All of these lines connect to the FPGA on the NI PXI-781*x*R/783*x*R. The PXI local bus right lines on the NI PXI-781*x*R/783*x*R are PXI/PXI_Lbr<0..12>. The PXI local bus left lines on the NI PXI-781*x*R/783*x*R are PXI/PXI_Lbl<0..12>.

The NI PXI-781*x*R/783*x*R can configure each PXI local bus line either as an input or an output signal. Only one device can drive the same physical local bus line at a time. For example, if the NI PXI-781*x*R/783*x*R is configured to drive a signal on PXI/PXI_Lbr 0, the device in the slot immediately to the right must have its PXI/PXI_Lbl 0 line configured as an input.

Caution Do *not* drive the same PXI local bus line with the NI PXI-781*x*R/783*x*R and another device simultaneously. Such signal driving can damage both devices. NI is *not* liable for any damage resulting from such signal driving.

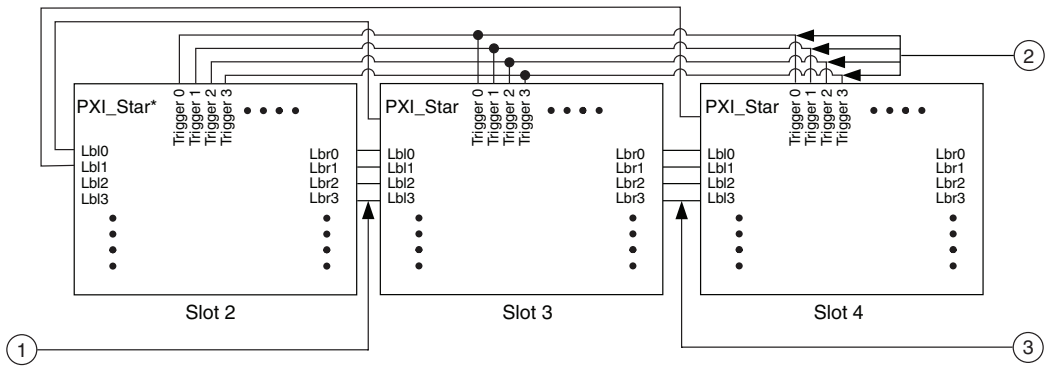
The NI PXI-781*x*R/783*x*R local bus lines are only compatible with 3.3 V signaling LVTTL and LVCMOS levels.

Caution Do *not* enable the local bus lines on an adjacent device if the device drives anything other than 0–3.3V LVTTL signal levels on the NI PXI-781*x*R/783*x*R. Enabling the lines in this way can damage the NI PXI-781*x*R/783*x*R. NI is *not* liable for any damage resulting from enabling such lines.

The left local bus lines from the left peripheral slot of a PXI backplane (Slot 2) are routed to the star trigger lines of up to 13 other peripheral slots in a two-segment PXI system. This configuration provides a dedicated, delay-matched trigger signal between the first peripheral slot and the other peripheral slots for precise trigger timing signals. For example—as shown in Figure 2-12—an NI PXI-781*x*R/783*x*R in Slot 2 can send an independent trigger signal to each device plugged into Slots <3..15> using the PXI/PXI_Lbl<0..12>. Each device receives its trigger signal on its own dedicated star trigger line.

Caution Do *not* configure the NI 781*x*R/783*x*R and another device to drive the same physical star trigger line simultaneously. Such signal driving can damage the NI 781*x*R/783*x*R and the other device. NI is *not* liable for any damage resulting from such signal driving.

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1 Shared Local Bus Lines between Slot 2 and Slot 3
2 Shared Trigger Lines between Slot 2, Slot 3, and Slot 4
3 Shared Local Bus Lines between Slot 3 and Slot 4

Figure 2-12. PXI Star Trigger Connections in a PXI Chassis

Refer to the *PXI Hardware Specification Revision 2.1* and *PXI Software Specification Revision 2.1* at `www.pxisa.org` for more information about PXI triggers.

Switch Settings (NI 781*x*R/783*x*R Only)

Refer to Figure 2-13 for the location of switches on the NI PCI-781*x*R and Figure 2-14 for the location of switches on the NI PXI-781*x*R. Refer to Figure 2-15 for the location of switches on the NI PCI-783*x*R and Figure 2-16 for the location of switches on the NI PXI-783*x*R. For normal operation, SW1 is in the OFF position. To prevent a VI stored in Flash memory from loading to the FPGA at power up, move SW1 to the ON position, as shown in Figure 2-17.

Note SW2 and SW3 are not connected.

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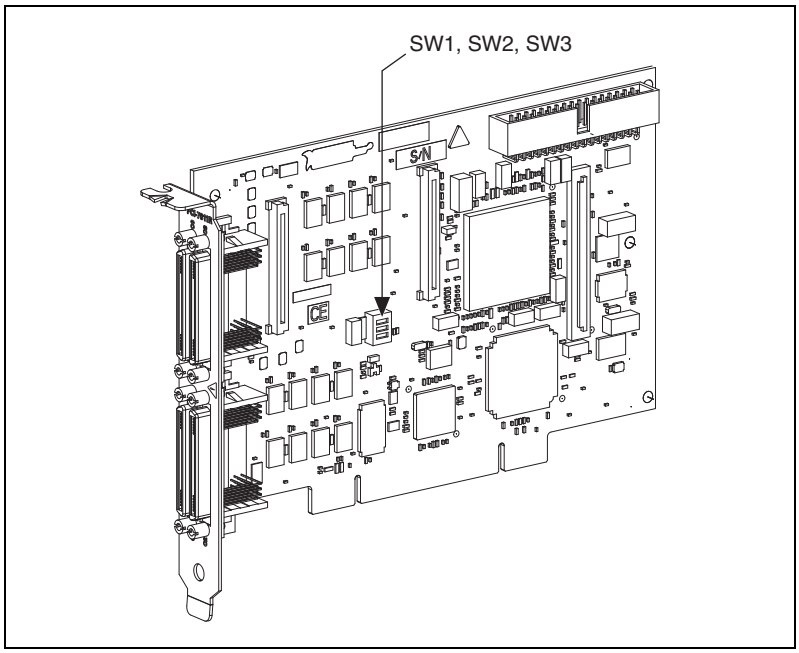


Figure 2-13. Switch Location on the NI PCI-781*x*R

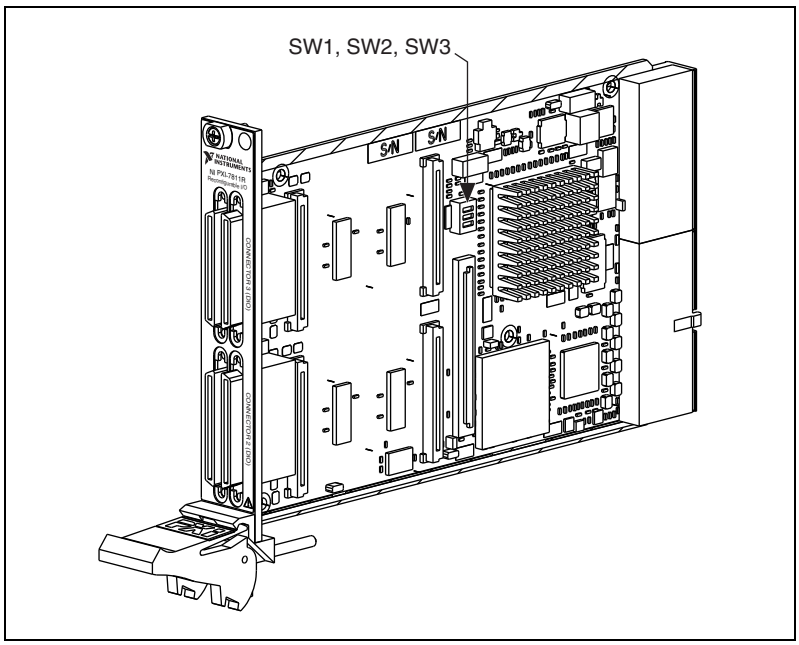


Figure 2-14. Switch Location on the NI PXI-781*x*R

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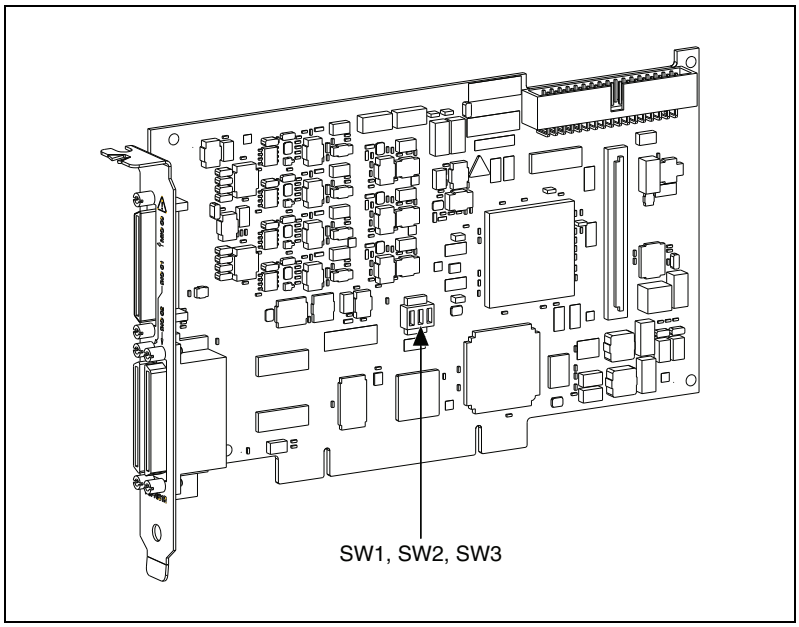


Figure 2-15. Switch Location on the NI PCI-783*x*R

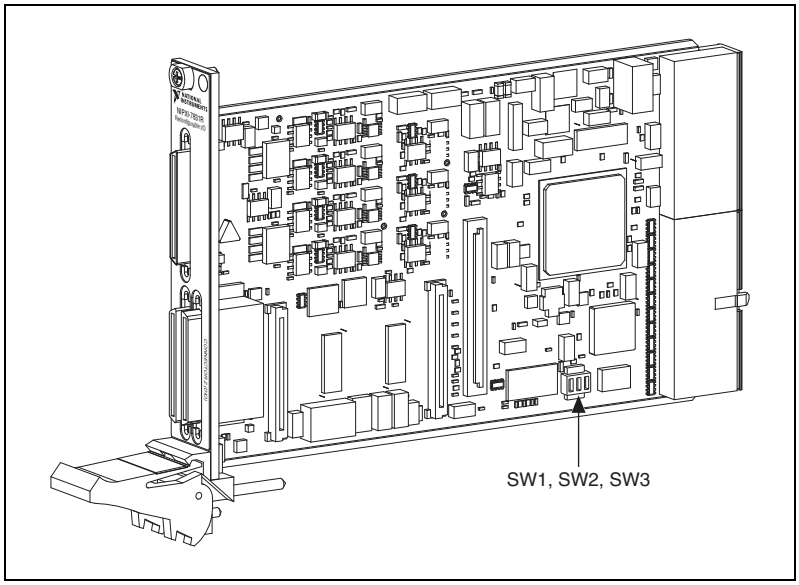


Figure 2-16. Switch Location on the NI PXI-783*x*R

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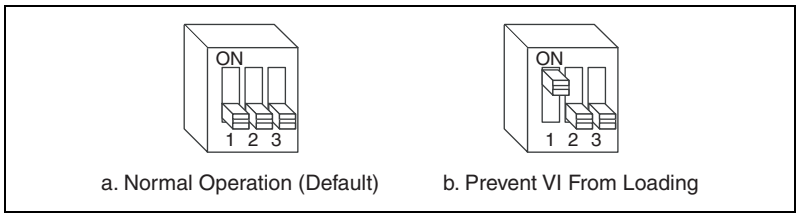


Figure 2-17. Switch Settings

Complete the following steps to prevent a VI stored in Flash memory from loading to the FPGA:

1. Power off and unplug the PXI/CompactPCI chassis or PCI computer.
2. Remove the NI 781*x*R/783*x*R from the PXI/CompactPCI chassis or PCI computer.
3. Move SW1 to the ON position, as shown in Figure 2-17b.
4. Reinsert the NI 781*x*R/783*x*R into the PXI/CompactPCI chassis or PCI computer. Refer to the *Installing the Hardware* section of the *Getting Started with R Series Multifunction RIO* document for installation instructions.
5. Plug in and power on the PXI/CompactPCI chassis or PCI computer.

After completing this procedure, a VI stored in Flash memory does not load to the FPGA at power-on. You can use software to configure the NI 78*xx*R, if necessary. To return to the defaults of loading from Flash memory, repeat the previous procedure but return SW1 to the OFF position in step 3. You can use this switch to enable/disable the ability to load from Flash memory. In addition to this switch, you must configure the NI 78*xx*R with the software to autoload an FPGA VI.

Note When the NI 781*x*R/783*x*R is powered on with SW1 in the ON position, the analog circuitry does not return properly calibrated data. Move the switch to the ON position only while you are using software to reconfigure the NI 781*x*R/783*x*R for the desired power-up behavior. Afterward, return SW1 to the OFF position.

+5 V Power Source

The +5 V terminals on the I/O connector supply +5 V referenced to DGND. Use these terminals to power external circuitry.

Newer revision NI 781*x*R/783*x*R devices have a traditional fuse to protect the supply from overcurrent conditions. This fuse is not customer-replaceable; if the fuse permanently opens, return the device to NI for repair.

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Older revision NI 781*x*R/783*x*R devices have a self-resetting fuse to protect the supply from overcurrent conditions. This fuse resets automatically within a few seconds after the overcurrent condition is removed. For more information about the self-resetting fuse and precautions to take to avoid improper connection of +5 V and ground terminals, refer to the KnowledgeBase document, *Self-Resetting Fuse Additional Information*, by going to `ni.com/info` and entering the info code `pptc`.

(NI 784*x*R/785*x*R Devices) All NI 784*x*R/785*x*R devices have a user-replaceable socketed fuse to protect the supply from overcurrent conditions. When an overcurrent condition occurs, check your cabling to the +5 V terminals and replace the fuse as described in the *Device Fuse Replacement (NI 784xR/785xR Only)* section.

Caution *Never* connect the +5 V power terminals to analog or digital ground or to any other voltage source on the NI 78*xx*R device or any other device. Doing so can damage the device and the computer. NI is *not* liable for damage resulting from such a connection.

The power rating on most devices is +4.75 to +5.25 VDC at 1 A.

Refer to the *NI R Series Multifunction RIO Specifications* document, available at `ni.com/manuals`, to obtain the power rating for your device.

Device Fuse Replacement (NI 784*x*R/785*x*R Only)

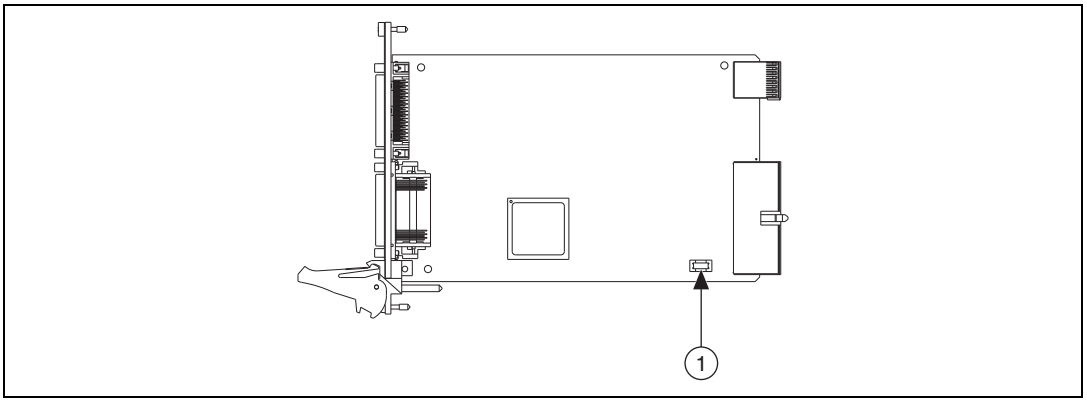
NI 784*x*R/785*x*R devices have a replaceable fuse, Littelfuse part number 0453004, that protects the device from overcurrent through the power connector.

To replace a blown fuse in the NI 784*x*R/785*x*R, complete the following steps:

1. Power down and unplug the computer or PXI chassis.
2. Remove the PCI/PCI Express device from the expansion slot on the computer, or the PXI device from the PXI slot in the PXI chassis.

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3. Replace the blown fuse while referring to Figure 2-18 for the fuse locations.



1 NI PCIe-784*x*R/785*x*R Fuse Location 2 NI PXI-784*x*R/785*x*R Fuse Location

Figure 2-18. NI 784*x*R/785*x*R Replacement Fuse Location (Littelfuse Part Number 0453004)

4. Reinstall the PCI, PCI Express, or PXI device into the computer or PXI chassis.

PCI Express Device Disk Drive Power Connector

(NI PCIe-784xR/785xR Devices) The disk drive power connector is a four-pin hard drive connector on PCI Express devices that, when connected, increases the current the device can supply on the +5 V terminal.

When to Use the Disk Drive Power Connector

PCI Express R Series devices without the disk drive power connector installed perform identically to other R Series devices for most applications and with most accessories. For most applications, it is not necessary to install the disk drive power connector.

However, you should install the disk drive power connector in either of the following situations:

- You need more power than listed in the device specifications
- You are using an R Series accessory with no external power supply, such as the cRIO-9151

Refer to the specifications document for your device for more information about PCI Express power requirements and power limits.

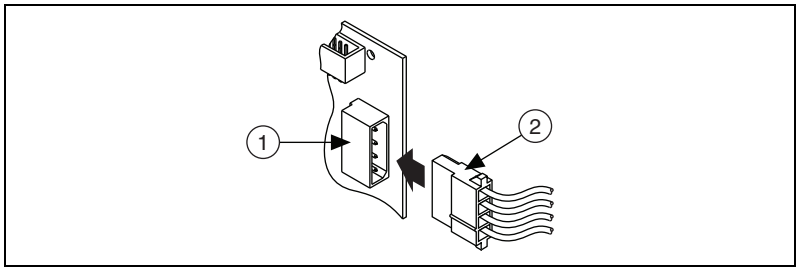
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Disk Drive Power Connector Installation

Before installing the disk drive power connector, you must install and set up the R Series PCI Express device as described in the *Getting Started with R Series Multifunction RIO* document. Complete the following steps to install the disk drive power connector.

1. Power off and unplug the computer.
2. Remove the computer cover.
3. Attach the PC disk drive power connector to the disk drive power connector on the device, as shown in Figure 2-19.

Note The power available on the disk drive power connectors in a computer can vary. For example, consider using a disk drive power connector that is not in the same power chain as the hard drive.



1 Device Disk Drive Power Connector 2 PC Disk Drive Power Connector

Figure 2-19. Connecting to the Disk Drive Power Connector

4. Replace the computer cover, and plug in and power on the computer.
5. Use the NI 78xxR Calibration Utility to run a self-calibration on the NI PCIe-784*x*R/785*x*R device. Refer to the *Self-Calibration* section of Chapter 3, *Calibration (NI 783xR/784xR/785xR Only)*, for more information.

Note Connecting or disconnecting the disk drive power connector can affect the analog performance of your device. To compensate for this, NI recommends that you self-calibrate after connecting or disconnecting the disk drive power connector.

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Field Wiring Considerations (NI 783*x*R/784*x*R/785*x*R Only)

Environmental noise can seriously affect the measurement accuracy of the device if you do not take proper care when running signal wires between signal sources and the device. The following recommendations mainly apply to AI signal routing to the device, as well as signal routing in general.

Take the following precautions to minimize noise pickup and maximize measurement accuracy:

- Use differential AI connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect AI signals to the device. With this type of wire, the signals attached to the positive and negative inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.
- Route signals to the device carefully. Keep cabling away from noise sources. The most common noise source in a PXI DAQ system is the video monitor. Keep the monitor and the analog signals as far apart as possible.

Use the following recommendations for all signal connections to the NI 783*x*R/784*x*R/785*x*R:

- Separate NI 783*x*R/784*x*R/785*x*R signal lines from high-current or high-voltage lines. These lines can induce currents in or voltages on the NI 783*x*R/784*x*R/785*x*R signal lines if they run in parallel paths at a close distance. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel or run the lines at right angles to each other.
- Do *not* run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

Refer to the NI Developer Zone tutorial, *Field Wiring and Noise Considerations for Analog Signals*, at `ni.com/zone` for more information.

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Calibration (NI 783*x*R/784*x*R/785*x*R Only)

Calibration is the process of determining and/or adjusting the accuracy of an instrument to minimize measurement and output voltage errors. On the NI 783*x*R/784*x*R/785*x*R, onboard calibration DACs (CalDACs) correct these errors. Because the analog circuitry handles calibration, the data read from the AI channels or written to the AO channels in the FPGA VI is already calibrated.

Three levels of calibration are available for the NI 783*x*R/784*x*R/785*x*R to ensure the accuracy of its analog circuitry. The first level, loading calibration constants, is the fastest, easiest, and least accurate. The intermediate level, internal self-calibration, is the preferred method of assuring accuracy in your application. The last level, external calibration, is the slowest, most difficult, and most accurate.

Loading Calibration Constants

The NI 783*x*R/784*x*R/785*x*R is factory calibrated before shipment at approximately 25 °C to the levels indicated in the device specifications. Refer to the *NI R Series Multifunction RIO Specifications*, available at `ni.com/manuals`, for more information calibration levels. The onboard nonvolatile Flash memory stores the calibration constants for the device. Calibration constants are the values that were written to the CalDACs to achieve calibration in the factory. The NI 783*x*R/784*x*R/785*x*R hardware reads these constants from the Flash memory and loads them into the CalDACs at power-on. This occurs before you load a VI into the FPGA.

Self-Calibration

With self-calibration, the NI 783*x*R/784*x*R/785*x*R can internally measure and correct almost all of its calibration-related errors without any external signal connections. NI provides software to perform an self-calibration. This internal self-calibration process, which generally takes less than two minutes, is the preferred method of assuring accuracy in your

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application. Self-calibration minimizes the effects of any offset and gain drifts, particularly those due to changes in temperature. During the self-calibration process, the AI and AO channels are compared to the NI 783*x*R/784*x*R/785*x*R onboard voltage reference. The offset and gain errors in the analog circuitry are calibrated out by adjusting the CalDACs to minimize these errors.

Note The NI 78xxR Calibration Utility does not support NI 781*x*R devices.

If you have NI-RIO installed, you can find the self-calibration utility at **Start»All Programs»National Instruments»NI-RIO»Calibrate 78xxR Device**. *Device* is the NI PXI-783*x*R/784*x*R/785*x*R or NI PCI-783*x*R device.

Immediately after self-calibration, the only significant residual calibration error is gain error due to time and temperature drift of the onboard voltage reference. You can minimize gain errors by performing an external calibration. If you are primarily taking relative measurements, then you can ignore a small amount of gain error and self-calibration is sufficient.

The Flash memory on the NI 783*x*R/784*x*R/785*x*R stores the results of a self-calibration so the CalDACs automatically load with the newly calculated calibration constants the next time the NI 783*x*R/784*x*R/785*x*R is powered on.

External Calibration

An external calibration refers to calibrating your device with a known external reference rather than relying on the onboard reference. The NI 783*x*R/784*x*R/785*x*R has an onboard calibration reference to ensure the accuracy of self-calibration. The reference voltage is measured at the factory and stored in the Flash memory for subsequent self-calibrations. Externally calibrate the device annually or more often if you use it at extreme temperatures.

During the external calibration process, the onboard reference value is re-calculated. This compensates for any time or temperature drift-related errors in the onboard reference that might have occurred since the last calibration. You can save the results of the external calibration process to Flash memory so that the NI 783*x*R/784*x*R/785*x*R loads the new calibration constants the next time it is powered on. The device uses the newly measured onboard reference level for subsequent self-calibrations.

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To externally calibrate your device, use an external reference several times more accurate than the device itself. For more information on externally calibrating your NI 783*x*R/784*x*R/785*x*R device, refer to the *NI 783xR/784xR/785xR Calibration Procedure for NI-RIO*, found on `ni.com/manuals`.

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A

Connecting I/O Signals

This appendix describes how to make input and output signal connections to the NI 78*xx*R I/O connectors.

Figure A-1 shows the I/O connector pin assignments and locations for NI PCI-7811R/7813R and NI PXI-7811R/7813R.

Figure A-2 shows the I/O connector pin assignments and locations for NI PCI-7830R/7831R/7833R, NI PCIe-7841R/7842R/7851R/7852R, and the NI PXI-7830R/7831R/7833R/7841R/7842R/7851R/7852R/7853R/7854R.

Note The NI PXI-7830R and NI PCI-7830R do not have Connector 2 (RDIO).

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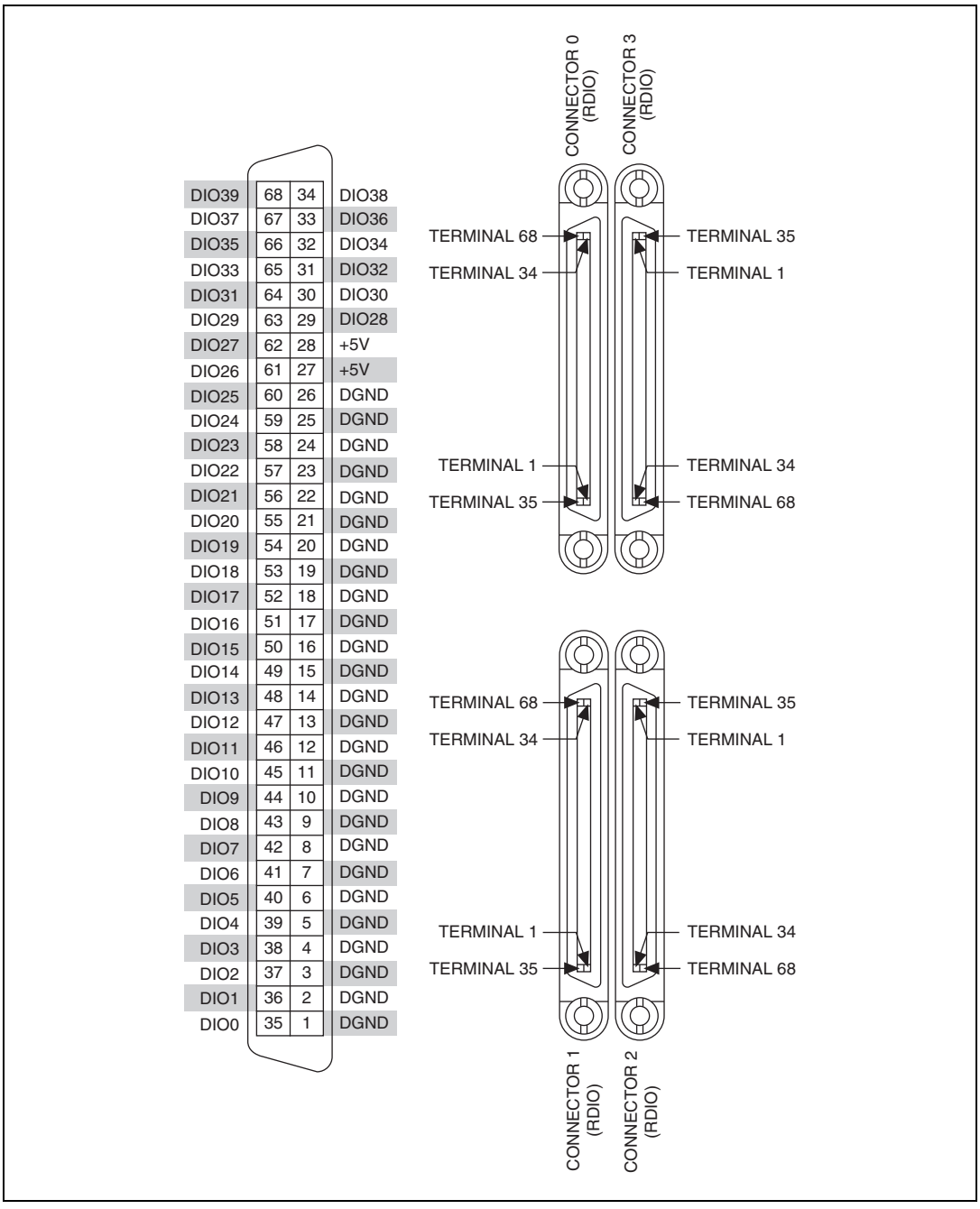


Figure A-1. NI 781*x*R Connector Pin Assignments and Locations

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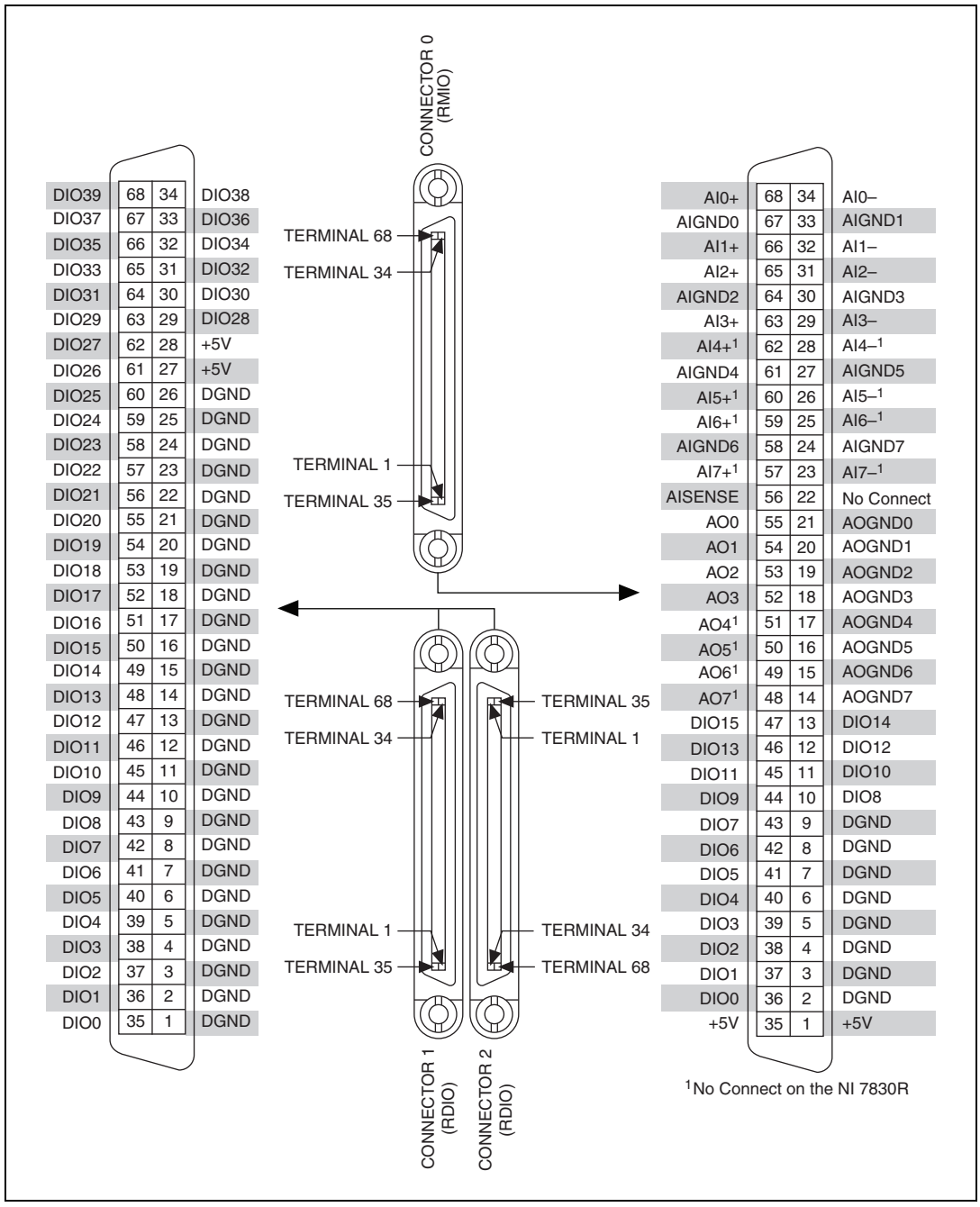


Figure A-2. NI 783*x*R/784*x*R/785*x*R Connector Pin Assignments and Locations

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To access the signals on the I/O connectors, you must connect a cable from the I/O connector to a signal accessory. Plug the small VHDCI connector end of the cable into the appropriate I/O connector and connect the other end of the cable to the appropriate signal accessory.

Table A-1. I/O Connector Signal Descriptions

Signal Name	Reference	Direction	Description
+5V	DGND	Output	+5 VDC Source—These pins supply 5 V from the computer power supply. For more information on the +5V terminals, refer to the *+5 V Power Source* section in Chapter 2, *Hardware Overview of the NI 78xxR*.
Analog Signals (NI 783*x*R/784*x*R/785*x*R Only)			
AI<0..7>+	AIGND	Input	Positive input for Analog Input channels 0 through 7.
AI<0..7>–	AIGND	Input	Negative input for Analog Input channels 0 through 7.
AIGND	—	—	Analog Input Ground—These pins are the reference point for single-ended measurements in RSE configuration and the bias current return point for differential measurements. All three ground references—AIGND, AOGND, and DGND—are connected to each other on the NI 783*x*R/784*x*R/785*x*R.
AISENSE	AIGND	Input	Analog Input Sense—This pin serves as the reference node for AI <0..7> when the device is configured for NRSE mode.
AO<0..7>	AOGND	Output	Analog Output channels 0 through 7. Each channel can source or sink up to 2.5 mA.
AOGND	—	—	Analog Output Ground—The analog output voltages are referenced to this node. All three ground references—AIGND, AOGND, and DGND—are connected to each other on the NI 783*x*R/784*x*R/785*x*R.
Digital Signals (All NI 78*xx*R Devices)			
DGND	—	—	Digital Ground—These pins supply the reference for the digital signals at the I/O connector and the 5 V supply. All three ground references—AIGND, AOGND, and DGND—are connected to each other on the NI 783*x*R/784*x*R/785*x*R.
DIO<0..39> Connector <0..3> (NI 781*x*R) DIO<0..15> Connector 0 (NI 783*x*R/784*x*R/785*x*R) DIO<0..39> Connector <1..2> (NI 783*x*R/784*x*R/785*x*R)	DGND	Input or Output	Digital I/O signals.

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Caution Connections that exceed any of the maximum ratings of input or output signals on the NI 78*xx*R can damage the NI 78*xx*R and the computer. Maximum input ratings for each signal are in the *Protection* column of Table A-2. NI is *not* liable for any damage resulting from such signal connections

Table A-2. NI 78*xx*R I/O Signal Summary

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time	Bias
+5V	DO	—	—	—	—	—	—
Analog Signals (NI 783*x*R/784*x*R/785*x*R Only)							
AI<0..7>+	AI	10 GΩ in parallel with 100 pF	42/35	—	—	—	±2 nA
AI<0..7>–	AI	10 GΩ in parallel with 100 pF	42/35	—	—	—	±2 nA
AIGND	AO	—	—	—	—	—	—
AISENSE	AI	10 GΩ in parallel with 100 pF	42/35	—	—	—	±2 nA
AO<0..7>	AO	1.25 Ω	Short circuit to ground	2.5 at 10	2.5 at –10	10 V/µs	—
AOGND	AO	—	—	—	—	—	—
Digital Signals (All NI 78*xx*R Devices)				—	—	—	—
DIO<0..39> Connector <0..3> (NI 781*x*R) DIO<0..15> Connector 0 (NI 783*x*R, NI 784*x*R, and NI 785*x*R) DIO<0..39> Connector <1..2> (NI 783*x*R, NI 784*x*R, and NI 785*x*R)	DIO	—	–0.5 to +7.0 (NI 783*x*R) –20 to 20 (NI 784*x*R/ NI 785*x*R)	4.0 at 2.4	4.0 at 0.4	—	—
AI = Analog Input AO = Analog Output DIO = Digital Input/Output DO = Digital Output							

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Connecting to 5B and SSR Analog Signal Conditioning (NI 783*x*R/784*x*R/785*x*R Only)

NI provides cables that allow you to connect signals from the NI 783*x*R/784*x*R/785*x*R directly to 5B backplanes for analog signal conditioning and SSR backplanes for digital signal conditioning.

The NSC68-262650 cable connects the signals on the NI 783*x*R/784*x*R/785*x*R RMIO connector directly to 5B and SSR backplanes. This cable has a 68-pin male VHDCI connector on one end that plugs into the NI 783*x*R/784*x*R/785*x*R RMIO connector. The other end of this cable provides two 26-pin female headers plus one 50-pin female header.

One of the 26-pin headers contains all the NI 783*x*R/784*x*R/785*x*R analog input signals. You can plug this connector directly into a 5B backplane for analog input signal conditioning. The NI 783*x*R/784*x*R/785*x*R AI<0..*n*> correspond to the 5B backplane channels <0..*n*> in sequential order. Configure the AI channels to use the NRSE input mode when using 5B signal conditioning.

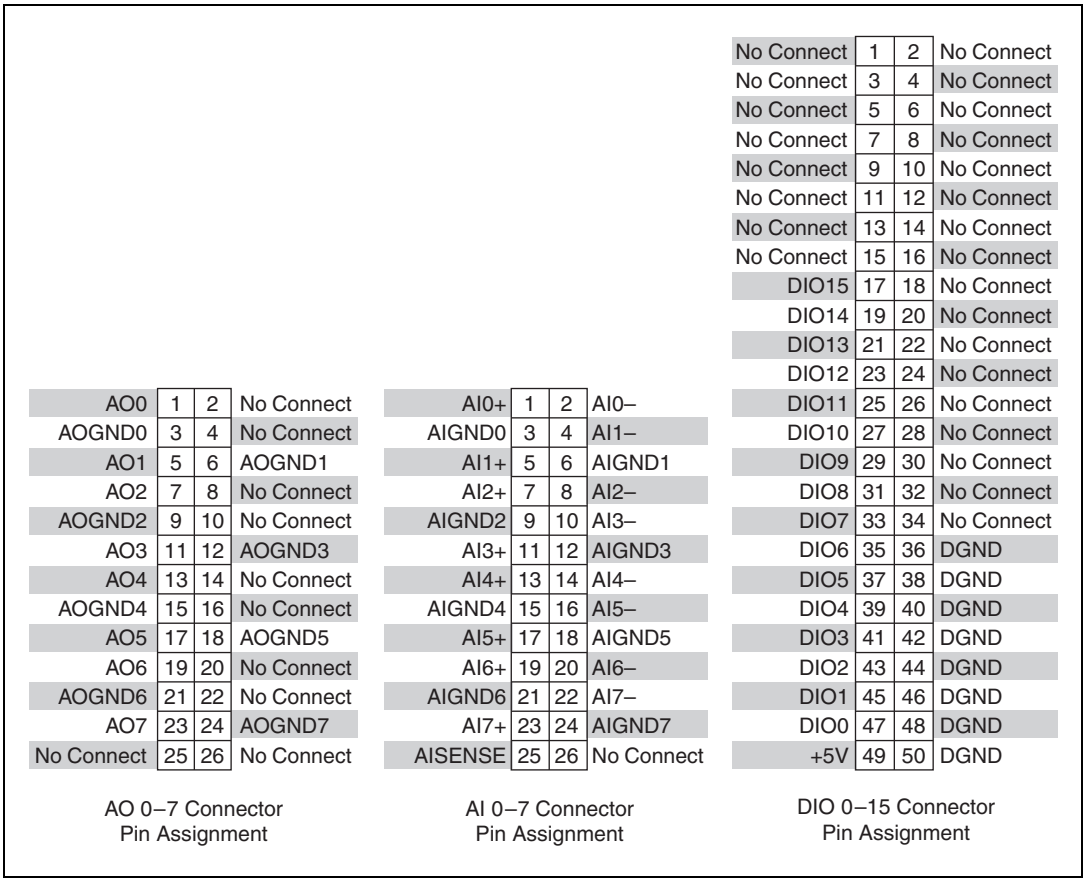
The other 26-pin header contains all the NI 783*x*R/784*x*R/785*x*R analog output signals. You can plug this connector directly into a 5B backplane for AO signal conditioning. The NI 783*x*R/784*x*R/785*x*R AO<0..*n*> correspond to the 5B backplane channels <0..*n*> in sequential order.

The 50-pin header contains the 16 DIO lines available on the NI 783*x*R/784*x*R/785*x*R RMIO connector. You can plug this header directly into an SSR backplane for digital signal conditioning. DIO lines <0..15> correspond to the 5B backplane Slots <0..15> in sequential order.

The 5B connector pinouts are compatible with 8-channel 5B08 backplanes and 16-channel 5B01 backplanes. The NI 7830R can accept analog input from the first four channels of a 16-channel backplane. The NI 7831R/7833R/784*x*R/785*x*R can accept analog input from the first eight channels of a 16-channel backplane. The SSR connector pinout is compatible with 8-, 16-, 24-, and 32-channel SSR backplanes. You can connect to an SSR backplane containing a number of channels unequal to the 16 DIO lines available on the 50-pin header. In this case, you have access to only the channels that exist on both the SSR backplane and the NSC68-262650 cable 50-pin header.

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Figure A-3 shows the connector pinouts when using the NSC68-262650 cable.



AO0	1	2	No Connect
AOGND0	3	4	No Connect
AO1	5	6	AOGND1
AO2	7	8	No Connect
AOGND2	9	10	No Connect
AO3	11	12	AOGND3
AO4	13	14	No Connect
AOGND4	15	16	No Connect
AO5	17	18	AOGND5
AO6	19	20	No Connect
AOGND6	21	22	No Connect
AO7	23	24	AOGND7
No Connect	25	26	No Connect

AO 0–7 Connector Pin Assignment

AI0+	1	2	AI0–
AIGND0	3	4	AI1–
AI1+	5	6	AIGND1
AI2+	7	8	AI2–
AIGND2	9	10	AI3–
AI3+	11	12	AIGND3
AI4+	13	14	AI4–
AIGND4	15	16	AI5–
AI5+	17	18	AIGND5
AI6+	19	20	AI6–
AIGND6	21	22	AI7–
AI7+	23	24	AIGND7
AISENSE	25	26	No Connect

AI 0–7 Connector Pin Assignment

No Connect	1	2	No Connect
No Connect	3	4	No Connect
No Connect	5	6	No Connect
No Connect	7	8	No Connect
No Connect	9	10	No Connect
No Connect	11	12	No Connect
No Connect	13	14	No Connect
No Connect	15	16	No Connect
DIO15	17	18	No Connect
DIO14	19	20	No Connect
DIO13	21	22	No Connect
DIO12	23	24	No Connect
DIO11	25	26	No Connect
DIO10	27	28	No Connect
DIO9	29	30	No Connect
DIO8	31	32	No Connect
DIO7	33	34	No Connect
DIO6	35	36	DGND
DIO5	37	38	DGND
DIO4	39	40	DGND
DIO3	41	42	DGND
DIO2	43	44	DGND
DIO1	45	46	DGND
DIO0	47	48	DGND
+5V	49	50	DGND

DIO 0–15 Connector Pin Assignment

Figure A-3. Connector Pinouts when Using NSC68-262650 Cable

Connecting to SSR Digital Signal Conditioning

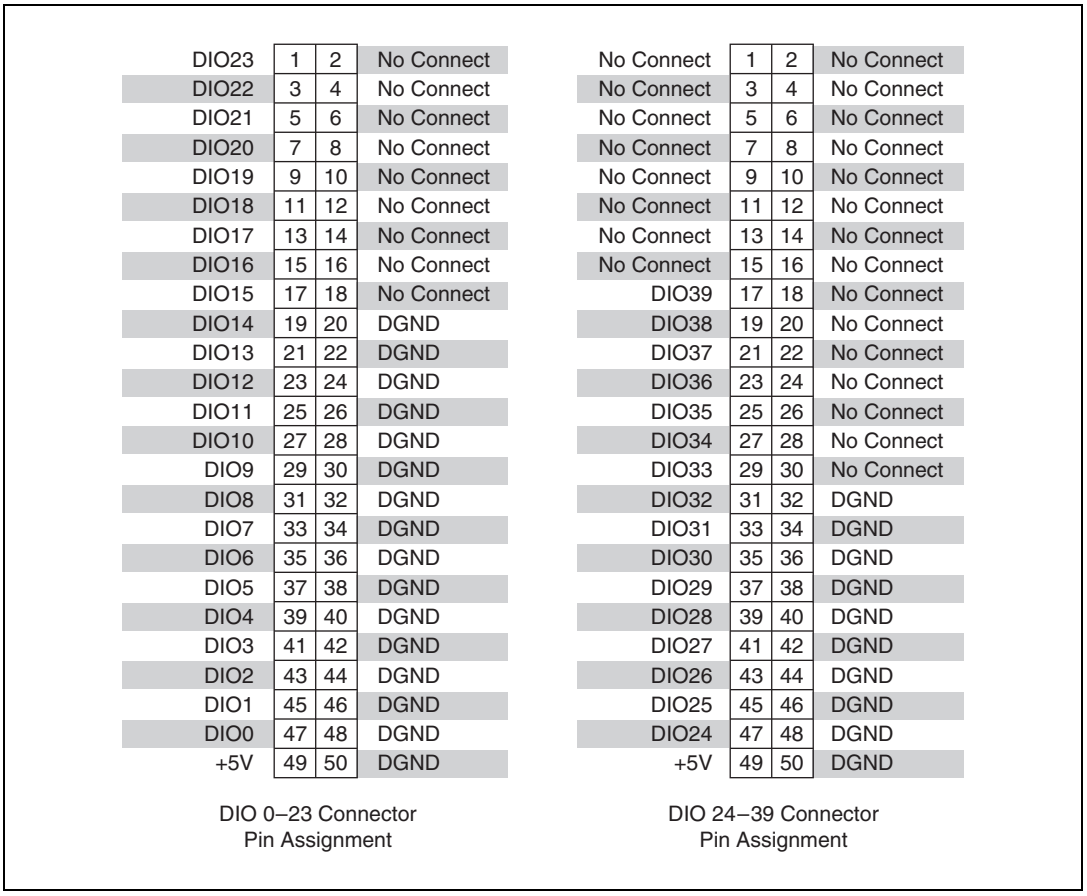
NI provides cables that allow you to connect signals from the NI 78*xx*R directly to SSR backplanes for digital signal conditioning.

The NSC68-5050 cable connects the signals on the NI 78*xx*R RDIO connectors directly to SSR backplanes for digital signal conditioning. This cable has a 68-pin male VHDCI connector on one end that plugs into the NI 78*xx*R RDIO connectors. The other end of this cable provides two 50-pin female headers.

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You can plug each of these 50-pin headers directly into an 8-, 16-, 24-, or 32-channel SSR backplane for digital signal conditioning. One of the 50-pin headers contains DIO<0..23> from the NI 78*xx*R RDIO connector. These lines correspond to Slots <0..23> on an SSR backplane in sequential order. The other 50-pin header contains DIO<24..39> from the NI 78*xx*R RDIO connector. These lines correspond to Slots <0..15> on an SSR backplane in sequential order. You can connect to an SSR backplane containing a number of channels unequal to the number of lines on the NSC68-5050 cable header. In this case, you have access only to the channels that exist on both the SSR backplane and the NSC68-5050 cable header you are using.

Figure A-4 shows the connector pinouts when using the NSC68-5050 cable.



DIO23	1	2	No Connect
DIO22	3	4	No Connect
DIO21	5	6	No Connect
DIO20	7	8	No Connect
DIO19	9	10	No Connect
DIO18	11	12	No Connect
DIO17	13	14	No Connect
DIO16	15	16	No Connect
DIO15	17	18	No Connect
DIO14	19	20	DGND
DIO13	21	22	DGND
DIO12	23	24	DGND
DIO11	25	26	DGND
DIO10	27	28	DGND
DIO9	29	30	DGND
DIO8	31	32	DGND
DIO7	33	34	DGND
DIO6	35	36	DGND
DIO5	37	38	DGND
DIO4	39	40	DGND
DIO3	41	42	DGND
DIO2	43	44	DGND
DIO1	45	46	DGND
DIO0	47	48	DGND
+5V	49	50	DGND

DIO 0–23 Connector Pin Assignment

No Connect	1	2	No Connect
No Connect	3	4	No Connect
No Connect	5	6	No Connect
No Connect	7	8	No Connect
No Connect	9	10	No Connect
No Connect	11	12	No Connect
No Connect	13	14	No Connect
No Connect	15	16	No Connect
DIO39	17	18	No Connect
DIO38	19	20	No Connect
DIO37	21	22	No Connect
DIO36	23	24	No Connect
DIO35	25	26	No Connect
DIO34	27	28	No Connect
DIO33	29	30	No Connect
DIO32	31	32	DGND
DIO31	33	34	DGND
DIO30	35	36	DGND
DIO29	37	38	DGND
DIO28	39	40	DGND
DIO27	41	42	DGND
DIO26	43	44	DGND
DIO25	45	46	DGND
DIO24	47	48	DGND
+5V	49	50	DGND

DIO 24–39 Connector Pin Assignment

Figure A-4. Connector Pinouts when Using the NSC68-5050 Cable

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B

Using the SCB-68 Shielded Connector Block

This appendix describes how to connect input and output signals to the NI 78*xx*R with the SCB-68 shielded connector block.

The SCB-68 has 68 screw terminals for I/O signal connections. To use the SCB-68 with the NI 78*xx*R, you must configure the SCB-68 as a general-purpose connector block. Refer to Figure B-1 for the general-purpose switch configuration.

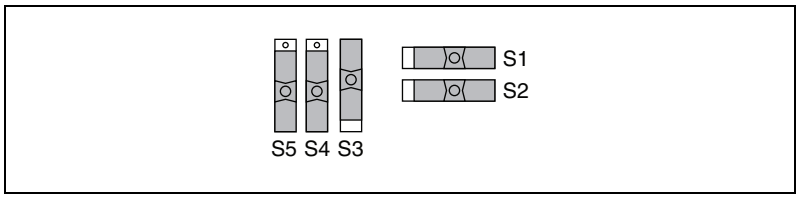


Figure B-1. General-Purpose Switch Configuration for the SCB-68 Terminal Block

After configuring the SCB-68 switches, you can connect the I/O signals to the SCB-68 screw terminals. Refer to Appendix A, *Connecting I/O Signals*, for the connector pin assignments for the NI 78*xx*R. After connecting I/O signals to the SCB-68 screw terminals, you can connect the SCB-68 to the with the SHC68-68-RMIO (for Connector 0 on the NI 783*x*R/784*x*R/785*x*R) or SHC68-68-RDIO (Connector <0..3> on the NI 781xR and Connector <1..2> on the NI 783*x*R/784*x*R/785*x*R) shielded cables.

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C

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Glossary

Symbol	Prefix	Value
p	pico	10^{-12}
n	nano	10^{-9}
µ	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^{3}
M	mega	10^{6}
G	giga	10^{9}

Numbers/Symbols

°	Degrees.
>	Greater than.
≥	Greater than or equal to.
<	Less than.
≤	Less than or equal to.
–	Negative of, or minus.
Ω	Ohms.
/	Per.
%	Percent.
±	Plus or minus.
+	Positive of, or plus.
$\sqrt{\ }$	Square root of.
+5V	+5 VDC source signal.

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A

A	Amperes.
A/D	Analog-to-digital.
AC	Alternating current.
ADC	Analog-to-digital converter—An electronic device, often an integrated circuit, that converts an analog voltage to a digital number.
AI	Analog input.
AI<*i*>	Analog input channel signal.
AIGND	Analog input ground signal.
AISENSE	Analog input sense signal.
AO	Analog output.
AO<*i*>	Analog output channel signal.
AOGND	Analog output ground signal.

B

bipolar	A signal range that includes both positive and negative values (for example, –5 to +5 V).

C

C	Celsius.
CalDAC	Calibration DAC.
CH	Channel—Pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels.
cm	Centimeter.

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CMOS	Complementary metal-oxide semiconductor.
CMRR	Common-mode rejection ratio—A measure of an instrument's ability to reject interference from a common-mode signal, usually expressed in decibels (dB).
common-mode voltage	Any voltage present at the instrumentation amplifier inputs with respect to amplifier ground.
CompactPCI	Refers to the core specification defined by the PCI Industrial Computer Manufacturer's Group (PICMG).

D

D/A	Digital-to-analog.
DAC	Digital-to-analog converter—An electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current.
DAQ	Data acquisition—A system that uses the computer to collect, receive, and generate electrical signals.
dB	Decibel—The unit for expressing a logarithmic measure of the ratio of two signal levels: dB = 20log10 V1/V2, for signals in volts.
DC	Direct current.
DGND	Digital ground signal.
DIFF	Differential mode.
DIO	Digital input/output.
DIO<*i*>	Digital input/output channel signal.
DMA	Direct memory access—A method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
DNL	Differential nonlinearity—A measure in LSB of the worst-case deviation of code widths from their ideal value of 1 LSB.
DO	Digital output.

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E

EEPROM	Electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed.

F

FPGA	Field-Programmable Gate Array.
FPGA VI	A configuration that is downloaded to the FPGA and that determines the functionality of the hardware.

G

glitch	An unwanted signal excursion of short duration that is usually unavoidable.

H

h	Hour.
HIL	Hardware-in-the-loop.
Hz	Hertz.

I

I/O	Input/output—The transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces.
INL	Relative accuracy.

L

LabVIEW	Laboratory Virtual Instrument Engineering Workbench. LabVIEW is a graphical programming language that uses icons instead of lines of text to create programs.
LSB	Least significant bit.

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M

m	Meter.
max	Maximum.
min	Minimum.
MIO	Multifunction I/O.
monotonicity	A characteristic of a DAC in which the analog output always increases as the values of the digital code input to it increase.
mux	Multiplexer—A switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel.

N

noise	An undesirable electrical signal—Noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.
NRSE	Nonreferenced single-ended mode—All measurements are made with respect to a common (NRSE) measurement system reference, but the voltage at this reference can vary with respect to the measurement system ground.

O

OUT	Output pin—A counter output pin where the counter can generate various TTL pulse waveforms.

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P

PCI	Peripheral Component Interconnect—A high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations. PCI offers a theoretical maximum transfer rate of 132 MB/s.
PCI Express	Peripheral Component Interconnect Express— A version of PCI that maintains the PCI software usage model and replaces the physical bus with a high-speed serial bus serving multiple lanes.
port	(1) A communications connection on a computer or a remote controller. (2) A digital port, consisting of four or eight lines of digital input and/or output.
pu	Pull-up.
PWM	Pulse-width modulation.
PXI	PCI eXtensions for Instrumentation—An open specification that builds off the CompactPCI specification by adding instrumentation-specific features.

R

RAM	Random-access memory—The generic term for the read/write memory that is used in computers. RAM allows bits and bytes to be written to it as well as read from. Various types of RAM are DRAM, EDO RAM, SRAM, and VRAM.
resolution	The smallest signal increment that can be detected by a measurement system. Resolution can be expressed in bits, in proportions, or in percent of full scale. For example, a system has 12-bit resolution, one part in 4,096 resolution, and 0.0244% of full scale.
RIO	Reconfigurable I/O.
rms	Root mean square.
RSE	Referenced single-ended mode—All measurements are made with respect to a common reference measurement system or a ground. Also called a grounded measurement system.
RTSI	Real-time system integration bus—The timing and triggering bus that connects multiple devices directly. This allows for hardware synchronization across devices.

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S

s	Seconds.
S	Samples.
S/s	Samples per second—Used to express the rate at which a DAQ board samples an analog signal.
signal conditioning	The manipulation of signals to prepare them for digitizing.
slew rate	The voltage rate of change as a function of time. The maximum slew rate of an amplifier is often a key specification to its performance. Slew rate limitations are first seen as distortion at higher signal frequencies.

T

THD	Total harmonic distortion—The ratio of the total rms signal due to harmonic distortion to the overall rms signal, in decibel or a percentage.
thermocouple	A temperature sensor created by joining two dissimilar metals. The junction produces a small voltage as a function of the temperature.
TTL	Transistor-transistor logic.
two's complement	Given a number x expressed in base 2 with n digits to the left of the radix point, the (base 2) number $2n - x$.

V

V	Volts.
VDC	Volts direct current.
VHDCI	Very high density cabled interconnect.
VI	Virtual instrument—Program in LabVIEW that models the appearance and function of a physical instrument.
V_{IH}	Volts, input high.
V_{IL}	Volts, input low.

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V_{OH}	Volts, output high.
V_{OL}	Volts, output low.
V_{rms}	Volts, root mean square.

W

waveform	Multiple voltage readings taken at a specific sampling rate.

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