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Find the *National Instruments PXIe-1086* at our website: ***Click HERE***

Installation

Ensure there is no visible damage to the new fan assembly before installing it. Verify that there is no foreign material inside the connector on the new fan assembly.

The fans for this chassis are redundant and hot swappable. You can install any fan with main AC power connected to the system.

Complete the following steps to install a fan assembly:

1. Open the fan door by sliding the door latches inward and rotating the door down.
2. Slide the fan module into an empty fan slot with the connector facing the chassis until it latches.
3. Verify that the fan is properly installed by pulling it forward with a light force without pressing the latch. If the fan does not slide out without pressing in the latch, it is installed correctly.
4. Close the fan door.

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A

Specifications

This appendix contains specifications for the PXIe-1086 chassis.

Caution Specifications are subject to change without notice.

Electrical

Input voltage range ..... 100 to 240 VAC
Operating voltage range[1] ..... 90 to 264 VAC
Input current rating ..... 12 to 6 A
Input frequency range ..... 50/60 Hz
Operating frequency range[1] ..... 47 to 63 Hz
Efficiency ..... 70% typical
Power disconnect ..... The AC power cables provide main power disconnect. Do not position the equipment so that it is difficult to disconnect the power cord. The front panel power switch causes the internal chassis power supply to provide DC power to the CompactPCI/PXI Express backplane. You also can use the front panel terminal block 4-pin connector and power mode switch to control the internal chassis power supply.

DC Output

DC current capacity (I_{MP})

Voltage	Maximum Current Single Power Supply	Maximum Current Dual Power Supplies
+3.3 V	50 A	60 A
+5 V	40 A	49 A
+12 V	50 A	62 A
-12 V	4 A	4 A
5 V_{AUX}	1.5 A	1.5 A

[1] This operating range is guaranteed by design.

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Note Maximum combined +12 V and -12 V power of a single power supply is 588 W.

Note Maximum total available power of a single power supply is 855 W.

Backplane slot current capacity

Slot	+5 V	V (I/O)	+3.3 V	+12 V	-12 V	5 V_{AUX}
System Controller Slot	15 A	—	15 A	30 A	—	1 A
System Timing Slot	—	—	6 A	4 A	—	1 A
Hybrid Peripheral Slot with PXI-1 Peripheral	6 A	5 A	6 A	1 A	1 A	—
Hybrid Peripheral Slot with PXI-5 Peripheral	—	—	6 A	4 A	—	1 A
PXI-1 Peripheral Slot	6 A	11 A	6 A	1 A	1 A	—

Note Total system slot current should not exceed 45 A.

Note PCI V(I/O) pins in PXI-1 peripheral slots and hybrid peripheral slots are connected to +5 V.

Note The maximum power dissipated in the system slot should not exceed 140 W.

Note The maximum power dissipated in a peripheral slot should not exceed 38.25 W.

Load regulation

Voltage	Load Regulation
+3.3 V	<5%
+12 V	<5%
+5 V	<5%
-12 V	<5%

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Maximum ripple and noise (20 MHz bandwidth)

Voltage	Maximum Ripple and Noise
+3.3 V	50 mV_{pp}
+12 V	120 mV_{pp}
+5 V	50 mV_{pp}
-12 V	120 mV_{pp}

Over-current protection ..... All outputs protected from short circuit and overload with automatic recovery

Over-voltage protection, 3.3 V and 5 V ..... Clamped at 25 to 40% above nominal output voltage

Power supply MTTR ..... Replacement in under 1 minute

Chassis Cooling

Module cooling system..... Forced air circulation (positive pressurization) through six 150 cfm fans (three sets of dual stacked fans) with High/Auto speed selector.

Slot airflow direction..... Bottom of module to top of module

Module cooling intake..... Bottom of chassis

Module cooling exhaust..... Along top of chassis

Power supply cooling system ..... Forced air circulation through integrated fan

Power supply cooling intake..... Rear of chassis

Power supply cooling exhaust ..... Top of chassis

Environmental

Maximum altitude..... 4600 m (570 mbar) (at 25 °C ambient)

Note Fan speed selector must be set to High to meet the maximum altitude specification.

Pollution Degree 2

For indoor use only.

Operating Environment

Ambient temperature range ..... 0 to 50 °C
(Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 temperature limits.)

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Relative humidity range.....5 to 95%, noncondensing
(Tested to temperature and humidity levels specified in MIL-PRF-28800F)

Storage Environment

Ambient temperature range .....-40 to 71 °C
(Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 temperature limits.)

Relative humidity range.....5 to 95%, noncondensing
(Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Operational shock .....30 g peak, half-sine, 11 ms pulse
(Tested in accordance with IEC 60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)

Random Vibration

Operating .....5 to 500 Hz, 0.3 g_{rms}

Caution When using a single power supply unit, you must use a power supply filler panel (NI P/N 784057-01) in the empty slot to meet operational shock and vibration specifications.

Acoustic Emissions

Sound Pressure Level (at Operator Position)

(Tested in accordance with ISO 7779. Meets MIL-PRF-28800F requirements.)

Auto fan (up to ~30 °C ambient) .....57.0 dBA

High fan .....69.0 dBA

Sound Power

Auto fan (up to ~30 °C ambient) .....63.3 dBA

High fan .....79.3 dBA

Caution The protection provided by the PXIe-1086 can be impaired if it is used in a manner not described in this document.

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Safety

This product is designed to meet the requirements of the following standards of safety for information technology equipment:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light industrial, and heavy industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations and certifications and additional information, refer to the *Online Product Certification* section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2014/35/EC; Low-Voltage Directive (safety)
- 2014/13/EC; Electromagnetic Compatibility Directive (EMC)

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Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)



EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit `ni.com/environment/weee`.

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中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。 (For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

Backplane

Size	3U-sized; one system slot (with three system expansion slots) and 17 peripheral slots. Compliant with IEEE 1101.10 mechanical packaging. PXI Express Specification compliant. Accepts both PXI Express and CompactPCI (PICMG 2.0 R 3.0) 3U modules.
Backplane bare-board material	UL 94 V-0 Recognized
Backplane connectors	Conforms to IEC 917 and IEC 1076-4-101, and are UL 94 V-0 rated

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System Synchronization Clocks (PXI_CLK10, PXIe_CLK100, PXIe_SYNC100)

10 MHz System Reference Clock: PXI_CLK10

Maximum slot-to-slot skew ..... 1 ns

Accuracy ..... ±25 ppm max. (guaranteed over the operating temperature range)

Maximum jitter ..... 5 ps RMS phase-jitter (10 Hz to 1 MHz range)

Duty-factor ..... 45% to 55%

Unloaded signal swing ..... 3.3 V ±0.3 V

Note For other specifications, refer to the *PXI-1 Hardware Specification*.

100 MHz System Reference Clock: PXIe_CLK100 and PXIe_SYNC100

Maximum slot-to-slot skew ..... 100 ps

Accuracy ..... ±25 ppm max. (guaranteed over the operating temperature range)

Maximum jitter ..... 3 ps RMS phase-jitter (10 Hz to 12 kHz range)
2 ps RMS phase-jitter (12 kHz to 20 MHz range)

Duty-factor for PXIe_CLK100 ..... 45% to 55%

Absolute single-ended voltage swing
(When each line in the differential pair
has 50 W termination to 1.30 V
or Thévenin equivalent) ..... 400 to 1000 mV

Note For other specifications, refer to the *PXI-5 PXI Express Hardware Specification*.

External 10 MHz Reference Out (SMA on front panel of chassis)

Accuracy ..... ±25 ppm max. (guaranteed over the operating temperature range)

Maximum jitter ..... 5 ps RMS phase-jitter (10 Hz to 1 MHz range)

Output amplitude ..... 1 V_{PP} ±20% square-wave into 50 Ω 2 V_{PP} unloaded

Output impedance ..... 50 Ω ±5 Ω

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External Clock Source

Frequency ..... 10 MHz ±100 PPM

Input amplitude

Front-panel SMA ..... 200 mV_{PP} to 5 V_{PP} square-wave or sine-wave

System timing slot
PXI_CLK10_IN ..... 5 V or 3.3 V TTL signal

Front-panel SMA input impedance ..... 50 Ω ±5 Ω

Maximum jitter introduced
by backplane ..... 1 ps RMS phase-jitter (10 Hz to 1 MHz range)

PXIe_SYNC_CTRL

V_{IH} ..... 2.0 to 5.5 V

V_{IL} ..... 0 to 0.8 V

PXI Star Trigger

Maximum slot-to-slot skew ..... 250 ps

Backplane characteristic impedance ..... 65 Ω ±10%

Note For PXI slot to PXI Star mapping refer to the *System Timing Slot* section of Chapter 1, *Getting Started*.

For other specifications refer to the *PXI-1 Hardware Specification*.

PXI Differential Star Triggers (PXIe-DSTARA, PXIe-DSTARB, PXIe-DSTARC)

Maximum slot-to-slot skew ..... 150 ps

Maximum differential skew ..... 25 ps

Backplane differential impedance ..... 100 Ω ±10%

Note For PXI Express slot to PXI_DSTAR mapping refer to the *System Timing Slot* section of Chapter 1, *Getting Started*.

For other specifications, the PXIe-1086 complies with the *PXI-5 PXI Express Hardware Specification*.

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Mechanical

Overall dimensions, standard chassis

- Height ..... 10.59 in. (268.7 mm)
- Width ..... 18.39 in. (467.1 mm)
- Depth ..... 18.76 in. (476.5 mm)

Note 1.84 in. (46.8 mm) is added to height when feet are installed.

Weight

- With two power supplies ..... 37.6 lb (17.1 kg)
- With single power supply ..... 31.5 lb (14.3 kg)

Chassis materials ..... Sheet Aluminum (5052-H32, 3003-H14, and 6061-T6), Extruded Aluminum (6060-T6), and Cold Rolled Steel, PC-ABS, Santoprene, Nylon

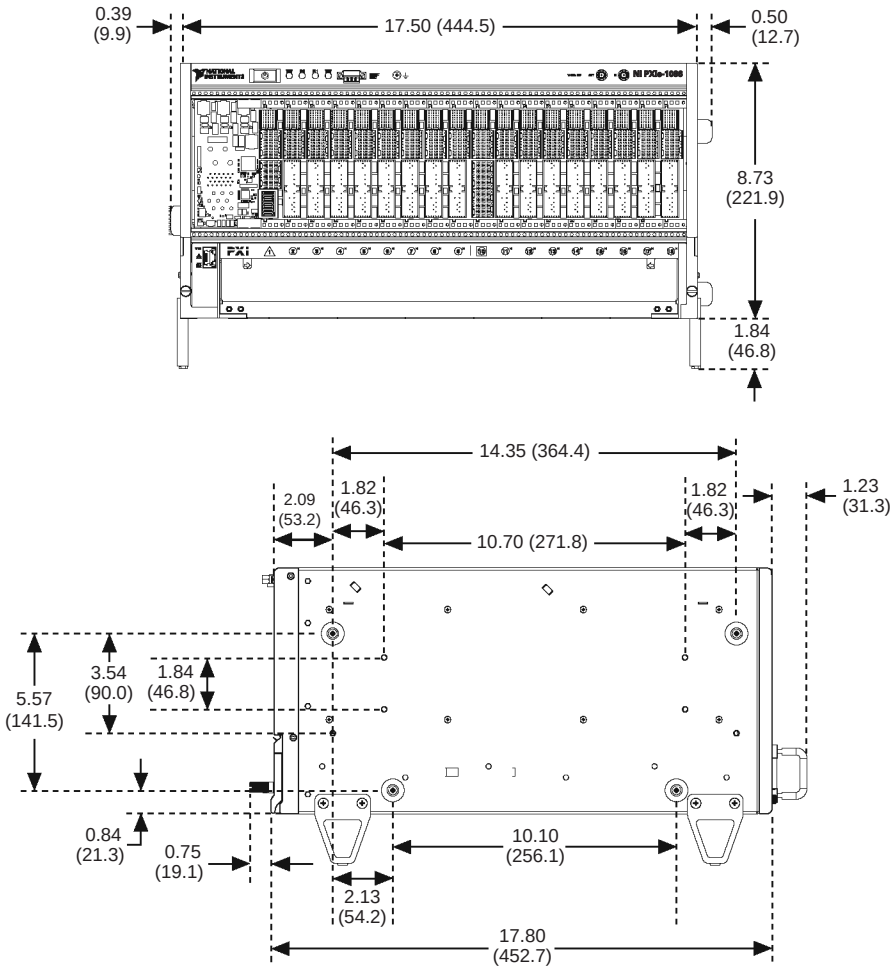
Finish ..... Conductive Clear Iridite on Aluminum
Electroplated Nickel
on Cold Rolled Steel
Polyurethane Enamel

Figures A-1 and A-2 show the PXIe-1086 chassis dimensions. The holes shown are for the installation of the optional rack mount kits. You can install those kits on the front or rear of the chassis, depending on which end of the chassis you want to face toward the front of the instrument cabinet. Notice that the front and rear chassis mounting holes (size M4) are symmetrical.

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Figure A-1. NI PXIe-1086 Chassis Dimensions (Front and Side)

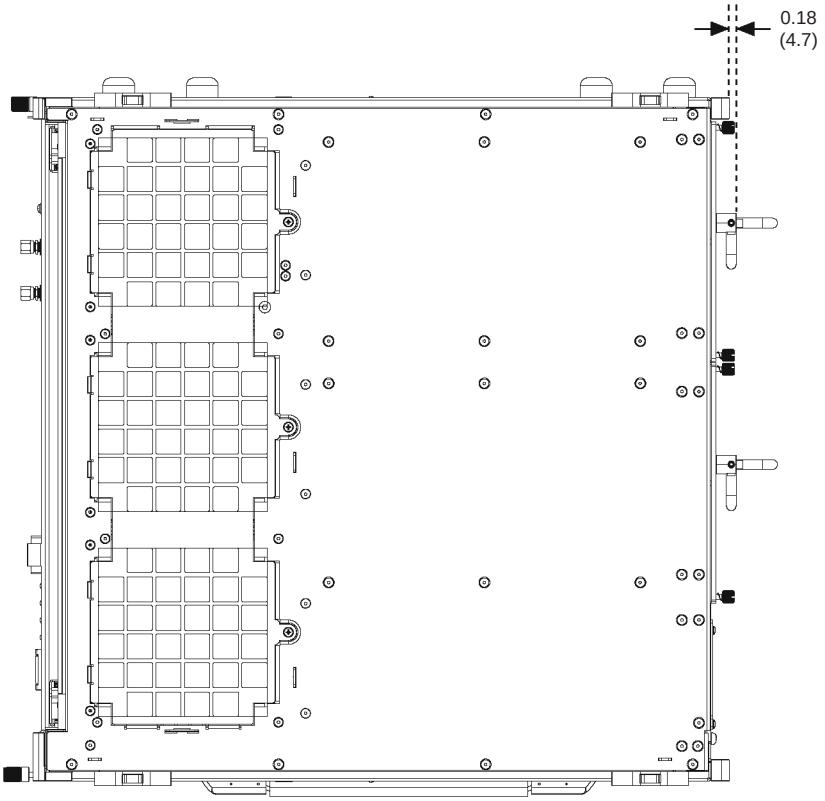
Dimensions are in inches (millimeters)



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Figure A-2. NI PXIe-1086 Chassis Dimensions (Bottom)

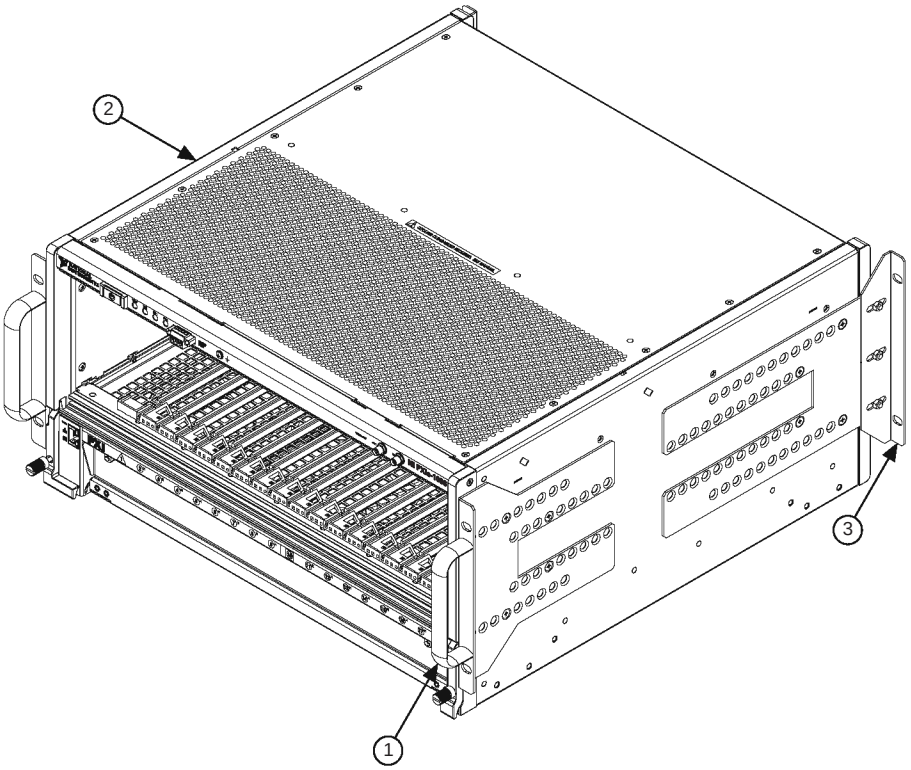
Dimensions are in inches (millimeters)



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Figure A-3 shows the chassis rack mount kit components.

Figure A-3. NI Chassis Rack Mount Kit Components



1	Front Rack Mount Kit	2	NI Chassis	3	Optional Rear Rack Mount Kit

Note For more information about rack mounting the PXIe-1086 chassis, refer to the printed installation guide included with your rack mount kit.

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B

Pinouts

This appendix describes the connector pinouts for the PXIe-1086 chassis backplane.

Table B-1 shows the XP1 connector pinout for the System Controller slot.

Table B-2 shows the XP2 connector pinout for the System Controller slot.

Table B-3 shows the XP3 connector pinout for the System Controller slot.

Table B-4 shows the XP4 connector pinout for the System Controller slot.

Table B-5 shows the TP1 connector pinout for the System Controller slot.

Table B-6 shows the TP2 connector pinout for the System Timing slot.

Table B-7 shows the XP3 connector pinout for the System Timing slot.

Table B-8 shows the XP4 connector pinout for the System Timing slot.

Table B-9 shows the P1 connector pinout for the peripheral slots.

Table B-10 shows the P2 connector pinout for the peripheral slots.

Table B-11 shows the P1 connector pinout for the Hybrid peripheral slots.

Table B-12 shows the XP3 connector pinout for the Hybrid peripheral slots.

Table B-13 shows the XP4 connector pinout for the Hybrid peripheral slots.

For more detailed information, refer to the *PXI-5 PXI Express Hardware Specification*, Revision 2.0. Contact the PXI Systems Alliance for a copy of the specification.

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System Controller Slot Pinouts

Table B-1. XP1 Connector Pinout for the System Controller Slot

Pins	Signals
A	GND
B	12V
C	12V
D	GND
E	5V
F	3.3V
G	GND

Table B-2. XP2 Connector Pinout for the System Controller Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	3PETp1	3PETn1	GND	3PERp1	3PERn1	GND	3PETp2	3PETn2	GND
2	3PETp3	3PETn3	GND	3PERp3	3PERn3	GND	3PERp2	3PERn2	GND
3	4PETp0	4PETn0	GND	4PERp0	4PERn0	GND	4PETp1	4PETn1	GND
4	4PETp2	4PETn2	GND	4PERp2	4PERn2	GND	4PERp1	4PERn1	GND
5	4PETp3	4PETn3	GND	4PERp3	4PERn3	GND	RSV	RSV	GND
6	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
7	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
8	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
9	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
10	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND

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Table B-3. XP3 Connector Pinout for the System Controller Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
2	RSV	RSV	GND	PWR_OK	PS_ON#	GND	LINKCAP	PWRBTN#	GND
3	SMBDAT	SMBCLK	GND	4RefClk+	4RefClk-	GND	2RefClk+	2RefClk-	GND
4	RSV	PERST#	GND	3RefClk+	3RefClk-	GND	1RefClk+	1RefClk-	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	2PETp0	2PETn0	GND
8	2PETp1	2PETn1	GND	2PERp1	2PERn1	GND	2PERp0	2PERn0	GND
9	2PETp2	2PETn2	GND	2PERp2	2PERn2	GND	2PETp3	2PETn3	GND
10	3PETp0	3PETn0	GND	3PERp0	3PERn0	GND	2PERp3	2PERn3	GND

Table B-4. XP4 Connector Pinout for the System Controller Slot

Pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	RSV	RSV	RSV	RSV	RSV	GND
4	GND	RSV	RSV	RSV	RSV	RSV	GND
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND
6	GND	PXI_TRIG2	GND	RSV	PXI_STAR	PXI_CLK10	GND
7	GND	PXI_TRIG1	PXI_TRIG0	RSV	GND	PXI_TRIG7	GND
8	GND	RSV	GND	RSV	RSV	PXI_LBR6	GND

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System Timing Slot Pinouts

Table B-5. TP1 Connector Pinout for the System Timing Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_ DSTARA3+	PXIe_ DSTARA3-	GND	NC	NC	GND	NC	NC	GND
2	PXIe_ DSTARC4+	PXIe_ DSTARC4-	GND	PXI_ STAR12	PXI_ STAR13	GND	NC	NC	GND
3	PXIe_ DSTARB4+	PXIe_ DSTARB4-	GND	NC	NC	GND	NC	NC	GND
4	PXIe_ DSTARA4+	PXIe_ DSTARA4-	GND	NC	NC	GND	NC	NC	GND
5	PXIe_ DSTARC5+	PXIe_ DSTARC5-	GND	PXI_ STAR14	PXI_ STAR15	GND	NC	NC	GND
6	PXIe_ DSTARB5+	PXIe_ DSTARB5-	GND	NC	NC	GND	NC	NC	GND
7	PXIe_ DSTARA5+	PXIe_ DSTARA5-	GND	NC	NC	GND	NC	NC	GND
8	PXIe_ DSTARC6+	PXIe_ DSTARC6-	GND	PXI_ STAR16	RSV	GND	NC	NC	GND
9	PXIe_ DSTARB6+	PXIe_ DSTARB6-	GND	NC	NC	GND	NC	NC	GND
10	PXIe_ DSTARA6+	PXIe_ DSTARA6-	GND	NC	NC	GND	NC	NC	GND

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Table B-6. TP2 Connector Pinout for the System Timing Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	NC	NC	GND	PXIe_ DSTAR C8+	PXIe_ DSTAR C8-	GND	PXIe_ DSTAR B8+	PXIe_ DSTAR B8-	GND
2	NC	NC	GND	NC	NC	GND	PXIe_ DSTAR A8+	PXIe_ DSTAR A8-	GND
3	NC	NC	GND	PXIe_ DSTAR C1+	PXIe_ DSTAR C1-	GND	NC	NC	GND
4	PXIe_ DSTAR B1+	PXIe_ DSTAR B1-	GND	PXI_ STAR0	PXI_ STAR1	GND	NC	NC	GND
5	PXIe_ DSTAR A1+	PXIe_ DSTAR A1-	GND	PXI_ STAR2	PXI_ STAR3	GND	NC	NC	GND
6	PXIe_ DSTAR C2+	PXIe_ DSTAR C2-	GND	PXI_ STAR4	PXI_ STAR5	GND	NC	NC	GND
7	PXIe_ DSTAR B2+	PXIe_ DSTAR B2-	GND	PXI_ STAR6	PXI_ STAR7	GND	NC	NC	GND
8	PXIe_ DSTAR A2+	PXIe_ DSTAR A2-	GND	PXI_ TAR8	PXI_ STAR9	GND	PXIe_ DSTAR C11+	PXIe_ DSTAR C11-	GND
9	PXIe_ DSTAR C3+	PXIe_ DSTAR C3-	GND	PXI_ STAR10	PXI_ STAR11	GND	PXIe_ DSTAR A11+	PXIe_ DSTAR A11-	GND
10	PXIe_ DSTAR B3+	PXIe_ DSTAR B3-	GND	NC	NC	GND	PXIe_ DSTAR B11+	PXIe_ DSTAR B11-	GND

Table B-7. XP3 Connector Pinout for the System Timing Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_ CLK 100+	PXIe_ CLK 100-	GND	PXIe_ SYNC 100+	PXIe_ SYNC 100-	GND	PXIe_ DSTAR C+	PXIe_ DSTAR C-	GND
2	PRSNT#	PWREN#	GND	PXIe_ DSTAR B+	PXIe_ DSTAR B-	GND	PXIe_ DSTAR A+	PXIe_ DSTAR A-	GND
3	SMB DAT	SMB CLK	GND	RSV	RSV	GND	RSV	RSV	GND

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Table B-7. XP3 Connector Pinout for the System Timing Slot (Continued)

Pin	A	B	ab	C	D	cd	E	F	ef
4	MPWR GD*	PERST#	GND	RSV	RSV	GND	1RefClk+	1RefClk-	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND

Table B-8. XP4 Connector Pinout for the System Timing Slot

Pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	12V	12V	GND	GND	GND	GND
4	GND	GND	GND	3.3V	3.3V	3.3V	GND
5	GND	PXI_TRIG3	PXI_ TRIG4	PXI_ TRIG5	GND	PXI_ TRIG6	GND
6	GND	PXI_TRIG2	GND	ATNLED	PXI_CLK10_IN	PXI_ CLK10	GND
7	GND	PXI_TRIG1	PXI_ TRIG0	ATNSW#	GND	PXI_ TRIG7	GND
8	GND	PXIe_SYNC_ CTRL	GND	RSV	PXI_LBL6	PXI_ LBR6	GND

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Peripheral Slot Pinouts

Table B-9. P1 Connector Pinout for the Peripheral Slot

Pin	Z	A	B	C	D	E	F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
12 to 14	Key Area						
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND
4	GND	IPMB_PWR	HEALTHY	V(I/O)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND

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Table B-10. P2 Connector Pinout for the Peripheral Slot

Pin	Z	A	B	C	D	E	F
22	GND	**GA4**	**GA3**	**GA2**	**GA1**	**GA0**	GND
21	GND	**PXI_LBR0**	GND	**PXI_LBR1**	**PXI_LBR2**	**PXI_LBR3**	GND
20	GND	**PXI_LBR4**	**PXI_LBR5**	**PXI_LBL0**	GND	**PXI_LBL1**	GND
19	GND	**PXI_LBL2**	GND	**PXI_LBL3**	**PXI_LBL4**	**PXI_LBL5**	GND
18	GND	**PXI_TRIG3**	**PXI_ TRIG4**	**PXI_ TRIG5**	GND	**PXI_ TRIG6**	GND
17	GND	**PXI_TRIG2**	GND	RSV	**PXI_ STAR**	**PXI_ CLK10**	GND
16	GND	**PXI_TRIG1**	**PXI_ TRIG0**	RSV	GND	**PXI_ TRIG7**	GND
15	GND	**PXI_ BRSVA15**	GND	RSV	**PXI_LBL6**	**PXI_LBR6**	GND
14	GND	RSV	RSV	RSV	GND	RSV	GND
13	GND	RSV	GND	V(I/O)	RSV	RSV	GND
12	GND	RSV	RSV	RSV	GND	RSV	GND
11	GND	RSV	GND	V(I/O)	RSV	RSV	GND
10	GND	RSV	RSV	RSV	GND	RSV	GND
9	GND	RSV	GND	V(I/O)	RSV	RSV	GND
8	GND	RSV	RSV	RSV	GND	RSV	GND
7	GND	RSV	GND	V(I/O)	RSV	RSV	GND
6	GND	RSV	RSV	RSV	GND	RSV	GND
5	GND	RSV	GND	V(I/O)	RSV	RSV	GND
4	GND	V(I/O)	64EN#	RSV	GND	RSV	GND
3	GND	**PXI_LBR7**	GND	**PXI_LBR8**	**PXI_LBR9**	**PXI_ LBR10**	GND
2	GND	**PXI_LBR11**	**PXI_ LBR12**	UNC	**PXI_LBL7**	**PXI_LBL8**	GND
1	GND	**PXI_LBL9**	GND	**PXI_ LBL10**	**PXI_ LBL11**	**PXI_ LBL12**	GND

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Hybrid Slot Pinouts

Table B-11. P1 Connector Pinout for the Hybrid Slot

Pin	Z	A	B	C	D	E	F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
12 to 14	Key Area						
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND

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Table B-12. XP3 Connector Pinout for the Hybrid Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_ CLK 100+	PXIe_ CLK 100-	GND	PXIe_ SYNC 100+	PXIe_ SYNC100-	GND	PXIe_ DSTARC+	PXIe_ DSTAR C-	GND
2	PRSNT#	PWREN#	GND	PXIe_ DSTAR B+	PXIe_ DSTARB-	GND	PXIe_ DSTARA+	PXIe_ DSTAR A-	GND
3	SMB DAT	SMB CLK	GND	RSV	RSV	GND	RSV	RSV	GND
4	MPWR GD*	PERST#	GND	RSV	RSV	GND	1RefClk+	1Ref Clk-	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND

Table B-13. XP4 Connector Pinout for the Hybrid Slot

Pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	12V	12V	GND	GND	GND	GND
4	GND	GND	GND	3.3V	3.3V	3.3V	GND
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND
6	GND	PXI_TRIG2	GND	ATNLED	PXI_STAR	PXI_CLK10	GND
7	GND	PXI_TRIG1	PXI_TRIG0	ATNSW#	GND	PXI_TRIG7	GND
8	GND	RSV	GND	RSV	PXI_LBL6	PXI_LBR6	GND

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Glossary

Symbol	Prefix	Value
p	pico	10^{-12}
n	nano	10^{-9}
µ	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^{3}
M	mega	10^{6}
G	giga	10^{9}
T	tera	10^{12}

Symbols

°	Degrees.
≥	Equal or greater than.
≤	Equal or less than.
%	Percent.

A

A	Amperes.
AC	Alternating current.
ANSI	American National Standards Institute.
Auto	Automatic fan speed control.
AWG	American Wire Gauge.

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B

backplane	An assembly, typically a printed circuit board, with connectors and signal paths that bus the connector pins.
BNC	Bayonet Neill Concelman connector—A commonly used coaxial connector.

C

C	Celsius.
cfm	Cubic feet per minute.
CFR	Code of Federal Regulations.
cm	Centimeters.
CompactPCI	An adaptation of the Peripheral Component Interconnect (PCI) Specification 2.1 or later for industrial and/or embedded applications requiring a more robust mechanical form factor than desktop PCI. It uses industry standard mechanical components and high-performance connector technologies to provide an optimized system intended for rugged applications. It is electrically compatible with the PCI Specification, which enables low-cost PCI components to be utilized in a mechanical form factor suited for rugged environments.
CSA	Canadian Standards Association.

D

daisy-chain	A method of propagating signals along a bus, in which the devices are prioritized on the basis of their position on the bus.
DB-9	A 9-pin D-SUB connector.
DC	Direct current.
DoC	Declaration of Conformity.
D-SUB	Subminiature D connector.

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E

efficiency	Ratio of output power to input power, expressed as a percentage.
EIA	Electronic Industries Association.
EMC	Electromagnetic Compatibility.
EMI	Electromagnetic Interference.

F

FCC	Federal Communications Commission.
filler panel	A blank module front panel used to fill empty slots in the chassis.

G

g	(1) grams; (2) a measure of acceleration equal to 9.8 m/s^2.
GPIB	General Purpose Interface Bus (IEEE 488).
g_{RMS}	A measure of random vibration. The root mean square of acceleration levels in a random vibration test profile.

H

hr	Hours.
Hz	Hertz—Cycles per second.

I

IEC	International Electrotechnical Commission—An organization that sets international electrical and electronics standards.
IEEE	Institute of Electrical and Electronics Engineers.
I_{MP}	Mainframe peak current.

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in.	Inches.
inhibit	To turn off.

J

jitter	A measure of the small, rapid variations in clock transition times from their nominal regular intervals. Units: seconds RMS.

K

kg	Kilograms.
km	Kilometers.

L

lb	Pounds.
LED	Light emitting diode.
line regulation	The maximum steady-state percentage that a DC voltage output will change as a result of a specified change in input AC voltage (step change from 90 to 132 VAC or 180 to 264 VAC).
load regulation	The maximum steady-state percentage that a DC voltage output will change as a result of a step change from no-load to full-load output current.

M

m	Meters.
MHz	Megahertz—One million Hertz; one Hertz equals one cycle per second.
mi	Miles.
ms	Milliseconds.
MTBF	Mean time between failure.

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MTTR	Mean time to repair.

N

NEMA	National Electrical Manufacturers Association.
NI	National Instruments.

P

power supply shuttle	A removable module that contains the chassis power supply.
PXI	PCI eXtensions for Instrumentation.
PXI_CLK10	10 MHz PXI system reference clock.

R

RH	Relative humidity.
RMS	Root mean square.

S

s	Seconds.
skew	Deviation in signal transmission times.
slot blocker	An assembly installed into an empty slot to improve the airflow in adjacent slots.
standby	The backplane is unpowered (off), but the chassis is still connected to AC power mains.
System controller	A module configured for installation in Slot 1of a PXI chassis. This device is unique in the PXI system in that it performs the system controller functions, including clock sourcing and arbitration for data transfers across the backplane. Installing such a device into any other slot can damage the device, the PXI backplane, or both.

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system reference clock	A 10 MHz clock, also called PXI_CLK10, that is distributed to all peripheral slots in the chassis, as well as a BNC connector on the rear of chassis labeled *10 MHz REF OUT*. The system reference clock can be used for synchronization of multiple modules in a measurement or control system. The 10 MHz REF IN and OUT BNC connectors on the rear of the chassis can be used to synchronize multiple chassis to one reference clock. The PXI backplane specification defines implementation guidelines for PXI_CLK10.
System Timing slot	This slot is located at slot 4 and has dedicated trigger lines to other slots.

T

TTL	Transistor-transistor logic.

U

UL	Underwriter's Laboratories.

V

V	Volts.
VAC	Volts alternating current.
V_{pp}	Peak-to-peak voltage.

W

W	Watts.

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