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SPECIFICATIONS

PXIe-5172

250 MS/s, 14-bit Reconfigurable Oscilloscope

These specifications apply to the PXIe-5172 with 4 channels and the PXIe-5172 with 8 channels.

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Definitions and Conditions

Specifications are subject to change without notice. For the most recent PXIe-5172 specifications, visit *ni.com/manuals*. Unless otherwise noted, the following conditions were used for each specification:

Specifications are valid under the following conditions unless otherwise noted:

- All vertical ranges
- All bandwidths and bandwidth limit filters
- Sample rate set to 250 MS/s
- Onboard Sample clock locked to onboard Reference clock
- Calibration IP is used properly when using LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes (instrument design libraries) to create FPGA bitfiles. Refer to the *NI Reconfigurable Oscilloscopes Help* for more information about the calibration IP.

Warranted specifications are valid for the ambient temperature range 0 °C to 45 °C and include guardband for measurement uncertainty unless otherwise noted. Warranted specifications are valid under the following conditions unless otherwise noted:

- The PXIe-5172 module is warmed up for 15 minutes at ambient temperature.
- Calibration cycle is maintained.
- The PXI Express chassis fan speed is set to HIGH, the foam fan filters are removed if present, and the empty slots contain PXI chassis slot blockers and filler panels. For more information about cooling, refer to the *Maintain Forced-Air Cooling Note to Users* available at *ni.com/manuals*.
- External calibration is performed at 23 °C ± 3 °C.

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Typical specifications describe useful device performance beyond warranted values. Typical specifications are not covered by warranty, do not include guardband for measurement uncertainty, and may not be verified on all units shipped from the factory. Unless otherwise noted, typical specifications describe the expected performance of units, with a 90% confidence level based on measurements taken during development or production, over the ambient temperature range 0 °C to 45 °C.

Characteristics (or supplemental information) describe basic functions and attributes of the device established by design.

Data in this document are *Warranted* unless otherwise noted.

Safety Guidelines



Note Do not operate the PXIe-5172 in a manner not specified in this document. Product misuse can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to NI for repair.



Caution This icon denotes a caution advising you take precautions to avoid injury.



Hazardous Voltage This icon denotes a warning advising you to take precautions to avoid electrical shock.



Hot Surface This icon denotes that the component may be hot. Touching this component may result in bodily injury. If the PXIe-5172 has been in use, it may exceed safe handling temperatures and cause burns. Allow the PXIe-5172 to cool before removing it from the chassis. Refer to the *Environment* section for operating temperatures of this device.



Caution Clean the hardware with a soft, nonmetallic brush. Make sure that the hardware is completely dry and free from contaminants before returning it to service.

Vertical

Analog Input

Number of channels	
PXIe-5172 (4 CH)	Four (simultaneously sampled)
PXIe-5172 (8 CH)	Eight (simultaneously sampled)
Input type	Referenced single-ended
Connectors	SMB, ground referenced

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Impedance and Coupling

Input impedance	50 Ω ±1.5%, typical 1 MΩ ±0.5%
Input capacitance (1 MΩ)	16 pF ±1.2 pF, typical
Input coupling	AC, DC

Figure 1. 50 Ω Voltage Standing Wave Ratio (VSWR), Characteristic

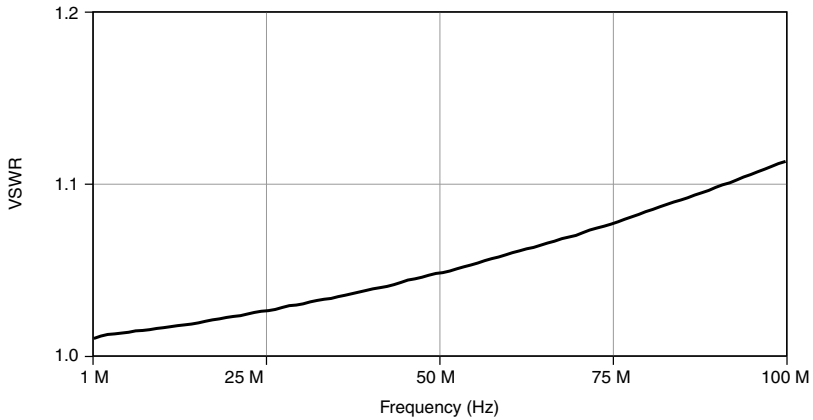
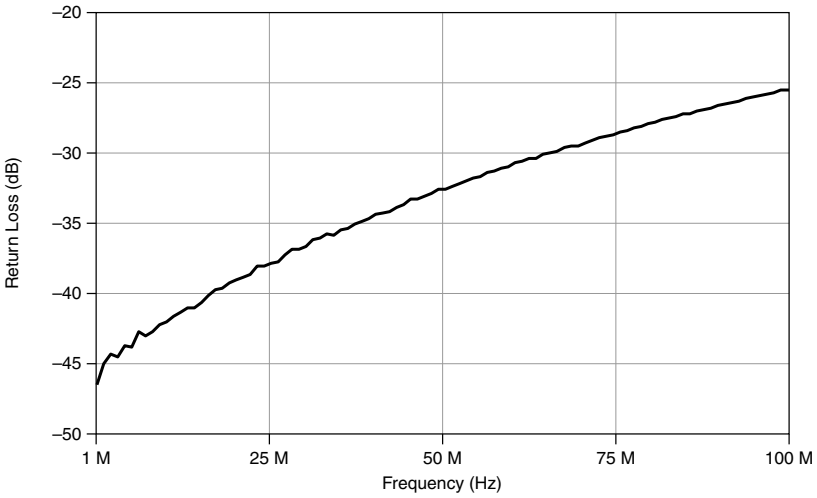


Figure 2. 50 Ω Input Return Loss, Characteristic



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Voltage Levels

Table 1. 50 Ω FS Input Range and Vertical Offset Range

Input Range (V_{pk-pk})	Vertical Offset Range (V)
0.2 V	±0.5
0.7 V	±0.5
1.4 V	±0.5
5 V	±2.5
10 V[1]	0

Table 2. 1 MΩ FS Input Range and Vertical Offset Range

Input Range (V_{pk-pk})	Vertical Offset Range (V)
0.2 V	±0.5
0.7 V	±0.5
1.4 V	±0.5
5 V	±4.5
10 V	±4.5
40 V	±20
80 V	0

Maximum input overload, characteristic[2]	
50 Ω	7 V_{rms} with |Peaks| ≤10 V
1 MΩ	|Peaks| ≤42 V

[1] Derated to 5 V_{pk-pk} for periodic waveforms with frequencies below 100 kHz.
[2] Signals exceeding the maximum input overload may cause damage to the device.

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Accuracy

Resolution	14 bits
DC accuracy[3]	
50 Ω	±[(0.45% × |*Reading* - *Vertical Offset*|) + (0.4% × |*Vertical Offset*|) + (0.05% of *FS*) + 0.4 mV]
1 MΩ, 40 V_{pk-pk} range	±[(0.45% × |*Reading* - *Vertical Offset*|) + (0.5% × |*Vertical Offset*|) + (0.05% of *FS*) + 0.4 mV]
1 MΩ, all other ranges	±[(0.45% × |*Reading* - *Vertical Offset*|) + (0.4% × |*Vertical Offset*|) + (0.05% of *FS*) + 0.4 mV]
DC drift, characteristic[4]	±[(0.010% × |*Reading* - *Vertical Offset*|) + (0.003% × |*Vertical Offset*|) + (0.006% of FS)] per °C
AC amplitude accuracy[3]	
1 MΩ, 40 V_{pk-pk} and 80 V_{pk-pk} ranges	±0.25 dB at 50 kHz
50 Ω and 1 MΩ, all other ranges	±0.15 dB at 50 kHz

Note This device may experience increased peak to peak noise when connected cables are routed in an environment with radiated or conducted electromagnetic interference. To limit the effects of this interference and to ensure that this device functions within specifications, take precautions when designing, selecting, and installing measurement probes and cables.

Table 3. Crosstalk 50 Ω, Characteristic[5]

Frequency	Level
1 MHz	-75 dB
50 MHz	-75 dB
100 MHz	-70 dB

[3] Within ± 5 °C of self-calibration temperature. Accuracy is warranted only when using DC input coupling.

[4] Used to calculate errors when on board temperature changes more than ±5 °C from the self-calibration temperature.

[5] Measured on one channel with test signal applied to another channel, with the same range setting on both channels.

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Table 4. Crosstalk 1 MΩ, Characteristic[5]

Frequency	Level (0.2 V_{pk-pk} Range to 10 V_{pk-pk} Range)	Level (40 V_{pk-pk} Range)
1 MHz	-75 dB	-65 dB
50 MHz	-75 dB	-65 dB
100 MHz	-70 dB	-65 dB

Bandwidth and Transient Response

Table 5. Bandwidth (-3 dB)[6]

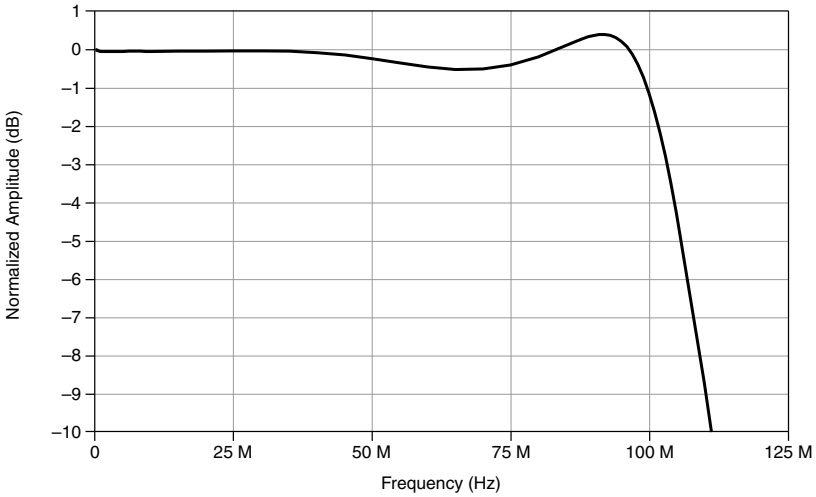
Input Impedance	Input Range (V_{pk-pk}	Bandwidth
50 Ω	0.2 V	99 MHz
	All other input ranges	100 MHz
1 MΩ[7]	All input ranges	98 MHz

Bandwidth-limiting filters[6,8]	20 MHz noise filter, characteristic
AC-coupling cutoff (-3 dB)[9]	16.50 Hz, characteristic
Rise/fall time[10]	
50 Ω	5.15 ns, characteristic
1 MΩ	5.25 ns, characteristic

6 Normalized to 50 kHz.
7 Verified using a 50 Ω source and 50 Ω feedthrough terminator.
8 Only available using NI-SCOPE.
9 Verified using a 50 Ω source.
10 50% FS input pulse.

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Figure 3. 50 Ω Full Bandwidth Frequency Response, 1.4 V_{pk-pk}, Characteristic



Spectral Characteristics[11]

Table 6. Spurious-Free Dynamic Range (SFDR), Characteristic[12]

Input Range (V_{pk-pk})	Input Frequency	Full Bandwidth
0.2 V	≤30 MHz	-70 dBc
0.7 V		-78 dBc
1.4 V		-71 dBc
5 V		-80 dBc

[11] For 1 MΩ, verified using a 50 Ω source and 50 Ω feedthrough terminator.
[12] -1 dBFS input signal corrected to FS. 358 Hz resolution bandwidth.

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Table 7. Total Harmonic Distortion (THD)[13]

Input Range (V_{pk-pk})	Input Frequency	Full Bandwidth
0.2 V	≤30 MHz	-74 dBc
0.7 V		-77 dBc
1.4 V		-70 dBc
5 V		-77 dBc

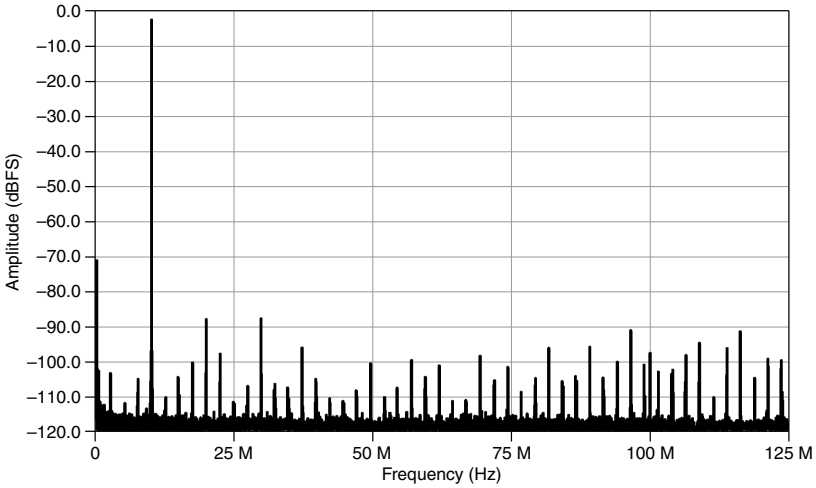
Table 8. Effective Number of Bits (ENOB), Characteristic[12]

Input Range (V_{pk-pk})	Input Frequency	20 MHz Filter Enabled	Full Bandwidth
0.2 V	≤10 MHz	9.8	9.5
	>10 MHz to ≤30 MHz	—	9.5
0.7 V	≤10 MHz	11.4	10.8
	>10 MHz to ≤30 MHz	—	10.8
1.4 V	≤10 MHz	11.9	10.8
	>10 MHz to ≤30 MHz	—	10.8
5 V	≤10 MHz	11.8	11.0
	>10 MHz to ≤30 MHz	—	11.0

[13] -1 dBFS input signal corrected to FS. Includes the 2nd through the 5th harmonics.

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Figure 4. 50 Ω Single-Tone Spectrum, 1.4 V_{pk-pk} Input Range, Full Bandwidth, 9.9 MHz Input Tone at -1 dBFS, Characteristic



Noise[14]

Table 9. RMS Noise

Input Impedance	Input Range (V_{pk-pk})	RMS Noise (% of Full Scale)
50 Ω	0.2 V	0.045
	All other input ranges	0.018
1 MΩ	0.2 V	0.045
	All other input ranges	0.018

[14] Verified using a 50 Ω terminator connected to input.

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Figure 5. 50 Ω Average Noise Density, 1.4 V_{pk-pk} Range, Characteristic

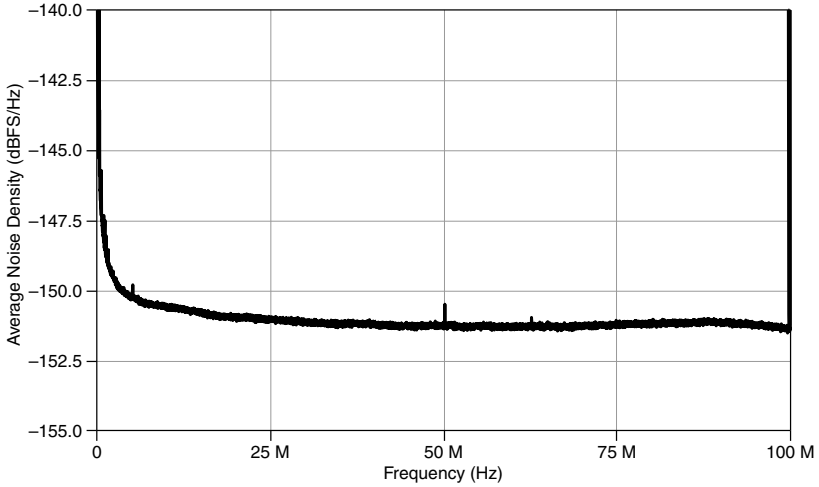
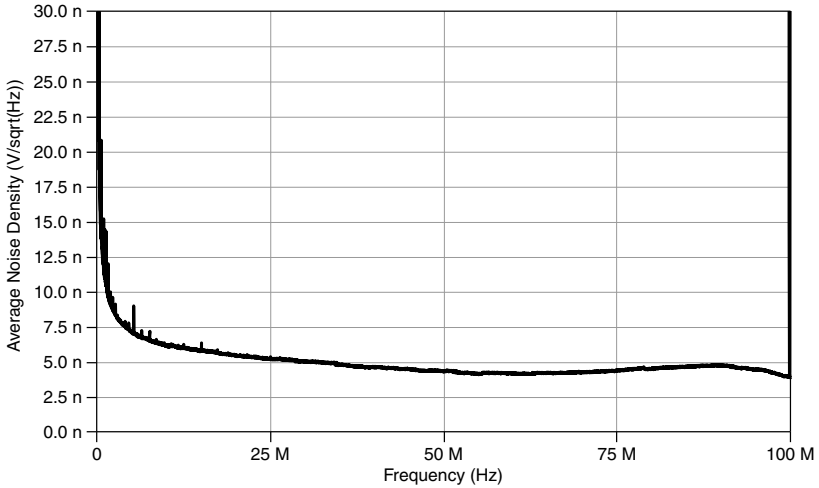


Figure 6. 50 Ω Average Noise Density, 0.2 V_{pk-pk} Range, Characteristic



Skew

Channel-to-channel skew[15]	<120 ps, characteristic

[15] For input frequencies less than 90 MHz.

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Horizontal

ADC Clock

Sources	
Internal	Onboard clock
External	CLK IN (from front panel AUX 0 connector) PXIe_DStarA (from backplane)
Duty cycle	45% to 55%
Frequency	
Internal	250 MHz
External	150 MHz to 250 MHz
DC accuracy sampling drift, ±(% of |*Reading*|) per MHz from 250 MHz[16]	±0.0127, characteristic

Reference Clock

Sources	None (internal VCXO) CLK IN (from AUX 0) PXI_Clk10 (from backplane)
Duty cycle tolerance	45% to 55%
Frequency[17]	10 MHz

Onboard Clock

ADC clock frequency	250 MHz
Real-time sample rate range[18]	3.815 kS/s to 250 MS/s
Sample clock jitter[19]	700 fs_{rms}, characteristic
ADC clock accuracy	
Phase-locked to onboard clock	±25 ppm
Phase-locked to external clock	Equal to the external clock accuracy

[16] Used to calculate additional DC accuracy error when using an external Sample clock that is less than 250 MHz. To calculate the additional error, take the difference of the external Sample clock rate from 250 MHz, divide by 1,000,000, and multiply by the DC accuracy sampling drift.

[17] The PLL Reference Clock must be accurate to ±25 ppm.

[18] Divide by n decimation from 250 MS/s. For more information about the Sample clock and decimation, refer to the *NI Reconfigurable Oscilloscopes Help* at *ni.com/manuals*.

[19] Integrated from 100 Hz to 10 MHz. Includes the effects of the converter aperture uncertainty and the clock circuitry jitter.

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CLK IN

Source	AUX 0
Impedance	50 Ω, characteristic
Coupling	AC
Input voltage range	
As a 250 MHz sine wave	1 dBm through 18 dBm
As a fast slew rate input (square wave, V_{pk-pk})	0.4 V to 5 V
Maximum input overload	
As a 250 MHz sine wave	20 dBm
As a fast slew rate input (square wave, V_{pk-pk})	6 V

PXIe_DStarA

Source	System timing slot
Destinations	ADC clock FPGA

PXI_Clk10

Source	PXI backplane
Destination	Reference clock

PXI_Clk100

Source	PXI backplane
Destination	FPGA

CLK OUT

Destination	AUX 0
Source	Reference clock PXI_CLK10
Output impedance	50 Ω, characteristic
Logic type	3.3 V LVCMOS
Maximum current drive	±8 mA, characteristic

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Trigger[20]

Dead time	*Sample clock period**10, characteristic
Holdoff	From dead time to [(2^{64} - 1) × *Sample clock period*]
Delay	From 0 to [(2^{51} - 1) × *Sample clock period*]

Analog Trigger

Trigger types	Edge Hysteresis Window
Trigger sources	
PXIe-5172 (4 CH)	CH <0..3>
PXIe-5172 (8 CH)	CH <0..7>
Time resolution	
With interpolator	*Sample clock period*/1024
Without interpolator	Sample clock period
Rearm time	
With interpolator	*Sample clock period**124
Without interpolator	*Sample clock period**84

Table 10. Trigger Accuracy, Characteristic[21]

Input Range (V_{pk-pk})	Trigger Accuracy (% of Full Scale)
0.2 V	0.75
0.7 V, 1.4 V, 5 V	0.5

Trigger jitter[21]	15 ps_{rms}, characteristic
Minimum threshold duration[22]	Sample clock period

[20] Refer to the *LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes Help* for information on supported data triggers. Specifications apply when Data Trigger IP is used properly when using instrument design libraries to create FPGA bitfiles.

[21] For input frequencies less than 90 MHz.

[22] Data must exceed each corresponding trigger threshold for at least the minimum duration to ensure analog triggering.

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Digital Trigger

Trigger types	Edge Immediate
Trigger sources	AUX 0/PFI <0..7> PXI_Trig <0..6>
Time resolution	*Sample clock period**2
Rearm time	*Sample clock period**84

Software Trigger

Trigger destinations	Start trigger (acquisition arm) Reference (stop) trigger Arm Reference trigger Advance trigger
Time resolution	*Sample clock period**2
Rearm time	*Sample clock period**84

Programmable Function Interface (AUX 0/ PFI <0..7>)

Connector	AUX 0
Direction	Bidirectional per channel
Direction control latency	125 ns
As an input (trigger)	
Destinations	FPGA diagram Start trigger (acquisition arm) Reference (stop) trigger Arm Reference trigger Advance trigger
Input impedance	49.9 kΩ, characteristic
V_{IH}	2 V
V_{IL}	0.8 V
Maximum input overload	0 V to 3.3 V nominal, 5 V tolerant
Minimum pulse width	10 ns

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As an output (event)	
Sources	FPGA diagram Ready for Start Start trigger (acquisition arm) Ready for Reference Reference (stop) trigger End of Record Ready for Advance Advance trigger Done (End of Acquisition)
Output impedance	50 Ω, characteristic
Logic type	3.3 V CMOS
Maximum current drive	12 mA, characteristic
Minimum pulse width	10 ns

Power Output (+3.3 V)

Connector	AUX 0/+3.3 V front panel connector
Voltage output	3.3 V ± 10%, characteristic
Maximum current drive	200 mA, characteristic
Output impedance	<1 Ω, characteristic

Waveform

Onboard memory size[23]	
PXIe-5172 (4 CH)	0.75 GB
PXIe-5172 (8 CH)	1.5 GB
Minimum record length	1 sample
Number of pretrigger samples	Zero up to (record length - 1)
Number of posttrigger samples	Zero up to record length

Figure 7. Maximum Number of Records in Onboard Memory

$$\frac{\text{total onboard memory}}{48 \times \text{number of channels}}$$

where *number of channels* is the number of channels enabled rounded up to the nearest power of two

[23] Onboard memory is shared among all enabled channels.

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Figure 8. Allocated Onboard Memory Per Record

$$\text{Roundup}\left(\text{Roundup}\left(\frac{\text{coerced number of samples} + \text{number of samples per sample word}}{\text{number of samples per memory word}}\right) \times \text{number of samples per memory word} + 3 \times \text{number of samples per memory word}\right) \times \text{bytes per sample} \times \text{number of channels}$$

where

number of samples per sample word = 16 samples / number of channels

number of samples per memory word = 48 samples / number of channels

coerced number of samples is the number of pretrigger samples rounded up to the next multiple of *number of samples per sample word* + the number of posttrigger samples rounded up to the next multiple of *number of samples per sample word*

number of channels is the number of channels enabled rounded up to the nearest power of two

Memory Sanitization

For information about memory sanitization, refer to the letter of volatility for your device, which is available at *ni.com/manuals*.

FPGA

FPGA support	Xilinx Kintex-7 XC7K325T FPGA Xilinx Kintex-7 XC7K410T FPGA[24]

Table 11. FPGA Resources

Resource Type	Xilinx Kintex-7 XC7K325T	Xilinx Kintex-7 XC7K410T
Slice registers	407,600	508,400
Slice look-up tables (LUT)	203,800	254,200
DSPs	840	1,540
18 Kb block RAMs	890	1,590

Note Note that some of these resources are consumed by the logic necessary to operate the device and integrate with software, and are thus out of the control of users.

[24] Only available for the 8-channel PXIe-5172.

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Calibration

External Calibration

External calibration yields the following benefits:

- Corrects for gain and offset errors of the onboard references used in self-calibration.
- Adjusts timebase accuracy.
- Compensates the 1 MΩ ranges.

All calibration constants are stored in nonvolatile memory.

Self-Calibration

Self-calibration is done on software command. The calibration corrects for the following aspects:

- Gain
- Offset
- Intermodule synchronization errors

Refer to the *NI High-Speed Digitizers Help* for information about when to self-calibrate the device.

Calibration Specifications

Interval for external calibration	2 years
Warm-up time[25]	15 minutes

Software

Driver Software

This device was first supported in NI-SCOPE 17.1 and NI LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes 17.1. NI LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes is an IVI-compliant driver that allows you to configure,

[25] Warm-up begins after the chassis and controller or PC is powered. In some RIO applications, the power consumed by the module can be significantly higher than the default image for the module. In these cases, you can improve performance by loading your image and configuring the device before warm-up time begins. Self-calibration is recommended following the specified warm-up time.

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control, and calibrate the device. NI-SCOPE provides application programming interfaces for many development environments.

Related Information

For more information about available software options, refer to the PXIe-5172 Getting Started Guide.

Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

Interactive Soft Front Panel and Configuration

The NI-SCOPE Soft Front Panel (SFP) allows interactive control of the PXIe-5172.

Interactive control of the PXIe-5172 was first available in NI-SCOPE SFP version 17.1. The NI-SCOPE SFP is included on the NI-SCOPE media.

NI Measurement Automation Explorer (MAX) also provides interactive configuration and test tools for the PXIe-5172. MAX is included on the NI-SCOPE and the NI LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes media.

TClk Specifications

You can use the NI TClk synchronization method and the NI-TClk driver to align the Sample clocks on any number of supported devices, in one or more chassis. For more information about TClk synchronization, refer to the *NI-TClk Synchronization Help*, which is located within the *NI High-Speed Digitizers Help*. For other configurations, including multichassis systems, contact NI Technical Support at *ni.com/support*.

Intermodule Synchronization Using NI-TClk for Identical Modules

Synchronization specifications are valid under the following conditions:

- All modules are installed in one PXI Express chassis.
- The NI-TClk driver is used to align the Sample clocks of each module.
- All parameters are set to identical values for each module.

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- Modules are synchronized without using an external Sample clock.
- Self-calibration is completed.

Note Although you can use NI-TClk to synchronize non-identical modules, these specifications apply only to synchronizing identical modules.

Skew[26]	300 ps, characteristic
Skew after manual adjustment	≤10 ps, characteristic
Sample clock delay/adjustment resolution	3.5 ps, characteristic

Power

Note Power consumed depends on the FPGA image and driver software used. Specifications for instrument design libraries reflect the performance of a device using the FPGA image from the Multirecord Acquisition sample project. Maximum power consumption occurs at the highest operating temperature.

PXIe-5172 (4 CH) power consumption	
+3.3 VDC	6.5 W, typical
+12 VDC	13.75 W, typical
Total power	20.25 W, typical
PXIe-5172 (8 CH) power consumption	
+3.3 VDC	8.5 W, typical
+12 VDC	18 W, typical
Total power	26.5 W, typical
Total maximum power allowed	38.25 W

Physical

Dimensions	3U, one-slot, PXI Express Gen 2 x8 Module 18.5 cm × 2.0 cm × 13.0 cm (7.3 in × 0.8 in × 5.1 in)
Weight	
PXIe-5172 (4 CH)	449 g (15.8 oz)
PXIe-5172 (8 CH)	461 g (16.3 oz)

[26] Caused by clock and analog path delay differences. No manual adjustment performed. Tested with a NI PXIe-1082 chassis with a maximum slot-to-slot skew of 100 ps. Valid within ±1 °C of self-calibration.

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Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 45 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 4 high temperature limit.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g_{rms} (Tested in accordance with IEC 60068-2-64.)
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC 60068-2-64. Test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

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Compliance and Certifications

Safety

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the *Online Product Certification* section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

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Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit *ni.com/certification*, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at *ni.com/environment*. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)



EU Customers At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit *ni.com/environment/weee*.

电子信息产品污染控制管理办法（中国 RoHS）



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376616C-01 December 12, 2017

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