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SPECIFICATIONS

NI PXIe/PCIe-6535/6536/6537 and NI PCIe-6535B/6536B/6537B

10/25/50 MHz Digital I/O Device

このドキュメントには、日本語ページも含まれています。

This document provides specifications for NI PXIe/PCIe-6535/6536/6537 (NI 6535/6536/6537) and NI PCIe-6535B/6536B/6537B (NI 6535B/6536B/6537B) digital I/O devices.

Specifications are subject to change without notice. For the most recent specifications visit `ni.com/manuals`.

Caution All values were obtained using a 1 m cable (SHC68-C68-D4 recommended). Performance specifications are not guaranteed when using longer cables.

Warranted specifications are warranted not to exceed these values within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

Typical specifications are unwarranted values that are representative of a majority (3σ) of units within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

Nominal specifications are unwarranted values that are relevant to the use of the product and convey the expected performance of the product.

All specifications are *Typical* unless otherwise noted. These specifications are valid within the operating temperature range. All warranted specifications will be specifically denoted as *Warranted* in the comment section of the specification.

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Channel Specifications

Specification	Value	Comments
Number of data channels	32	—
Direction control of data channels	Per channel	—
Number of Programmable Function Interface (PFI) channels	6	Refer to the *Waveform Specifications* section for more information about the PFI channels.
Direction control of PFI channels	Per channel	—

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Specification	Value		Comments
Number of RTSI/PXI trigger channels	**PXI Express**	**PCI Express**	PXI_TRIG7 is not supported as input trigger.
	10 (PXI_TRIG<0..7>, PXIe_DSTARB, PXIe_DSTARC)	8 (RTSI <0..7>)	
Direction control of RTSI/PXI trigger channels	RTSI <0..7>/PXI_TRIG<0..7>: Bidirectional; per channel PXIe_DSTARB: Unidirectional input (PXI Express only) PXIe_DSTARC: Unidirectional output (PXI Express only)		
Number of Sample clock terminals	3 bidirectional clock terminals (PFI 4, PFI 5, RTSI 7) 1 exported clock terminal (PXIe_DSTARC) (PXI Express only) 2 clock source terminals (PXIe_DSTARA, PXI_STAR) (PXI Express only)		Refer to *Timing Specifications* for more information about clock sources.

Generation Channels (Data and PFI <0..5> Channels)

Specification	Value				Comments
Generation voltage families	2.5 V, 3.3 V (5 V TTL compatible)				—
Generation signal type	Single-ended				—
Generation voltage levels	**Low Voltage Levels**		**High Voltage Levels**		Warranted. Into high impedance load. Production tested for data channels.
	Typical	**Maximum**	**Minimum**	**Typical**	
2.5 V	0.0 V	0.1 V	2.4 V	2.5 V	
3.3 V	0.0 V	0.1 V	3.2 V	3.3 V	
5.0 V	0.0 V	0.1 V	3.2 V	3.3 V	
Output impedance	50 Ω, nominal				—
Maximum DC drive strength	±16 mA at 2.5 V ±32 mA at 3.3 V				—
Data channel driver enable/disable control	Per channel				Software-selectable.

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Specification	Value	Comments
Channel power-up state	Software programmable (Tristate, 0, or 1 at 2.5 V or 3.3 V)	Channel data is typically valid 1.5 s after the power-up state is set.
Output protection	The device can indefinitely sustain a short to any voltage between 0 V and 5 V.	—

Acquisition Channels (Data and PFI <0..5> Channels)

Specification	Value		Comments
Acquisition voltage families	2.5 V, 3.3 V (5 V TTL compatible)		—
Acquisition voltage levels	**Low Voltage Thresholds Maximum**	**High Voltage Thresholds Minimum**	Warranted. Production tested for data channels.
2.5 V	0.75 V	1.75 V	
3.3 V	1.00 V	2.30 V	
5.0 V	1.00 V	2.30 V	
Input impedance	High-impedance (50 kΩ to ground)		—
Input protection	-1 V to +6 V		Diode clamps in the design may provide additional protection outside this range.

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Timing Specifications

Sample Clock

<table>
<tr><th>Specification</th><th colspan="2">Value</th><th>Comments</th></tr>
<tr><td>Sample clock sources</td><td colspan="2">1. On Board Clock (Sample Clock Timebase with divider)
2. PFI <4..5>
3. PXI_TRIG7 (PXI backplane)†
RTSI 7 (RTSI bus)‡
4. PXI_STAR (PXI backplane)†
5. PXIe_DSTARA (PXI backplane)†</td><td rowspan="2">Refer to the Clocking diagram in the NI 6535/6536/6537 and NI 6535B/6536B/6537B Help for an illustration of the various clock and timebase sources.</td></tr>
<tr><td>Sample clock timebase sources</td><td colspan="2">1. 200 MHz Timebase (internal oscillator)
2. PFI <0..5>
3. PXI_TRIG<0..6> (PXI backplane)†
RTSI <0..7> (RTSI bus)‡
4. PXIe_DSTARB (PXI backplane)†</td></tr>
<tr><td>On Board Clock frequency range</td><td colspan="2">NI 6535/6535B: 48 Hz to 10 MHz
Configurable to 200 MHz/N; 20 ≤ N ≤ 4,194,307
NI 6536/6536B: 48 Hz to 25 MHz
Configurable to 200 MHz/N; 8 ≤ N ≤ 4,194,307
NI 6537/6537B: 48 Hz to 50 MHz
Configurable to 200 MHz/N; 4 ≤ N ≤ 4,194,307</td><td>—</td></tr>
<tr><td rowspan="2">Imported Sample clock frequency range</td><td>PFI <4..5>
PXIe_DSTARA†</td><td>PXI_TRIG7†
RTSI 7‡</td><td rowspan="2">—</td></tr>
<tr><td>NI 6535/6535B:
0 Hz to 10 MHz
NI 6536/6536B:
0 Hz to 25 MHz
NI 6537/6537B:
0 Hz to 50 MHz</td><td>NI 6535/6535B:
0 Hz to 10 MHz
NI 6536/6536B and
NI 6537/6537B:
0 Hz to 25 MHz</td></tr>
<tr><td colspan="4">† PXI Express only
‡ PCI Express only</td></tr>
</table>

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<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td>Minimum detectable Sample clock pulse width</td><td>PFI <4..5>
8 ns</td><td>PXIe_DSTARA†
NI 6535/6535B and NI 6536/6536B: 15 ns
NI 6537/6537B: 8 ns</td><td>PXI_TRIG7†
RTSI 7‡
15 ns</td><td>Positive and negative pulse width at voltage thresholds.</td></tr>
<tr><td>Imported timebase clock frequency range</td><td colspan="2">PFI <0..5>
PXIe_DSTARB†
NI 6535/6535B: 0 Hz to 10 MHz
NI 6536/6536B: 0 Hz to 25 MHz
NI 6537/6537B: 0 Hz to 50 MHz</td><td colspan="2">PXI_TRIG7†
RTSI 7‡
NI 6535/6535B: 0 Hz to 10 MHz
NI 6536/6536B and NI 6537/6537B: 0 Hz to 25 MHz</td><td>—</td></tr>
<tr><td>Minimum detectable imported timebase clock pulse width</td><td colspan="2">PFI <4..5>
PXIe_DSTARB†
6.5 ns</td><td colspan="2">PXI_TRIG7†
RTSI 7‡
15 ns</td><td>Positive and negative pulse width at voltage thresholds.</td></tr>
<tr><td>Exported Sample clock destinations</td><td colspan="2">Generation
1. PFI 4
2. RTSI 7† PXI_TRIG7‡
3. PXIe_DSTARC†</td><td colspan="2">Acquisition
PFI 5</td><td>—</td></tr>
<tr><td>Exported Sample clock duty cycle</td><td colspan="4">Internal Sample clock or divided-down timebase: 33% to 67%
Imported Sample clock: Limited by input duty cycle</td><td>Nominal.</td></tr>
<tr><td colspan="5">† PXI Express only
‡ PCI Express only</td></tr>
</table>

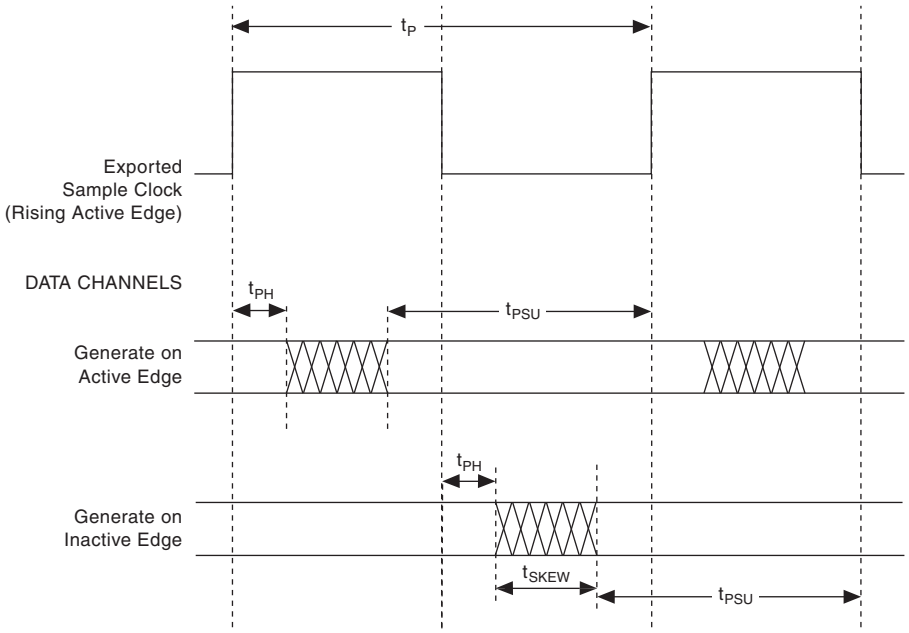
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Pattern Generation Timing (Data and PFI 4 Channels)

Specification	Value		Comments
Maximum data channel toggle rate	**NI 6535/6535B**: 5.0 MHz **NI 6536/6536B**: 12.5 MHz **NI 6537/6537B**: 25.0 MHz		—
Data position modes	**Data Channels**	**PFI Channels**	Relative to Sample clock; Active edge may be rising or falling.
	Active edge, Inactive edge	Active edge	
Minimum provided hold time with respect to PFI 4 (t_{PH})	**PXI Express**	**PCI Express**	t_P is the Sample clock interval; values assume the sample is generated and acquired on the same clock edge; includes maximum channel-to-channel skew; valid for all data.
	750 ps	1.1 ns	
Minimum provided setup time with respect to PFI 4 (t_{PSU})	Sample clock interval (t_P) - 5.35 ns	Sample clock interval (t_P) - 5 ns	

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Figure 1. Provided Setup and Hold Times



$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{PH} = Minimum Provided Hold Time

t_{PSU} = Minimum Provided Setup Time

t_{SKEW} = Maximum Channel-to-Channel Skew and Clock Uncertainty

Note Provided setup and hold times include channel-to-channel skew and jitter.

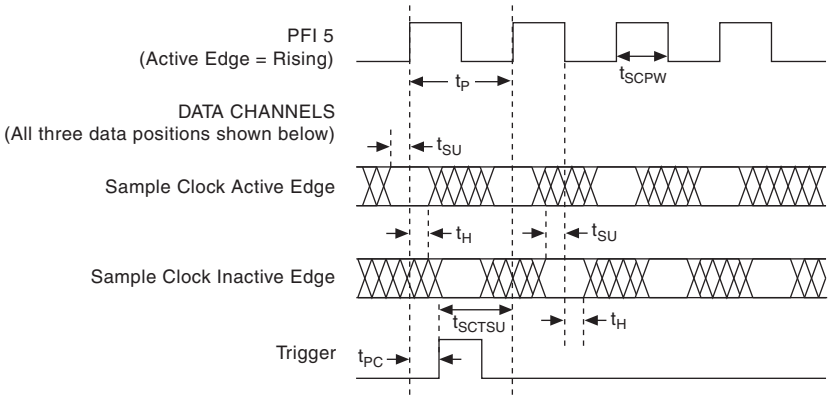
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Pattern Acquisition Timing (Data and PFI 5 Channels)

Specification	Value	Comments
Setup time with respect to PFI 5 (t_{SU})	**NI 6535/6536/6537 Rev C* or later** and **NI 6535B/6536B/6537B**: 2.8 ns **NI PCIe-6535/6536/6537 Rev B***: 2.0 ns	Includes maximum data channel-to-channel skew; valid for data and all triggers except the Start trigger when using the Sample Clock sample timing type. * Refer to assembly number sticker on device for revision information
Hold time with respect to PFI 5 (t_H)	**NI 6535/6536/6537 Rev C* or later** and **NI 6535B/6536B/6537B**: 1.5 ns **NI PCIe-6535/6536/6537 Rev B*:** 2.0 ns	
Setup time of triggers with respect to PFI 5 (t_{SCTSU})	15 ns	Nominal.
Trigger delay from PFI 5 to trigger edge (t_{PC})	9 ns	Nominal.

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Figure 2. Acquisition Timing Diagram Using PFI 5 as the Sample Clock



t_{SU} = Setup Time with Respect to PFI 5

t_H = Hold Time with Respect to PFI 5

$t_P = \frac{1}{f}$ = Sample Clock Period

t_{SCPW} = Minimum Detectable Sample Clock Pulse Width

t_{PC} = Trigger Delay from PFI 5 to Trigger Edge*

t_{SCTSU} = Setup Time of Trigger with Respect to PFI 5*

*Sample Clock Sample Timing Type only.

Handshaking

Specification	Value	Comments
Asynchronous handshaking modes	Handshake (8255) sample timing type	8255 emulation equivalent.
Synchronous handshaking modes	1. Burst sample timing type 2. Pipelined Sample Clock sample timing type	—
Control line polarity	1. Active high 2. Active low	—
Programmable delay resolution for Handshake sample timing type	20 ns	—

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Change Detection

Specification	Value	Comments
Change detection resolution	Sample clock period	—
Sources	P0.<0..7>, P1.<0..7>, P2.<0..7>, P3.<0..7>	Per data channel selectable.
Valid sample position	1. Active edge 2. Inactive edge	
Valid changes	1. Don't care 2. Rising edge 3. Falling edge 4. Rising or falling edge	

Waveform Specifications

Memory

Specification	Value	Comments
Onboard memory size	2,048 samples (S)	First-in first-out based, regardless of port size.
Transfer type	1. DMA 2. Programmed I/O (On Demand sample timing type only)	—
Generation waveform quantum	Waveform size must be an integer multiple of 1 S.	—
Acquisition minimum buffer size	2 S	—

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Triggers

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td>Supported triggers (by sample timing type)</td><td>Sample Timing Type</td><td>Acquisition</td><td>Generation</td><td rowspan="6">Generation operations do not support pattern match triggers.</td></tr>
<tr><td>Sample Clock</td><td>Start, Reference</td><td>Start</td></tr>
<tr><td>Pipelined Sample Clock</td><td>Pause, Start, Reference</td><td>Pause, Start</td></tr>
<tr><td>Burst Handshake</td><td>Pause (not including the pattern match type trigger)</td><td>Pause</td></tr>
<tr><td>Handshake</td><td>Handshake</td><td>Handshake</td></tr>
<tr><td>Change Detection</td><td>Start</td><td>N/A</td></tr>
<tr><td>Sources</td><td colspan="3">1. PFI <0..5> (DDC connector)
2. PXI_TRIG<0..6> (PXI backplane)†
RTSI <0..7> (RTSI bus)‡
3. PXIe_DSTARB (PXI backplane)†
4. Pattern match (Acquisition sessions only)
5. Disabled (Do not wait for a trigger)</td><td>—</td></tr>
<tr><td>Trigger detection</td><td colspan="3">1. Start Trigger (Edge detection: rising or falling; Pattern match: match or does not match)
2. Pause Trigger (Level detection: high or low; Pattern match: match or does not match)
3. Reference Trigger (Edge detection: rising or falling; Pattern match: match or does not match)
4. Handshaking Trigger (Interlocked: high or low)</td><td>—</td></tr>
<tr><td>Destinations</td><td colspan="3">1. PFI <0..5> (DDC Connector)
2. PXI_TRIG<0..7> (PXI backplane)†
RTSI <0..7> (RTSI bus)
3. PXIe_DSTARC (PXI backplane)†</td><td>—</td></tr>
</table>

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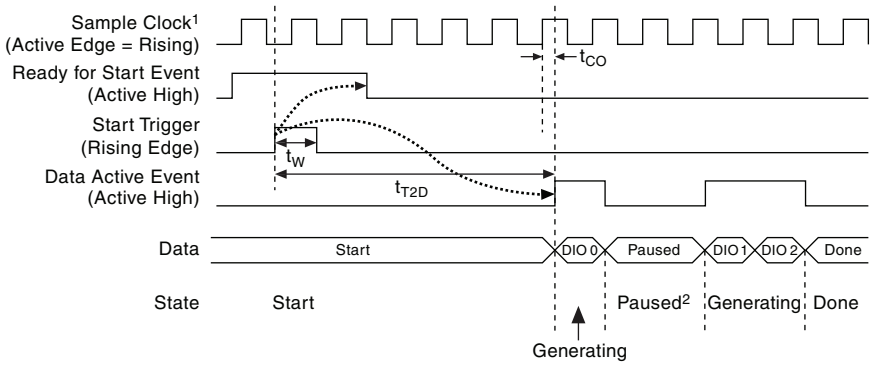
<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td rowspan="3">Delay from Pause trigger to Paused state (t_{P2S})</td><td colspan="2">Generation</td><td rowspan="2">Acquisition</td><td rowspan="3">Use the Data Active event during generation operations to determine on a sample-by-sample basis when the NI device has entered the Paused state. Pause trigger only supported by Pipelined Sample Clock sample timing type.</td></tr>
<tr><td>Minimum</td><td>Maximum</td></tr>
<tr><td>6 Sample clock cycles + 6.7 ns</td><td>NI PCIe-6535/6536/6537: 7 Sample clock cycles + 15.4 ns
NI PXIe-6535/6536/6537: 7 Sample clock cycles + 17 ns
NI 6535B/6536B/6537B: 7 Sample clock cycles + 65 ns</td><td>Synchronous to the data</td></tr>
<tr><td colspan="5">† PXI Express only
‡ PCI Express only</td></tr>
<tr><td rowspan="3">Delay from trigger to digital data output (t_{T2D})</td><td colspan="2">Generation</td><td rowspan="2">Acquisition</td><td rowspan="3">Nominal.</td></tr>
<tr><td>Minimum</td><td>Maximum</td></tr>
<tr><td>65 ns</td><td>NI 6535/6536/6537: 1 Sample clock cycle + 130 ns
NI 6535B/6536B/6537B: 1 Sample clock cycle + 150 ns</td><td>N/A</td></tr>
<tr><td rowspan="2">Minimum detectable trigger pulse width (t_W)</td><td colspan="2">Sample Clock Sample Timing Type Triggers and Pipelined Sample Timing Type Generation Start Trigger</td><td>Burst and Pipelined Sample Timing Type Generation Pause Trigger</td><td>Nominal.
Maximum required pulse width to guarantee sampling by an asynchronous clock; synchronous triggers have same setup and hold requirements as data.</td></tr>
<tr><td colspan="2">10 ns</td><td>Sample clock period + 4 ns</td></tr>
</table>

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Specification	Value	Comments
Maximum required setup and hold of Sample Clock sample timing type triggers with respect to PFI 5	Refer to the *Pattern Acquisition Timing (Data and PFI 5 Channels)* section of this document.	—
Maximum required delay from data to Handshake trigger (t_{DT})	5 ns	Nominal. Maximum required time between data valid and the Handshake trigger; Handshake sample timing type only.
Maximum required delay from Handshake trigger to data (t_{TD})	50 ns	Nominal. Maximum required time between the Handshake Trigger and data invalid; Handshake sample timing type only.

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Figure 3. Pipelined Generation Timing Diagram



[1] Must be free-running.

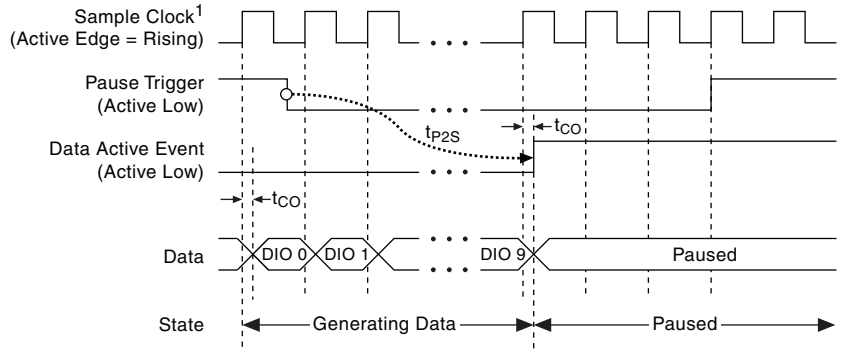
[2] Generation pauses if the DAQmx Underflow property/attribute is set to Pause Until Data Available or Pause Trigger Received.

t_W = Minimum detectable trigger pulse width.

t_{CO} = Exported Sample clock offset.

t_{T2D} = Delay from trigger to digital data out.

Figure 4. Pipelined Generation Handshaking Timing Diagram



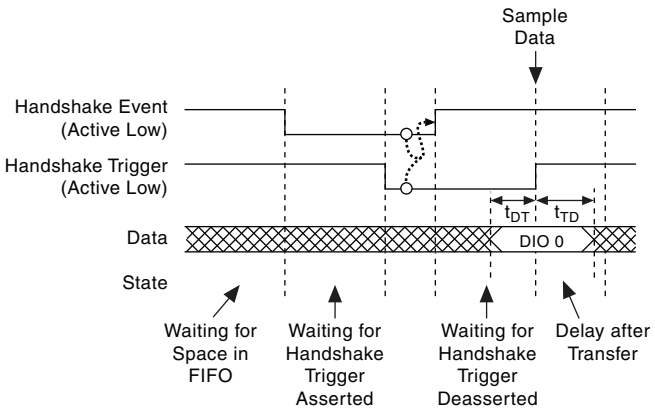
[1] Must be free-running.

t_{P2S} = Pause trigger to Paused state.

t_{CO} = Exported Sample clock offset.

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Figure 5. Handshake (8255) Acquisition Timing Diagram



t_{DT} = Maximum required delay from data valid to trigger.
t_{TD} = Maximum required delay from trigger to data invalid.

Events

Specification	Value			Comments
Supported events (by sample timing type)	**Sample Timing Type**	**Acquisition**	**Generation**	—
	Sample Clock	Ready for Start	Ready for Start, Data Active	
	Pipelined Sample Clock	Ready for Transfer, Ready for Start	Ready for Start, Data Active	
	Burst Handshake	Ready for Transfer	Ready for Transfer	
	Handshake	Handshake	Handshake	
	Change Detection	Change Detection, Ready for Start	N/A	
Destinations	1. PFI <0..5> (DDC Connector) 2. PXI_TRIG<0..7> (PXI backplane)† RTSI <0..7> (RTSI bus)‡ 3. PXIe_DSTARC (PXI backplane)†			—

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Specification	Value		Comments
Pulse width for the exported Change Detection event	**Frequency ≤ 10 MHz**	**Frequency > 10 MHz***	Software determined based on Sample clock frequency. * Frequency >10 MHz does not apply for NI 6535/6535B.
	50 ns	15 ns	
† PXI Express only ‡ PCI Express only			
Delay from Change Detect to event	**Minimum**	**Maximum**	Nominal. Delay from data at the DDC connector to the event generated on the DDC connector.
	90 ns	**NI PCIe-6535/6536/6537**: 1 Sample clock cycle + 100 ns **NI PXIe-6535/6536/6537**: 1 Sample clock cycle + 105 ns **NI 6535B/6536B/6537B**: 1 Sample clock cycle + 120 ns	

Nonvolatile Storage

Specification	Value	Comments
Description	16 Mbit storage for firmware and power up states	—
Write Cycles	75,000 minimum	—

Power

Specification	Value		Comments
	NI 6535/6536/6537	**NI 6535B/6536B/6537B**	Maximum. Into high-impedance loads.
+3.3 VDC	750 mA	1 A	
+12 VDC	300 mA	225 mA	
Total power	6.1 W	6 W	

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Physical Specifications

Specification	Value		Comments
Dimensions	**PXI Express**	**PCI Express**	—
	21.4 cm × 2.0 cm × 13.1 cm (8.42 in. × 0.79 in. × 5.14 in.)	18.1 cm × 2.2 cm × 12.6 cm (7.13 in. × 0.85 in. × 4.93 in.)	
Weight	144.58 g (5.1 oz)	107.7 g (3.8 oz)	—

Software

Specification	Value	Comments
Driver software	**NI 6535**: NI-DAQmx driver software version 8.8 or later **NI 6536/6537**: NI-DAQmx driver software version 8.5 or later **NI 6535B/6536B/6537B**: NI DAQmx driver software version 9.6.1 or later	—
Application software	NI-DAQmx provides programming interfaces for the following application development environments (ADEs): • National Instruments LabVIEW • National Instruments LabWindows™/CVI™ • Microsoft Visual Studio	Refer to the *NI-DAQ Readme* for more information about supported ADE versions.
Test Panel	National Instruments Measurement & Automation Explorer (MAX) provides test panels with basic acquisition and generation functionality for the NI 6535/6536/6537 and NI 6535B/6536B/6537B. MAX is included on the NI-DAQmx instrument driver media.	—

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Environment

Note The NI 6535/6536/6537 and NI 6535B/6536B/6537B are intended for indoor use only.

Specification	Value	Comments
Operating temperature	**PCI Express**: 0 ºC to +45 ºC **PXI Express**: 0 ºC to +55 ºC	—
Storage temperature	-20 ºC to +70 ºC	—
Operating relative humidity	10% to 90% relative humidity, noncondensing (Meets IEC 60068-2-56.)	—
Storage relative humidity	5% to 95% relative humidity, noncondensing (Meets IEC 60068-2-56.)	—
Operating shock	30 g, half-sine, 11 ms pulse (Meets IEC 60068-2-27. Test profile developed in accordance with MIL PRF-28800F.)	**PXI Express** only
Storage shock	50 g, half-sine, 11 ms pulse (Meets IEC 60068-2-27. Test profile developed in accordance with MIL PRF-28800F.)	
Operating vibration	5 Hz to 500 Hz, 0.31 g_{rms} (Meets IEC 60068-2-64.)	
Storage vibration	5 Hz to 500 Hz, 2.46 g_{rms} (Meets IEC 60068-2-64. Test profile exceeds requirements of MIL PRF-28800F, Class B.)	
Altitude	0 m to 2,000 m above sea level (at 25 ºC ambient temperature)	—
Pollution Degree	2	—

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Safety, Electromagnetic Compatibility, and CE Compliance

Caution The protection provided by this equipment may be impaired if it is used in a manner not described in this document.

Specification	Value	Comments
Safety	This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use: • IEC 61010-1, EN 61010-1 • UL 61010-1, CSA 61010-1	—
Note: For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.		
Electromagnetic Compatibility	This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use: • EN 61326 (IEC 61326): Class A emissions; Basic immunity • EN 55011 (CISPR 11): Group 1, Class A emissions • AS/NZS CISPR 11: Group 1, Class A emissions • FCC 47 CFR Part 15B: Class A emissions • ICES-001: Class A emissions	With use of SHC68-C68-D2 or SHC68-C68-D4 shielded cable.
Note: For the standards applied to access the EMC of this product, refer to the *Online Product Certification* section. **Note**: For EMC compliance, device *must* be operated with shielded cabling. In addition, filler panels must be installed.		
CE Compliance CE	This product meets the essential requirements of applicable European Directives as follows: • 2006/95/EC; Low-Voltage Directive (safety) • 2004/108/EC; Electromagnetic Compatibility Directive (EMC)	—
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