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Find the *National Instruments PXIe-6548* at our website: *Click HERE*

SPECIFICATIONS

PXIe-6548

200 MHz Digital Waveform Generator/Analyzer

This document provides the specifications for the PXIe-6548.



Hot Surface If the PXIe-6548 has been in use, it may exceed safe handling temperatures and cause burns. Allow the PXIe-6548 to cool before removing it from the chassis.



Note All values were obtained using a 1 m cable (SHC68-C68-D4 recommended). Performance specifications are not guaranteed when using longer cables.

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Definitions and Conditions

Specifications are valid for the range 0 °C to 55 °C unless otherwise noted.

Maximum and *minimum* specifications are warranted not to exceed these values within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

Typical specifications are unwarranted values that are representative of a majority (3σ) of units within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

Characteristic specifications are unwarranted values that are representative of an average unit operating at room temperature.

Nominal specifications are unwarranted values that are relevant to the use of the product and convey the expected performance of the product.

All specifications are Typical unless otherwise noted.

Channels

Data	
Number of channels	
SDR selected (data clocked using Sample clock rising or falling edge)	32
DDR selected (data clock using both Sample clock edges)[1]	16 per direction
Extended data mode selected[2]	24
Direction control	Per channel Per cycle

[1] Generation and acquisition sessions may be independently configured for DDR operation on either the lower data channels (<0..15>) or the upper data channels (<16..31>).

[2] Used for hardware comparison and cycle-to-cycle tristate operations.

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Time to tristate (t_{PZ}), 2 kΩ and 15 pF load	6.2 ns, nominal
Programmable Function Interface (PFI)	
Number of channels	4
Direction control	Per channel
Clock terminals	
Input	2
Output	2

Related Information

Triggers on page 22
Events on page 24
CLK IN on page 17
CLK OUT on page 19

Generation Channels

Channels	Data DDC CLK OUT PFI <0..3>
Generation signal type	Single-ended
Generation voltage features, all Data, PFI, and clock channels	
Number of programmable generation voltage levels	1 voltage high level (V_{OH}) Generation voltage low level (V_{OL}) is always set to 0 V
Range	1.2 V to 3.3 V
Resolution	100 mV
DC generation voltage accuracy[3]	±35 mV, typical ±200 mV, maximum

[3] Into 1 MΩ; does not include system crosstalk.

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Table 1. Generation Voltage Levels

Logic Family[4]	Voltage Low Level (V_{OL})		Voltage High Level (V_{OH})		Accuracy for Nominal Values into 1 MΩ Load
	Nominal	Max	Min	Nominal	
1.2 V (V_{OH} = 1.2 V)	0.0 V	0.2 V	1 V	1.2 V	±35 mV, typical
1.5 V (V_{OH} = 1.5 V)			1.3 V	1.5 V	
1.8 V (V_{OH} = 1.8 V)			1.6 V	1.8 V	
2.5 V (V_{OH} = 2.5 V)			2.3 V	2.5 V	
3.3 V (V_{OH} = 3.3 V)			3.1 V	3.3 V	

Note Generation and acquisition sessions share a common voltage resource. Simultaneous operations must be set to the same logic family.

Output impedance	50 Ω, nominal
Maximum allowed DC drive strength per channel, by logic family	
1.2 V	±12 mA, nominal
1.5 V	±15 mA, nominal
1.8 V	±18 mA, nominal
2.5 V	±25 mA, nominal
3.3 V	±33 mA, nominal
Data channel driver enable/disable control	Software-selectable: per channel
Channel power-on state	Drivers disabled, 50 kΩ nominal input impedance

[4] For all data, PFI, and clock channels. Does not include system crosstalk.

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Output protection	
Range	0 V to 5 V
Duration	Indefinite

Related Information

CLK OUT on page 19
DDC CLK OUT on page 20

Acquisition Channels

Channels	Data STROBE PFI <0..3>
Acquisition signal type	Single-ended
Acquisition threshold features, all Data, PFI, and clock channels	
Number of programmable acquisition thresholds	1 ($V_{IH} = V_{IL}$)
Range	0.6 V to 1.65 V
Resolution	50 mV
Accuracy[5]	±150 mV, typical ±30%, maximum

Table 2. Acquisition Voltage Threshold Accuracy

Logic Family[6]	Voltage Thresholds Low (V_{IL})		Voltage Thresholds High (V_{IH})	
	Minimum	Typical	Typical	Maximum
1.2 V (V_{IH}, V_{IL} = 0.60 V)	420 mV	450 mV	750 mV	780 mV
1.5 V (V_{IH}, V_{IL} = 0.75 V)	525 mV	600 mV	900 mV	975 mV
1.8 V (V_{IH}, V_{IL} = 0.90 V)	630 mV	750 mV	1.05 V	1.17 V

[5] Does not include system crosstalk.
[6] For all data, PFI, and clock channels. Does not include system crosstalk.

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Table 2. Acquisition Voltage Threshold Accuracy (Continued)

Logic Family[6]	Voltage Thresholds Low (V_{IL})		Voltage Thresholds High (V_{IH})	
	Minimum	Typical	Typical	Maximum
2.5 V (V_{IH}, V_{IL} = 1.25 V)	875 mV	1.10 V	1.40 V	1.625 V
3.3 V (V_{IH}, V_{IL} = 1.65 V)	1.155 V	1.50 V	1.80 V	2.145 V

Note Generation and acquisition sessions share a common voltage resource. Simultaneous operations must be set to the same logic family.

Input impedance	High-impedance (50 kΩ), nominal
Input protection[7]	-1 V to 5 V

Timing

Sample Clock

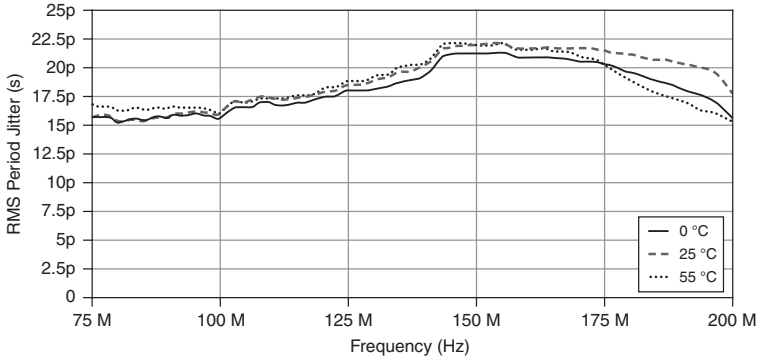
Sources	1. On Board clock (internal 800 MHz VCO with 32-bit DDS) 2. CLK IN (SMA jack connector) 3. STROBE (Digital Data & Control [DDC] connector; acquisition only)
Frequency range	
On Board clock	100 Hz to 200 MHz
CLK IN	20 kHz to 200 MHz
STROBE	100 Hz to 200 MHz
On Board clock characteristics	
Resolution[8]	0.2 Hz, maximum
Accuracy[9]	±150 ppm + 5 ppm per year

6 For all data, PFI, and clock channels. Does not include system crosstalk.
7 Internal diode clamps may begin conduction outside the -0.5 V to 3.5 V range.
8 Varies with Sample clock frequency. You can query NI-HSDIO for the programmed frequency value.
9 Accuracy may be increased by using a higher-performance external Reference clock.

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On Board clock characteristics valid only when PLL reference source is set to None	
Frequency accuracy	±150 ppm (including temperature effects), typical
Aging	±5 ppm first year, nominal
Sample clock relative delay adjustment[10]	
Range	
Acquisition sessions	0.0 to 1.0 Sample clock periods
Generation sessions	0.0 ns to 5.0 ns
Resolution	0.5 ps
Exported Sample clock destinations	DDC CLK OUT (DDC connector) CLK OUT (SMA jack connector)
Exported Sample clock delay	
Range	0.0 to 1.0 Sample clock periods
Resolution (δ_C)[11]	117 ps to 143 ps, nominal
Frequency	
On Board clock	All supported frequencies
External clock	Frequencies ≥20 MHz
Exported Sample clock jitter, using On Board clock	
Period	24 ps_{rms}, characteristic
Cycle-to-cycle	43 ps_{rms}, characteristic

Figure 1. Characteristic Period Jitter (RMS) vs. Frequency



[10] You can apply a delay or phase adjustment to the On Board clock to align multiple devices.

[11] Resolution is nonlinearly dependent on clock frequency. You can query clock frequency using NI-HSDIO.

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Table 3. Exported Sample Clock Duty Cycle

Logic Family	DDC Clock Out[12]	
	Minimum	Maximum
1.2 V	37%	50%
1.5 V	41%	53%
1.8 V	42%	55%
2.5 V	45%	57%
3.3 V	48%	58%

Related Information

CLK IN on page 17
STROBE on page 19

Generation Timing

Channels	Data DDC CLK OUT PFI <0..3>
Data channel-to-channel skew[13]	±300 ps, maximum

Table 4. Maximum Data Rate by Logic Family[14]

Logic Family	SDR	DDR[15]
3.3 V	200 Mbps	400 Mbps
2.5 V		400 Mbps
1.8 V		375 Mbps
1.5 V		350 Mbps
1.2 V		300 Mbps

[12] Does not include the effects of system crosstalk.
[13] Maximum skew across all data channels, PFI channels, and voltage levels when using the same data position or data delay bank.
[14] Includes maximum data channel-to-channel skew and typical crosstalk.
[15] Generates two samples per clock cycle in DDR mode.

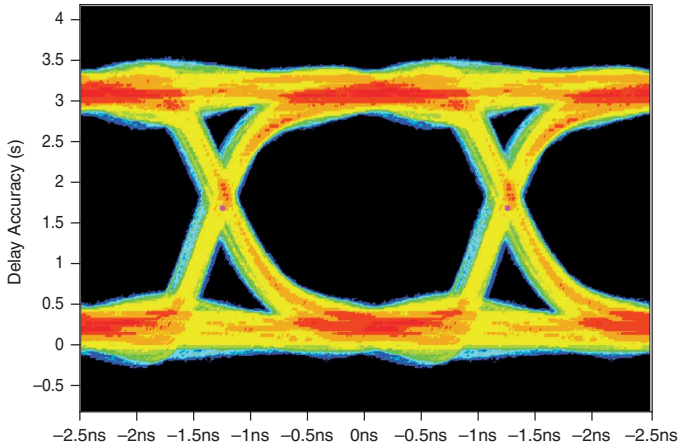
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Table 5. Maximum Data Rate by Voltage Level[14]

Voltage Levels	SDR	DDR[16]
2.5 V to 3.3 V	200 Mbps	400 Mbps
1.8 V to 2.4 V		375 Mbps
1.5 V to 1.7 V		350 Mbps
1.2 V to 1.4 V		300 Mbps

The following figure shows an eye diagram of a 400 Mbps pseudorandom bit sequence (PRBS) waveform in DDR mode at 3.3 V. This waveform was captured on DIO 0 at room temperature into high impedance.

Figure 2. Characteristic Eye Diagram (High Impedance)

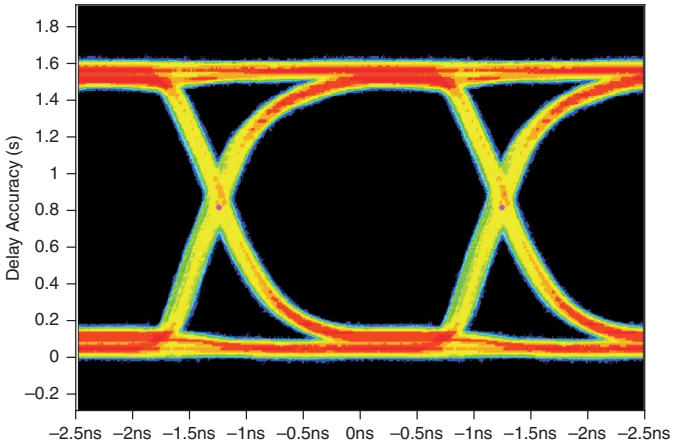


The following figure shows an eye diagram of a 400 Mbps PRBS waveform in DDR mode at 3.3 V. This waveform was captured on DIO 0 at room temperature into 50 Ω termination.

[16] Generates two samples per clock cycle in DDR mode.

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Figure 3. Characteristic Eye Diagram (50 Ω Termination, Characteristic)



Data position modes	Sample clock rising edge Sample clock falling edge Delay from Sample clock rising edge
Data delay banks	
Bank 0	DIO <0..3> DIO <16..19> DIO <28..31> PFI <0..3>
Bank 1	DIO <4..7> DIO <20..23>
Bank 2	DIO <8..15> DIO <24..27>

Note Multibank data delay was first available in NI-HSDIO 1.7.

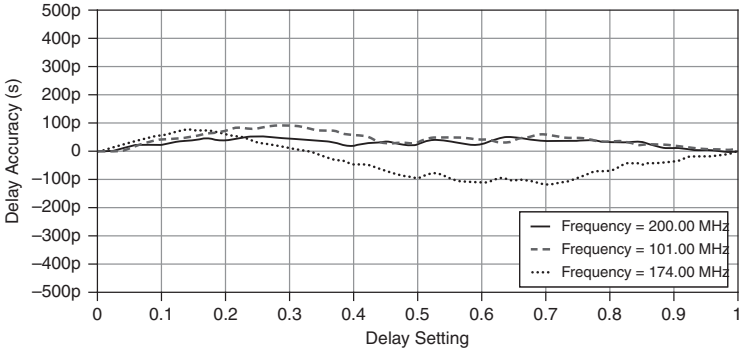
Generation data delay	
Range (δ_G)	0.0 to 1.0 Sample clock periods
Resolution (δ_G)[17]	117 ps to 143 ps, nominal

[17] Resolution is nonlinearly dependent on clock frequency. You can query resolution using NI-HSDIO.

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Generation data delay frequency	
On Board clock	All supported frequencies
External clock	Frequencies ≥20 MHz

Figure 4. Characteristic Data Delay Accuracy



Exported Sample clock offset (t_{CO})[18]	0.0 ns or 1.65 ns (default), nominal
Time delay from On Board Sample clock to DDC connector (t_{SCDDC})	8.1 ns, characteristic; exported Sample clock offset = 0 ns

Generation Provided Setup and Hold Times

Compare the setup and hold times from the datasheet of your device under test (DUT) to the values in the table. The provided setup and hold times must be greater than the setup and hold times required for the DUT. If you require more setup time, configure your exported Sample clock mode to Inverted and/or delay your clock or data relative to the Sample clock. This table includes worst-case effects of channel-to-channel skew and intersymbol interference.

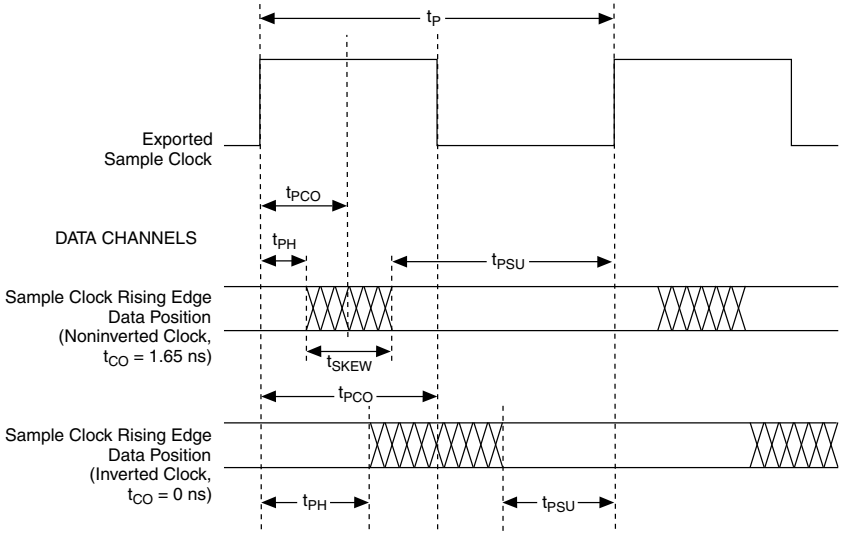
Exported Sample Clock Offset (t_{PCO})	Minimum Provided Setup Time (t_{PSU})	Minimum Provided Hold Time (t_{PH})
1.65 ns	t_p - 2.15 ns	1.15 ns
0.0 ns	t_p - 500 ps	-500 ps

Note This table assumes the data position is set to Sample clock rising edge and the noninverted Sample Clock is exported to the DDC connector.

[18] Software-selectable for DDC_CLK_ OUT.

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Figure 5. Generation Provided Setup and Hold Times Timing Diagram



$t_P = \frac{1}{f}$ = Sample Clock Period

t_{PH} = Minimum Provided Hold Time

t_{PSU} = Minimum Provided Set-Up Time

t_{PCO} =Time from Rising Clock Edge to Data Transition (Provided Clock to Out Time)

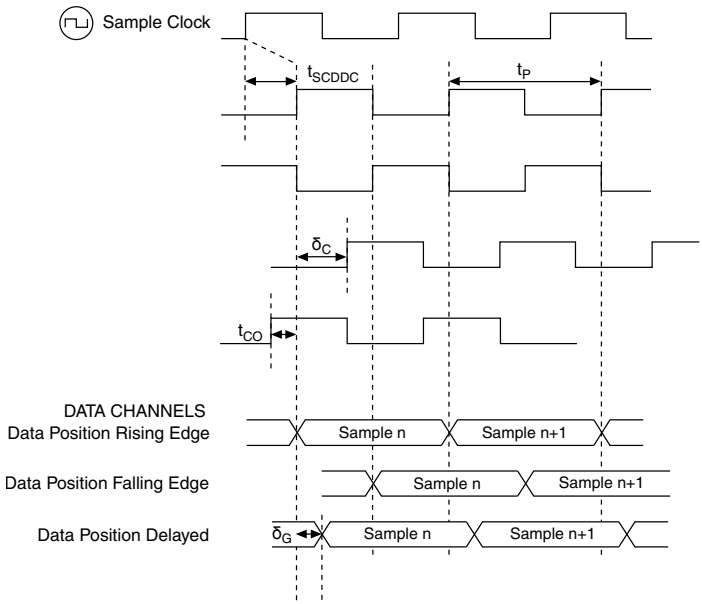
t_{CO} = Exported Sample Clock Offset

t_{SKEW} = Maximum Channel-to-Channel Skew and Clock Uncertainty

Note Provided setup and hold times account for maximum channel-to-channel skew and jitter.

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Figure 6. Generation Timing Diagram



t_{SCDDC} : Time Delay from Sample Clock (Internal) to DDC Connector

$0 \le \delta_C \le 1$: Exported Sample Clock Delay (Fraction of t_P)

$0 \le \delta_G \le 1$: Pattern Generation Data Delay (Fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{CO} = Exported Sample Clock Offset; 1.65 ns, Software-Selectable

Acquisition Timing

Channels	Data STROBE PFI <0..3>
Channel-to-channel skew[19]	±350 ps

[19] Maximum skew across all data channels, PFI channels, and voltage levels when using the same data position or data delay bank.

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Table 6. Maximum Data Rate Per Channel by Logic Family[20]

Logic Family	SDR	DDR[21]
3.3 V	200 Mbps	300 Mbps
2.5 V		300 Mbps
1.8 V		250 Mbps
1.5 V		225 Mbps
1.2 V		200 Mbps

Table 7. Maximum Data Rate Per Channel by Voltage Threshold[20]

Voltage Threshold	SDR	DDR[21]
1.25 V to 1.65 V	200 Mbps	300 Mbps
0.90 V to 1.20 V		250 Mbps
0.75 V to 0.85 V		225 Mbps
0.60 V to 0.70 V		200 Mbps

Data position modes	Sample clock rising edge Sample clock falling edge Delay from Sample clock rising edge

[20] Includes maximum data channel-to-channel skew and typical crosstalk.
[21] Acquires two samples per clock cycle in DDR mode.

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Table 8. Setup and Hold Times to STROBE, Characteristic[22]

Voltage Threshold	Setup Times (t_{sus})		Hold Time (t_{hs})	
	f <20 MHz	f ≥20 MHz	f <20 MHz	f ≥20 MHz
1.25 V to 1.65 V	2.8 ns	1.15 ns	2.4 ns	900 ps
0.90 V to 1.20 V		1.20 ns		1.00 ns
0.75 V to 0.85 V		1.40 ns		1.10 ns
0.60 V to 0.70 V		1.75 ns		1.25 ns

Setup and hold times to Sample clock[23]	
Setup time (t_{susc})	900 ps, nominal
Hold time (t_{HSC})	425 ps, nominal
Data delay banks[24]	
Bank 0	DIO <0..3> DIO <16..19> DIO <28..31> PFI <0..3>
Bank 1	DIO <4..7> DIO <20..23>
Bank 2	DIO <8..15> DIO <24..27>
Time delay from DDC connector to internal Sample clock	6.8 ns, nominal
Acquisition data delay	
Frequency	
On Board clock	All supported frequencies
External clock and STROBE	Frequencies ≥20 MHz
Range	0.0 to 1.0 Sample clock periods
Resolution[25]	117 ps to 143 ps, nominal

22 Includes maximum data channel-to-channel skew and uncertainty, but does not include system crosstalk. Performance may vary with system crosstalk performance.

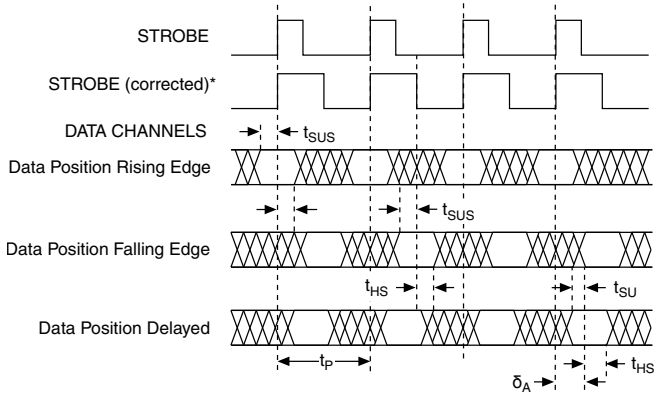
23 Does not include channel-to-channel skew, t_{DDCSC}, or t_{SCDDC}

24 Multibank data delay was first made available NI-HSDIO 1.7.

25 Resolution is nonlinearly dependent on clock frequency. You can query resolution using NI-HSDIO.

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Figure 7. Acquisition Timing Diagram Using STROBE as the Sample Clock



t_{SUS} = Set-Up Time to STROBE

t_{HS} = Hold Time from STROBE

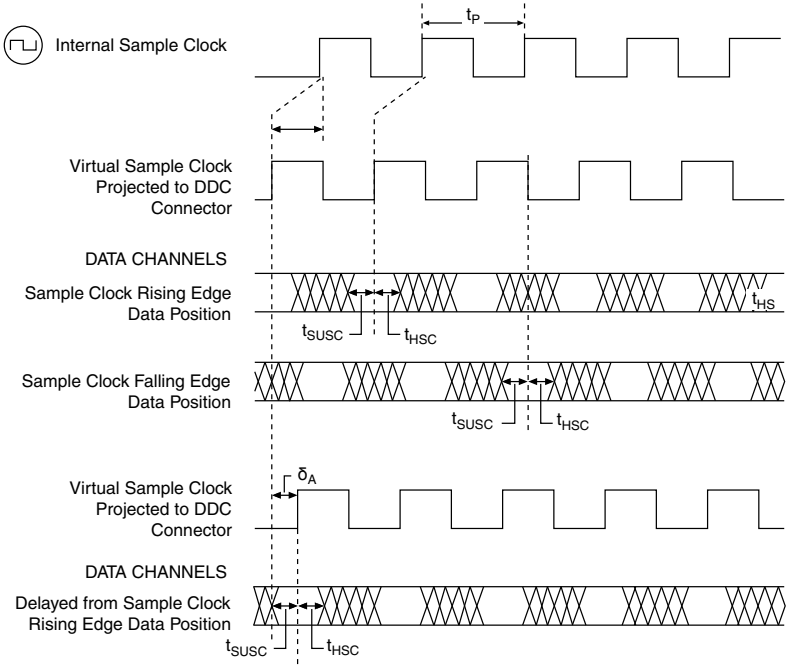
$0 \le \delta_A \le 1$: Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Sample Clock Period

*Note: When using an external Sample clock greater than 20 MHz, the duty cycle is corrected to 50%.

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Figure 8. Acquisition Timing Diagram with Sample Clock Sources Other than STROBE



t_{DDCSC} : Time Delay from DDC Connector to Internal Sample Clock

$0 \le \delta_A \le 1$: Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{SUSC} = Set-Up Time to Sample Clock

t_{HSC} = Hold Time to Sample Clock

Related Information

STROBE on page 19

CLK IN

Connector	SMA jack
Direction	Input
Destinations	1. Reference clock (PLL) 2. Sample clock
Input coupling	AC
Input protection	±10 VDC, nominal

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Input impedance	Software-selectable: 50 Ω (default) or 1 kΩ, nominal
Minimum detectable pulse width	2 ns, nominal
Clock requirements	Free-running (continuous) clock

Waveform Voltage Ranges

Square wave voltage range	0.65 V_{pk-pk} to 5.0 V_{pk-pk}

Table 9. Sine Wave Voltage Ranges

Voltage Range (V_{pk-pk})	Frequency Range
0.65 to 5.0	20 MHz to 200 MHz
1.0 to 5.0	13 MHz to 200 MHz
1.3 to 5.0	10 MHz to 200 MHz
2.6 to 5.0	5 MHz to 200 MHz

CLK IN Implementations

As Sample clock[26]	
Frequency range	20 kHz to 200 MHz
Duty cycle range	
f <20 MHz	25% to 75%
f ≥20 MHz	40% to 60%
As Reference clock	
Frequency range	5 MHz to 100 MHz (integer multiples of 1 MHz)
Frequency accuracy[27]	±0.1%
Duty cycle range	25% to 75%

Related Information

Channels on page 2
Sample Clock on page 6

[26] Nominal 3 dB cutoff point at 100 MHz when using 1 kΩ input impedance.
[27] Required accuracy of the external Reference clock source.

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STROBE

Connector	DDC
Direction	Input
Destination	Sample clock (acquisition only)
Frequency range	100 Hz to 200 MHz
Duty cycle range (at the programmed threshold)	
f <20 MHz	25% to 75%
f ≥20 MHz	40% to 60% (corrected to 50%)
Minimum detectable pulse width[28]	2 ns, nominal
Clock requirements	Free-running (continuous) clock
Input impedance	50 kΩ, nominal

Related Information

Acquisition Timing on page 13
Sample Clock on page 6

CLK OUT

Connector	SMA jack
Direction	Output
Sources	1. Sample clock (excluding STROBE) 2. Reference clock (PLL)
Output impedance	50 Ω, nominal
Logic type	Matched with generation and acquisition sessions

Related Information

Channels on page 2
Generation Channels on page 3

[28] Required at acquisition voltage thresholds.

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DDC CLK OUT

Connector	DDC
Direction	Output
Source	Sample clock (generation only)

Note STROBE and acquisition Sample clock cannot be routed to DDC CLK OUT.

Related Information

Generation Channels on page 3

Reference Clock (PLL)

Sources[29]	1. PXI_CLK100 (PXI Express backplane) 2. CLK IN (SMA jack connector) 3. None (internal oscillator locked to an internal reference)
Destination	CLK OUT (SMA jack connector)
Lock time	150 ms, maximum (not including software latency)
Frequency range	5 MHz to 100 MHz (integer multiples of 1 MHz), 0.1% required accuracy
Duty cycle range	25% to 75%

Waveform

Memory and Scripting

Memory architecture	This device uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters such as number of script instructions, maximum number of waveforms in memory, and number of samples (S) available for waveform storage are flexible and user defined.

[29] Provides the frequency for the PLL.

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Onboard memory size[30]	
1 Mbit per channel	
Acquisition	1 Mbit per channel (4 MBytes total)
Generation	1 Mbit per channel (4 MBytes total)
8 Mbit per channel	
Acquisition	8 Mbit per channel (32 MBytes total)
Generation	8 Mbit per channel (32 MBytes total)
64 Mbit per channel	
Acquisition	64 Mbit per channel (256 MBytes total)
Generation	64 Mbit per channel (256 MBytes total)
Generation	
Single-waveform mode	Generates a single waveform once, *n* times, or continuously
Scripted mode[31]	Generates a simple or complex sequence of waveforms.
Finite repeat count	1 to 16,777,216
Waveform quantum[32]	
Data width = 4	1 sample
Data width = 2	2 samples
Waveform block size (in physical memory)	
Data width = 4	32 samples
Data width = 2	64 samples

Table 10. Generation Minimum Waveform Size[33]

Configuration	Sample Rate	
	200 MHz	100 MHz
Single waveform	1 S	1 S
Continuous waveform	128 S	64 S

30 Maximum limit for generation sessions assumes no scripting instructions.
31 Use scripts to describe the waveforms to be generated, the order in which the waveforms are generated, how many times the waveforms are generated, and how the device responds to Script Triggers.
32 DDR mode sets data width to 2.
33 Sample rate dependent. Increasing sample rate increases minimum waveform size requirement.

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Table 10. Generation Minimum Waveform Size[33] (Continued)

Configuration	Sample Rate	
	200 MHz	100 MHz
Stepped sequence	128 S	64 S
Burst sequence	1056 S	512 S

Acquisition

Minimum waveform size[34]	1 S
Record quantum	1 S
Total number of records[35]	2,147,483,647
Total pre-Reference trigger samples	0 up to full record
Total post-Reference trigger samples	0 up to full record

Triggers

Types	Sessions	Edge Detection	Level Detection
1. Start	Acquisition and generation	Rising or falling	—
2. Pause	Acquisition and generation	—	High or low
3. Script <0..3>	Acquisition	Rising or falling	High or low
4. Reference	Acquisition	Rising or falling	—

[33] Sample rate dependent. Increasing sample rate increases minimum waveform size requirement.
[34] Regardless of waveform size, NI-HSDIO allocates at least 640 bytes for a record.
[35] The session should fetch quickly enough that unfetched data is not overwritten.

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Types	Sessions	Edge Detection	Level Detection
5. Advance	Acquisition	Rising or falling	—
6. Stop	Generation	Rising or falling	—

Sources	1. PFI 0 (SMA jack connector) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG <0..7> (PXI Express backplane) 4. Pattern match (acquisition sessions only) 5. Software (user function call) 6. Disabled (do not wait for a trigger)
Destinations, excluding Pause trigger[36]	1. PFI 0 (SMA jack connector) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG <0..6> (PXI Express backplane)
Minimum required trigger pulse width	15 ns
Trigger rearm time	
Start to Reference trigger	150 S, maximum
Start to Advance trigger	220 S, maximum
Advance to Advance trigger	220 S, maximum
Reference to Reference trigger	220 S, maximum
Delay from Pause trigger to Pause state and Stop trigger to Done state[37]	
Generation sessions	50 Sample clock periods + 300 ns, maximum
Acquisition sessions	Synchronous with the data
Delay from Start trigger and Script trigger to digital data output	3 Sample clock periods + 600 ns, maximum

Related Information

Channels on page 2

[36] Each trigger can be routed to any destination except the Pause trigger. The Pause trigger cannot be exported.

[37] Use the Data Active event during generation to determine on a sample-by-sample basis when the device enters the Pause or Done states.

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Events

Types	Sessions
1. Marker <0..2>	Generation
2. Data Active	Generation
3. Ready for Start	Acquisition and generation
4. Ready for Advance	Acquisition
5. End of Record	Acquisition

Destinations (excluding Data Active event)[38]	1. PFI 0 (SMA jack connectors) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG <0..6> (PXI Express backplane)
Marker time resolution (placement)	
SDR	Can be placed at any sample
DDR	Must be placed at an integer multiple of two samples

Related Information

Channels on page 2

Software

Driver Software

Driver support for this device was first available in NI-HSDIO 1.6.

NI-HSDIO is an IVI-compliant driver that allows you to configure, control, and calibrate the PXIe-6548. NI-HSDIO provides application programming interfaces for many development environments.

Application Software

NI-HSDIO provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio

[38] The Data Active event can only be routed to the PFI channels.

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- Microsoft Visual C/C++
- .NET (C# and VB.NET)

NI Measurement Automation Explorer

NI Measurement Automation Explorer (MAX) provides interactive configuration and test tools for the PXIe-6548. MAX is included on the NI-HSDIO media.

Power

Note Characteristic results are commensurate with an average user application using all data channels into high impedance load. Maximum results include worst-case data pattern.

VDC	Current, Characteristic	Current, Maximum
+3.3 V	1.75 A	1.77 A
+12 V	2.2 A	2.3 A

Total power	32.2 W, characteristic 33.5 W, maximum
Warm-up time	15 minutes

Physical

Dimensions	Single 3U, CompactPCI Express slot, PXI Express compatible 21.6 cm × 2.0 cm × 13.0 cm
Weight	519 g (18.3 oz)

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I/O Panel Connectors

Label	Connector Type	Description
CLK IN	SMA jack	External Sample clock, external Reference clock
PFI 0		Events, triggers
CLK OUT		External Sample clock, exported Reference clock
DIGITAL DATA & CONTROL	68-pin VHDCI	Digital data channels, exported Sample clock, STROBE, events, triggers

Environment

Note To ensure that the PXIe-6548 cools effectively, follow the guidelines in the *Maintain Forced Air Cooling Note to Users* included with the PXIe-6548 or available at *ni.com/manuals*. The PXIe-6548 is intended for indoor use only.

Operating temperature	0 °C to 55 °C in all NI PXI Express chassis and hybrid NI PXI Express chassis
Operating relative humidity	10 to 90% relative humidity, noncondensing (meets IEC 60068-2-56)
Storage temperature	-20 °C to 70 °C
Storage relative humidity	5 to 95% relative humidity, noncondensing (meets IEC 60068-2-56)
Operating shock	30 g, half-sine, 11 ms pulse (meets IEC 60068-2-27; test profile developed in accordance with MIL-PRF-28800F)
Operating vibration	5 Hz to 500 Hz, 0.31 g_{rms} (meets IEC 60068-2-64)
Storage shock	50 g, half-sine, 11 ms pulse (meets IEC 60068-2-27; test profile developed in accordance with MIL-PRF-28800F)
Storage vibration	5 Hz to 500 Hz, 2.46 g_{rms} (meets IEC 60068-2-64; test profile exceeds requirements of MIL-PRF-28800F, Class B)

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Altitude	0 to 2,000 m above sea level (at 25 °C ambient temperature)
Pollution degree	2

Compliance and Certifications

Safety

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the *Online Product Certification* section.

Caution Refer to the *Read Me First: Safety and Electromagnetic Compatibility* document for important safety and electromagnetic compatibility information. To

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obtain a copy of this document online, visit *ni.com/manuals* and search for the document title.

Caution To ensure the specified EMC performance, operate this product only with shielded cables and accessories. Do not use unshielded cables or accessories unless they are installed in a shielded enclosure with properly designed and shielded input/output ports and connected to the product using a shielded cable. If unshielded cables or accessories are not properly installed and shielded, the EMC specifications for the product are no longer guaranteed.

Note SHC68-C68-D4 shielded cable and the provided snap-on ferrite beads, National Instruments part number 711627-01, must be used when operating the PXIe-6548.

Caution To ensure the specified EMC performance, the length of all I/O cables must be no longer than 3 m (10 ft).

Caution To ensure the specified EMC performance, you must install PXI EMC Filler Panels, National Instruments part number 778700-01, in all open chassis slots.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit *ni.com/certification*, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at *ni.com/environment*. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit *ni.com/environment/weee*.

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