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PXI Express

NI PXIe-6672 User Manual

Timing and Synchronization Module for PXI Express

November 2010
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This product is intended for use in residential, commercial and industrial locations. There is no guarantee that harmful interference will not occur in a particular installation or when the product is connected to a test object. To minimize the potential for the product to cause interference to radio and television reception or to experience unacceptable performance degradation, install and use this product in strict accordance with the instructions in the product documentation.

Furthermore, any changes or modifications to the product not expressly approved by National Instruments could void your authority to operate it under your local regulatory rules.



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Caution To ensure the specified EMC performance, operate this product only with shielded cables and accessories.



Caution Changes or modifications not expressly approved by National Instruments could void the user's authority to operate the hardware under the local regulatory rules.



Caution To ensure the specified EMC performance, you must install PXI EMC Filler Panels, National Instruments part number 778700-01, in all open chassis slots.

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About This Manual

Thank you for purchasing the National Instruments NI PXIe-6672 Timing and Synchronization Module. The NI PXIe-6672 enables you to pass PXI timing and trigger signals between two or more PXI Express chassis. The NI PXIe-6672 can generate and route clock signals between devices in multiple chassis, providing a method to synchronize multiple devices in a multichassis PXI Express system.

This manual describes the electrical and mechanical aspects of the NI PXIe-6672 and contains information concerning its operation and programming.

Conventions

The following conventions appear in this manual:

<> — Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, AO <3..0>.

» — The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **Options»Settings»General** directs you to pull down the **Options** menu, select the **Settings** item, and select **General** from the last dialog box.

 This icon denotes a tip, which alerts you to advisory information.

 This icon denotes a note, which alerts you to important information.

 This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on the product, refer to the *Safety Information* section of Chapter 1, *Introduction*, for precautions to take.

bold — Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names and hardware labels.

italic — Italic text denotes variables, emphasis, a cross-reference, or an introduction to a key concept. Italic text also denotes text that is a placeholder for a word or value that you must supply.

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`monospace`	Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames, and extensions.
NI PXIe-6672	This phrase refers to the NI PXIe-6672 module for the PXI Express bus.

National Instruments Documentation

The *NI PXIe-6672 User Manual* is one piece of the documentation set for your measurement system. You could have any of several other documents describing your hardware and software. Use the documentation you have as follows:

- Measurement hardware documentation—This documentation contains detailed information about the measurement hardware that plugs into or is connected to the computer. Use this documentation for hardware installation and configuration instructions, specifications about the measurement hardware, and application hints.
- Software documentation—Refer to the *NI-Sync User Manual*, available at `ni.com/manuals`.

You can download NI documentation from `ni.com/manuals`.

Related Documentation

The following documents contain information that you might find helpful as you read this manual:

- *PICMG 2.0 R3.0, CompactPCI Core Specification*, available from PICMG at `www.picmg.org`
- *PXI-5 PXI Express Hardware Specification*, Revision 1.0, available from `www.pxisa.org`
- *NI-VISA User Manual*, available from `ni.com/manuals`
- *NI-VISA Help*, included with the NI-VISA software
- *NI-Sync User Manual*, available from `ni.com/manuals`

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1 Introduction

The NI PXIe-6672 timing and triggering module enables you to pass PXI timing signals between two or more PXI Express chassis. The NI PXIe-6672 module generates and routes clock signals between devices in multiple chassis, providing a method for synchronizing multiple devices in a PXI Express system.

What You Need to Get Started

To set up and use the NI PXIe-6672, you need the following items:

- ❑ NI PXIe-6672 Timing and Triggering Module
- ❑ *NI PXIe-6672 User Manual*
- ❑ *NI-Sync* CD
- ❑ An Application Development Environment such as:
  - LabVIEW
  - LabWindows™/CVI™
  - Microsoft Visual C++ (MSVC)
- ❑ PXI Express chassis
- ❑ PXI Express embedded controller or a desktop computer connected to the PXI Express chassis using MXI-Express hardware

For information on using the driver software for synchronization, refer to the *NI-Sync User Manual*, which you can find on the *NI-Sync* CD or download from `ni.com/manuals`.

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Unpacking

The NI PXIe-6672 is shipped in an antistatic package to prevent electrostatic damage to the module. Electrostatic discharge (ESD) can damage several components on the module.

Caution *Never* touch the exposed pins of connectors.

To avoid such damage in handling the module, take the following precautions:

- Ground yourself using a grounding strap or by touching a grounded object.
- Touch the antistatic package to a metal part of the computer chassis before removing the module from the package.

Remove the module from the package and inspect the module for loose components or any sign of damage. Notify NI if the module appears damaged in any way. Do *not* install a damaged module into the computer.

Store the NI PXIe-6672 in the antistatic envelope when not in use.

Software Programming Choices

When programming the NI PXIe-6672, you can use NI application development environment (ADE) software such as LabVIEW or LabWindows/CVI, or you can use other ADEs such as Visual C/C++.

LabVIEW features interactive graphics, a state-of-the-art interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

LabWindows/CVI is a complete ANSI C ADE that features an interactive user interface, code generation tools, and the LabWindows/CVI Data Acquisition and Easy I/O libraries.

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Safety Information

The following section contains important safety information that you *must* follow when installing and using the product.

Do *not* operate the product in a manner not specified in this document. Misuse of the product can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to National Instruments for repair.

Do *not* substitute parts or modify the product except as described in this document. Use the product only with the chassis, modules, accessories, and cables specified in the installation instructions. You *must* have all covers and filler panels installed during operation of the product.

Do *not* operate the product in an explosive atmosphere or where there may be flammable gases or fumes. If you must operate the product in such an environment, it must be in a suitably rated enclosure.

If you need to clean the product, use a soft, nonmetallic brush. The product *must* be completely dry and free from contaminants before you return it to service.

Operate the product only at or below Pollution Degree 2. Pollution is foreign matter in a solid, liquid, or gaseous state that can reduce dielectric strength or surface resistivity. The following is a description of pollution degrees:

- Pollution Degree 1 means no pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- Pollution Degree 2 means that only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- Pollution Degree 3 means that conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to condensation.

You *must* insulate signal connections for the maximum voltage for which the product is rated. Do *not* exceed the maximum ratings for the product. Do not install wiring while the product is live with electrical signals. Do not remove or add connector blocks when power is connected to the system. Avoid contact between your body and the connector block signal when hot swapping modules. Remove power from signal lines before connecting them to or disconnecting them from the product.

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Operate the product at or below the measurement category[1] marked on the hardware label. Measurement circuits are subjected to working voltages[2] and transient stresses (overvoltage) from the circuit to which they are connected during measurement or test. Measurement categories establish standard impulse withstand voltage levels that commonly occur in electrical distribution systems. The following is a description of measurement categories:

- Measurement Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS[3] voltage. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special hardware, limited-energy parts of hardware, circuits powered by regulated low-voltage sources, and electronics.
- Measurement Category II is for measurements performed on circuits directly connected to the electrical distribution system (MAINS[3]). This category refers to local-level electrical distribution, such as that provided by a standard wall outlet (for example, 115 AC voltage for U.S. or 230 AC voltage for Europe). Examples of Measurement Category II are measurements performed on household appliances, portable tools, and similar hardware.
- Measurement Category III is for measurements performed in the building installation at the distribution level. This category refers to measurements on hard-wired hardware such as hardware in fixed installations, distribution boards, and circuit breakers. Other examples are wiring, including cables, bus bars, junction boxes, switches, socket outlets in the fixed installation, and stationary motors with permanent connections to fixed installations.
- Measurement Category IV is for measurements performed at the primary electrical supply installation typically outside buildings. Examples include electricity meters and measurements on primary overcurrent protection devices and on ripple control units.

---

[1] Measurement categories, also referred to as overvoltage or installation categories, are defined in electrical safety standard IEC 61010-1 and IEC 60664-1.

[2] Working voltage is the highest rms value of an AC or DC voltage that can occur across any particular insulation.

[3] MAINS is defined as a hazardous live electrical supply system that powers hardware. Suitably rated measuring circuits may be connected to the MAINS for measuring purposes.

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2

Installing and Configuring

This chapter describes how to install the NI PXIe-6672 hardware and software and how to configure the device.

Installing the Software

Refer to the `readme.htm` file that accompanies the *NI-Sync* CD for software installation directions.

Note Be sure to install the driver software *before* installing the NI PXIe-6672 hardware.

Installing the Hardware

The following are general installation instructions. Consult the chassis user manual or technical reference manual for specific instructions and warnings about installing new modules.

1. Power off and unplug the chassis.
2. Locate the System Timing Slot in your chassis. It is marked by either a square glyph shown in Figure 2-1, or a square glyph with a circle inside of it, as shown in Figure 2-2.

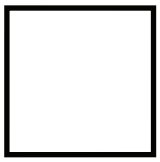


Figure 2-1. System Timing Device Slot Indicator Glyph without Circle

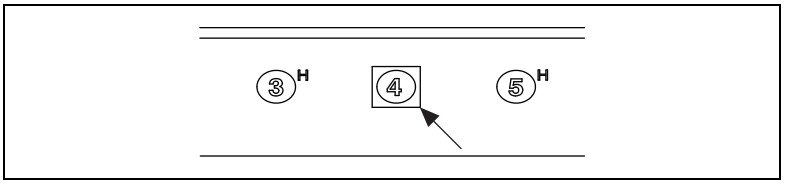


Figure 2-2. System Timing Device Slot Indicator Glyph on the NI PXIe-1062Q Chassis

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Note The slot number printed on the glyph may vary from chassis to chassis.

The circle inside of the square indicates that the slot may also be used as a PXI Express peripheral slot.

3. Remove the filler panel for the PXI slot you located in step 2.
4. Ground yourself using a grounding strap or by holding a grounded object. Follow the ESD protection precautions described in the *Unpacking* section of Chapter 1, *Introduction*.
5. Remove any packing material from the front panel screws and backplane connectors.
6. Insert the NI PXIe-6672 into the PXI Express slot. Use the injector/ejector handle to fully insert the module into the chassis.
7. Screw the front panel of the device to the front panel mounting rail of the chassis.

Caution To ensure the specified EMC performance, you must install PXI EMC Filler Panels, National Instruments part number 778700-01, in all open chassis slots.

8. Visually verify the installation. Make sure the module is not touching other modules or components and is fully inserted into the slot.
9. Plug in and power on the chassis.

The NI PXIe-6672 is now installed.

Configuring the Module

The NI PXIe-6672 is completely software configurable. The system software automatically allocates all module resources.

The two LEDs on the front panel provide information about module status. The front panel description sections of Chapter 3, *Hardware Overview*, describe the LEDs in greater detail.

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3

Hardware Overview

This chapter presents an overview of the hardware functions of the NI PXIe-6672. Figure 3-1 provides a functional overview of the NI PXIe-6672 hardware.

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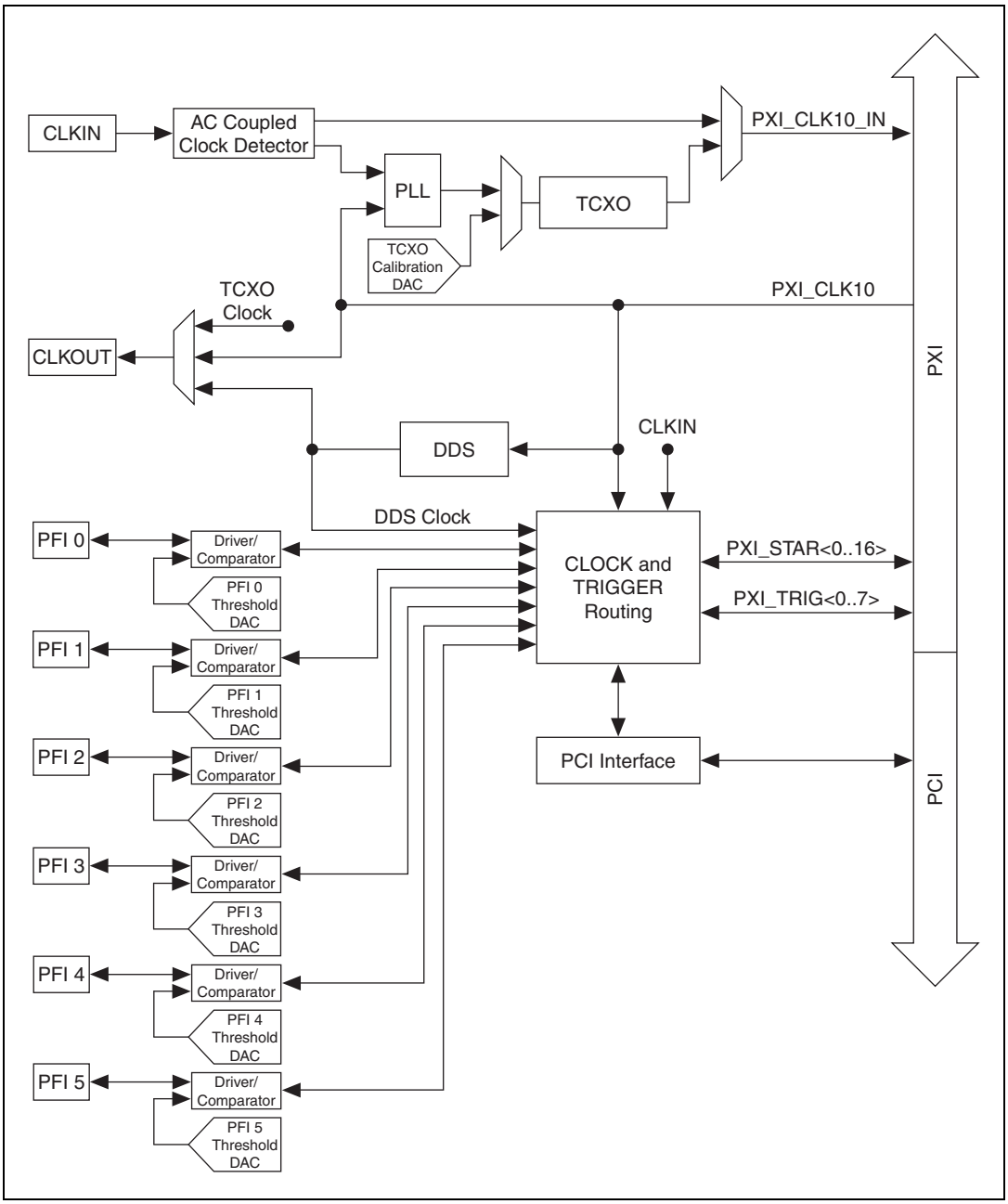
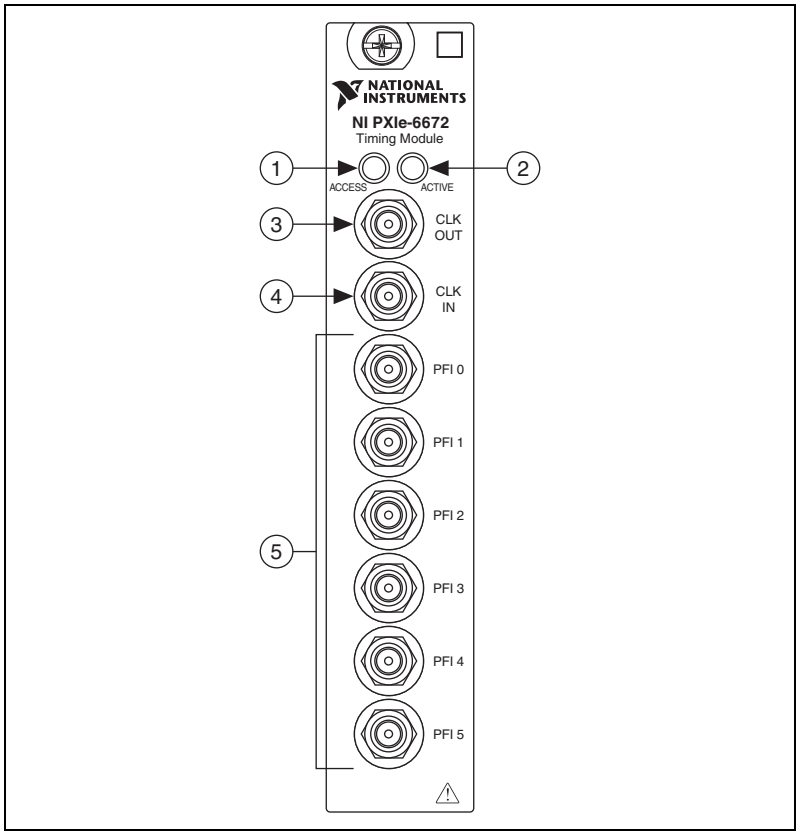


Figure 3-1. Functional Overview of the NI PXIe-6672

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NI PXIe-6672 Front Panel

Figure 3-2 shows the connectors and LEDs on the front panel of the NI PXIe-6672.



1	Access LED	4	CLKIN Connector
2	Active LED	5	PFI <0..5> Connectors
3	CLKOUT Connector		

Figure 3-2. NI PXIe-6672 Front Panel

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Access LED

The Access LED indicates the communication status of the NI PXIe-6672. Refer to Figure 3-2 for the location of the Access LED.

Table 3-1 summarizes what the Access LED colors represent.

Table 3-1. Access LED Color Indication

Color	Status
Off	Module is not yet functional.
Green	Driver has initialized the module.
Amber	Module is being accessed. The Access LED flashes amber for 50 ms when the module is accessed.

Active LED

The Active LED can indicate an error or phase-locked loop (PLL) activity. You can change the Active LED to amber, unless an error overrides the selection. Refer to Figure 3-2 for the location of the Active LED.

Tip Changing the Active LED color to amber is helpful when you want to identify devices in a multichassis situation or when you want an indication that your application has reached a predetermined section of the code.

Table 3-2 illustrates the meaning of each Active LED color.

Table 3-2. Active LED Color Quick Reference Table

Color	PXI_CLK10 Stopped	PLL Error	User Setting	PLL Active
Red	Yes	Yes	—	—
Amber	No	No	Yes	—
Green	No	No	No	Yes
Off	No	No	No	No

Note A red Active LED can indicate that either PXI_CLK10 has stopped or that there is a PLL error.

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Connectors

This section describes the connectors on the front panel of the NI PXIe-6672.

- **CLKIN**—Clock Input. This connector supplies the module with a clock that can be programmatically routed to the onboard PLL for use as a reference or routed directly to the PXI backplane (PXI_CLK10_IN) for distribution to the other modules in the chassis.
- **CLKOUT**—Clock Output. This connector is used to source a clock that can be routed programmatically from the temperature-compensated crystal oscillator (TCXO), direct digital synthesis (DDS), or backplane clock (PXI_CLK10).
- **PFI <0..5>**—Programmable Function Interface <0..5>. These connectors can be used for either input or output. Additionally, **PFI 0** can be used as a clock input for internally synchronizing other signals. Refer to the *Synchronous Routing* section for more information about this functionality. You can program the behavior of these PFI connections individually.

Refer to Figure 3-2 for a diagram showing the locations of these connections on the NI PXIe-6672 front panel.

Caution Connections that exceed any of the maximum ratings of input or output signals on the NI PXIe-6672 can damage the module and the computer. NI is *not* liable for any damage resulting from such signal connections.

Hardware Features

The NI PXIe-6672 perform two broad functions:

- Generating clock and trigger signals
- Routing internally or externally generated signals from one location to another

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Table 3-3 outlines the function and direction of the signals discussed in detail in the remainder of this chapter.

Table 3-3. Signal Descriptions

Signal Name	Direction	Description
PXI_CLK10_IN	Out	This is a signal that can replace the native 10 MHz oscillator on the PXI backplane. PXI_CLK10_IN may originate from the onboard TCXO or from an external source.
PXI_CLK10	In	This signal is the PXI 10 MHz backplane clock. By default, this signal is the output of the native 10 MHz oscillator in the chassis. An NI PXIe-6672 in the System Timing Slot can replace this signal with PXI_CLK10_IN.
TCXO Clock	Out	This is the output of the 10 MHz TCXO. The TCXO is an extremely stable and accurate frequency source.
CLKIN	In	CLKIN is a signal connected to the SMB input pin of the same name. CLKIN can serve as PXI_CLK10_IN, a phase lock reference for the TCXO, or as a source for routing to PXI_STAR.
CLKOUT	Out	CLKOUT is the signal on the SMB output pin of the same name. Either the TCXO clock, DDS clock, or PXI_CLK10 may be routed to this location.
DDS Clock	Out	This is the output of the DDS. The DDS frequency can be programmed with fine granularity from 1 Hz to 105 MHz. The DDS chip automatically phase-locks to PXI_CLK10.
PXI_STAR <0..16>	In/Out	The PXI star trigger bus connects the System Timing Slot to all other slots in a star configuration. The electrical paths of each star line are closely matched to minimize intermodule skew. An NI PXIe-6672 in System Timing Slot can route signals to all other slots using the star trigger bus.
PFI <0..5>	In/Out	The Programmable Function Interface pins on the NI PXIe-6672 route timing and triggering signals between multiple PXI chassis. A wide variety of input and output signals can be routed to or from the PFI lines.
PXI_TRIG <0..7>	In/Out	The PXI trigger bus consists of eight digital lines shared among all slots in the PXI chassis. The NI PXIe-6672 can route a wide variety of signals to and from these lines.

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The remainder of this chapter describes how these signals are used, acquired, and generated by the NI PXIe-6672 hardware, and explains how you can route the signals between various locations to synchronize multiple measurement devices and PXI chassis.

Clock Generation

The NI PXIe-6672 can generate two types of clock signals. The first clock is generated using the onboard DDS chip, and the second is generated with a precise 10 MHz oscillator. The following sections describe the two types of clock generation and explain the considerations for choosing either type.

Direct Digital Synthesis (DDS)

DDS is a method of generating a clock with programmable frequency. DDS consists of a *frequency tuning word*, an accumulator, a sine-lookup table, a D/A converter (DAC), and a comparator.

The frequency tuning word is a number that specifies the desired frequency. Each master clock cycle, the frequency tuning word is added to the accumulator, which rolls over when it gets to its maximum value. The accumulator value is used to get a point in the sine-lookup table, which is converted to an analog voltage by the DAC. For example, if the sine table is 128 points long, and the frequency tuning word is one, the accumulator takes 128 clock cycles to output one sine wave. If you change the frequency tuning word to 3, the accumulator steps through the sine table three times as fast, and outputs a sine wave in 128/3, or 42.6, clock cycles.

The output of the DAC is run through an analog filter to smooth the sine wave. The filtered output is then run through a comparator, which changes the output to a square wave with the specified frequency.

You can specify the programmable DDS frequency on the NI PXIe-6672 with a precision of approximately .07 Hz within the range 1 Hz to 105 MHz. The accuracy of the frequency depends on the PXI_CLK10 reference clock, so a precise 10 MHz source improves the accuracy of the DDS output. You can replace the 10 MHz clock with the TCXO for more accurate DDS timing.

When the DDS is programmed an update signal must be sent to it before it will begin operating as programmed. The source for this update signal is either immediate (DDS starts outputting the programmed frequency as soon as software programs it) or one of the eight PXI triggers. When one

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of the PXI trigger lines is used as the source for the update, frequency generation will not start until a rising edge occurs on the PXI trigger selected.

Note NI-Sync software defaults to an immediate update. If a PXI trigger is used instead, the user must specify the update signal source before setting any of the other DDS properties.

When more then one NI PXIe-6672 is used in a multiple chassis setup, the DDS frequency of both boards can be synchronized. The DDS system clock is phase locked to PXI_CLK10, when two or more chassis share a common 10 MHz clock, the DDS outputs will also be phase locked (refer to the *Using the PXI_CLK10 PLL* section for information on how to ensure that two or more chassis have close PXI_CLK10 phase alignment). To fully synchronize the DDS outputs a common update signal source must be used and routed to the selected PXI trigger. A synchronous route to PXI_CLK10 provides the best results. Refer to the *Routing Signals* section for details on routing trigger signals.

The NI PXIe-6672 DDS can adjust the phase of the generated clock by up to ±5 ns. This may be used to tighten the synchronization between two or more DDS devices in a multi-chassis setup, or to compensate for delays caused by different cable lengths.

PXI_CLK10 and TCXO

The NI PXIe-6672 features a precision 10 MHz TCXO. The frequency accuracy of this clock is several orders of magnitude greater than the frequency accuracy of the native 10 MHz PXI backplane clock (PXI_CLK10).

The TCXO contains circuitry to measure the temperature of the oscillator. It uses the temperature to adjust its frequency output according to the crystal's known frequency variation across its operating temperature range.

An NI PXIe-6672 module in the System Timing Slot of a PXI Express chassis can replace the native PXI 10 MHz backplane frequency reference clock (PXI_CLK10) with the more stable and accurate output of the TCXO. All other PXI modules in the chassis that reference the 10 MHz backplane clock benefit from this more accurate frequency reference. Furthermore, the DDS chip on the NI PXIe-6672 references its output to the backplane clock and also takes advantage of the superior TCXO accuracy. The TCXO does not automatically replace the native 10 MHz

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clock; this feature must be explicitly enabled in software. The TCXO output also can be routed out to the CLKOUT connector.

In addition to replacing the native backplane clock directly, the TCXO can phase lock to an external frequency source. This operation is discussed in detail in the *Using the PXI_CLK10 PLL* section.

Routing Signals

The NI PXIe-6672 has versatile trigger routing capabilities. It can route signals to and from the front panel, the PXI triggers, and the PXI star triggers.

The CLKIN SMB input on the NI PXIe-6672 may be used for PXI_CLK10 replacement by either routing a 10 MHz signal directly from the CLKIN input to PXI_CLK10_IN, or by using the CLKIN input as a phase lock reference for the TCXO. When phase locking the TCXO to CLKIN, CLKIN may be any multiple of 1 MHz to 105 MHz. In addition, CLKIN is a valid source for PXI_Star.

The CLKOUT SMB on the NI PXIe-6672 may also be used to route the TCXO, PXI_CLK10, or DDS Clock.

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Figures 3-3 and 3-4 summarize the routing features of the NI PXIe-6672. The remainder of this chapter details the capabilities and constraints of the routing architecture.

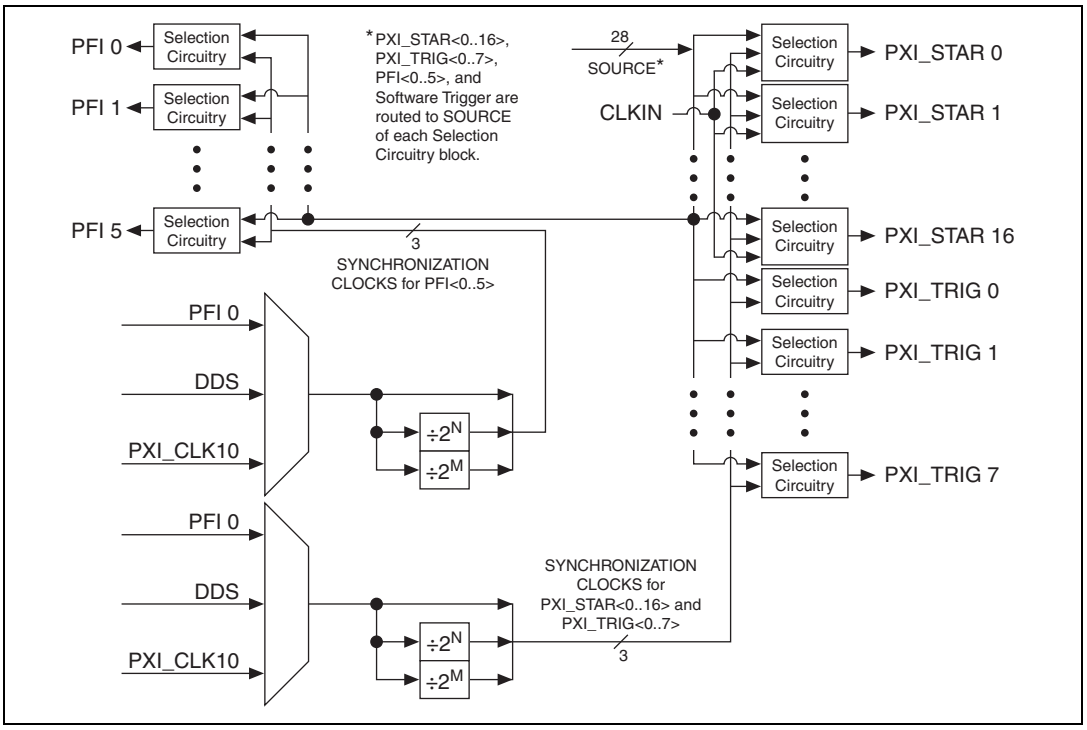


Figure 3-3. High-Level Schematic of NI PXIe-6672 Signal Routing Architecture

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Figure 3-4 provides a more detailed view of the *Selection Circuitry* referenced in Figure 3-3.

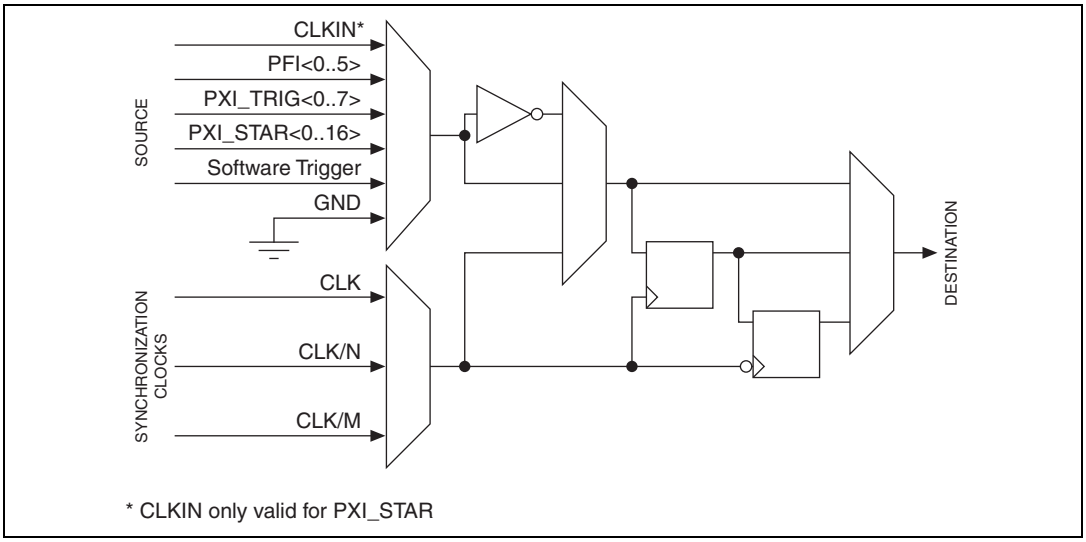


Figure 3-4. Signal Selection Circuitry Diagram

Determining Sources and Destinations

All signal routing operations can be characterized by a *source* (input) and a *destination*. In addition, synchronous routing operations must also define a third signal known as the *synchronization clock*. Refer to the *Choosing the Type of Routing* section for more information on synchronous versus asynchronous routing.

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Table 3-4 summarizes the sources and destinations of the NI PXIe-6672. The destinations are listed in the horizontal heading row, and the sources are listed in the column at the far left. A ✓ in a cell indicates that the source and destination combination defined by that cell is a valid routing combination.

Table 3-4. Sources and Destinations for NI PXIe-6672 Signal Routing Operations

			Destinations					
			Front Panel		Backplane			Onboard
Sources	Front Panel		CLKOUT	PFI <0..5>	PXI_ CLK10_IN	PXI_Star Trigger <0..16>	PXI TRIG <0..7>	TCXO Reference PLL
		CLKIN	➳*	✓*	✓	✓	✓*	✓
		PFI <0..5>		✓		✓	✓	
	Backplane	PXI_ CLK10	✓	✓†		✓†	✓†	
		PXI_STAR <0..16>		✓		✓	✓	
		PXI TRIG <0..7>		✓		✓	✓	
	Onboard	TCXO	✓	✓*	✓	✓*	✓*	
		DDS	✓	✓†		✓†	✓†	
		Global Software Trigger		✓		✓	✓	

* Can be accomplished in two stages by routing source to PXI_CLK10_IN, replacing PXI_CLK10 with PXI_CLK10_IN (occurs automatically in most chassis), and then routing PXI_CLK10 to the destination. The source must be 10 MHz.

† Routing PXI_CLK10 or DDS to PFI, PXI_Star, or PXI_Trigger is accomplished by setting PXI_CLK10 or DDS to be the synchronization clock (NI-Sync Property Node) and then routing the synchronization clock as the source.

Using Front Panel PFIs As Inputs

The front-panel PFIs can receive external signals from 0 to +5 V. They can be terminated programmatically with 50 Ω resistances to match the cable impedance and minimize reflections.

Note Terminating the signals with a 50 Ω resistance is recommended when the source is another NI PXIe-6672 or any other source with a 50 Ω output.

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The voltage thresholds for the front-panel PFI inputs are programmable. The input signal is generated by comparing the input voltage on the PFI connectors to the voltage output of software-programmable DACs. The thresholds for the PFI lines are individually programmable, which is useful if you are importing signals from multiple sources with different voltage swings. The front panel PFI inputs can be routed to any PXI_Star triggers, PXI triggers, or other front panel PFI outputs.

Using Front Panel PFIs As Outputs

The front panel PFI outputs are +3.3 V drivers with 50 Ω output impedance. The outputs can drive 50 Ω loads, such as a 50 Ω coaxial cable with a 50 Ω receiver. This cable configuration is the recommended setup to minimize reflections. With this configuration, the receiver sees a single +1.6 V step—a +3.3 V step split across the 50 Ω resistors at the source and the destination.

You also can drive a 50 Ω cable with a high-impedance load. The destination sees a single step to +3.3 V, but the source sees a reflection. This cable configuration is acceptable for low-frequency signals or short cables. You can select the signal source from the front panel triggers (PFI <0..5>), the PXI star triggers, the PXI triggers, or the synchronization clock (PXI_CLK10, the DDS clock, or PFI 0). The synchronization clock concept is explained in more detail in the *Choosing the Type of Routing* section.

You can independently select the output signal source for each PFI line from one of the following sources:

- Another PFI <0..5>
- PXI triggers <0..7> (PXI_TRIG <0..7>)
- PXI_STAR <0..16>
- Global software trigger
- PFI synchronization clock

The PFI synchronization clock may be any of the following signals:

- DDS clock
- PXI_CLK10
- PFI 0 Input
- Any of the previously listed signals divided by the first frequency divider (2^n, up to 512)

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- Any of the previously listed signals divided by the second frequency divider (2^m, up to 512)

Refer to the *Choosing the Type of Routing* section for more information on the synchronization clock.

Note The PFI synchronization clock is the same for all routing operations in which PFI <0..5> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

Using the PXI Triggers

The PXI triggers go to all the slots in the chassis. All modules receive the same PXI triggers, so PXI trigger 0 is the same for Slot 2 as it is for Slot 3, and so on. This feature makes the PXI triggers convenient in situations where you want, for instance, to start an acquisition on several devices at the same time because all modules will receive the same trigger.

The frequency on the PXI triggers should not exceed 20 MHz to preserve signal integrity. The signals do not reach each slot at precisely the same time. A difference of several nanoseconds between slots can occur in an eight-slot chassis. However, this delay is not a problem for many applications. You can route signals to the PXI triggers from PFI <0..5>, from the PXI star triggers, or from other PXI triggers. You also can route PXI_CLK10 or the DDS clock to a PXI trigger line (PXI_TRIG <0..7>) using the synchronization clock.

You can independently select the output signal source for each PXI trigger line from one of the following sources:

- PFI <0..5>
- Another PXI trigger <0..7> (PXI_TRIG <0..7>)
- PXI_STAR <0..16>
- Global software trigger
- PXI_Trig/PXI_Star synchronization clock

The PXI_Trig/PXI_Star synchronization clock may be any of the following signals:

- DDS clock
- PXI_CLK10
- PFI 0 Input
- Any of the previously listed signals divided by the first frequency divider (2^n, up to 512)

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- Any of the previously listed signals divided by the second frequency divider (2^m, up to 512)

Refer to the *Choosing the Type of Routing* section for more information about the synchronization clock.

Note The PXI_Trig/PXI_Star synchronization clock is the same for all routing operations in which PXI_TRIG <0..7> or PXI_STAR <0..16> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

Using the PXI Star Triggers

There are up to 17 PXI star triggers per chassis. Each trigger line is a dedicated connection between the System Timing Slot and one other slot. The *PXI Specification*, Revision 2.1, requires that the propagation delay along each star trigger line be matched to within 1 ns. A typical upper limit for the skew in most NI PXI chassis is 500 ps. The low skew of the PXI star trigger bus is useful for applications that require triggers to arrive at several modules nearly simultaneously.

The star trigger lines are bidirectional, so signals can be sent to System Timing Slot from a module in another slot or from System Timing Slot to the other module.

You can independently select the output signal source for each PXI star trigger line from one of the following sources:

- PFI <0..5>
- PXI triggers <0..7> (PXI_TRIG <0..7>)
- Another PXI star trigger line (PXI_STAR <0..16>)
- Global software trigger
- PXI_Trig/PXI_Star synchronization clock
- CLKIN

Refer to the *Using the PXI Triggers* section for more information on the PXI_Trig/PXI_Star synchronization clock.

Choosing the Type of Routing

The NI PXIe-6672 routes signals in one of two ways: asynchronously or synchronously. The following sections describe the two routing types and the considerations for choosing each type.

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Asynchronous Routing

Asynchronous routing is the most straightforward method of routing signals. Any asynchronous route can be defined in terms of two signal locations: a source and a destination. A digital pulse or train comes in on the source and is propagated to the destination. When the source signal goes from low to high, this rising edge is transferred to the destination after a propagation delay through the module. Figure 3-5 illustrates an asynchronous routing operation.

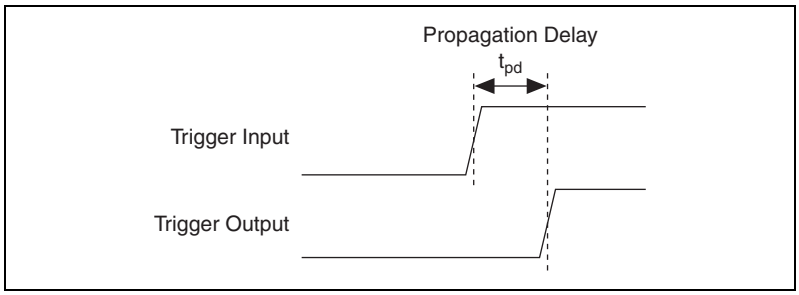


Figure 3-5. Asynchronous Routing Operation

Some delay is always associated with an asynchronous route, and this delay varies among NI PXIe-6672 modules, depending on variations in temperature and chassis voltage. Typical delay times in the NI PXIe-6672 for asynchronous routes between various sources and destinations are given in Appendix A, *Specifications*.

Asynchronous routing works well if the total system delays are not too long for the application. Propagation delay could be caused by the following reasons:

- Output delay on the source
- Propagation delay of the signal across the backplane(s) and cable(s)
- Propagation delay of the signal through the NI PXIe-6672
- Time for the receiver to recognize the signal

Both the source and the destination of an asynchronous routing operation on the NI PXIe-6672 can be any of the following lines:

- Any front panel PFI pin (PFI <0..5)
- Any PXI star trigger line (PXI_STAR <0..16>)
- Any PXI trigger line (PXI_TRIG <0..7>)

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Synchronous Routing

A synchronous routing operation is defined in terms of three signal locations: a source, a destination, and a *synchronization clock*. A digital signal comes in on the source and is propagated to the destination after the edge has been realigned with the synchronization clock.

Unlike asynchronous routing, the output of a synchronous routing operation does not directly follow the input after a propagation delay. Instead, the output waits for the next rising edge of the clock before it follows the input. Thus, the output is said to be “synchronous” with this clock.

Figure 3-6 shows a timing diagram that illustrates synchronous routing.

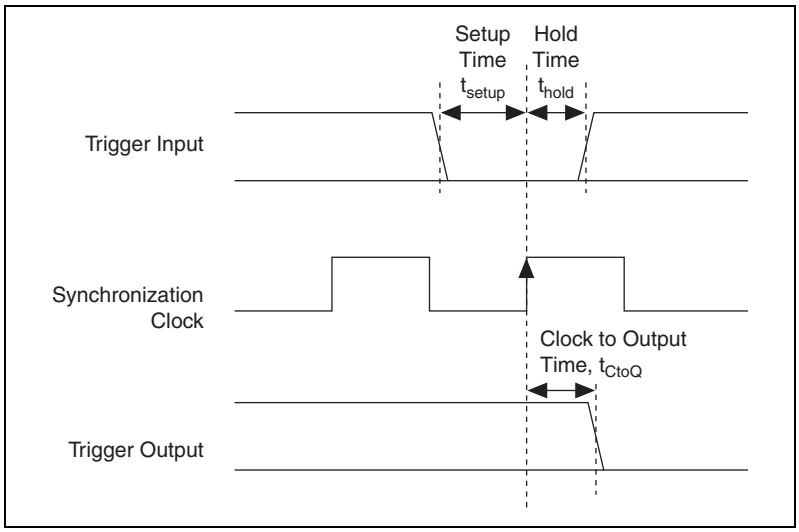


Figure 3-6. Synchronous Routing Operation

Synchronous routing can send triggers to several places in the same clock cycle or send the trigger to those same places after a deterministic skew of a known number of clock cycles. If a signal arrives at two chassis within the same clock cycle, each NI PXIe-6672 realigns the signal with the synchronization clock and distributes it to the modules in each chassis at the same time. Synchronous routing can thus remove uncertainty about when triggers are received. If the delays through the system are such that an asynchronous trigger might arrive near the edge of the receiver clock, the receiver might see the signal in the first clock cycle, or it might see it in

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the second clock cycle. However, by synchronizing the signal, you can eliminate the ambiguity, and the signal will always be seen in the second clock cycle.

One useful feature of synchronous routing is that the signal can be propagated on either the rising or falling edge of the synchronization clock. In addition, the polarity of the destination signal can be inverted, which is useful when handling active-low digital signals.

Possible sources for synchronous routing include the following sources:

- Any front panel PFI pin
- Any PXI star trigger line (PXI_STAR <0..16>)
- Any PXI trigger line (PXI_TRIG <0..7>)
- Global software trigger
- The synchronization clock itself

Note The possible destinations for a synchronous route are identical to those for an asynchronous route. The destinations include any front panel PFI pin, any PXI star trigger line, or any PXI trigger line.

The synchronization clock for a synchronous route can be any of the following signals:

- 10 MHz PXI backplane clock signal
- DDS clock on the NI PXIe-6672
- Front panel PFI 0 Input
- One of two “divided copies” of any of the previously listed three signals. The NI PXIe-6672 includes two clock-divider circuits that can divide the synchronization clock signals by any power of 2 up to 512.

Refer to Figures 3-3 and 3-4 for an illustration of how the NI PXIe-6672 performs synchronous routing operations.

Generating a Single Pulse (Global Software Trigger)

The global software trigger is a single pulse with programmable delay that is fired on a software command. This signal is always routed synchronously with a clock. Therefore, asynchronous routing is not supported when the signal source is the global software trigger.

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The software trigger can be delayed by up to 15 clock cycles on a per route basis. This feature is useful if a single pulse must be sent to several destinations with significantly different propagation delays. By delaying the pulse on the routes with shorter paths, you can compensate for the propagation delay. An example of such a situation would be when a trigger pulse must arrive nearly simultaneously at the local backplane and the backplane of another chassis separated by 50 m of coaxial cable.

Using the PXI_CLK10 PLL

A module in System Timing Slot of a PXI Express chassis can replace the PXI_CLK10 reference clock. The NI PXIe-6672 offers three options for this replacement. This section describes each option.

- The first option is to replace PXI_CLK10 directly with the TCXO output on the NI PXIe-6672. This oscillator is a more stable and accurate reference than the native backplane clock.
- The second option is to route a 10 MHz clock directly from CLKIN on the front panel to PXI_CLK10_IN, which is the pin on the backplane that will replace PXI_CLK10. There is a delay through the module, as well as a distribution delay on the backplane. These delays tend to be similar for chassis of the same model, so routing the same clock to a pair of chassis usually matches PXI_CLK10 to within a few nanoseconds.
- The third option is to employ the NI PXIe-6672 PLL circuitry for the TCXO. As in option 1, the output of the TCXO replaces the native 10 MHz signal. However, this scheme also requires an input signal on CLKIN. This signal must be a stable clock, and its frequency must be a multiple of 1 MHz (5 MHz or 13 MHz, for example) between 1 MHz and 105 MHz. The PLL feedback circuit generates a voltage proportional to the phase difference between the reference input on PXI_CLK10 and the output of the TCXO. This PLL voltage output then tunes the output frequency of the TCXO. As long as the incoming signal is a stable 1 MHz frequency multiple, the PLL circuit quickly locks the TCXO to the reference, eliminating all phase drift between the two signals.

Using the PLL provides several advantages over the other two options for replacing the PXI backplane clock:

- CLKIN is not required to be 10 MHz. If you have a stable reference that is a multiple of 1 MHz, such as 13 or 5 MHz, you can frequency-lock the chassis to it.

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- If CLKIN stops or becomes disconnected, PXI_CLK10 is still present in the chassis.
- If CLKIN is 10 MHz, the NI PXIe-6672 can compensate for distribution delays in the backplane. The feedback in the PLL comes from PXI_CLK10. This PLL makes it possible for the NI PXIe-6672 to align clock edges at CLKIN with the edges of PXI_CLK10 that the modules receive. If you split an external (accurate) 10 MHz reference and route it to two chassis, they can both lock to it. The result is a tighter synchronization of PXI_CLK10 on the chassis.

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4

Calibration

This chapter discusses the calibration of the NI PXIe-6672.

Calibration consists of verifying the measurement accuracy of a device and correcting for any measurement error. The NI PXIe-6672 is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the corrections that were needed to meet specifications—are stored in the onboard nonvolatile memory (EEPROM). The driver software uses these stored values.

Factory Calibration

The factory calibration of the NI PXIe-6672 involves calculating and storing four calibration constants. These values control the accuracy of four features of the device, which are discussed in the following sections.

TCXO Frequency

The TCXO frequency can be varied over a small range. The output frequency of the TCXO is adjusted using this constant to meet the specification listed in Appendix A, *Specifications*. This calibration applies only to the NI PXIe-6672.

PXI_CLK10 Phase

When using the PLL to lock PXI_CLK10 to an external reference clock, the phase between the clocks can be adjusted. The time between rising edges of PXI_CLK10 and the input clock is minimized using this constant.

DDS Start Trigger Phase

To start the DDS reliably, the DDS start trigger must arrive within a certain window of time. The phase of the DDS start trigger is controlled by this constant to meet the setup and hold-time requirements of the DDS.

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DDS Initial Phase

The phase of the DDS output is adjusted using this constant so that the DDS outputs from multiple NI PXIe-6672 modules are aligned.

Additional Information

Refer to `ni.com/calibration` for additional information on NI calibration services.

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A

Specifications

CLKIN Characteristics

CLKIN fundamental frequency range[1] ..... 1 MHz to 105 MHz, sine or square wave

Input impedance ..... 50 Ω, nominal

Input coupling ..... AC

Voltage range

- DC ..... ±20 V
- AC ..... 400 mV_{p-p} to 5 V_{p-p}

Absolute maximum input voltage[2] ..... ±26 V, max

CLKIN to PXI_CLK10_IN delay without PLL ..... 14 ns to 14.7 ns, typical

CLKIN to PXI_CLK10 delay with PLL ..... ±1 ns, max

CLKIN frequency accuracy requirement

- For PLL and TCXO ..... ±5.0 ppm
- For replacing PXI_CLK10 (no PLL) ..... ±100 ppm[3]

[1] CLKIN fundamental frequency can be any multiple of 1 MHz within the range specified when the PLL is engaged and PXI_CLK10 is locking to it. The frequency must be 10 MHz when replacing PXI_CLK10 without the PLL.

[2] Stresses beyond those listed can cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods of time can affect device reliability. Functional operation of the device outside the conditions indicated in the operational parts of the specification is not implied.

[3] This is a requirement of the PXI specification.

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Jitter added to CLKIN

Without PLL.....0.5 ps_{rms}, 10 Hz to 100 kHz, typical

With PLL.....0.6 ps_{rms}, 10 Hz to 100 kHz, typical

Duty cycle distortion of CLKIN to PXI_CLK10_IN without PLL .....±1%, max

Required input duty cycle when using PLL.....45 to 55%

CLKOUT Characteristics

Output frequency

From PXI_CLK10.....10 MHz

From TCXO.....10 MHz

From DDS .....1 MHz[1] to 105 MHz

Duty cycle.....43 to 55%[2]

Output impedance.....50 Ω, nominal

Output coupling .....AC

Amplitude, software configurable to two voltage levels (low and high drive)

Open Load	Square Wave
Low Drive	2.0 V_{p-p}, typical
High Drive	5.0 V_{p-p}, typical

50 Ω Load	Square Wave
Low Drive	1.0 V_{p-p}, typical
High Drive	2.5 V_{p-p}, typical

[1] The lower limit is load dependent because of the AC coupling. This limit is less than 1 MHz for high-impedance loads.

[2] The duty cycle specification covers both DDS range and TCXO.

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Square wave rise/fall time (10 to 90%)

Low drive ..... 0.5 ns min, 2.5 ns max

High drive ..... 0.5 ns min, 2.5 ns max

PFI <0..5>

Input Characteristics

Frequency range ..... DC to 105 MHz

Input impedance ..... 50 Ω, nominal, or 1 kΩ ±10%, || 35 pF, software-selectable

Input coupling ..... DC

Voltage level ..... 0 to 5 V

Absolute maximum input voltage[1] ..... ±5.25 V, max

Input threshold

Voltage level ..... 0 to 4.3 V, software-selectable

Voltage resolution ..... 16.8 mV (8 bits)

Error ..... ±40 mV

Hysteresis ..... 50 mV

Asynchronous delay, t_{pd}

PFI <0..5> to PXI_TRIG <0..7> output ..... 19 to 26 ns, typical

PFI <0..5> to PXI_STAR <0..12> output ..... 10 to 19 ns, typical

Synchronized trigger input setup time, t_{setup}[2] ..... 16.5 ns, typical

Synchronized trigger input hold time, t_{hold}[2] ..... –9.9 ns, typical

[1] Stresses beyond those listed can cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods of time can affect device reliability. Functional operation of the device outside the conditions indicated in the operational parts of the specifications is not implied.

[2] Relative to PXI_CLK10 at the backplane connector. When PLL is used to route CLKIN to PXI_CLK10_IN, CLKIN and PXI_CLK10 are phase locked with ±1 ns max phase difference. Refer to the *Synchronous Routing* section of Chapter 3, *Hardware Overview*, for more details.

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Output Characteristics

Frequency range .....DC to 105 MHz

Output impedance.....50 Ω, nominal

Output coupling .....DC

Voltage level.....0 to 1.6 V into 50 Ω;
0 to 3.3 V into open circuit,
typical

Absolute maximum applied voltage[1].....±5.25 V, max

PXI_CLK10 synchronized trigger clock
to out time, t_{CtoQ}[2].....10.7 ns, typical

Output-to-output skew, synchronous.....500 ps, typical

PXI_STAR Trigger Characteristics

PXI_STAR <0..16> to
PXI_STAR <0..16> output skew
at NI PXIe-6672 backplane connector....300 ps[3], typical

Asynchronous delays, t_{pd}

PXI_STAR <0..16> to
PFI <0..5> output.....13 to 17 ns, typical

PXI_STAR <0..16> to
PXI_TRIG <0..7> output.....18 to 24 ns, typical

[1] Stresses beyond those listed can cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods of time can affect device reliability. Functional operation of the device outside the conditions indicated in the operational parts of the specifications is not implied.

[2] Relative to PXI_CLK10 at backplane connector.

[3] This specification applies to all synchronous routes to the PXI_Star lines, as well as asynchronous routes from the PFI inputs to the PXI_Star lines.

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PXI Trigger Characteristics

PXI_TRIG <0..7> to
PXI_TRIG <0..7> output skew
at NI PXIe-6672 backplane connector ... 5 ns, typical

Asynchronous delay, t_{pd}
PXI_TRIG <0..7> to
PFI <0..5> output ..... 15 to 22 ns, typical

TCXO Characteristics

Frequency ..... 10 MHz

Initial accuracy ..... ±2.5 ppm

Long-term stability (1 year)[1] ..... ±1 ppm

Temperature stability (0 to 55 °C)[2] ..... ±2 ppm

DDS Characteristics

Frequency range ..... 1 Hz to 105 MHz

Frequency resolution ..... < 0.075 Hz

Frequency accuracy ..... Equivalent to PXI_CLK10 accuracy[3]

Physical

Chassis requirement ..... One 3U PXI Express System Timing Slot

Front panel connectors ..... SMB male, 50 Ω

Front panel indicators ..... Two tricolor LEDs (green, red, and amber)

---

[1] Includes stability of TCXO and supporting circuitry.

[2] Includes temperature stability of TCXO and supporting circuitry.

[3] The DDS frequency inherits the relative frequency of PXI_CLK10. For example, if you route the TCXO to PXI_CLK10, the DDS output inherits the same relative frequency accuracy as the TCXO output.

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Recommended maximum cable length[1]

PFI/CLKOUT, DC to 10 MHz .....200 m

CLKOUT High Gain, 105 MHz.....80 m[2]

PFI/CLKOUT Low Gain, 105 MHz.....30 m[3]

Weight .....0.459 lb (208 g)

Power Requirements

+3.3 V .....800 mA, max

+12 V .....700 mA, max

Environment

Maximum altitude.....2,000 m (800 mbar) (at 25 °C ambient temperature)

Pollution Degree 2

Indoor use only.

Caution When required, clean the NI PXIe-6672 with a soft nonmetallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Operating Environment

Ambient temperature range .....0 to 55 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.)

[1] Cable length measurements were made with an RG 58 cable. Maximum cable length performance will vary depending on the cable type used.

[2] Maximum cable length with a direct cable connection. Loss from a signal splitter would reduce maximum cable length.

[3] Maximum cable length with a direct cable connection. Loss from a signal splitter would reduce maximum cable length.

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Relative humidity range ..... 10% to 90%, noncondensing (Tested in accordance with IEC-60068-2-56.)

Storage Environment

Ambient temperature range..... –40 to 71 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit.)

Relative humidity range ..... 5% to 95% noncondensing (Tested in accordance with IEC-60068-2-56.)

Shock and Vibration

Operational shock ..... 30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC-60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)

Random vibration

- Operating ..... 5 to 500 Hz, 0.3 g_{rms}
- Nonoperating ..... 5 to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Note Specifications are subject to change without notice.

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Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia and New Zealand (per CISPR 11) Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generates radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations and certifications, and additional information, refer to the *Online Product Certification* section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

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Online Product Certification

To obtain product certifications and the Declaration of Conformity (DoC) for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)



EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit ni.com/environment/weee.

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  - **Self-Help Technical Resources**—For answers and solutions, visit `ni.com/support` for software drivers and updates, a searchable KnowledgeBase, product manuals, step-by-step troubleshooting wizards, thousands of example programs, tutorials, application notes, instrument drivers, and so on. Registered users also receive access to the NI Discussion Forums at `ni.com/forums`. NI Applications Engineers make sure every question submitted online receives an answer.
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- **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting `ni.com/certification`.
- **Calibration Certificate**—If your product supports calibration, you can obtain the calibration certificate for your product at `ni.com/calibration`.

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Glossary

Symbol	Prefix	Value
p	pico	10^{-12}
n	nano	10^{-9}
µ	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^{3}
M	mega	10^{6}

Symbols

%	percent
±	plus or minus
+	positive of, or plus
–	negative of, or minus
/	per
°	degree
Ω	ohm

A

accumulator	A part where numbers are totaled or stored.
ADE	application development environment
asynchronous	A property of an event that occurs at an arbitrary time, without synchronization to a reference clock.

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B

backplane	An assembly, typically a printed circuit board (PCB), with connectors and signal paths that bus the connector pins.
bus	The group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. An example of a PC bus is the PCI bus.

C

C	Celsius
CLKIN	CLKIN is a signal connected to the SMB input pin of the same name. CLKIN can serve as PXI_CLK10_IN or be used as a phase lock reference for the OCXO.
CLKOUT	CLKOUT is the signal on the SMB output pin of the same name. Either the OCXO clock or PXI_CLK10 can be routed to CLKOUT.
clock	Hardware component that controls timing for reading from or writing to groups.
CompactPCI	A Eurocard configuration of the PCI bus for industrial applications.

D

D/A	digital-to-analog
DAC	Digital-to-analog converter—an electronic device that converts a digital number into a corresponding analog voltage or current.
DAQ	Data acquisition—(1) collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing; (2) collecting and measuring the same kinds of electrical signals with A/D and/or DIO devices plugged into a computer, and possibly generating control signals with D/A and/or DIO devices in the same computer.

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DC	direct current
DDS	Direct digital synthesis—a method of creating a clock with a programmable frequency.

E

EEPROM	Electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed.
ESD	electrostatic discharge

F

frequency	The basic unit of rate, measured in events or oscillations per second using a frequency counter or spectrum analyzer. Frequency is the reciprocal of the period of a signal.
frequency tuning word	A number that specifies the frequency.
front panel	The physical front panel of an instrument or other hardware.

H

Hz	Hertz—the number of scans read or updates written per second.

I

in.	inch or inches

J

jitter	The rapid variation of a clock or sampling frequency from an ideal constant frequency.

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L

LabVIEW	A graphical programming language.
LED	Light-emitting diode—a semiconductor light source.

M

master	The requesting or controlling device in a master/slave configuration.
Measurement & Automation Explorer (MAX)	A controlled centralized configuration environment that allows you to configure all of your National Instruments DAQ, GPIB, IMAQ, IVI, Motion, VISA, and VXI devices.

N

NI-DAQ	National Instruments driver software for DAQ hardware.

O

oscillator	A device that generates a fixed frequency signal. An oscillator most often generates signals by using oscillating crystals, but also may use tuned networks, lasers, or atomic clock sources. The most important specifications on oscillators are frequency accuracy, frequency stability, and phase noise.
output impedance	The measured resistance and capacitance between the output terminals of a circuit.

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P

PCI	Peripheral component interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 Mbytes/s.
PCI Express	Peripheral component interconnect express—a high-performance expansion bus architecture that expands on and doubles the data transfer rates of original PCI. PCI Express is a two-way, serial connection that carries data in packets along two pairs of point-to-point data lanes, compared to the single parallel data bus of traditional PCI that routes data at a set rate. Initial bit rates for PCI Express reach 2.5Gb/s per lane direction, which equate to data transfer rates of approximately 200 Mbytes/s.
PFI	programmable function interface
PLL	phase-locked loop
precision	The measure of the stability of an instrument and its capability to give the same measurement over and over again for the same input signal.
propagation delay	The amount of time required for a signal to pass through a circuit.
PXI	A rugged, open system for modular instrumentation based on CompactPCI, with special mechanical, electrical, and software features. The PXIbus standard was originally developed by National Instruments in 1997, and is now managed by the PXIbus Systems Alliance.
PXI Express	An open system for modular instrumentation based on PXI and CompactPCI Express. PXI Express enhances system timing and software frameworks while preserving backward compatibility with PXI. The system controller slot is capable of supporting up to a x16 PCI Express link, plus a x8 link, providing a total of 6 GB/s bandwidth to the PXI backplane, which is more than 45 times improvement upon PXI backplane throughput
PXI star	A special set of trigger lines in the PXI backplane for high-accuracy device synchronization with minimal latencies on each PXI slot.
PXI_Trig/PXI_Star synchronization clock	The clock signal that is used to synchronize the PXI triggers or PXI_STAR triggers on an NI PXIe-6672.

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S

s	seconds
skew	The actual time difference between two events that would ideally occur simultaneously. Inter-channel skew is an example of the time differences introduced by different characteristics of multiple channels. Skew can occur between channels on one module, or between channels on separate modules (intermodule skew).
slave	A computer or peripheral device controlled by another computer.
slot	The place in the computer or chassis in which a card or module can be installed.
SMB	Sub miniature type B—a small coaxial signal connector that features a snap coupling for fast connection.
synchronous	A property of an event that is synchronized to a reference clock.

T

t_{CtoQ}	clock to output time
t_{hold}	hold time
t_{pd}	propagation delay time
TRIG	trigger signal
trigger	A digital signal that starts or times a hardware event (for example, starting a data acquisition operation).
t_{setup}	setup time

V

V	volts
VI	virtual instrument

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