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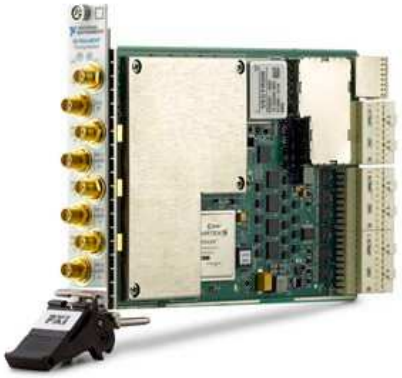
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Requirements and Compatibility | Detailed Specifications
For user manuals and dimensional drawings, visit the product page resources tab on ni.com.

Last Revised: 2014-11-06 07:13:54.0

NI PXIe-6674T

Timing and Synchronization Module



- Onboard routing of internal and external clock and trigger signals
- Synchronize multiple PXI Express and PXI chassis
- Onboard high-stability 10 MHz OCXO (50 ppb accuracy)
- High-resolution DDS clock generation, 0.3 Hz to 1 GHz
- Advanced trigger and timing routing with PXIe-DStar differential star trigger lines
- Use the traditional PXI Star trigger controller and PXI trigger bus control
- Discipline 10 MHz to GPS, IEEE 1588, or IRIG, when coupled with the NI PXI-6682H

Overview

The NI PXIe-6674T offers the most advanced timing and synchronization capabilities for PXI Express systems. The module generates and routes clocks and triggers between devices in a PXI Express chassis. In addition, it can route these signals to other PXI and PXI Express chassis as well as third-party instrumentation. The NI PXIe-6674T unlocks the advanced LVDS trigger buses, PXIe-DStarA, B, and C, on PXI Express while still fully supporting the PXI trigger bus, PXI_TRIG. The NI PXIe-6674T can generate two types of clock signals: a highly stable 10 MHz clock based on an onboard precision OCXO reference, and a second clock up to 1 GHz from the direct digital synthesis (DDS) clock generation circuit.

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Driver Information

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- LabVIEW
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- Measurement Studio Visual C++ Support

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Application and Technology

Functional Overview

The NI PXIe-6674T can help you enhance your PXI Express system applications. In addition to providing a precision, high-stability clock reference, this module offers the flexibility to route timing signals internal and external to your system. With the use of PXIe-DStar trigger signals, skew is minimized to less than 500 ps with delays as low as 10 ns. You can configure all of the programmable function interface (PFI) connectors on the front panel of the module as either single-ended or differential connections.

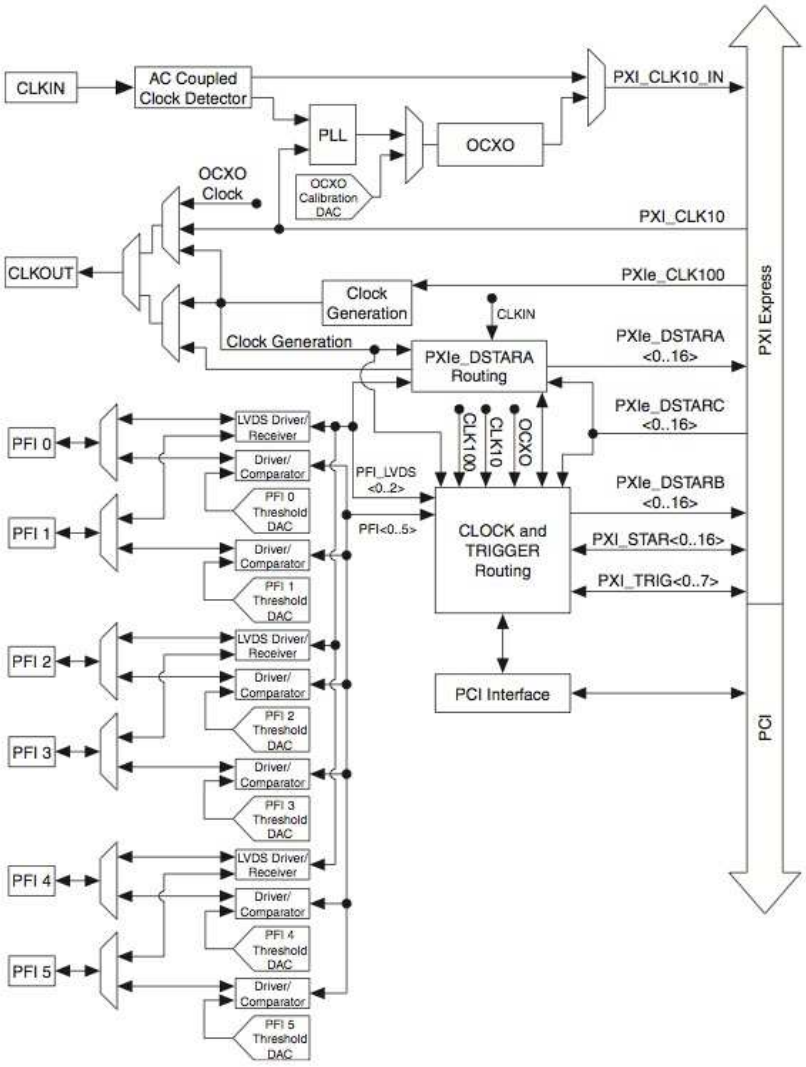


Figure 1. Functional Overview of the NI PXIe-6674T

High-Stability 10 MHz Reference

The NI PXIe-6674T overrides the built-in 10 MHz reference clock in a PXI Express chassis. Typically, most chassis provide a 10 MHz reference clock with 25 ppm accuracy (10 MHz, ±250 Hz). This accuracy is improved to 50 ppb (10 MHz, ±0.5 Hz) with the NI PXIe-6674T. Many modules, such as the NI PXIe-5xxx and PXI-5xxx, have phase-locked-loop (PLL) circuitry to synchronize with the 10 MHz reference clock. In addition to being highly accurate, the OCXO has increased stability over the built-in 10 MHz reference in the chassis, reducing the phase noise of the clock reference. Having the NI PXIe-6674T installed in your system improves the accuracy of your measurements.

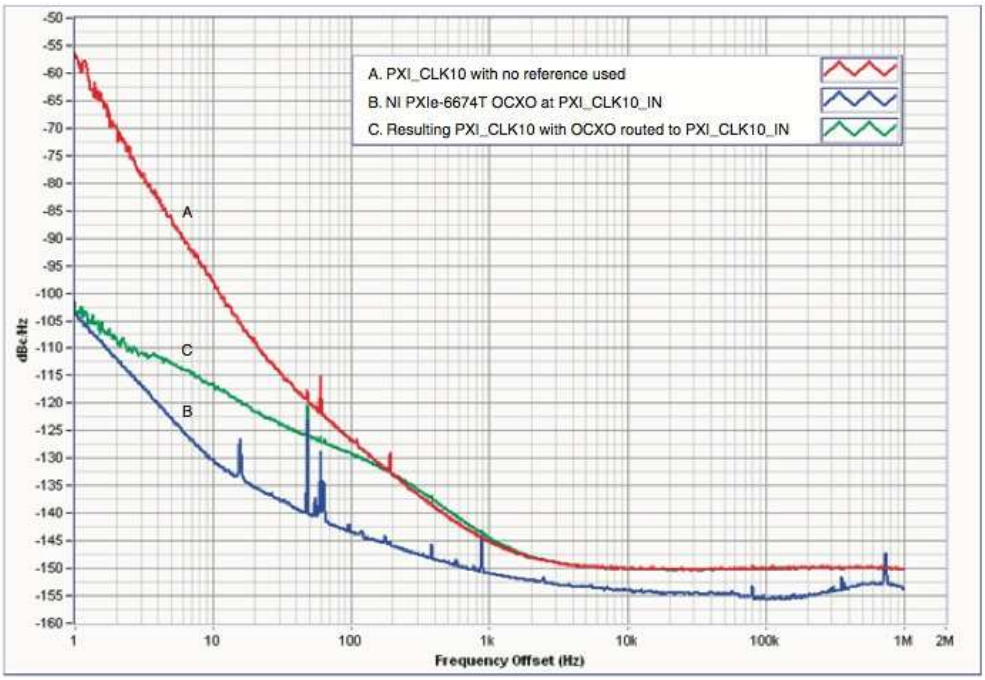


Figure 2. Phase Noise on a Representative Module of PXI_CLK10 When OCXO Is Routed to PXI_CLK10_IN

High-Resolution DDS Clock

The onboard direct digital synthesis (DDS) clock of the NI PXIe-6674T provides an extremely high-resolution programmable clock source that can generate clocks from 0.3 Hz to 1 GHz in frequency with microhertz resolution. Use this clock as a common timebase for a variety of other modules. You can distribute this clock via the DStar trigger lines or export them through a PFI line on the front panel.

Multichassis Synchronization

Using the combination of an NI PXIe-6674T in your master chassis and an NI PXIe-6674T or NI PXIe-6672 in each slave chassis, you can tightly synchronize multiple PXI Express chassis. In applications where your systems are distributed over large distances, you can couple the NI PXIe-6674T with the NI PXI-6682H module to synchronize your system with GPS, IEEE 1588, or IRIG-B. (For more information, see the Clock Disciplining product page.) With these modules, you can create high-channel-count synchronized systems for data acquisition, control, and instrumentation.

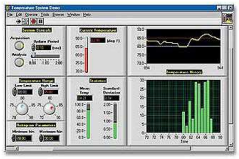
NI-Sync Software

The included NI-Sync driver software provides powerful and easy-to-use control of the NI timing and synchronization modules. You can use NI application development environments (ADEs) such as LabVIEW or LabWindows™/CVI or other ADEs such as Visual C/C++ for programming these modules. For example programs, visit ni.com/examples.

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Software Recommendations

LabVIEW Professional Development System for Windows



- Advanced software tools for large project development
- Automatic code generation using DAQ Assistant and Instrument I/O Assistant
- Tight integration with a wide range of hardware
- Advanced measurement analysis and digital signal processing
- Open connectivity with DLLs, ActiveX, and .NET objects
- Capability to build DLLs, executables, and MSI installers

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Support and Services

System Assurance Programs

NI system assurance programs are designed to make it even easier for you to own an NI system. These programs include configuration and deployment services for your NI PXI, CompactRIO, or Compact FieldPoint system. The NI Basic System Assurance Program provides a simple integration test and ensures that your system is delivered completely assembled in one box. When you configure your system with the NI Standard System Assurance Program, you can select from available NI system driver sets and application development environments to create customized, reorderable software configurations. Your system arrives fully assembled and tested in one box with your software preinstalled. When you order your system with the standard program, you also receive system-specific documentation including a bill of materials, an integration test report, a recommended maintenance plan, and frequently asked question documents. Finally, the standard program reduces the total cost of owning an NI system by providing three years of warranty coverage and calibration service. Use the online product advisors at ni.com/advisor to find a system assurance program to meet your needs.

Calibration

NI measurement hardware is calibrated to ensure measurement accuracy and verify that the device meets its published specifications. To ensure the ongoing accuracy of your measurement hardware, NI offers basic or detailed recalibration service that provides ongoing ISO 9001 audit compliance and confidence in your measurements. To learn more about NI calibration services or to locate a qualified service center near you, contact your local sales office or visit ni.com/calibration.

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Get answers to your technical questions using the following National Instruments resources.

- **Support -** Visit ni.com/support to access the NI KnowledgeBase, example programs, and tutorials or to contact our applications engineers who are located in NI sales offices around the world and speak the local language.
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Repair

While you may never need your hardware repaired, NI understands that unexpected events may lead to necessary repairs. NI offers repair services performed by highly trained technicians who quickly return your device with the guarantee that it will perform to factory specifications. For more information, visit ni.com/repair.

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NI offers options for extending the standard product warranty to meet the life-cycle requirements of your project. In addition, because NI understands that your requirements may change, the extended warranty is flexible in length and easily renewed. For more information, visit ni.com/warranty.

OEM

NI offers design-in consulting and product integration assistance if you need NI products for OEM applications. For information about special pricing and services for OEM customers, visit ni.com/oem.

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Detailed Specifications

This appendix lists the system specifications for NI PXIe-6674T modules. These specifications are typical at 25 °C, unless otherwise stated.

Note Specifications are subject to change without notice.

CLKIN Characteristics	
Input coupling	AC
Input impedance	50 Ω, nominal

Minimum and Maximum Input Levels		
Setting	**Attentuation Setting On**	**Attentuation Setting Off**
Attenuation Setting	On (default)	Off
Attenuation Behavior	5:1	1:1
Minimum Input Swing with 50% Duty Cycle*	750 mV_{pp}	150 mV_{pp}
Maximum Input Swing with 50% Duty Cycle†	5.0 V_{pp}	1.2 V_{pp}
Absolute Maximum Input Powered On‡	5.6 V_{pp}	2.8 V_{pp}
Absolute Maximum Input Powered Off**	1.5 V_{pp}	

* A duty cycle other than 50% will increase the minimum input swing. Refer to the first figure for more information.

† A duty cycle other than 50% will increase the minimum input swing. Refer to the second figure for more information.

‡ Operation above the Absolute Maximum Input Powered On may cause damage to the device.

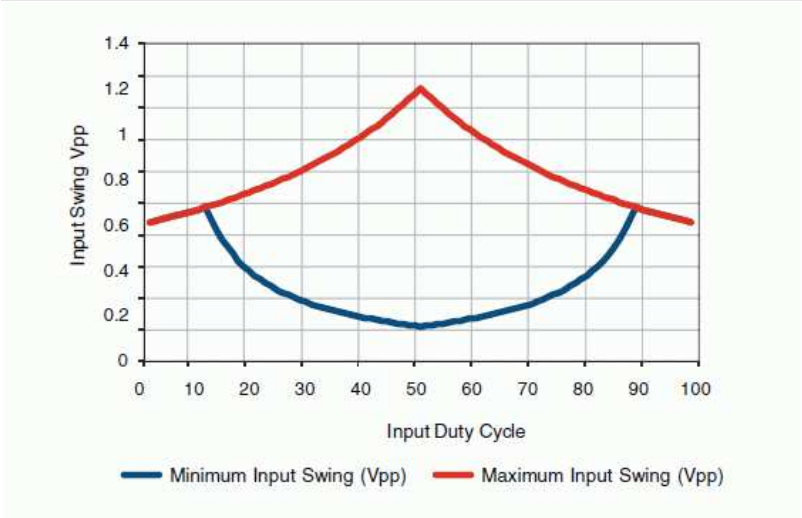
** Absolute Maximum Input Powered Off is the maximum input signal amplitude that the device can tolerate before damage might occur while in an unpowered state.

Note Input can be either square wave or sinusoidal.

Maximum and Minimum Input Swing with Attenuation On



Maximum and Minimum Input Swing with Attenuation Off



Minimum Frequency	1 MHz [1]
Maximum Frequency	
To Clk10PLL	100 MHz
To FPGA	200 MHz
To PXIe-DStarA	1 GHz
ClkIn to PXI_Clk10_In Delay (PLL not used)	
Typical at 25 °C	6.75 ns
Maximum over temperature	14.8 ns

OCXO

Nominal Frequency	10 MHz
Warm Up Time	3 minutes until ± 10 ppb of final frequency (1 hour reading) at 25 °C
24 Hour Frequency Accuracy [2]	± 5 ppb
Retrace [3]	± 1.5 ppb, typical
Short-term stability	±1 ppb/day
Long-term stability	±50 ppb/year
Versus Temperature	±5 ppb, referenced to 25 °C
Tuning Range	

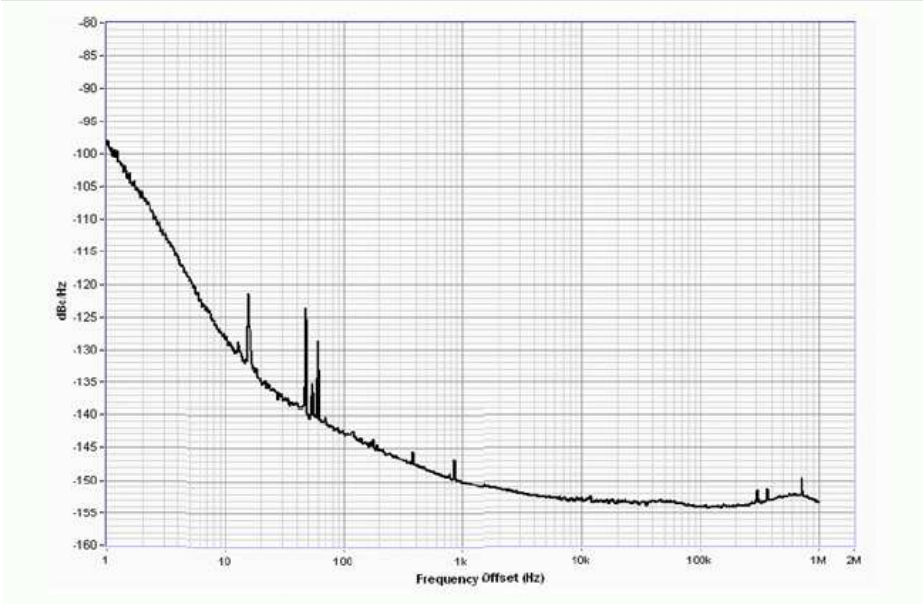
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		±1.5 ppm minimum, ± 2 ppm typical, ± 4 ppm max
Tuning DAC Resolution		16 bits, 0.0625 ppb per step typical
OCXO Tuning Calibration Interval		1 year

Maximum Phase Noise of the OCXO	
Offset	**Phase Noise**
1 Hz	–80 dBc/Hz
10 Hz	–120 dBc/Hz
100 Hz	–140 dBc/Hz
1 kHz	–145 dBc/Hz
10 kHz	–150 dBc/Hz

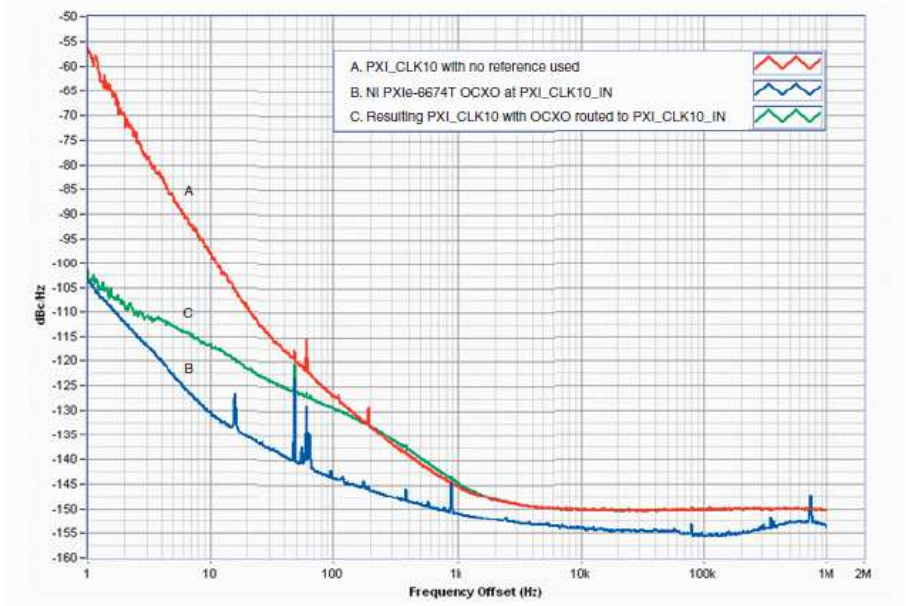
The following figure shows the phase noise on a representative module. OCXO is routed to the ClkOut SMA, measured in a PXIe-1082 chassis with low fan speed [4] . The integrated jitter from 10 Hz to 1 MHz is 507 fs rms.

Phase Noise on a Representative Module with OCXO Routed to ClkOut SMA



The following figure shows the phase noise on a representative module of PXI_CLK10 when OCXO is routed to PXI_CLK10_IN [5] , measured in a PXIe-1082 chassis with low fan speed:

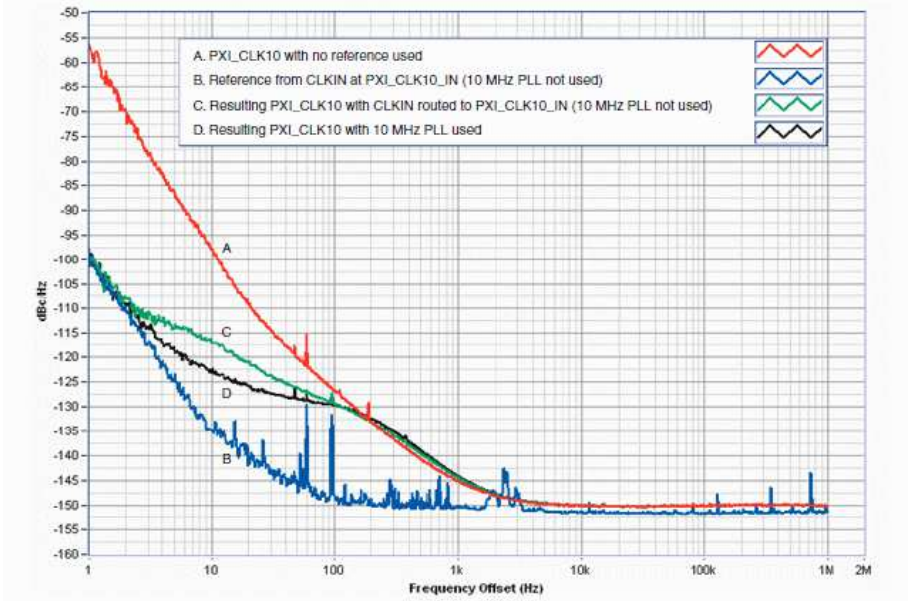
Phase Noise on a Representative Module of PXI_CLK10 when OCXO is routed to PXI_CLK10_IN



10MHz PLL	
Reference Frequency Range (from ClkIn)	1 MHz to 100 MHz, in increments of 1 MHz
Recommended ClkIn Frequency [6]	10 MHz
Reference Frequency Required Accuracy	± 1.5 ppm
Reference Frequency Duty Cycle	40% to 60%
PLL Loop Bandwidth	100 Hz

The following figure shows the phase noise on a representative module of PXI_CLK10 when CLKIN is routed to PXI_CLK10_IN with and without the 10 MHz PLL, measured in a PXIe-1082 chassis with low fan speed [5] .

Phase Noise on a Representative Module of PXI_CLK10 with CLKIN Routing to PXI_CLK10_IN



ClkOut

	Low Speed ClkOut	High Speed ClkOut
Coupling	AC Coupled	AC Coupled
Expected Termination	50 Ω or high impedance	50 Ω
Frequency Range	1 MHz to 50 MHz*	1 MHz to 1 GHz†
Typical Amplitude	2.57 V_{pp} into 50 Ω, 5 V_{pp} into high Z	800 mV_{pp}
Rising/Falling Edge (20%, 80%)	270 ps, typical	180 ps, typical
Duty Cycle of output with Clock Generation as source	45% to 55%	45% to 55%
Available Sources	PXI_CLK10, 10 MHz OCXO, Clock Generation up to 50 MHz	Clock Generation, PXIe-DStarA Network‡

* Operation of low speed ClkOut above 50 MHz is possible however NI does not guarantee performance. Use ClkOutLS as the destination terminal to force NI-Sync to use the low speed driver above 50 MHz.

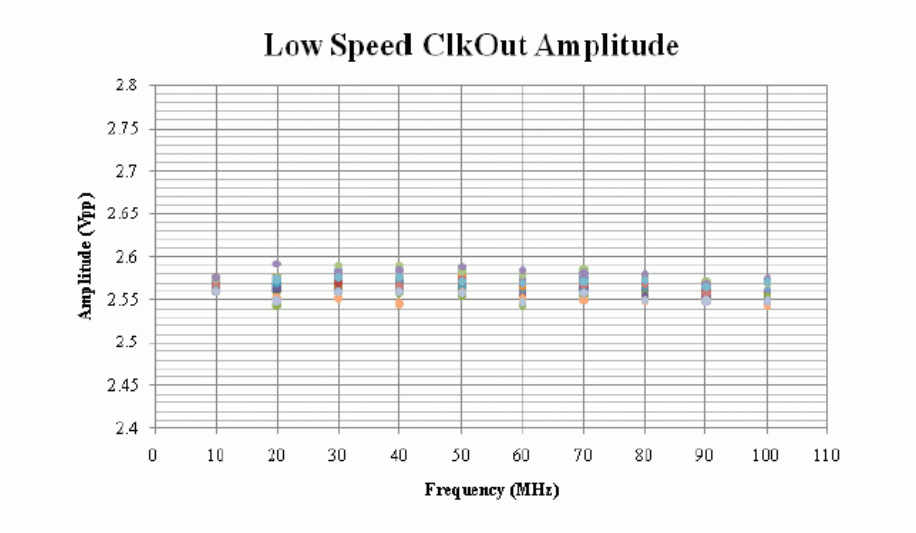
† Operation above 1 GHz is possible but NI does not guarantee performance.

‡ Routing PXIe-DStarA to ClkOut requires routing through either Banks 0, 1, or 2. Refer to the *Hardware Overview* chapter in the *NI PXIe-6674T User Manual* for additional information.

PXI_CLK10 to ClkOut Delay	
Typical at 25 °C	20.2 ns
Maximum over temperature	47.75 ns

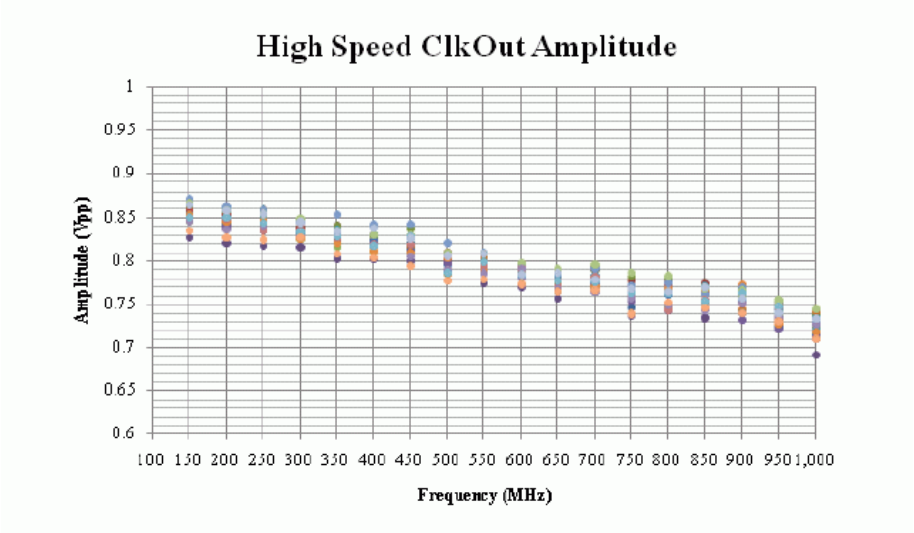
The following figure shows the typical Low Speed ClkOut Amplitude performance, with a sample size of 19 modules.

Typical Low Speed ClkOut Amplitude Performance



The following figure shows the typical High Speed ClkOut Amplitude performance, with a sample size of 19 modules.

Typical High Speed ClkOut Amplitude Performance



Clock Generation

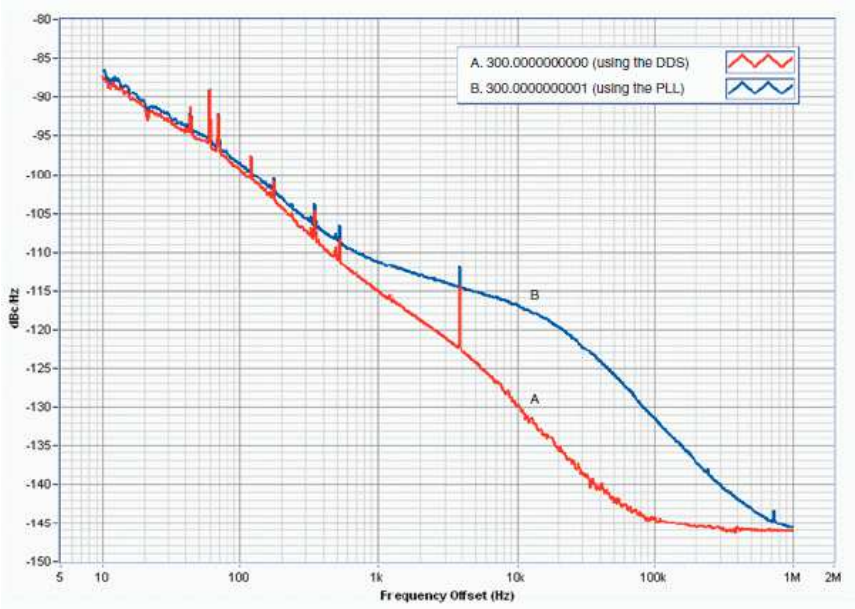
Reference Frequency Source [7]	PXIe_Clk100
Base Frequency Resolution (150 MHz to 300 MHz)	2.84217 µHz [8]
Minimum Generated Frequency [9]	
With FPGA divider	0.2794 Hz
Without FPGA divider	4.6875 MHz
Maximum Generated Frequency	1 GHz [10]

Clock Generation Phase Noise Performance

Note All Phase Noise Measurements were made on a Representative Module of various Clock Generation frequencies routed to ClkOut. All Measurement made in an NI PXIe-1062 chassis with low fan speed and OCXO connected to PXI_Clk10_IN.

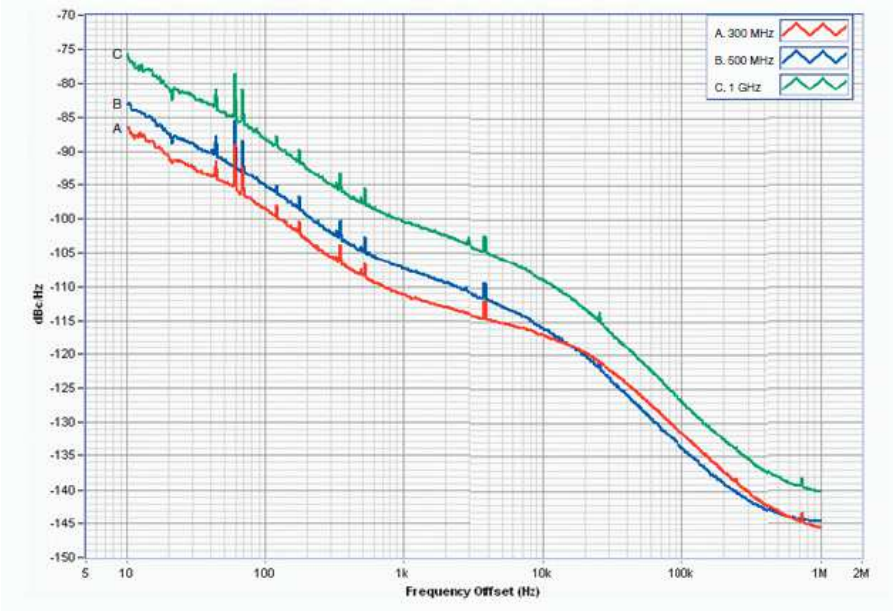
The phase noise performance of the clock generation circuitry varies depending on what elements are used to generate the requested frequency. To generate frequencies above 300MHz, a PLL is used to multiply the DDS frequency up which results in increased phase noise versus when the DDS is used directly (all frequencies below 300MHz).

Phase Noise Performance



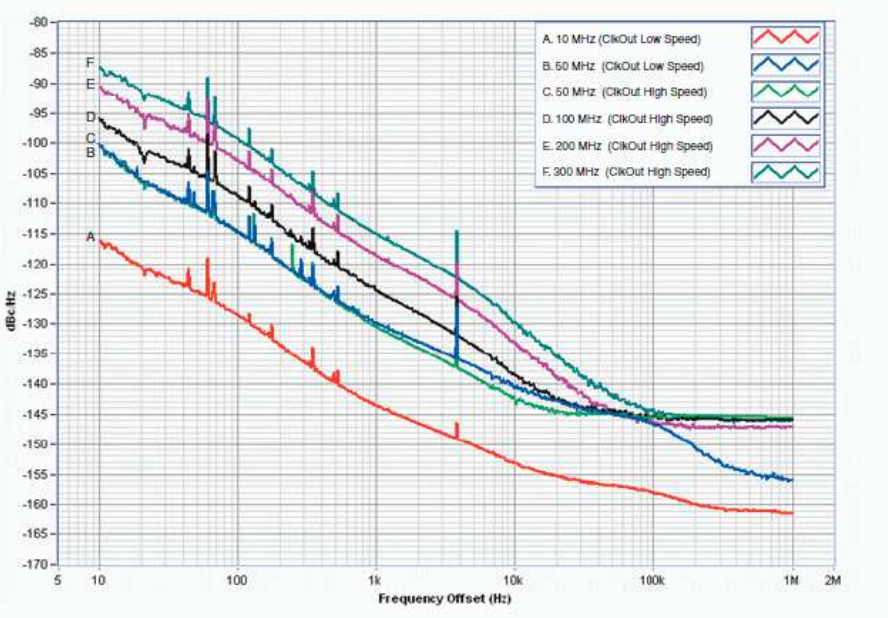
The following figure shows the phase noise of various frequencies coming from the multiplying PLL.

Phase Noise of Frequencies From the Multiplying PLL



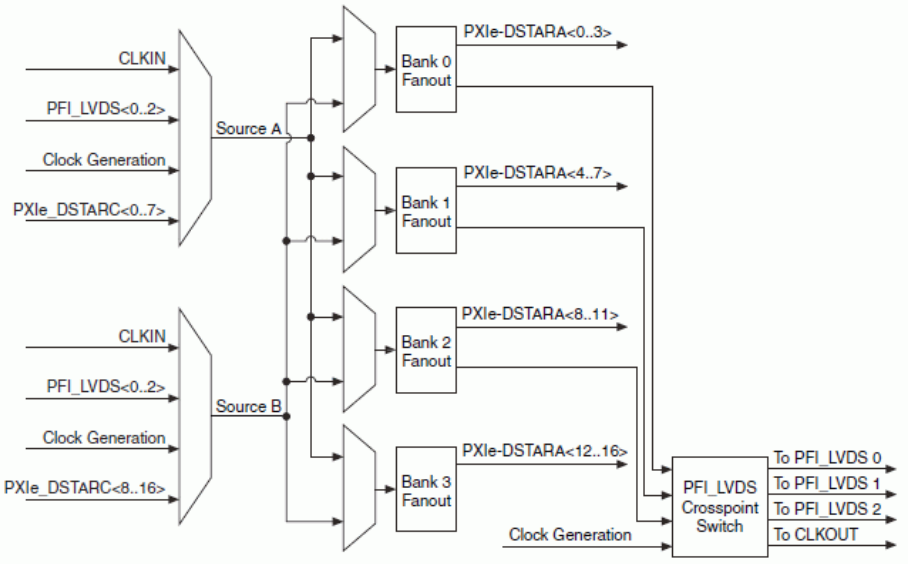
At 50 MHz, NI-Sync software will automatically switch between the high speed and low speed ClkOut drivers [11] . The phase noise performance of these two drivers differs, as shown in the following figure.

Phase Noise of Frequencies from DDS



PXIe-DStarA

PXIe-DStarA Topology



PXIe-DStarA Maximum Frequency	1 GHz [12]

PXIe-DStarA LVPECL Signal Characteristics			
	Minimum	Typical	Maximum
Voltage High Output	2.155 V	2.280 V	2.405 V
Voltage Low Output	1.355 V	1.530 V	1.700 V
Rise Time/Fall Time 20%, 80%	125 ps	180 ps	275 ps

ClkIn to PXIe-DStarA Delay	
Typical at 25 °C	4.21 ns
Maximum over temperature	4.36 ns
PXIe-DStarA to PXIe-DStarA Skew	
Typical	< 100 ps
Maximum over temperature	250 ps

Triggers

PFI Single Ended

Input Characteristics

Termination Setting	High Impedance	50 Ω
Input Impedance	10kΩ, ± 20%	50 Ω, ± 5%
Input Coupling	DC	DC
Hysteresis	50 mV typical	58 mV typical
Adjustable Threshold Range	15 mV to 3.795 V	16.8 mV 4.25 V
Adjustable Threshold Resolution	15 mV	16.8 mV
Adjustable Threshold Error*	± 5 mV	± 5 mV
Default Threshold Setting	1.005 V	1.008 V
Minimum Input Voltage Swing†	400 mV_{pp}	450 mV_{pp}
Frequency Range‡	DC to 150 MHz	DC to 150 MHz
Recommended Maximum Input Voltage Range	0.0 V to 5.0 V	0.0 V to 5.0 V
Maximum Input Voltage Range**	–0.5 V to 5.5 V	–0.5V to 5.5 V
PFI Open Circuit Voltage††	0.45 V, typical	N/A

* PFI Input switching behavior is a function of both the threshold setting and hysteresis.

† Input Voltage Swing below 400mV may be possible but performance is not guaranteed.

‡ Operation beyond 150MHz frequency may be possible but performance is not guaranteed.

** Voltages beyond the maximum range may cause damage to the device.

†† PFI line will float to 0.45V when configured in high impedance mode with no external signal connected as input.

Output Characteristics

Output Impedance	50 Ω, nominal
Output Coupling	DC
Output Voltage Range into 50 Ω load	0 V to 1.63 V, typical
Output Voltage Range into open load	0 V to 3.22 V, typical
Output Rising/Falling Edge into 50 Ω load	450 ps to 500 ps, 20%–80%, typical
Maximum Output Frequency*	DC to 150 MHz

* Operation beyond 150 MHz frequency may be possible but performance is not guaranteed.

PFI LVDS

Input Characteristics

Minimum Differential Input Voltage	100 mV_{pp}
Recommended Maximum Differential Input Voltage*	1 V
Maximum Input Voltage Range†	0 V to 4 V
Differential Input Resistance	100 Ω, ± 10%
Maximum Input Frequency—Routed to DStarA‡	1 GHz
Maximum Input Frequency—Routed to FPGA**	200 MHz

* Operation with greater voltage swing will not damage the device but performance characteristics are not guaranteed.

† Maximum Input Voltage Range is any combination of input voltage swing and common mode voltage. For example, a 200 mV differential swing with common mode voltage of 100 mV is acceptable as the lowest applied voltage to the input would be 0 V. A 200 mV differential swing with common mode less than 100 mV would cause the applied voltage to fall below 0 V and therefore would not be acceptable.

‡ Operation beyond 1 GHz is possible but performance is not guaranteed.

** Operation beyond 200 MHz is possible but performance is not guaranteed. This limitation comes from the FPGA, not the LVDS receiver.

Output Characteristics

Differential Output Voltage into 100 ohm differential load (at DC)	600 mV_{pp} typical
Output Common Mode Voltage	1.125 V to 1.375 V

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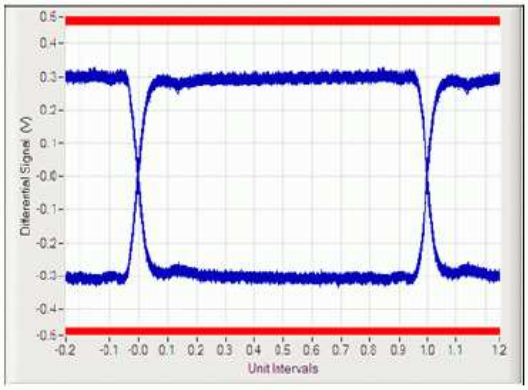
Maximum Output Frequency—Sourced from Cross Point Switch*	1 GHz
Maximum Output Frequency—Sourced from FPGA†	200 MHz
Differential Rise and Fall Time	180 ps, typical

* Operation beyond 1 GHz is possible but performance is not guaranteed.

† Operation beyond 200 MHz is possible but performance is not guaranteed. This limitation comes from the FPGA, not the LVDS driver.

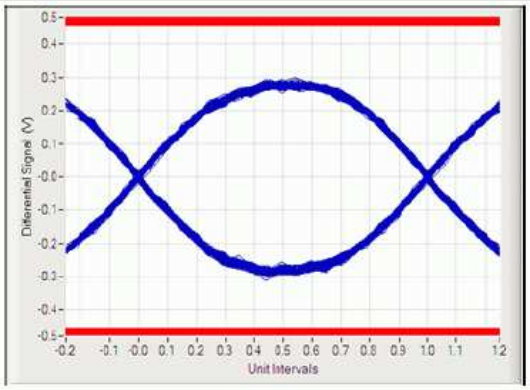
The following figure shows the representative LVDS output operating at 100 MHz. 1 unit interval in this figure equals 5 ns.

Representative LVDS Output Operating at 100 MHz



The following figure shows the representative LVDS output operating at 1 GHz. 1 unit interval in the figure equals 500 ps.

Representative LVDS output operating at 1 GHz



PXI-Triggers

I/O Voltage Level	3.3 V CMOS, 5 V input tolerant

PXI-Star

I/O Voltage Level	3.3 V CMOS, 5 V input tolerant

PXIe-DStarB

The PXIe-DStarB signals are LVDS signals that allow the NI PXIe-6674T to route high speed trigger signals to any other PXIe slot in a chassis. Each PXI Express slot in a chassis has its own PXIe-DStarB connection with the System Timing Slot.

By default, these are driven logic low until configured by software.

Maximum operating frequency	200 MHz

PXIe-DStarC

The PXIe-DStarC signals are LVDS signals that come from other PXI Express slots in a chassis. Each PXI Express slot in a chassis has a PXIe-DStarC connection with the System Timing Slot. These allow other modules in a PXIe-Chassis to share a trigger or clock signal with the NI PXIe-6674T. The NI PXIe-6674T can connect a signal received through PXIe-DStarC to the PXIe-DStarA network (when sharing a clock signal) or treat the PXIe-DStarC as a trigger source.

Maximum operating frequency when used with the PXIe-DStarA network	1 GHz
Maximum operating frequency when used for triggering	200 MHz

Trigger Timing

Asynchronous Trigger Delays and Skew

Asynchronous Trigger Delays and Skew Values			
Trigger Source	**Trigger Destination**	**Typical Delay***	**Typical Skew†**
Single Ended PFI	Single Ended PFI	23.4 ns	< .5 ns
Single Ended PFI	LVDS PFI	22.4 ns	< .5 ns
Single Ended PFI	PXI-Trigger	38.7 ns	< 1.5 ns
Single Ended PFI	PXI-Star	26.8 ns	< .75 ns
Single Ended PFI	PXIe-DStarB	23.2 ns	< .5 ns
LVDS PFI	Single Ended PFI	13.7 ns	< .5 ns
LVDS PFI	LVDS PFI	11.8 ns	< .5 ns
LVDS PFI	PXI-Trigger	28.9 ns	< 1.5 ns
LVDS PFI	PXI-Star	17.5 ns	< .75 ns
LVDS PFI	PXIe-DStarB	13.8 ns	< .5 ns
PXI-Trigger	Single Ended PFI	17.8 ns	< .5 ns
PXI-Trigger	LVDS PFI	16.6 ns	< .5 ns
PXI-Trigger	PXI-Trigger	33.8 ns	< 1.5 ns
PXI-Trigger	PXI-Star	21.0 ns	< .75 ns
PXI-Trigger	PXIe-DStarB	15.9 ns	< .5 ns
PXI-Star	Single Ended PFI	17.0 ns	< .5 ns
PXI-Star	LVDS PFI	15.6 ns	< .5 ns
PXI-Star	PXI-Trigger	26.2 ns	< 1.5 ns
PXI-Star	PXI-Star	20.2 ns	< .75 ns
PXI-Star	PXIe-DStarB	16.0 ns	< .5 ns
PXIe-DStarC	Single Ended PFI	13.6 ns	< .5 ns
PXIe-DStarC	LVDS PFI	7.2 ns	< .5 ns
PXIe-DStarC	PXI-Trigger	28.1 ns	< 1.5 ns
PXIe-DStarC	PXI-Star	16.8 ns	< .75 ns
PXIe-DStarC	PXIe-DStarB	13.0 ns	< .5 ns

* Typical Delay is measured from the input to the PXIe-6674T at the connector to the output at the connector. For example, Single Ended PFI to PXI-Star is the delay from the Single Ended PFI SMA connector to the PXI-Star at the backplane connector.

† Typical Skew is defined as the difference in arrival time of a rising edge on a common source to two or more outputs within a trigger destination, as seen as the connector. For example, if Single Ended PFI(0) is asynchronously routed to all PXI-Star lines, the typical skew would be less than .75 ns.

Synchronized Trigger PXI_Clk10 to Out

Trigger Destination	Clock to Out Time*
Single Ended PFI	11.2 ns Typical, 19.9 ns Max
LVDS PFI	9.8 ns Typical, 14.8 ns Max
PXI-Trigger	28.2 ns Typical, 30.2 ns Max
PXI-Star	14.8 ns Typical, 24.5 ns Max
PXIe-DStarB	9.4 ns Typical, 14.0 ns Max

* Clock to Out Time is the amount of time it takes for a logic change on a synchronous trigger to appear (at the connector) with respect to the rising edge of PXI-Clk10 (at the backplane connector) that it is synchronized to. Refer to the *Hardware Overview* chapter in the *NI PXIe-6674T User Manual* for additional information.

Synchronized Trigger Setup and Hold Timing with Respect to PXI-Clk10

Trigger Source	Trigger Destination	Setup Time*	Hold Time†
Single Ended PFI	Single Ended PFI	11.2 ns Typical, 13.2 ns Max	–8.2 ns Typical, 1.1 ns Max
Single Ended PFI	LVDS PFI	11.2 ns Typical, 13.5 ns Max	–8.5 ns Typical, 0.8 ns Max
Single Ended PFI	PXI-Trigger	11.3 ns Typical, 14.2 ns Max	–7.5 ns Typical, 1.3 ns Max
Single Ended PFI	PXI-Star	11.2 ns Typical, 13.1 ns Max	–6.9 ns Typical, 2.0 ns Max
Single Ended PFI	PXIe-DStarB	13.2 ns Typical, 15.4 ns Max	–9.8 ns Typical, –0.4 ns Max
LVDS PFI	Single Ended PFI	0.6 ns Typical, 4.0 ns Max	0.4 ns Typical, 3.9 ns Max
LVDS PFI	LVDS PFI	–0.3 ns Typical, 4.3 ns Max	1.2 ns Typical, 3.5 ns Max
LVDS PFI	PXI-Trigger	–0.2 ns Typical, 3.6 ns Max	1.1 ns Typical, 5.0 ns Max

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Trigger Source	Trigger Destination	Setup Time*	Hold Time†
LVDS PFI	PXI-Star	–0.1 ns Typical, 3.7 ns Max	1.4 ns Typical, 5.0 ns Max
LVDS PFI	PXIe-DStarB	2.1 ns Typical, 5.7 ns Max	–0.5 ns Typical, 2.6 ns Max
PXI-Trigger	Single Ended PFI	11 ns Typical, 17.5 ns Max	–9.5 ns Typical, –4.8 ns Max
PXI-Trigger	LVDS PFI	10.9 ns Typical, 18.1 ns Max	–9.8 ns Typical, –5.4 ns Max
PXI-Trigger	PXI-Trigger	10.1 ns Typical, 17.0 ns Max	–7.8 ns Typical, –3.6 ns Max
PXI-Trigger	PXI-Star	9.7 ns Typical, 16.2 ns Max	–7.4 ns Typical, –3.1 ns Max
PXI-Trigger	PXIe-DStarB	10.7 ns Typical, 17.8 ns Max	–9.0 ns Typical, –5.1 ns Max
PXI-Star	Single Ended PFI	3.9 ns Typical, 10.9 ns Max	–2.5 ns Typical, –0.5 ns Max
PXI-Star	LVDS PFI	3.9 ns Typical, 11.1 ns Max	–3.1 ns Typical, –0.8 ns Max
PXI-Star	PXI-Trigger	2.7 ns Typical, 9.9 ns Max	–0.9 ns Typical, 0.9 ns Max
PXI-Star	PXI-Star	2.0 ns Typical, 9.6 ns Max	–0.1 ns Typical, 1.1 ns Max
PXI-Star	PXIe-DStarB	4.3 ns Typical, 11.7 ns Max	–2.4 ns Typical, –1.1 ns Max
PXIe-DStarC	Single Ended PFI	0.5 ns Typical, 3.9 ns Max	0.4 ns Typical, 3.7 ns Max
PXIe-DStarC	LVDS PFI	–0.3 ns Typical, 4.4 ns Max	0.5 ns Typical, 3.1 ns Max
PXIe-DStarC	PXI-Trigger	–1.1 ns Typical, 2.8 ns Max	1.9 ns Typical, 5.2 ns Max
PXIe-DStarC	PXI-Star	–0.5 ns Typical, 3.2 ns Max	3.1 ns Typical, 4.9 ns Max
PXIe-DStarC	PXIe-DStarB	1.3 ns Typical, 5.6 ns Max	0.2 ns Typical, 2.4 ns Max

* Setup Time is the amount of time before a rising edge of PXI-Clk10 (at the backplane connector) that a logic level must be valid on the trigger source (at the connector) in order for the trigger destination to update. Refer to the *Hardware Overview* chapter in the *NI PXIe-6674T User Manual* for additional information.

† Hold Time is the amount of time after a rising edge of PXI-Clk10 (at the backplane connector) that a logic level must be valid on the trigger source (at the connector) in order for the trigger destination to update. Refer to the *Hardware Overview* chapter in the *NI PXIe-6674T User Manual* for additional information.

FPGA Functionality

Trigger Routing

The following table shows the routes that can be made.

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		Destinations									
		Front Panel			Backplane						On board
		CLK OUT	PFI <0..5>	PFI LVDS <0..2>	PXI CLK 10 IN	PXI Star Trigger <0..16>	PXI TRIG <0..7>	PXIe SYNC CTRL	D STARA <0..16>	D STARB <0..16>	OCXO Ref PLL
Sources: Front Panel	CLK IN	✓	✓†	✓†	✓	✓†	✓†		✓	✓†	✓
Sources: Front Panel	PFI <0..5>		✓	✓		✓	✓	✓		✓	
Sources: Front Panel	PFI LVDS <0..2>		✓	✓		✓	✓	✓	✓	✓	
Sources: Backplane	PXI CLK 10	✓	✓†	✓†		✓†	✓†			✓†	
Sources: Backplane	PXI CLK 100	✓	✓†	✓†		✓†	✓†			✓†	
Sources: Backplane	PXI STAR <0..16>		✓	✓		✓	✓	✓		✓	
Sources: Backplane	PXI TRIG <0..7>		✓	✓		✓	✓	✓		✓	
Sources: Backplane	DSTARC <0..16>		✓	✓		✓	✓	✓	✓	✓	
Sources: Onboard	OCXO	✓	✓†	✓†	✓	✓†	✓†			✓†	
Sources: Onboard	Clock Gen	✓	✓†	✓		✓†	✓†		✓	✓†	
Sources: Onboard	Global Software Trigger		✓	✓		✓	✓	✓		✓	

† Routing PXI_CLK10, PXIe_CLK100, OCXO or ClkGen is accomplished by setting the synchronization clock (NI-Sync Property Node) to the desired clock source and then routing the synchronization clock as the source.

Route through the FPGA.

Route to PFI LVDS can be made through the FPGA when used as a trigger, or through the PXIe-DTARA network when used as a clock.

Frequency Measurement	
Maximum Measurable Frequency [13]	200 MHz
Reference Counter Source [14]	PXIe_Clk100
Frequency Counter Sources	All Trigger inputs plus Clock In and the OCXO
Trigger Sync Clock	
Two independent synchronization clock zones: ▪ Front Synchronization Clock for PFI Single Ended and PFI LVDS ▪ Rear Synchronization Clock for PXI-Star, PXI-Trigger, and PXIe-DStarB	
Synchronization Clock Sources	PXI_Clk10, PXIe_Clk100, Clock In, OCXO, and Clock Generation
Two division ratios can be specified in powers of 2 from 2 to 512. These ratios are used in all synchronization clock zones to divide down the selected full speed synchronization clock.	
Physical	
Chassis requirement	One 3U PXI Express slot (system timing slot)
Front panel connectors	Eight SMA female, 50 Ω
Front panel indicators	Two tricolor LEDs (green, red, and amber)
Power Requirements	
+3.3 V	2.54 A, max
+12 V	2.25 A, max
+5 VAUX	0 A, max

Environmental

Operating Environment	
Ambient temperature range	0 to 55 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC-60068-2-56.)
Maximum altitude	2,000 m
Pollution Degree	2
Indoor use only	
Storage Environment	
Ambient temperature range	–40 to 71 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC-60068-2-56.)

Shock and Vibration

Operational Shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)
Random Vibration	
Operating	5 to 500 Hz, 0.3 g_{rms}
Nonoperating	5 to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Caution Clean the NI PXIe-6674T module with a soft nonmetallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Note Specifications are subject to change without notice.

Safety Standards

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note For EMC declarations and certifications, refer to the *Online Product Certification* section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

To obtain product certifications and the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

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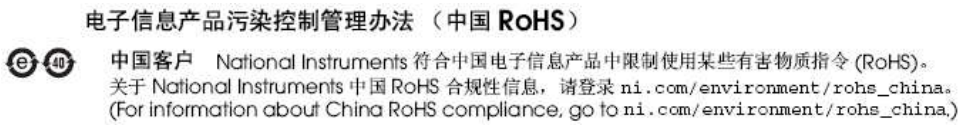
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[1] The minimum frequency is limited by AC coupling.

[2] 24 Hour Frequency Accuracy refers to the 24 hour period after calibration. It includes error from frequency measurement and error from frequency reference.

[3] Retrace accounts for error in the ability of the OCXO to return to a set frequency after a period of being powered off.

[4] OCXO also driven to PXI_CLK10_IN.

[5] The PXIe backplane employs a PLL to phase lock PXI_CLK10 to the signal on PXI_CLK10_IN. As a result, the phase noise of PXI_CLK10 above about 1 kHz offset is unchanged, regardless of reference used.

[6] 10 MHz PLL filter is designed for a 10 MHz phase detector frequency. Any other reference frequency will default to a phase detector frequency of 1 MHz resulting in a slight degradation of PLL performance.

[7] Frequency Accuracy is inherited from PXIe_Clk100/PXI_Clk10. Use OCXO for PXIe_Clk100/PXI_Clk10 replacement for improved frequency accuracy and phase noise.

[8] This is the frequency resolution of the DDS used in the Clock Generation circuitry. For Clock Generation frequencies below 150 MHz, this resolution is divided down and for frequencies above 300 MHz, this resolution is multiplied up. Refer to the *Hardware Overview* chapter in the *NI PXIe-6674T User Manual* for additional information.

[9] When routed to ClkOut Low Speed or used as a trigger synchronization clock, Clock Generation can be further divided by the FPGA by factors of two up to 24. This extends the Clock Generation range down to 4.6875 MHz/2^{24}=.2794 Hz. When routed to ClkOut High Speed the minimum frequency is 4.6875 MHz. Use ClkOutHS as the destination terminal to force NI-Sync to use the low speed driver below 50 MHz. Note that AC coupling on ClkOut limits the minimum frequency which can be used.

[10] Clock Generation can be operated beyond the upper limit; however, NI does not guarantee performance beyond 1 GHz. 2 GHz is the maximum output frequency by design.

[11] Use ClkOutHS as the destination terminal to force NI-Sync to use the high speed driver below 50 MHz.

[12] Maximum Frequency may exceed 1 GHz however performance is not guaranteed.

[13] Operation beyond 200 MHz is possible but performance is not guaranteed.

[14] Accuracy of frequency measurement is relative to the frequency accuracy of the reference counter source. The frequency measure vi in NI-Sync does not account for error from the reference source.

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