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VICB8001 VME 64x DIGITAL IO AND INDUSTRY PACK CARRIER BOARD

USERS MANUAL

For Issue 3 PCB with FPGA Version 8001V305 – 8001V309 SPROMS (512Kbytes)

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WARNING

It is important to note that all cards in a crate must use the same geographical address lines and VME address lines in their decoding of extended memory addresses.

If this is not observed a VME bus clash may occur (see section 3.2).

1. INTRODUCTION

1.1 Key Features

- VME64 extensions digital I/O system component/ Industry Pack Carrier Board
- VME64x rear panel I/O
- Full EMC shielding and insertion/extraction handles
- Fully Hot-Swap capable with auto power-up and host interaction
- 6U VME base card handles 64 signals plus strobes and can operate as input, output or mixed function, depending on transition board.
- Input unit features change-of-state and contact de-bounce
- On board memory allows tracing of changes through time or Memory Driven digital outputs
- Selectable Internal or External clock from front panel or transition card (max 1MHz)
- Software selectable scan rates from 1MHz down to 1KHz
- External clock can be divided down by 1000, 100, 10 and 1 using software
- 3.3 Volts connected to P2 (Not Hot Swap).
- Interrupt release settable ROAK or RORA.
- User selectable VME interrupt level
- Geographical addressing
- Front panel TTL input to IP cards via Strobe lines
- Eight input/output strobes via transition card
- Thickened I/O lines to allow externally power supply to IPs
- VME 64x Configuration ROM
- On-board clock generation
- VME64x guide pin and slot keying
- 8MHz IP interface
- Two IP sites for extra functionality
- EPICS software driver and LabView code available.

1.2 Product Overview

The 8001 is a 6U (double height) VME board which handles 64 digital signals. The module can be configured using rear mounted transition cards (auto detectable) to work as either 64 digital inputs, 64 digital outputs or 32 digital inputs and outputs. The module features change-of-state detection and contact debounce. The on board memory of the 8001 allows for continuous tracing of the changes of state through time for sequence detection and analysis or to output a digital pattern from memory either as a single shot or as a repeated pattern. The number of output sequences per channel can be programmed up to 64k or 256k.

The unit is constructed to the VME64x standard, with EMC front panel, injector/ejector handles, guide pin and slot keying, static discharge protection, hot swap capability, geographical addressing, 5-row P1 and P2 connectors and 5-row P0 connector.

The 64 TTL signals plus 8 strobes are connect to the 8001 board according to the VME64x Greenspring pin-out for IP module carriers (to maintain compatibility).

The input states are latched and examined at a programmable rate up to 1MHz and stored in a RAM 64k or 256k deep per input. The input states are debounced at a programmable rate (including OFF) and changes detected. A VME interrupted can be generated if a change of state has occurred.

The function of the eight input/output strobes is programmable, including their use as a sample clock. There are two TTL inputs on the front panel for similar functions including history acquisition stop/start.

A micro-switch in one of the handles detects insertion/removal and a hot-swap controller powers the unit smoothly up and down without disturbing the rest of the system. Host interaction during insertion/removal is in accordance with the VME64x specification.

There are two IP sites on the board addressable on an individual basis which replace part of the input path (i.e. they take over the 32 IO lines). Addressing and handling of these IP sites is programmable through base control and status registers, including address offsets and interrupt mapping.

The unit supports addressing in A16/D32/D16/D08(EO), A24/D32/D16/D08(EO) and A32/D32/D16/D08(EO) modes as well as BLT32. The registers and 'history' memory can be read at any time but BLT32 is inhibited while sampling into or out of memory is active.

2. PRODUCT SPECIFICATIONS

2.1 Power Requirements

+5V @ IP dependent up to 3amps.
+12V @ IP dependent up to 2 amps.
-12V @ IP dependent up to 2 amps.

2.2 Operating Temperature Range

0 to +45 deg Celsius ambient.

2.3 Mechanical

6U single width VME module with access to 5 row P0, P1 and P2 connectors.

2.4 Front Panel Indicators

'VME' LED (green)illuminates for a minimum of 100msecs whenever the module is accessed via the VME bus.

'Not Configured' LED (blue) indicates the status of the VME module (ON = Not configured).

'EXT CLOCK' LED (yellow) illuminated when the front panel external clock is enabled (This is not illuminated when external clock is derived from the transition card via STROBE IN 1).

'IP ACK A/B' LED (red) illuminated by IP card on Data Acknowledge.

2.5 Signal Specifications

2.5.1 External

Clocks in the input data at 1MHz maximum.

Front Panel

Connector type: LEMO 0302
Signal: Single-ended TTL.

Transition Card

Clock in via Strobe IN 1

2.5.2 Inhibit Connector type: LEMO 0302

Suspends history memory update (active low).

Front Panel

Connector type: LEMO 0302
Signal: Single-ended TTL.
The front panel Inhibit can also be connected to the IP A and B Strobe lines by jumper connection.

Transition Card

Strobe IN 2, Strobe IN 3 and Strobe IN 4

2.5.3 Digital Inputs/Outputs 0-63

Connector type: P0 and P2 5 row VME connectors
Signal: Single-ended TTL

3. USE OF THE VME DATA BUS AND MEMORY ACCESS

3.1 VME Addressing

The module uses A16/D32/D16/D8 (EO) (Even and Odd byte) or A24/D32/D16/D8 (EO) for accesses to the IP I/O, IP ID and Carrier board Configuration Registers.
The base address of the carrier board configuration registers is determined either by PCB jumper settings (J6 to J10) or by geographical addressing lines GA0 to GA4.
The PCB jumpers are used only where geographical addressing is not available and will override the GA lines.

Address	Offset	Range	Assignment	Size
I/O Base+	0x0000	0x0000 0x007F	IP A I/O Space	128 Bytes
I/O Base+	0x0080	0x0080 0x00FF	IP A ID Space	128 Bytes
I/O Base+	0x0100	0x0100 0x017F	IP B I/O Space	128 Bytes
I/O Base+	0x0180	0x0180 0x01FF	IP B ID Space	128 Bytes
I/O Base+	0x0400	0x0400 0x047F	Carrier on-board registers	128 Bytes
I/O Base+	0x0600	0x0600 0x07FF	Carrier Configuration ROM Space (See appendix B)	512 Bytes

8001 I/O A16 and A24 D16 Address Map

3.1.1 Short Addressing (A16 AM29h and 2Dh)

In Short address mode the geographical addressing lines equate to the address lines GA0 =A11 to GA4=A15 and the jumper address setting J6=A11 to J10=A15.
A11 - A15 is the module address determined by the setting of the relevant PCB jumpers or geographical address lines.
IP I/O, IP ID and Carrier board Configuration Registers:
AM29 Short (A16) non-privilege
AM2D Short (A16) supervisory

3.1.2 Standard Addressing (A24 AM39h and 3Dh)

The A24 base address is determined either by PCB jumper settings J6=A19 to J10=A23 or by geographical addressing lines GA0 =A19 to GA4=A23.
IP I/O, IP ID and Carrier board Configuration Registers:
AM39 Standard (A24) non-privilege
AM3D Standard (A24) supervisory

3.1.3 Carrier board Configuration ROM (A24 AM2Fh)

See **appendix B** for the contents of the configuration ROM.
Address modifiers
AM2F Configuration ROM/Control & Status Registers.

3.2 Memory Access

The module uses A32/D32/D16/D8 (EO) (Even and Odd byte) for accesses to on board memory. For IP memory the module uses A32/D16/D8(EO).
The base address of the memory can be set by either the Geographical address lines/jumpers or by using the Memory Offset Register. Writing a 1 to bit 6 of the CSR CB (base+8h) selects the Memory Offset Register to set the base address
Using the Memory Offset Register to store the base address allows the address lines A22 to A31 to be used to set the base address.
Geographical addressing uses the lines GA0=A22 to GA4=A26 (A27 to A31 are not decoded).
First need to select whether Geographical address lines or the Memory Offset register are to define the extended memory start address. This is selected using MEM MODE (bit 6) of the CSR CB register.

MEM MODE (bit 6 CSR_CB)	**Memory Addressing Mode**
0	Geographical address lines A22-A26
1	Memory Offset register A22-A31

Bit 6 CSR CB setting the memory address mode

3.2.1 Carrier Board Memory Map

Address	Offset	Range	Assignment	Size
Memory Base +	0x000000	0x000000 0x0FFFFF	IP A Memory Space	1Megabytes
Memory Base +	0x100000	0x100000 0x1FFFFF	IP B Memory Space	1Megabytes
Memory Base +	0x200000	0x200000 0x3FFFFF	Carrier on board memory	2Megabytes Or 512kb

8001 carrier board memory map

3.3 BLT Memory Access

The unit also supports 32 bit VME block transfer mode BLT for memory access.

3.4 Memory Address Modifiers

Memory: AM09 or AM0D (extended non-priv. or supervisory)
BLT: AM0B or AM0F (extended non-priv. or supervisory)

WARNING

It is important to note that all cards in a crate must use the same geographical address lines and VME address lines in their decoding of extended memory addresses.

i.e. all boards must use Geographical address lines A22-A26. If this is not observed a VME bus clash may occur.

4. ON-BOARD FEATURES

The configuration and control of the 8001 module is via registers:

Base	Offset	Register	Description
Base +	0x400	IRQ Vector	VME interrupt vector address
Base +	0x404	Memory Offset	Sets base address of memory
Base +	0x408	Control & Status Register CB	Set up of VME & IP side of the 8001
Base +	0x40C		
Base +	0x410	IP Status	Allows state of IP ints and error flags to be monitored
Base +	0x414	Control & Status Register IO	Set up of I/O part of 8001
Base +	0x418	Mask Register Low	Select bits of bottom 32 bits of digital input to mask
Base +	0x41C	Mask Register High	Select bits of top 32 bits of digital input to mask
Base +	0x420	Debounce Bit Register Low	Select bits of bottom 32 bits of digital input to debounce
Base +	0x424	Debounce Bit Register High	Select bits of top 32 bits of digital input to debounce
Base +	0x428	Last Known Change Low	Holds the last change of bottom 32 bits of input
Base +	0x42C	Last Known Change High	Holds the last change of top 32 bits of input
Base +	0x430	Memory Address Counter	Holds the address to be written/read

8001 On-Board Registers

4.1 IRQ Vector (Read/Write)

Address: Read = Base + 0x400, Write = Base + 0x400

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V09	V08	V07	V06	V05	V04	V03	V02	V01	V00

4.2 Memory Offset (Read/Write)

Address: Read = Base + 0x404, Write = Base + 0x404

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	x	x	x	x	x	x

['x' = don't care]

4.3 Control & Status Register Carrier Board (CSR CB)

Control (Write)
Address: Base + 0x408

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
NU	NU	NU	NU	NU	INT REL	IPB INT0	IPA INT0	EXT INT	MEM MODE	NU	INTSEL 2	INTSEL 1	INTSEL 0	INTEN	Rst

Status (Read)
Address: Base + 0x408

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
T0	T1	T2	HYTEC IP	MEM SIZE	INT REL	IPB INT0	IPA INT0	EXT INT	MEM MODE	NU	INTSEL 2	INTSEL 1	INTSEL 0	INTEN	Rst

RST Writing '1' to this bit clears the CSR CB and the CSR I/O registers to zero.
INTEN This enables interrupts from IO change of state & IP card interrupts.
INTSEL0 Select VME interrupt line – 3-bit code: '000' No VME interrupt line selected.
INTSEL1 Select VME interrupt line
INTSEL2 Select VME interrupt line
MEMMODE Select memory base address to be defined by geographical address lines = '0' or by Memory offset register = '1'.
EXT INT Front Panel Inhibit/Transition board Strobe lines Interrupt Enable. Enable = '1'.
IP A INT 0 Enable IP A interrupt line 0.
IP B INT 0 Enable IP B interrupt line 0.
INT REL Interrupt Release Signal. '0' = RORA, '1' = ROAK.
MEMSIZE The Size of the onboard memory '1' = 128k x 32; '0' = 512k x 32 (Read only).
HYTECIP Reflects Status of the Jumper J1, should be set to '1' if Hytec Dual IP Width Digital I/O card fitted in IP sites A and B or '0' for all other IP Cards. (Read only).
T2 Denotes transition card type (Read only).
T1 Denotes transition card type (Read only).
T0 Denotes transition card type (Read only).

4.4 IP Status Register (Read Only)

Address: Base + 0x410

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	ERR B	ERR A	0	0	0	0	0	0	INT B 0	INT A 0

Shows the status of the IP cards (if used).

4.5 Control Status Register Digital IO (CSR IO)

Control (Write)
Address: Base + 0x414

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
COS BIT	IO INT EN	SCAN INH	Ring Mode	OM1	OM0	MEM EN	SH1	SH0	SCAN T1	SCAN T0	COS T1	COS T0	SCLK SEL1	SCLK SEL0	SCAN EN

Status (Read)
Address: Base + 0x414

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
COS BIT	IO INT EN	SCAN INH	Ring Mode	OM1	OM0	MEM EN	SH1	SH0	SCAN T1	SCAN T0	COS T1	COS T0	SCLK SEL1	SCLK SEL0	SCAN EN

SCAN EN Start scanning digital inputs or memory driven outputs.
SCLK SEL 0-1 Select source of scan clock: '00' = Internal clock; '01' = Ext. clock from front-panel input; '10' = Ext. clock from Strobe IN 1.
COS T0-T1 Debounce clock frequency select (see section 6).
SCAN T0-T1 Select scan rate of digital inputs (see section 6).
SH 0-1 Memory update inhibit source select: '00' = Front panel; '01' = Strobe IN 2; '10' = Strobe IN 3; '11' = Strobe IN 4.
MEM EN Enables memory update at the input scan rate. If OM0 and OM1 both set for output then MEM EN enables memory driven outputs.
OM 0-1 Enable digital lines: '00' = all inputs; '11' = all outputs; '10' = half out (C&D)/ half in (A&B) '01' = half in (C&D)/ half out (A&B).
RING MODE This enables memory driven output sequence to be repeatedly down loaded (OM='11' set to all outputs).
SCAN INH **S**tatus of the Front Panel Scan Inhibit input or IN Strobe lines from transition card connector P0.
IO INT EN Enable interrupts to be generated by a change of state of the IO inputs or a set number of outputs has been reached.
COS BIT This bit signifies a change of state which causes an interrupt to be generated. A '0' needs to be written to this bit to clear the interrupt (see section 6.8). Or if all outputs selected (OM 0-1='11') and a set number of outputs has been reached this bit is set. If not all output the COS bit will be change of state.

4.6 Digital Input Interrupt Mask Register Low (Read/Write)

Address: Base + 0x418

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
M31	M30	M29	M28	M27	M26	M25	M24	M23	M22	M21	M20	M19	M18	M17	M16

Each bit corresponds to an input line. Writing a '1' means that that input will **not** be monitored for change-of-state.

4.7 Digital Input Interrupt Mask Register High (Read/Write)

Address: Base + 0x41C

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M47	M46	M45	M44	M43	M42	M41	M40	M39	M38	M37	M36	M35	M34	M33	M32

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
M63	M62	M61	M60	M59	M58	M57	M56	M55	M54	M53	M52	M51	M50	M49	M48

4.8 Debounce Bit Register Low (Read/Write)

Address: Base + 0x420

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16

Each bit corresponds to an input line. Writing a '1' enables that bit to be de-bounced at the chosen rate.

4.9 Debounce Bit Register High (Read/Write)

Address: Base + 0x424

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
DB47	DB46	DB45	DB44	DB43	DB42	DB41	DB40	DB39	DB38	DB37	DB36	DB35	DB34	DB33	DB32

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
DB63	DB62	DB61	DB60	DB59	DB58	DB57	DB56	DB55	DB54	DB53	DB52	DB51	DB50	DB49	DB48

4.10 Last Known Change Register Low (Read/Write)

Address: Base + 0x42C

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
LKC15	LKC14	LKC13	LKC12	LKC11	LKC10	LKC9	LKC8	LKC7	LKC6	LKC5	LKC4	LKC3	LKC2	LKC1	LKC0

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
LKC31	LKC30	LKC29	LKC28	LKC27	LKC26	LKC25	LKC24	LKC23	LKC22	LKC21	LKC20	LKC19	LKC18	LKC17	LKC16

4.11 Last Known Change Register High (Read/Write)

Address: Base + 0x428

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
LKC47	LKC46	LKC45	LKC44	LKC43	LKC42	LKC41	LKC40	LKC39	LKC38	LKC37	LKC36	LKC35	LKC34	LKC33	LKC32

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
LKC63	LKC62	LKC61	LKC60	LKC59	LKC58	LKC57	LKC56	LKC55	LKC54	LKC53	LKC52	LKC51	LKC50	LKC49	LKC48

4.12 Memory Address Counter (Read/Write)

Address: Base + 0x430

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0	0	0	0	0	0	0	0	0	0	0	0	0	MA18	MA17	MA16

This shows the current memory address. MA0 corresponds to a long-word address in memory; thus address 00 would be the first sample of inputs 0-31 and address 01 would be the first sample of inputs 32-63.

4.13 Sequence Count Register (Read/Write)

Address: Base + 0x434

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0

When in memory output mode this register sets the number of output sequences per channel (up to 64K).

4.14 VME System Reset

A VME system reset will clear the following registers:

- CSR CB
- CSR IO
- Status Register
- Memory Offset Register
- Vector Register
- IP Interrupt Select register
- Mask Registers
- Debounce Registers
- Last Known Change register
- Memory Address register

5. Interrupt Settings

The interrupts line used by the unit is set using the CSR CB on-board register.
The interrupt vector for change-of-state interrupts is set using the Interrupt Vector register.

There are three types of interrupt sources:

1. The carrier board change of state registers here the interrupt vector is held in the IRQ vector register Base+0x400.
2. Front Panel Inhibit/Transition board Strobe lines here the interrupt vector is held in the IRQ vector register Base+0x400.
3. When IP cards are used. Here the interrupt vector is held on the individual cards and the interrupt acknowledge directed to the requesting card.

5.1 Enabling and Setting Interrupt Level

The interrupt level generated by the carrier board is set using the CSR CB register INTSEL0 (bit 2), INTSEL1 (bit 3) INTSEL2 (bit 4).

Interrupt Level	INTSEL 2	INTSEL 1	INTSEL 0
None	0	0	0
IRQ 1	0	0	1
IRQ 2	0	1	0
IRQ 3	0	1	1
IRQ 4	1	0	0
IRQ 5	1	0	1
IRQ 6	1	1	0
IRQ 7	1	1	1

Interrupt Level Select

To enable VME interrupts from the carrier board to the VMEbus backplane set bit 1 of the CSR CB (INTEN) to ‘1’. Writing a ‘0’ to this bit disables the interrupts.

5.2 Interrupt Release

If bit 10 set to '0' (RORA) in the CSR CB the interrupt is released when the interrupt service routine clears the interrupt enable bit in the CSR CB (bit 1 INTEN).
If bit 10 set to '1' (ROAK) in the CSR CB the VME interrupt is released automatically on acknowledge by the FPGA clearing the interrupt enable bit INTEN (bit 1) in the CSR CB.

5.3 Scan Inhibit Interrupts

If interrupts enabled and EXT_INT (bit7 CSR CB) set High then when scan Inhibit set (one of the inputs taken low) an interrupt is generated and SCAN INH (bit13) is set in CSR IO.

The Scan Inhibit interrupt is latched in the FPGA and is cleared by writing a '0' to SCAN INH (bit13) in CSR IO.

If scan inhibit is held low it will only interrupt once. To generate another interrupt the scan inhibit line must go high first to reset FPGA logic.

5.4 IP Interrupt

The IP Interrupt Select bits **IP A INT 0 and IP B INT 0** (bits 8 and 9) in the CSR CB register allows the user to enable only the IP interrupts required and mask of the rest. To select an IP interrupt write a '1' to the appropriate bit of the register.
The interrupt vector is held on the individual IP cards.

The IP interrupts are prioritised in the 8001 where IP A has the highest and IP B the lowest.
Each IP card can be loaded with a separate IP vector, then when an interrupt occurs the controller will be given the interrupt vector of the IP card which caused the interrupt.
If both card interrupt at the same time then IP A will be serviced first then IP B.
Reading the IP Status register of the 8001 at base + 0x10 (READ ONLY) shows which IP cards have interrupts pending.

6. CARRIER BOARD DIGITAL I/O OPERATION

6.1 Board configuration

The board configuration is set using the Hytec jumper J1.

6.1.1 Hytec Jumper J1 OUT

This configures IP sites A and B as digital IO using the Hytec 8501 double width IP card.

6.1.2 Hytec Jumper J1 IN

This configures the IP sites A and B to function as per the Green springs IP spec. Sites C and D function as digital IO regardless of the J1.

6.2 Digital Operation

The following procedures are required to set up the module to monitor and record digital inputs.
When the 8001 powers up it treats all I/O lines as inputs.
First, you need to check what kind of transition card is connected by reading the top 4 bits of the 16-bit CSR CB register, and to check that the 8001 is configured as a HYTEC Input/Output board (Jumper J1 OUT).

Transition Card		**CSR CB Register**			
		T0	**T1**	**T2**	**J1** (Hytec Jumper)
Type	**Description**	**15**	**14**	**13**	**12**
8301	Input all 64 bits (opto)	0	0	0	1
8302	Input/output (All 64 bits)	X	0	0	1
8303	Output all 64 bits (opto)	1	0	1	1
8305	Input 0-31; output 32-63 (all opto)	1	1	0	1
8304 NONE	Straight through connection No card or non Hytec card fitted	1	1	1	1

Where 'x' corresponds to the IN/OUT jumper of 8302 JP1. All other combinations of bits 15, 14 and 13 are non-valid (at the moment, until we do some new transition cards) and in particular, if a non-Hytec card is fitted, you should see all 'ones'.

6.2.1 Selecting Input or Output Mode

If the board is an output board as denoted by its transition card type bits then the 8001 can be configured to output digital data.
Before enabling the output buffers of the 8001 the value of the outputs should be set by writing to the Change of state registers at addresses 0x28 and 0x2C, using VME A16 or A24 with a data width of D8, D16 or D32.
The I/O outputs can now be enabled by writing '1's to bits 10 & 11 of the CSR IO register base+0x14 (no other bits should be set to '1'). If 1's are written to bits 10 & 11 of the CSR I/O and the transition card is **not** an output card the outputs will **not** be enabled.

If the transition board is an input card, then writing '0's to bits 10 & 11 of the CSR IO register will ensure correct operation

6.2.2 Using The 8302

Where 'x' in the table above corresponds to the IN/OUT jumper of 8302 JP1:
JP1 IN means input mode and 'x' = '0';
JP1 OUT means output mode and 'x' = '1'.

WARNING If the jumper JP1 of the 8302 transition card is in it will look like an 8301 which has inverted inputs.

If an 8302 is present with JP1 removed, the 8001 can drive the T0 line in order to change the 8302 from output to input mode, whilst still maintaining the cards identity as an 8302 i.e. T0 in CSR CB register will remain HIGH. The T0 line is driven LOW if the 8001 is set up as an input and HIGH if set to be outputs. The operating mode is set by bits 10 and 11 (OM0 & OM1) of the CSR IO register.

6.3 Setting Up The Digital Input Registers (see tables below)

1. Select Scan clock source by writing to bits 1 and 2 of CSR I/O register.
2. Select the Scan clock frequency by writing to bits 5 and 6 of CSR I/O.
3. Select the Debounce scan clock rate by writing to bits 3 and 4 of CSR I/O.
4. Select the memory inhibit source by writing to bits 7 and 8 of CSR I/O.
5. Select if memory is to be updated at input scan rate by writing a '1' to bit 9 of the CSR I/O.
6. Select which of the 64 input bits are to have there interrupts MASKED out by writing a '1' to the corresponding bit in the 64-bit Mask register.
7. If interrupts are to be used set the bit 14 of CSR IO.
8. Select which of the 64 input bits are to have debounce logic applied by writing a '1' to the corresponding bit in the 64-bit Debounce register.
9. When the system has been set up as above then the scan enable can be set by writing a '1' to bit 0 of the CSR I/O (with all the other CSR I/O bits as chosen above).

6.4 Setting up The Scan Clock

Bits1 and 2 of the Control register CSR I/O (base+14h) of the unit select the source for the input scan clock as follows:

Clock Source	CSR I/O		Comment
	Bit 2	Bit 1	
Internal Clock	0	0	This runs at 1MHz maximum frequency
External Clock	0	1	Input via front panel lemo 1MHz maximum frequency single TTL
IN Strobe 1	1	0	Input via transition card connector P0 pin C7 1MHz max frequency
Not Used	1	1	

The internal clock can be selected as 1KHz, 10KHz, 100KHz and 1MHz and the external clock can be divided down by 1000, 100, 10 and 1 by writing to the CSR I/O.

CSR I/O		Scan Rate	
Bit 6	Bit5	Internal Clock	Ext/Strobe clock
0	0	1KHz	Div 1000
0	1	10KHz	Div 100
1	0	100KHz	Div 10
1	1	1MHz	Div 1

6.5 Debounce Scan Rate

The frequency at which the debounce registers are updated is set by writing to the CSR I/O register bits 3 and 4 as follows:

CSR I/O		Debounce Scan rate	
Bit 4	**Bit 3**	**Internal Clock**	**Ext/Strobe clock**
0	0	100Hz	Div 10000
0	1	200Hz	Div 5000
1	0	500Hz	Div 2000
1	1	1KHz	Div 1000

When debounce logic is applied to an input, its state must be seen to be different from the last known value on two successive samples at the debounce rate for the change to be accepted.
i.e. using a debounce scan rate of 1KHz the signal must hold its new value for at least 2ms to be guaranteed of being registered as a change. Any debounce noise with less then 1ms pulse width will not be seen as a change. Pulse greater than 1ms but less than 2ms may or may not be registered as a change.

6.6 Scan Inhibit

The Inhibit input is used to suspend memory updates.

Inhibit Source	**CSR I/O**		**Comment**
	Bit 8	**Bit 7**	
Front Panel	0	0	Input via front panel LEMO INHIBIT (Take LOW to Inhibit)
In Strobe 2	0	1	Input via transition card connector P0 pin E7 (Take LOW to Inhibit)
In Strobe 3	1	0	Input via transition card connector P0 pin B8 (Take LOW to Inhibit)
In Strobe 4	1	1	Input via transition card connector P0 pin D8 (Take LOW to Inhibit)

6.6.1 Scan Inhibit Interrupts

If interrupt enabled and EXT_INT (bit7 CSR CB) set High then when scan Inhibit set (one of the inputs taken low) an interrupt is generated and SCAN INH (bit13) is set in CSR IO.
The Scan Inhibit interrupt is latched in the FPGA and is cleared by writing a '0' to SCAN INH (bit13) in CSR IO.
If scan inhibit is held low it will only interrupt once. To generate another interrupt the scan inhibit line must go high first to reset FPGA logic.

6.7 Monitoring the Binary Inputs From the Last Known Change Registers

Whenever a change occurs in the 64 bit digital inputs, the Last Known Change (LKC) registers are updated. If a bit changes state that is masked out in the Mask registers then the LKC registers will still be updated.
Also, if a bit changes state that has debounce logic applied it, it will need to keep this change of state for a known period as set by the debounce scan clock rate.

NOTE: **The FPGA Version 8001V301** differs as follows. If a bit changes state that is masked out in the Mask register then the LKC registers will not be updated.

6.8 Change Of State Interrupt

A change of state can also cause a VME interrupt to be generated, as long as the interrupt enable bit is set in the CSR CB register the CSR IO bit 14 set and the interrupt mask bit for a particular input not set..
When an interrupt occurs the interrupt flag (COS BIT) bit 15 of the CSR IO needs to be cleared by the interrupt service routine by writing a '0' to bit 15 of the CSR I/O register. NB leave rest of register unchanged.

6.9 Digital Input Updates To Memory

The memory on the module is used for holding the digital input history. When enabled, the memory is continuously updated at the same rate as the Scan rate clock. When the memory is full it wraps around to the start of the memory and overwrites the data. The debounce logic is not applied to the data stored in memory.
Carrier board memory data may be accessed as bytes, words or longwords using A32/D32/D16/D08 (EO). Words and bytes are accessed via D15-D00. A1 addresses the low order word of a longword, A0 the high order word (big endian), thus A0 accesses the first conversion, A1 the second, and so on. The memory can also be read using BLT.

D31															D16 D15														D00	
64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	Scan 2 high 32 bits
32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Scan 2 low 32 bits
64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	Scan 1 high 32 bits
32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Scan 1 low 32 bits

Input Digital Data

7. Memory Driven Outputs

In this mode the 8001 has the facility to load data in to the on board RAM memory and to then down load the data on to the 64 digital IO lines 32 bit blocks (IP site CD and then AB). The down load rate is set by the internal or external scan clock rate.

7.1 Single Shot Mode

The start address of the IO data can be set anywhere within the memory and will be pre loaded in to the address counter.
The number of output sequences per channel (up to 64K) can be set by writing to the sequence count register of the VCB8001.
The output sequence will be started by writing to a bit in the VCB8001 CSR IO register.
When the pre programme number of output sequences has been reached the start bit in the CSR IO register will be cleared and an interrupt generated.

7.2 Ring Mode

The sequence may be repeatedly down loaded by setting the Ring Mode bit in the CSR IO register. In this mode the memory start address **must be set to zero**. Again each time the set number of output sequences has been reached as set by the Sequence Count register an interrupt will be generated.

7.3 Output Update Rates

The output states are latched at a programmable rate from 1KHz to 1MHz, or via an external clock up to 1MHz.

7.4 Enabling Memory Output Mode

The following sequence of instructions should be used to enable memory output mode. First write to the CSR IO to set the digital IO to be all outputs (OM0=1, OM1=1) then enable the memory (MEM EN=1) then write '1' to SCAN EN bit 1 of CSR IO (to start output sequence). If this sequence is not followed the first output may not be correct i.e. out of sequence.

The 8001 I/O lines will be TRI STATE at switch on and will remain so. When the 8001 is set to outputs digital data by writing to the CSR IO reg. The 64 digital output line will remain tri-stated until SCAN EN is set in the CSR IO then the outputs will be enabled at the end of the first update cycle (sites CD then AB).

NOTE: if an external clock is used to output data from memory the outputs will be tri-stated until the external clock is set going.

NOTE: Because the outputs are tri-stated until the end of the first memory output update then the width of the first 64 bits of data will be 32ns approx smaller than the subsequent data sequences.

7.5 End of Memory Output sequence

After the sequence from memory has ended the outputs will remain at their last value in the sequence until the out put is disabled (by writing to the CSR IO reg OM='0' OM1='0') or a new sequence is down loaded, or the MEM EN bit in the CSR IO is zeroed to enable writing to the LKC reg at Base+28h or Base+2Ch which will put a new value on to the IO lines.

7.6 Timing Considerations

1. Using internal clock the SCAN CLOCK will be enabled on writing a 1 to the SCAN_EN bit of the CSR_IO register. The SCAN_EN bit will not be enabled until the end of the VME cycle. The theoretical minimum time the first out put will appear on sites CD will be 156.25ns the theoretical maximum time is 218.75ns.

2. Using external clock the first rising edge after SCAN CLOCK enabled will be the start of the sequence. The time from this first edge to the data being enabled on to the C and D sites minimum 93.75ns maximum of 156.25ns theoretical times. I.e. one 16MHz cycle (62.5ns).
3. The time from CD sites being clocked out to the AB sites being clocked out is 249.92ns approx.

4. Must write to the Pre Count register (nos of outputs) before writing to the CSR IO MEM EN=1 as this loads the value held in the Pre count reg into the Pre count counter.

8. VME64X KEYING AND ALIGNMENT PIN

The keying mechanism provides for three key holes on top and three keying holes on the bottom of each board and subrack slot. Each key hole can be keyed with a "No Key" or a keying peg in one of four positions. With three key holes top and bottom the scheme provides a total of 15,625 keying combinations.

9. Power up Problem On Some Backplanes

If the unit does not power up i.e. Blue Led 'ON' it maybe due to some VME backplanes grounding the LI/I* signal. This grounding should be removed for correct operation. If the grounding cannot be removed on the backplane please contact Hytec for a work around solution.

10. EPICS Software Driver

EPICS software driver written for the VIC8001.
For down loads go to:
www.hytec-electronics.co.uk/EPICS%20Drivers.html

11. APPENDIX A PCB JUMPERS

Jumper	Function
J1	'Hytec IP Board': 'Out' - board set up as a Hytec digital I/O module with all inputs/outputs available. 'In' means IP daughter cards in use. Normally **OUT**.
J2	When IN, over-rides the bottom ejector handle switch on the VME front panel. Normally **IN**.
J3	When IN, connects the Front panel INHIBIT to the /STROBE line of IP card sit A. Normally **OUT.**
J5	When IN, connects the Front panel INHIBIT to the /STROBE line of IP card sit B. Normally **OUT.**
J4	Factory set, issue 2 PCBs only (not fitted on later issue PCBs).
J6 – J10	Base address: use only when geographical address not present i.e. non VME 64x. Make according to required A15-A11 base address.
J11	Memory size select (factory set only). Out = 128K devices; IN = 512K devices. Normally **OUT**.
J12	Made when FPGA SPROM (IC9) installed. This must be **IN**.

12. **APPENDIX B** Carrier board Configuration ROM – offset 0x600.

Address Offset	Value	Definition
0x03	xx	Checksum
Length of ROM		
0x07	00	
0x0B	02	
0x0F	00	
Configuration ROM data access width		
0x13	0x83	
CSR data access width		
0x17	0x83	
CSR space Specification ID		
0x1B	0x02	VME64x-1997
Identify a Valid CR		
0x1F	0x43	'C'
0x23	0x52	'R'
Manufacturer's ID		
0x27	0x00	
0x2B	0x80	
0x2F	0x03	
Board ID		
0x33	0x80	Shows board type i.e. 8001
0x37	0x01	
0x3B	0x00	
0x3F	0x00	
Revision ID		
0x43	0x03	PCB Board Issue
0x47	0x03	Xilinx version nos shows which PCB issue it is designed for
0x4B	0x00	Version of Xilinx.
0x4F	0x05	Version of Xilinx.
ASCII string null terminated or 0x000000		
0x53	0x00	
0x57	0x00	
0x5B	0x00	
Reserved for future use		
0x5F to 0x7B		
Program ID code		
0x7F	0x01	No program, ID ROM only
Start of user defined area		
0x80		
Board Serial Number		
0xCB, 0xCF, 0xD3	0x	BEG_SN
0xD7, 0xDB, 0xDF	0x	END_SN
AM code mask		
0x123 .. 0x13F	0x22002200 0000AA00	AM codes 3D, 39, 2D, 29, 0F, 0D, 0B, 09

13. APPENDIX C VME64X PIN ASSIGNMENT

P0 pin assignment

ROW A	SIG	ROW B	SIG	ROW C	SIG	ROW D	SIG	ROW E	SIG	ROW F	SIG
P0.A01	IODO1	P0.B01	IOD02	P0.C01	IOD03	P0.DO1	IOD04	P0.E01	IOD05	P0.F01	GND
P0.A02	IOD06	P0.B02	IOD07	P0.C02	IOD08	P0.D02	IOD09	P0.E02	IODIO	P0.F02	GND
P0.A03	IOD11	P0.B03	IOD12	P0.C03	IOD13	P0.D03	IOD14	P0.E03	IOD15	P0.F03	GND
P0.A04	IOD16	P0.B04	IOD17	P0.C04	IOD18	P0.D04	IOD19	P0.E04	IOD20	P0.F04	GND
P0.A05	IOD21	P0.B05	IOD22	P0.C05	IOD23	P0.D05	IOD24	P0.E05	IOD25	P0.F05	GND
P0.A06	IOD26	P0.B06	IOD27	P0.C06	IOD28	P0.D06	IOD29	P0.E06	IOD30	P0.F06	GND
P0.A07	IOD31	P0.B07	IOD32	P0.C07	IOD33 IN STROBE 1	P0.D07	IOD34	P0.E07 IN STROBE 2	IOD35	P0.F07	GND
P0.A08	IOD36	P0.B08	IOD37 IN STROBE 3	P0.C08	IOD38	P0.D08 IN STROBE 4	IOD39	P0.E08	IOD40	P0.F08	GND
P0.A09	IOD41 OStrobe1	P0.B09	IOD42	P0.C09	IOD43 OStrobe2	P0.D09	IOD44	P0.E09	IOD45 OStrobe3	P0.F09	GND
P0.A10	IOD46	P0.B10	IOD47 OStrobe4	P0.C10	IOD48	P0.D10	IOD49	P0.E10	IOD50	P0.F10	GND
P0.A11	IOC01	P0 B11	IOC02	P0.C11	IOC03	P0.D11	IOC04	P0 E11	IOC05	P0.F11	GND
P0.A12	IOC06	P0.B12	IOC07	P0.C12	IOC08	P0.D12	IOC09	P0.E12	IOC10	P0.F12	GND
P0.A13	IOC11	P0.B13	IOC12	P0.C13	IOC13	P0.D13	IOC14	P0.E13	IOC15	P0.F13	GND
P0.A14	IOC16	P0.B14	IOC17	P0.C14	IOC18	P0.D14	IOC19	P0.E14	IOC20	P0.F14	GND
P0.A15	IOC21	P0.B15	IOC22	P0.C15	IOC23	P0.D15	IOC24	P0.E15	IOC25	P0.F15	GND
P0.A16	IOC26	P0.B16	IOC27	P0.C16	IOC28	P0.D16	IOC29	P0.E16	IOC30	P0.F16	GND
P0.A17	IOC31	P0.B17	IOC32	P0.C17	IOC33	P0.D17	IOC34	P0.E17	IOC35	P0.F17	GND
P0.A18	IOC36	P0.B18	IOC37	P0.C18	IOC38	P0.D18	IOC39	P0.E18	IOC40	P0.F18	GND
P0.A19	IOC41 CARD_T0	P0.B19	IOC42	P0.C19	IOC43 CARD_T1	P0.D19	IOC44	P0.E19	IOC45 CARD_T2	P0.F19	GND

P1 Pin Assignment

P1 ROW A	SIGNAL	P1 ROW B	SIGNAL	P1 ROW C	SIGNAL	P1 ROW D	SIGNAL	P1 ROW Z	SIGNAL
P1.A01	D00	P1.B01	N/C	P1.C01	D08	P1.D01	N/C	P1.Z01	N/C
P1.A02	D01	P1.B02	N/C	P1.C02	D09	P1.D02	N/C	P1.Z02	GND
P1.A03	D02	P1.B03	N/C	P1.C03	D10	P1.D03	N/C	P1.Z03	N/C
P1.A04	D03	P1.B04	BG0IN*	P1.C04	D11	P1.D04	N/C	P1.Z04	GND
P1.A05	D04	P1.B05	BG0OUT*	P1.C05	D12	P1.D05	N/C	P1.Z05	N/C
P1.A06	D05	P1.B06	BG1IN*	P1.C06	D13	P1.D06	N/C	P1.Z06	GND
P1.A07	D06	P1.B07	BG1OUT*	P1.C07	D14	P1.D07	N/C	P1.Z07	N/C
P1.A08	D07	P1.B08	BG2IN*	P1.C08	D15	P1.D08	N/C	P1.Z08	GND
P1.A09	GND	P1.B09	BG2OUT*	P1.C09	GND	P1.D09	N/C	P1.Z09	N/C
P1.A10	N/C	P1.B10	BG3IN*	P1.C10	N/C	P1.D10	N/C	P1.Z10	GND
P1.A11	GND	P1.B11	BG3OUT*	P1.C11	BERR*	P1.D11	N/C	P1.Z11	N/C
P1.A12	DS1*	P1.B12	N/C	P1.C12	RESET	P1.D12	+3.3V	P1.Z12	GND
P1.A13	DS0*	P1.B13	N/C	P1.C13	LWORD*	P1.D13	N/C	P1.Z13	N/C
P1.A14	WRITE	P1.B14	N/C	P1.C14	AM5	P1.D14	+3.3V	P1.Z14	GND
P1.A15	GND	P1.B15	N/C	P1.C15	A23	P1.D15	N/C	P1.Z15	N/C
P1.A16	DTACK*	P1.B16	AM0	P1.C16	A22	P1.D16	+3.3V	P1.Z16	GND
P1.A17	GND	P1.B17	AM1	P1.C17	A21	P1.D17	N/C	P1.Z17	N/C
P1.A18	AS	P1.B18	AM2	P1.C18	A20	P1.D18	+3.3V	P1.Z18	GND
P1.A19	GND	P1.B19	AM3	P1.C19	A19	P1.D19	N/C	P1.Z19	N/C
P1.A20	IACK	P1.B20	GND	P1.C20	A18	P1.D20	+3.3V	P1.Z20	GND
P1.A21	IACKIN*	P1.B21	N/C	P1.C21	A17	P1.D21	N/C	P1.Z21	N/C
P1.A22	IACKOUT	P1.B22	N/C	P1.C22	A16	P1.D22	+3.3V	P1.Z22	GND
P1.A23	AM4	P1.B23	GND	P1.C23	A15	P1.D23	N/C	P1.Z23	N/C
P1.A24	A07	P1.B24	IRQ7*	P1.C24	A14	P1.D24	+3.3V	P1.Z24	GND
P1.A25	A06	P1.B25	IRQ6*	P1.C25	A13	P1.D25	N/C	P1.Z25	N/C
P1.A26	A05	P1.B26	IRQ5*	P1.C26	A12	P1.D26	+3.3V	P1.Z26	GND
P1.A27	A04	P1.B27	IRQ4*	P1.C27	A11	P1.D27	N/C	P1.Z27	N/C
P1.A28	A03	P1.B28	IRQ3*	P1.C28	A10	P1.D28	+3.3V	P1.Z28	GND
P1.A29	A02	P1.B29	IRQ2*	P1.C29	A09	P1.D29	N/C	P1.Z29	N/C
P1.A30	A0l	P1.B30	IRQ1*	P1.C30	A08	P1.D30	+3.3V	P1.Z30	GND
P1.A31	-12V	P1.B31	N/C	P1.C31	+12V	P1.D31	N/C	P1.Z31	N/C
P1.A32	+5V	P1.B32	+5V	P1.C32	+5V	P1.D32	N/C	P1.Z32	GND

P2 pin assignment

ROWA	SIG	ROWB	SIG	ROWC	SIG	ROWD	SIG	ROWZ	SIG
P2.A01	IOB41	P2.B01	+5V	P2.C01	IOB42	P2.D01	IOC47	P2.Z01	IOC46
P2.A02	IOB43	P2.B02	GND	P2.C02	IOB44	P2.D02	IOC48	P2.Z02	GND
P2.A03	IOB45	P2.B03	N/C	P2.C03	IOB46	P2.D03	IOC50	P2.Z03	IOC49
P2.A04	IOB47	P2.B04	A24	P2.C04	IOB48	P2.D04	IOB0l	P2.Z04	GND
P2.A05	IOB49	P2.B05	A25	P2.C05	IOB50	P2.D05	IOB03	P2.Z05	IOB02
P2.A06	IOA01	P2.B06	A26	P2.C06	IOA02	P2.D06	IOB04	P2.Z06	GND
P2.A07	IOA03	P2.B07	A27	P2.C07	IOA04	P2.D07	IOB06	P2.Z07	IOB05
P2.A08	IOA05	P2.B08	A28	P2.C08	IOA06	P2.D08	IOB07	P2.Z08	GND
P2.A09	IOA07	P2.B09	A29	P2.C09	IOA08	P2.D09	IOB09	P2.Z09	IOB08
P2.A10	IOA09	P2.B10	A30	P2.C10	IOA10	P2.D10	IOB10	P2.Z10	GND
P2.A11	IOA11	P2.B11	A31	P2.C11	IOA12	P2.D11	IOB12	P2.Z11	IOB11
P2.A12	IOA13	P2.B12	GND	P2.C12	IOA14	P2.D12	IOB13	P2.Z12	GND
P2.A13	IOA15	P2.B13	+5V	P2.C13	IOA16	P2.D13	IOB15	P2.Z13	IOB14
P2.A14	IOA17	P2.B14	N/C	P2.C14	IOA18	P2.D14	IOB16	P2.Z14	GND
P2.A15	IOA19	P2.B15	N/C	P2.C15	IOA20	P2.D15	IOB18	P2.Z15	IOB17
P2.A16	IOA21	P2.B16	N/C	P2.C16	IOA22	P2.D16	IOB19	P2.Z16	GND
P2.A17	IOA23	P2.B17	N/C	P2.C17	IOA24	P2.D17	IOB21	P2.Z17	IOB20
P2.A18	IOA25	P2.B18	N/C	P2.C18	IOA26	P2.D18	IOB22	P2.Z18	GND
P2.A19	IOA27	P2.B19	N/C	P2.C19	IOA28	P2.D19	IOB24	P2.Z19	IOB23
P2.A20	IOA29	P2.B20	N/C	P2.C20	IOA30	P2.D20	IOB25	P2.Z20	GND
P2.A21	IOA31	P2.B21	N/C	P2.C21	IOA32	P2.D21	IOB27	P2.Z21	IOB26
P2.A22	IOA33	P2.B22	GND	P2.C22	IOA34	P2.D22	IOB28	P2.Z22	GND
P2.A23	IOA35	P2.B23	N/C	P2.C23	IOA36	P2.D23	IOB30	P2.Z23	IOB29
P2.A24	IOA37	P2.B24	N/C	P2.C24	IOA38	P2.D24	IOB31	P2.Z24	GND
P2.A25	IOA39	P2.B25	N/C	P2.C25	IOA40	P2.D25	IOB33	P2.Z25	IOB32
P2.A26	IOA41	P2.B26	N/C	P2.C26	IOA42	P2.D26	IOB34	P2.Z26	GND
P2.A27	IOA43	P2.B27	N/C	P2.C27	IOA44	P2.D27	IOB36	P2.Z27	IOB35
P2.A28	IOA45	P2.B28	N/C	P2.C28	IOA46	P2.D28	IOB37	P2.Z28	GND
P2.A29	IOA47	P2.B29	N/C	P2.C29	IOA48	P2.D29	IOB39	P2.Z29	IOB38
P2.A30	IOA49	P2.B30	N/C	P2.C30	IOA50	P2.D30	IOB40	P2.Z30	GND
P2.A31	+3.3V	P2.B31	GND	P2.C31	+3.3V	P2.D31	PC GND	P2.Z31	+3.3V
P2.A32	N/C	P2.B32	+5V	P2.C32	N/C	P2.D32	PC +5V	P2.Z32	GND

Issue 3 PCBs only

14. APPENDIX D VME64X PIN ASSIGNMENT WITH 8501 IP CARD FITTED

P0 pin assignment

ROW A	SIG	ROW B	SIG	ROW C	SIG	ROW D	SIG	ROW E	SIG	ROW F	SIG
P0.A01	**I/O48**	P0.B01	N/C	P0.C01	**I/O49**	P0.DO1	N/C	P0.E01	**I/O50**	P0.F01	GND
P0.A02	N/C	P0.B02	**I/O51**	P0.C02	N/C	P0.D02	**I/O52**	P0.E02	N/C	P0.F02	GND
P0.A03	**I/O53**	P0.B03	N/C	P0.C03	**I/O54**	P0.D03	N/C	P0.E03	**I/O55**	P0.F03	GND
P0.A04	N/C	P0.B04	**I/O56**	P0.C04	N/C	P0.D04	**I/O57**	P0.E04	N/C	P0.F04	GND
P0.A05	**I/O58**	P0.B05	N/C	P0.C05	**I/O59**	P0.D05	N/C	P0.E05	**I/O60**	P0.F05	GND
P0.A06	N/C	P0.B06	**I/O61**	P0.C06	N/C	P0.D06	**I/O62**	P0.E06	N/C	P0.F06	GND
P0.A07	**I/O63**	P0.B07	N/C	P0.C07	**IN STROBE 1**	P0.D07	N/C	P0.E07	**IN STROBE 2**	P0.F07	GND
P0.A08	N/C	P0.B08	**IN STROBE 3**	P0.C08	N/C	P0.D08	**IN STROBE 4**	P0.E08	N/C	P0.F08	GND
P0.A09	**OStrobe1**	P0.B09	N/C	P0.C09	**OStrobe2**	P0.D09	N/C	P0.E09	**OStrobe3**	P0.F09	GND
P0.A10	N/C	P0.B10	**OStrobe4**	P0.C10	N/C	P0.D10	N/C	P0.E10	N/C	P0.F10	GND
P0.A11	**I/O32**	P0 B11	N/C	P0.C11	**I/O33**	P0.D11	N/C	P0 E11	**I/O34**	P0.F11	GND
P0.A12	N/C	P0.B12	**I/O35**	P0.C12	N/C	P0.D12	**I/O36**	P0.E12	N/C	P0.F12	GND
P0.A13	**I/O37**	P0.B13	N/C	P0.C13	**I/O38**	P0.D13	N/C	P0.E13	**I/039**	P0.F13	GND
P0.A14	N/C	P0.B14	**I/O40**	P0.C14	N/C	P0.D14	**I/O41**	P0.E14	N/C	P0.F14	GND
P0.A15	**I/O42**	P0.B15	N/C	P0.C15	**I/O43**	P0.D15	N/C	P0.E15	**I/O44**	P0.F15	GND
P0.A16	N/C	P0.B16	**I/O45**	P0.C16	N/C	P0.D16	**I/O46**	P0.E16	N/C	P0.F16	GND
P0.A17	**I/O47**	P0.B17	N/C	P0.C17	N/C	P0.D17	N/C	P0.E17	N/C	P0.F17	GND
P0.A18	N/C	P0.B18	N/C	P0.C18	N/C	P0.D18	N/C	P0.E18	N/C	P0.F18	GND
P0.A19	CARD_T0	P0.B19	N/C	P0.C19	**CARD_T1**	P0.D19	N/C	P0.E19	**CARD_T2**	P0.F19	GND

P1 Pin Assignment

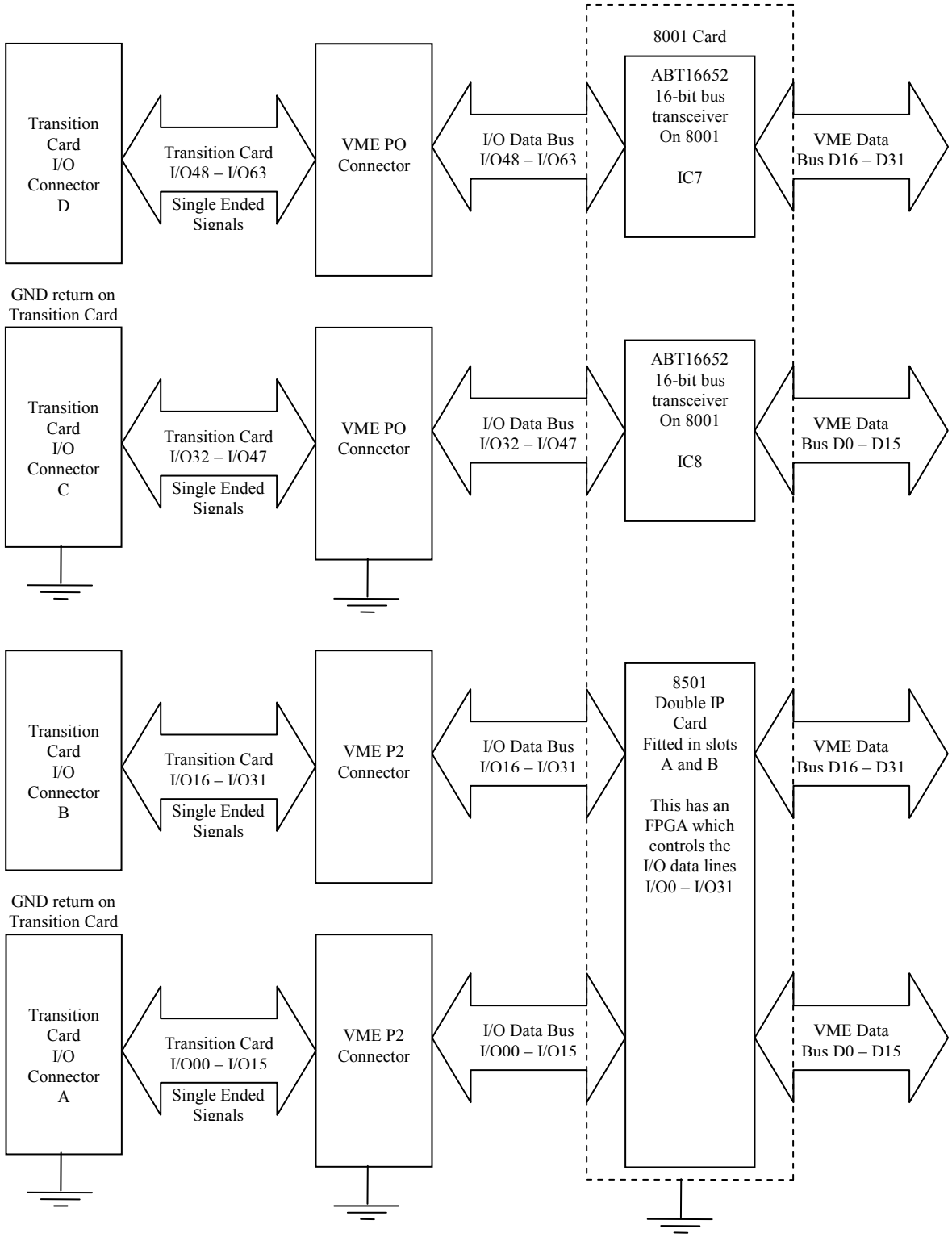
P1 ROW A	SIGNAL	P1 ROW B	SIGNAL	P1 ROW C	SIGNAL	P1 ROW D	SIGNAL	P1 ROW Z	SIGNAL
P1.A01	D00	P1.B01	N/C	P1.C01	D08	P1.D01	N/C	P1.Z01	N/C
P1.A02	D01	P1.B02	N/C	P1.C02	D09	P1.D02	N/C	P1.Z02	GND
P1.A03	D02	P1.B03	N/C	P1.C03	D10	P1.D03	N/C	P1.Z03	N/C
P1.A04	D03	P1.B04	BG0IN*	P1.C04	D11	P1.D04	N/C	P1.Z04	GND
P1.A05	D04	P1.B05	BG0OUT*	P1.C05	D12	P1.D05	N/C	P1.Z05	N/C
P1.A06	D05	P1.B06	BG1IN*	P1.C06	D13	P1.D06	N/C	P1.Z06	GND
P1.A07	D06	P1.B07	BG1OUT*	P1.C07	D14	P1.D07	N/C	P1.Z07	N/C
P1.A08	D07	P1.B08	BG2IN*	P1.C08	D15	P1.D08	N/C	P1.Z08	GND
P1.A09	GND	P1.B09	BG2OUT*	P1.C09	GND	P1.D09	N/C	P1.Z09	N/C
P1.A10	N/C	P1.B10	BG3IN*	P1.C10	N/C	P1.D10	N/C	P1.Z10	GND
P1.A11	GND	P1.B11	BG3OUT*	P1.C11	BERR*	P1.D11	N/C	P1.Z11	N/C
P1.A12	DS1*	P1.B12	N/C	P1.C12	RESET	P1.D12	+3.3V	P1.Z12	GND
P1.A13	DS0*	P1.B13	N/C	P1.C13	LWORD*	P1.D13	N/C	P1.Z13	N/C
P1.A14	WRITE	P1.B14	N/C	P1.C14	AM5	P1.D14	+3.3V	P1.Z14	GND
P1.A15	GND	P1.B15	N/C	P1.C15	A23	P1.D15	N/C	P1.Z15	N/C
P1.A16	DTACK*	P1.B16	AM0	P1.C16	A22	P1.D16	+3.3V	P1.Z16	GND
P1.A17	GND	P1.B17	AM1	P1.C17	A21	P1.D17	N/C	P1.Z17	N/C
P1.A18	AS	P1.B18	AM2	P1.C18	A20	P1.D18	+3.3V	P1.Z18	GND
P1.A19	GND	P1.B19	AM3	P1.C19	A19	P1.D19	N/C	P1.Z19	N/C
P1.A20	IACK	P1.B20	GND	P1.C20	A18	P1.D20	+3.3V	P1.Z20	GND
P1.A21	IACKIN*	P1.B21	N/C	P1.C21	A17	P1.D21	N/C	P1.Z21	N/C
P1.A22	IACKOUT	P1.B22	N/C	P1.C22	A16	P1.D22	+3.3V	P1.Z22	GND
P1.A23	AM4	P1.B23	GND	P1.C23	A15	P1.D23	N/C	P1.Z23	N/C
P1.A24	A07	P1.B24	IRQ7*	P1.C24	A14	P1.D24	+3.3V	P1.Z24	GND
P1.A25	A06	P1.B25	IRQ6*	P1.C25	A13	P1.D25	N/C	P1.Z25	N/C
P1.A26	A05	P1.B26	IRQ5*	P1.C26	A12	P1.D26	+3.3V	P1.Z26	GND
P1.A27	A04	P1.B27	IRQ4*	P1.C27	A11	P1.D27	N/C	P1.Z27	N/C
P1.A28	A03	P1.B28	IRQ3*	P1.C28	A10	P1.D28	+3.3V	P1.Z28	GND
P1.A29	A02	P1.B29	IRQ2*	P1.C29	A09	P1.D29	N/C	P1.Z29	N/C
P1.A30	A0l	P1.B30	IRQ1*	P1.C30	A08	P1.D30	+3.3V	P1.Z30	GND
P1.A31	-12V	P1.B31	N/C	P1.C31	+12V	P1.D31	N/C	P1.Z31	N/C
P1.A32	+5V	P1.B32	+5V	P1.C32	+5V	P1.D32	N/C	P1.Z32	GND

P2 pin assignment with 8501 IP card fitted

ROWA	SIG	ROWB	SIG	ROWC	SIG	ROWD	SIG	ROWZ	SIG
P2.A01	N/C	P2.B01	+5V	P2.C01	N/C	P2.D01	N/C	P2.Z01	N/C
P2.A02	N/C	P2.B02	GND	P2.C02	N/C	P2.D02	N/C	P2.Z02	GND
P2.A03	N/C	P2.B03	N/C	P2.C03	N/C	P2.D03	N/C	P2.Z03	N/C
P2.A04	N/C	P2.B04	A24	P2.C04	N/C	P2.D04	**I/O16**	P2.Z04	GND
P2.A05	N/C	P2.B05	A25	P2.C05	N/C	P2.D05	**I/O17**	P2.Z05	N/C
P2.A06	**I/O00**	P2.B06	A26	P2.C06	N/C	P2.D06	N/C	P2.Z06	GND
P2.A07	**I/O01**	P2.B07	A27	P2.C07	N/C	P2.D07	N/C	P2.Z07	**I/O18**
P2.A08	**I/O02**	P2.B08	A28	P2.C08	N/C	P2.D08	**I/O19**	P2.Z08	GND
P2.A09	**I/O03**	P2.B09	A29	P2.C09	N/C	P2.D09	**I/O20**	P2.Z09	N/C
P2.A10	**I/O04**	P2.B10	A30	P2.C10	N/C	P2.D10	N/C	P2.Z10	GND
P2.A11	**I/O05**	P2.B11	A31	P2.C11	N/C	P2.D11	N/C	P2.Z11	**I/O21**
P2.A12	**I/O06**	P2.B12	GND	P2.C12	N/C	P2.D12	**I/O22**	P2.Z12	GND
P2.A13	**I/O07**	P2.B13	+5V	P2.C13	N/C	P2.D13	**I/O23**	P2.Z13	N/C
P2.A14	**I/O08**	P2.B14	N/C	P2.C14	N/C	P2.D14	N/C	P2.Z14	GND
P2.A15	**I/O09**	P2.B15	N/C	P2.C15	N/C	P2.D15	N/C	P2.Z15	**I/O24**
P2.A16	**I/O10**	P2.B16	N/C	P2.C16	N/C	P2.D16	**I/O25**	P2.Z16	GND
P2.A17	**I/O11**	P2.B17	N/C	P2.C17	N/C	P2.D17	**I/O26**	P2.Z17	N/C
P2.A18	**I/O12**	P2.B18	N/C	P2.C18	N/C	P2.D18	N/C	P2.Z18	GND
P2.A19	**I/O13**	P2.B19	N/C	P2.C19	N/C	P2.D19	N/C	P2.Z19	**I/O27**
P2.A20	**I/O14**	P2.B20	N/C	P2.C20	N/C	P2.D20	**I/O28**	P2.Z20	GND
P2.A21	**I/O15**	P2.B21	N/C	P2.C21	N/C	P2.D21	**I/O29**	P2.Z21	N/C
P2.A22	N/C	P2.B22	GND	P2.C22	N/C	P2.D22	N/C	P2.Z22	GND
P2.A23	N/C	P2.B23	N/C	P2.C23	N/C	P2.D23	N/C	P2.Z23	**I/O30**
P2.A24	N/C	P2.B24	N/C	P2.C24	N/C	P2.D24	**I/O31**	P2.Z24	GND
P2.A25	N/C	P2.B25	N/C	P2.C25	N/C	P2.D25	N/C	P2.Z25	N/C
P2.A26	N/C	P2.B26	N/C	P2.C26	N/C	P2.D26	N/C	P2.Z26	GND
P2.A27	N/C	P2.B27	N/C	P2.C27	N/C	P2.D27	N/C	P2.Z27	N/C
P2.A28	N/C	P2.B28	N/C	P2.C28	N/C	P2.D28	N/C	P2.Z28	GND
P2.A29	N/C	P2.B29	N/C	P2.C29	N/C	P2.D29	N/C	P2.Z29	N/C
P2.A30	N/C	P2.B30	N/C	P2.C30	N/C	P2.D30	N/C	P2.Z30	GND
P2.A31	+3.3V	P2.B31	GND	P2.C31	+3.3V	P2.D31	PC GND	P2.Z31	+3.3V
P2.A32	N/C	P2.B32	+5V	P2.C32	N/C	P2.D32	PC +5V	P2.Z32	GND

15. **APPENDIX E** Diagram Showing I/O data Connections With 8501 Fitted

Schematic showing where all the pins on the P2 and P0 connectors connect.



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