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Building the Digital Infrastructure

PEAK 8920VL2 User Manual

Version 1.01

Nov 29, 2006

Packing Materials Checklist

Item	Description	Q'ty
1	PEAK8920VL2 BOARD SET	1
2	CPU COOLER	2
3	PS/2 KB/Mouse Y CABLE	1
4	CABLE SET (SIO+PIO P2.00)/(SIO P2.00)/IDE66	1
5	QUICK REFERENCE GUIDE	1
6	CD DRIVER	1

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Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class A

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment.

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Installation Suggestions

Ensure you have a stable, clean working environment. Dust and dirt can get into components and cause a malfunction. Use containers to keep small components separated.

Adequate lighting and proper tools can prevent you from accidentally damaging the internal components. Most of the procedures that follow require only a few simple tools, including the following:

A Philips screwdriver
A flat-tipped screwdriver
A grounding strap
An anti-static pad

Using your fingers can disconnect most of the connections. It is recommended that you do not use needlenose pliers to disconnect connections as these can damage the soft metal or plastic parts of the connectors.

Handling Precautions

1. Always disconnect the unit from the power outlet whenever you are installing or fixing a component inside the chassis.
2. If possible, always wear a grounded wrist strap when you are installing or fixing a component inside the chassis. Alternatively, discharge any static electricity by touching the bare metal chassis of the unit case, or the bare metal body of any other grounded appliance.
3. Hold electronic circuit boards by the edges only. Do not touch the components on the board unless it is necessary to do so. Do not flex or stress the circuit board.
4. Use the correct screws and do not overly tighten them.
5. Keep the original packaging and static-protective bag in case the unit has to be returned.

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NEXCOM RMA Policy

1. Warranty Period

NEXCOM manufactures products that are new or equivalent to new in accordance with industry standard. NEXCOM warrants that products will be free from defect in material and workmanship for 24 months beginning on the date of invoice by NEXCOM. HCP series products (Blade Server) which are manufactured by NEXCOM are covered by a three year warranty period.

2. RMA (Return Merchandise Authorization)

2.1 Customers shall enclose the "NEXCOM RMA Service Form" with the returned packages.

2.2 Customers must collect all the information about the problems encountered and note anything abnormal or, print out any on-screen messages, and describe the problems on the "NEXCOM RMA Service Form" for the RMA number apply process.

2.3 Customers can send back the faulty products with or, without accessories (manuals, cable, etc.) and any unnecessary components from the card, such as CPU and DRAM. If the components were suspected as part of the problems, please note clearly that which components are included. Otherwise, NEXCOM is not responsible for the devices/parts.

2.4 Customers are responsible to for the safe packaging of defective products are durable enough to be resistant against further damage and deterioration during transportation. In case of damages occurred during the transportation, the repair is treated as "Out of Warranty."

2.5 Any products returned by NEXCOM to other locations besides the customers' site will bear an extra charge and will be billed to the customer.

3. Repair service charges for out of warranty products

NEXCOM will charge for out of warranty products in two categories, one is basic diagnostic fee and another is component (product) fee.

3.1 System level

a. Component fee: NEXCOM will only charge for main components, such as SMD chip, BGA chip, etc. Passive components will be repaired for free, ex: resistor, capacitor.

b. Items will be replaced with NEXCOM products if the original one is not able to be repaired. Ex: motherboard, power supply, etc.

c. Replaced with 3rd party products if needed.

d. If RMA goods can not be repaired, NEXCOM will return it to customer without any charge.

3.2 Board level

a. Component fee: NEXCOM will only charge for main components, such as SMD chip, BGA chip, etc. Passive components will be repaired for free, ex: resistors, capacitors.

b. If RMA goods can not be repaired, NEXCOM will return it to customer without any charge.

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RoHS Compliance

NEXCOM RoHS Environmental Policy and Status Update

Nexcom is a global citizen for building the digital infrastructure. We are committed to providing green products and services, which are compliant with European Union RoHS (Restriction on Use of Hazardous Substance in Electronic Equipment) directive 2002/95/EU, to be your trusted green partner and to protect our environment.

RoHS restricts the use of Lead (Pb) < 0.1% or 1,000ppm, Mercury (Hg) < 0.1% or 1,000ppm, Cadmium (Cd) < 0.01% or 100ppm, Hexavalent Chromium (Cr6+) < 0.1% or 1,000ppm, Polybrominated biphenyls (PBB) < 0.1% or 1,000ppm, and Polybrominated diphenyl Ethers (PBDE) < 0.1% or 1,000ppm.

In order to meet the RoHS compliant directives, NEXCOM has established an engineering and manufacturing task force in to implement the introduction of green products. The task force will ensure that we follow the standard NEXCOM development procedure and that all the new RoHS components and new manufacturing processes maintain the highest industry quality levels for which NEXCOM are renowned.

The model selection criteria will be based on market demand. Vendors and suppliers will ensure that all designed components will be RoHS compliant.

How do you recognize NEXCOM RoHS Products?

For existing products where there are non-RoHS and RoHS versions, the suffix “(LF)” will be added to the compliant product name. For example, PEAK 7220VL2G RoHS version will become PEAK 7220VL2G(LF).

All new product models launched after January 2006 will be RoHS compliant. They will use the usual NEXCOM naming convention. For example, PEAK 870VL2, NBP14570, EBC 420 etc.

All RoHS compliant model and component manufacturing part numbers will be suffixed “XO”. For Example:

73AI064M03X0 CF CARD INDUSTRY, 64MB, T: 0-70°C, PQI:AC47-0640-0442, PBFREE

71A5500301X0 CPU+NB, AMD LX800, 500MHz/128K ,BGU481, AMD:ALXC800EETJ2VD

1E00042001X0 EBC420-LX8

Manual Revision History

Revision	Date	Description
1.01	Nov 29, 2006	Initial Draft

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Chapter 1 Product Introduction

1.1 Main Feature

The PEAK 8920VL2 has dual LGA771 sockets support up to two Quad-Core / Dual-Core Intel® Xeon® Processor 5100 series with 4 MB L2 cache and the Intel® Core™ microarchitecture supports up to 2.33 GHz with 1333 MHz FSB. Featuring an Intel® 5000P Chipset + Intel® ESB2, the PEAK 8920VL2 delivers higher throughput with dual point-to-point system buses, faster memory for I/O bandwidth, and Fully Buffered DIMM (FBDIMM) support.

The SBC PEAK 8920VL2 is successor to flagship PEAK 7220 SBC, which complied with PICMG 1.3 to ensure easy configuration, highest quality standard, and seamless compatibility with products from other manufactures.

PEAK 8920VL2 Main Feature Highlights:

- Dual LGA771 sockets support up to two Quad-Core / Dual-Core Intel Xeon processor
- Intel 5000P embedded chipset with longevity support.
- Robust mechanism design for enhanced product reliability.
- Up to 8 GB ECC/Register FBDIMM DDR 2 memory
- Dual PCI Express Gigabit Ethernet for high networking bandwidth.
- Four USB 2.0 directly output from bracket to save the cabling cost.
- Flexible design option for single or dual processors.
- Dedicated CPU cooler design for the thermal solution.

1.2 Block Diagram

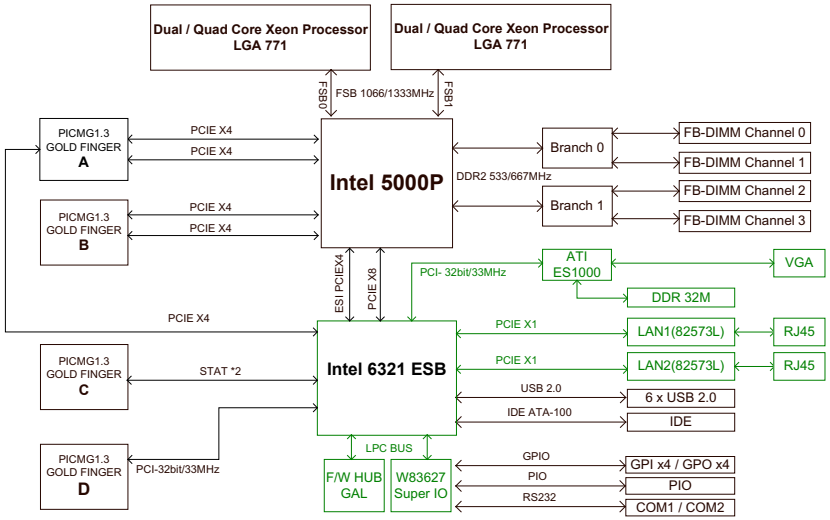


Figure 1.1: Block Diagram of PEAK 8920VL2

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1.3 Electrical Specifications

CPU Support

- Support Dual-Core Intel® Xeon® processor 5000 series and Quad-Core Intel®

Xeon® Processor 5300 series (80W)

- Intel Embedded Processor List (Intel® Longevity CPU):
  Dual Core Intel® Xeon® Processor (5130 & 5140)
  Dual Core Intel® Xeon® Processor LV (5128, 5138, 5148)
- 1066/1333 MHz FSB support

Main Memory

- 4 x 240-pin four channel DDR 2 FB-DIMM
- Support ECC / Register DDR2 memory up to 8GB

Chipset

- Intel® 5000P memory controller Hub
- Intel® 6321ESB I/O controller Hub

BIOS

- AMI BIOS
- Plug & Play support
- 8M-bit flash ROM
- Support Soft off, Wake on LAN, Power On by PS2 Keyboard Function Key, RTC

alarm Power On

- Power on after power failure

On-board LAN

- 2 x Intel® 82573L PCI Express Gigabit Ethernet
- Support Boot From LAN (PXE)
- Support Wake On LAN (When 5Vsb power available)
- 2 x RJ45 with LED

Display

- ATI ES1000 PCI graphic Controller
- 32MB DDR2 SDRAM VGA Memory
- 1 x DB15 VGA port

I/O Interface

- USB 2.0: 4 ports through I/O bracket
- USB 2.0: 2 ports, with 1x6 JST (2.5mm)
- Serial port: 2 ports, with 2x5 box-header (2.0mm) support RS-232 only
- Parallel port: 1 port , with 2x13 box-header (2.0mm), Bi-directional, EPP/ECP
- PS/2: 1 x Mini-Din Keyboard/Mouse
- GPIO: Support 4 sets of general purpose I/O each with TTL level (5V) interface
- FAN: 2 x 4-pin FAN JST connectors (for CPU coolers)
- 1 x on board buzzer
- 1 x 2-pin power on switch
- 1 x SMBus 2.0 to Backplane
- 1 x 2-pin header for reset
- 1 x 5-pin header for key lock
- 2 x 2-pin headers for power LED / HDD LED

Storage

- SATA: 2 ports, support RAID 0,1 through Backplane
- IDE: 1 x 40-pin IDE connector, support Ultra ATA 66/100/133
- 1 x 2-pin JST (2.5mm) power connector for DOM (Disk On Module)

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Watchdog Timer

- Watchdog Timer is programmable by software from 0 to 255 seconds
  (Tolerance 15% under room temperature 25°C)

On-board RTC

- On-chip RTC with battery back up
- 1 x External Li-Lon battery

Power Input

- Power source from backplane through PICMG 1.3 Golden Finger, support ATX mode

CPU Type (2 x Dual Core Xeon 3.0G) (4 x FBD DDR2 2.0GB)	+12 V	+5 V	+3.3 V	+5 Vsb
Full-Loading Mode	21.4 A	2.07 A	3.85 A	0.04 A
Light-Loading Mode	10.59 A	1.69 A	3.63 A	0.04 A

NOTE:

1. Full Loading: Utilize CPU 100% with Burn-in test running
2. Light Loading: Utilize CPU loading below 5% without data or application running.

Dimensions

- PICMG 1.3 form factor
  338.58 mm (L) x 122 mm (W) (13.3" x 4.8")

Environment

- Operating Temperature: 0°C ~ 60°C (for Board Level Only)
- Storage Temperature: -20˚C to 85˚C
- Relative Humidity:
  Operating: 10%~90% (non-condensing)
  Non-Operating: 5%~95% (non-condensing)

Certifications

- CE approval
- FCC Class A

1.4 Board Layout

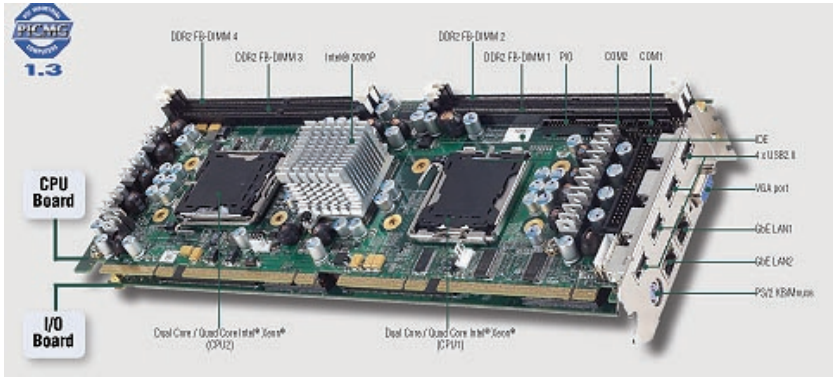


Figure 1.2 Board Layout view of the PEAK 8920VL2

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1.5 Board Dimensions

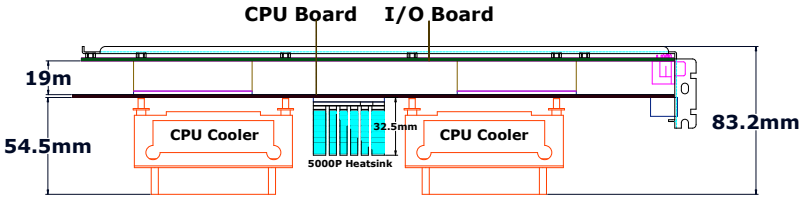


Figure 1.3 Top View of the PEAK 8920VL2

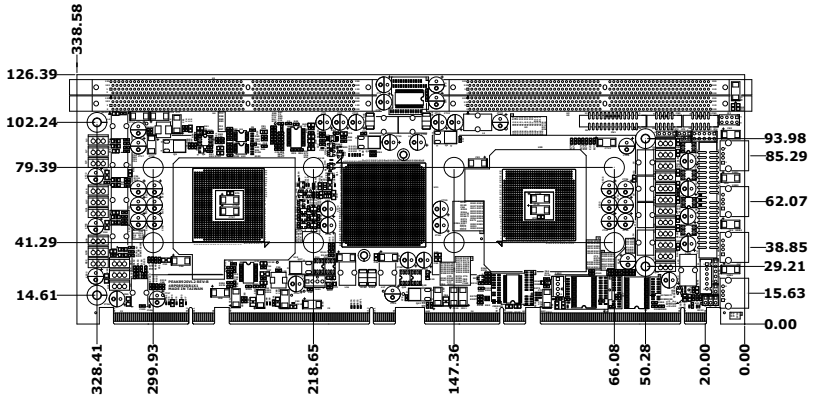


Figure 1.4 CPU Board Dimensions of the PEAK 8920VL2

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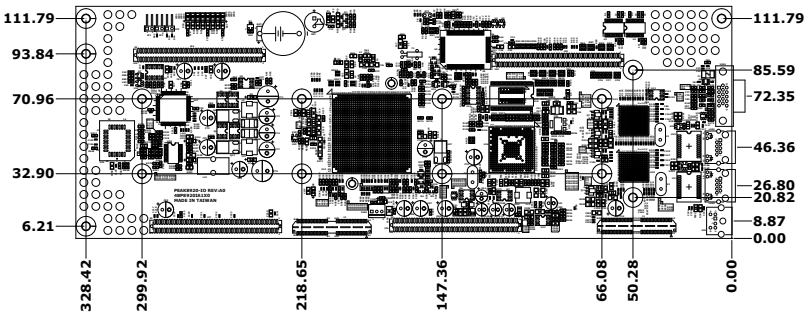


Figure 1.5 I/O Board Dimensions of the PEAK 8920VL2

1.6 Ordering Information

PEAK 8920VL2 (P/N: 1P00892000X0)	RoHS Compliant PICMG 1.3 Full-Size SHB Express (System Host Board), Intel® 5000P Chipset, LGA 771 socket support Dual Core /Quad Core Intel® Xeon® processors w/ 4 DDR2 FB-DIMM / 2 Express GbE / 6 USB2.0 / VGA/ 2 SATA.

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Chapter 2 Jumper Setting

2.1 Setting Jumpers

Table 2-1: Setting Jumpers

FAN1:CPU1 FAN FAN2:CPU0 FAN

◉ JP1:LAN Link/Active

Pin	Def.	Pin	Def.	Pin	Def.	Pin	Def.
7	3.3VSB	5	3.3VSB	3	3.3VSB	1	3.3VSB
8	LAN2_AC-TLED#	6	LAN2_ LINK#	4	LAN1_AC-TLED#	2	LAN1_ LINK#

◉ JP2:Speaker (Reserved)

Pin	Def.	Pin	Def.	Pin	Def.	Pin	Def.
4	IO_SPEAK-ER	3	GND	2	GND	1	+5V

◉ JP3:CMOS Clear

Pin	Def.	Pin	Def.	Pin	Def.
3	CMOS_CLEAR	2	ESB_RTCRST#	1	RTCRST#

◉ JP4:GPIO

Pin	Def.	Pin	Def.	Pin	Def.	Pin	Def.	Pin	Def.
9	GPO17	7	GPO16	5	GPO15	3	GPO14	1	+5V
10	GPI13	8	GPI12	6	GPI11	4	GPI10	2	GND

◉ JP5:DOM

Pin	Def.	Pin	Def.
2	GND	1	+5V

◉ JP6:Key lock

Pin	Def.
1	+5V
2	NC
3	GND
4	KBLOCK#
5	GND

◉ JP7 :Main power LED

Pin	Def.
1	+5V
2	GND

◉ JP8:HW Reset

Pin	Def.
1	HW_RST#
2	GND

◉ JP9:Push button

Pin	Def.
1	SIO_PBIN
2	GND

◉ JP10:HD LED

Pin	Def.
1	+5V
2	HD_LED

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⊙ **J1:USB port 4/5**

Pin	Def.
1	USB_VCC45
2	USB_4N
3	USB_4P
4	USB_5N
5	USB_5P
6	USB_GND

2.2 Location of Jumpers

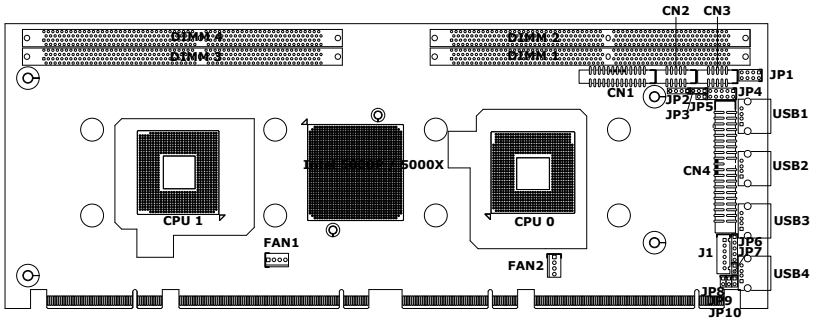


Figure 2-1: Jumper Location

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2.3 PCI Routing

Chip	Function	IDSEL	Interrupt Routing	Remark
ATI ES1000	PCI to VGA	AD18	IRQ_G	
W83627HF	SUPER I/O	LPC	REQ0	

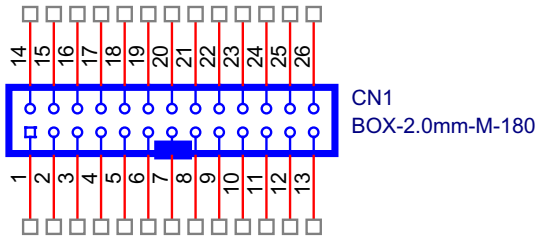
2.4 Pin Definition

Connector	Function
J1	USB 4/5
CN1	PIO
CN2	COM2
CN3	COM3
CN4	IDE
JP1	LAN1
JP2	Speaker (Reserved)
JP3	CMOS
JP4	GPIO
JP5	Disk On Module
JP6	Key Lock
JP7	Main Power LED
JP8	Power Reset
JP9	Push button
JP10	HDD LED
FAN1	CPU0 FAN
FAN2	CPU1 FAN
CON1	USB1
CON2	USB2
CON3	USB3
CON4	USB4
CON5	VGA
CON6	LAN1
CON7	LAN2
CON8	PS2 KB/Mouse

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J1: USB port 4/5 box header:

A.Connector size: 1 X 6 = 6 Pin

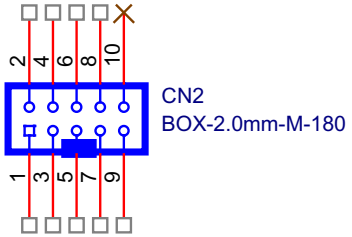


B.Connector pin definition

Pin	Signal
1	USB_VCC45
2	USB_4N
3	USB_4P
4	USB_5N
5	USB_5P
6	USB_GND

CN2: COM2 box header:

A. Connector size: 2 X 5 = 10 Pin



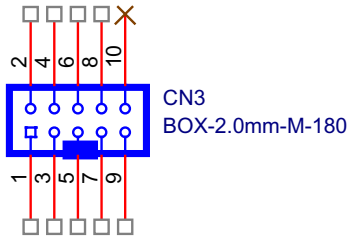
B. Connector pin definition

Pin	Signal	Pin	Signal
1	SIO_DCD#2_CON	2	SIO_RX2_CON
3	SIO_TX2_CON	4	SIO_DTR#2_CON
5	IO_GND	6	SIO_DSR#2_CON
7	SIO_RTS#2_CON	8	SIO_CTS#2_CON
9	SIO_RI#2_CON	10	NC

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CN3: COM1 box header:

A.Connector size: 2 X 5 = 10 Pin

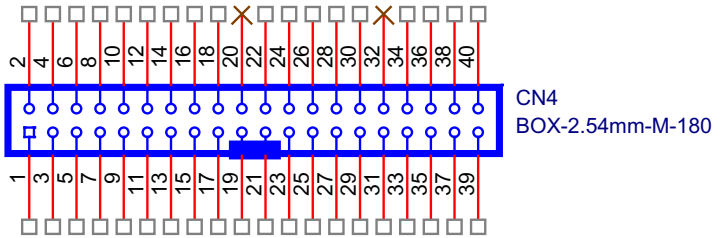


B.Connector pin definition

Pin	Signal	Pin	Signal
1	SIO_DCD#1_CON	2	SIO_RX1_CON
3	SIO_TX1_CON	4	SIO_DTR#1_CON
5	IO_GND	6	SIO_DSR#1_CON
7	SIO_RTS#1_CON	8	SIO_CTS#1_CON
9	SIO_RI#1_CON	10	NC

CN4: IDE box header:

A.Connector size: 2 X 20 = 40 Pin



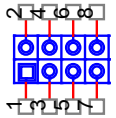
B.Connector pin definition

Pin	Signal	Pin	Signal
1	IDE_RST#_R	2	GND
3	IDE_D7	4	IDE_D8
5	IDE_D6	6	IDE_D9
7	IDE_D5	8	IDE_D10
9	IDE_D4	10	IDE_D11
11	IDE_D3	12	IDE_D12
13	IDE_D2	14	IDE_D13
15	IDE_D1	16	IDE_D14
17	IDE_D0	18	IDE_D15
19	GND	20	NC
21	ESB_IDE_DREQ	22	GND
23	IDE_IOW#	24	GND
25	IDE_IOR#	26	GND
27	ESB_IDE_IORDY	28	IDE_CABLE
29	ESB_IDE_DACK#	30	GND
31	IDE_IRQ14	32	NC
33	ESB_IDE_DA1	34	IDE_P66DET_R
35	ESB_IDE_DA0	36	ESB_IDE_DA2
37	IDE_CS1#	38	IDE_CS3#
39	IDE_LED#	40	GND

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JP1: LAN Link/Active pin header:

A.Connector size: 2 X 4 = 8 Pin



JP1
PIN-2.54mm-M-180

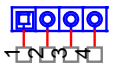
B.Connector pin definition

Pin	Signal	Pin	Signal
1	3.3VSB	2	LAN1_LINK#
3	3.3VSB	4	LAN1_ACTLED#
5	3.3VSB	6	LAN2_LINK#
7	3.3VSB	8	LAN2_ACTLED#

JP2: Speaker pin header: (Reserved)

A.Connector size: 1 X 4 = 4 Pin

JP2
PIN-2.54mm-M-180



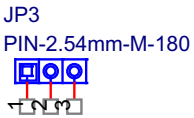
B.Connector pin definition

Pin	Signal
1	+5V
2	GND
3	GND
4	IO_SPEAKER

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JP3: CMOS Clear pin header:

A.Connector size: 1 X 3 = 3 Pin

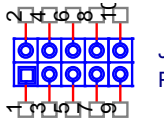


B.Connector pin definition

Pin	Signal
1	RTCRST#
2	ESB_RTCRST#
3	CMOS_CLEAR

JP4: GPIO pin header:

A.Connector size: 2 X 5 = 10 Pin



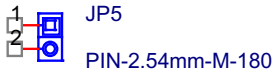
B.Connector pin definition

Pin	Signal	Pin	Signal
1	+5V	2	GND
3	GPO14	4	GPI10
5	GPO15	6	GPI11
7	GPO16	8	GPI12
9	GPO17	10	GPI13

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JP5: DOM pin header:

A.Connector size: 1 X 2 = 2 Pin

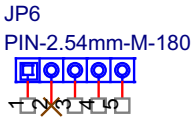


B.Connector pin definition

Pin	Signal
1	+5V
2	GND

JP6: Key lock pin header:

A.Connector size: 1 X 5 = 5 Pin



B.Connector pin definition

Pin	Signal
1	+5V
2	NC
3	GND
4	KBLOCK#
5	GND

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JP7: Main power LED pin header:

A.Connector size: 1 X 2 = 2 Pin



JP7

PIN-2.54mm-M-180

B.Connector pin definition

Pin	Signal
1	+5V
2	GND

JP8: HW Reset pin header:

A.Connector size: 1 X 2 = 2 Pin



JP8

PIN-2.54mm-M-180

B.Connector pin definition

Pin	Signal
1	HW_RST#
2	GND

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JP9: Push button pin header:

A.Connector size: 1 X 2 = 2 Pin



JP9

PIN-2.54mm-M-180

B.Connector pin definition

Pin	Signal
1	ATX5VSB
2	SIO_PBIN

JP10: HDD LED pin header:

A.Connector size: 1 X 2 = 2 Pin



JP10

PIN-2.54mm-M-18

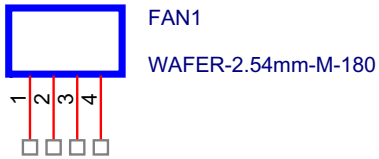
B.Connector pin definition

Pin	Signal
1	+5V
2	HD_LED

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FAN1: CPU0 FAN pin header:

A.Connector size: 1 X 4 = 4 Pin

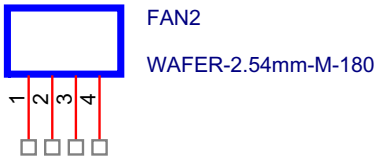


B.Connector pin definition

Pin	Signal
1	GND
2	VCC_12
3	CPU0_FAN
4	CPU0_FANPWM

FAN2: CPU1 FAN pin header:

A.Connector size: 1 X 4 = 4 Pin



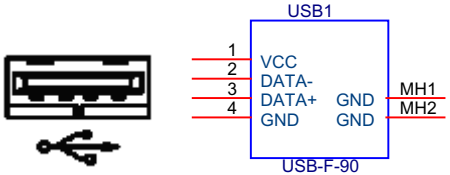
B.Connector pin definition

Pin	Signal
1	GND
2	VCC_12
3	CPU1_FAN
4	CPU1_FANPWM

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USB1 connector:

A.Connector size: USB port

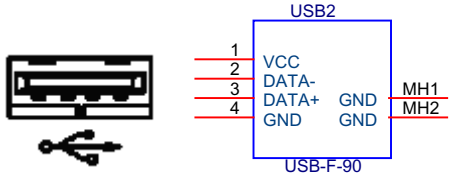


B.Connector pin definition

Pin	Signal
1	USB_VCC0
2	USB_0N
3	USB_0P
4	USB_GND
MH1	USB_GND
MH2	USB_GND

USB2 connector:

A.Connector size: USB port



B.Connector pin definition

Pin	Signal
1	USB_VCC1
2	USB_1N
3	USB_1P
4	USB_GND
MH1	USB_GND
MH2	USB_GND

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USB3 connector:

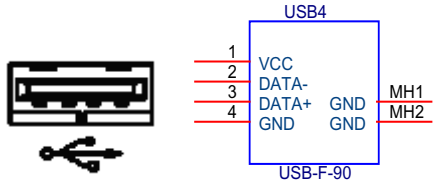
A.Connector size: USB port

B.Connector pin definition

Pin	Signal
1	USB_VCC2
2	USB_2N
3	USB_2P
4	USB_GND
MH1	USB_GND
MH2	USB_GND

USB4 connector:

A.Connector size: USB port



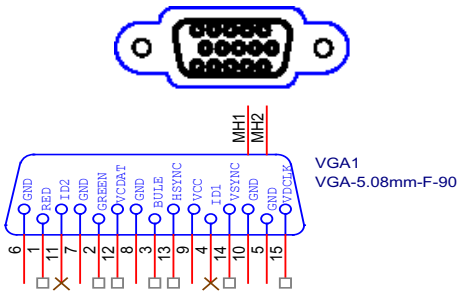
B.Connector pin definition

Pin	Signal
1	USB_VCC3
2	USB_3N
3	USB_3P
4	USB_GND
MH1	USB_GND
MH2	USB_GND

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VGA connector:

A.Connector size: 15 PIN D-SUB FEMALE

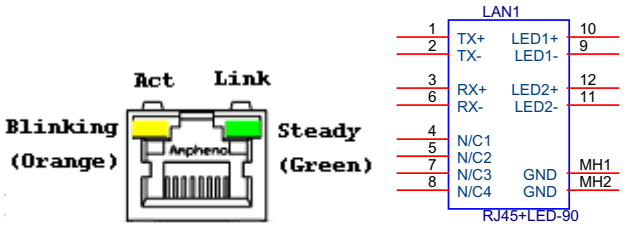


B.Connector pin definition

Pin	Signal	Pin	Signal
1	VGA_R_CON	2	VGA_G_CON
3	VGA_B_CON	4	NC
5	SGND	6	SGND
7	SGND	8	SGND
9	VGA_VCC	10	SGND
11	NC	12	VGA_I2CDAT_CON
13	VGA_HSYNC_CON	14	VGA_VSYNC_CON
15	VGA_I2CCLK_CON		
MH1	SGND	MH2	SGND

LAN1 connector:

A.Connector size: RJ45+LED



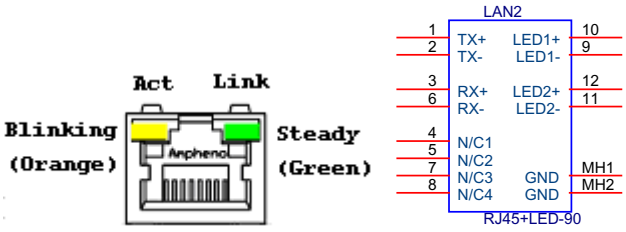
B.Connector pin definition

Pin	Signal	Pin	Signal
1	LAN1_M0P	2	LAN1_M0N
3	LAN1_M1P	4	LAN1_M2P
5	LAN1_M2N	6	LAN1_M1N
7	LAN1_M3P	8	LAN1_M3N
9	LAN1_LINK#	10	L1_CONVCC
11	LAN1_ACTLED#	12	L1_CONVCC_2
MH1	LAN_GND	MH2	LAN_GND

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LAN2 connector:

A.Connector size: RJ45+LED

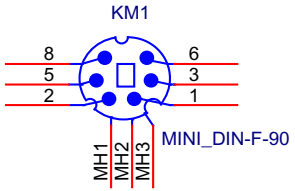


B.Connector pin definition

Pin	Signal	Pin	Signal
1	LAN2_M0P	2	LAN2_M0N
3	LAN2_M1P	4	LAN2_M2P
5	LAN2_M2N	6	LAN2_M1N
7	LAN2_M3P	8	LAN2_M3N
9	LAN2_LINK#	10	L2_CONVCC
11	LAN2_ACTLED#	12	L2_CONVCC_2
MH1	LAN_GND	MH2	LAN_GND

KM1: Keyboard/Mouse connector:

A. Connector size: MINI DIN 6PIN (PURPLE)



B. Connector pin definition

Pin	Signal	Pin	Signal
1	LKB_DAT	2	LMS_DAT
3	K/M_GND	5	LK/M_VCC
6	LKB_CLK	8	LMS_CLK
MH1	K/M_GND	MH2	K/M_GND
MH3	K/M_GND		

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2.5 POWER Consumption

- Power source from backplane through PICMG 1.3 Golden Finger, support ATX mode

CPU Type (2 x Dual Core Xeon 3.0G) (4 x FBD DDR2 2.0GB)	+12V	+5V	+3.3V	+5Vsb
Full-Loading Mode	21.4 A	2.07 A	3.85 A	0.04 A
Light-Loading Mode	10.59 A	1.69 A	3.63 A	0.04 A

NOTE:
1.Full Loading: Utilize CPU 100% with Burn-in test running
2.Light Loading: Utilize CPU loading below 5% without data or application running.

Chapter 3 Expansion

3.1 System Memory

Memory Allocation



Memory Installation reference chart

No of Memory installing	DIMM Location to use
1	DIMM1
2	DIMM1, DIMM2
4	DIMM1, DIMM2, DIMM3, DIMM4

Table 3-1: DIMM Configurations of the PEAK 8920VL2

3.2 Installing FB-DIMM

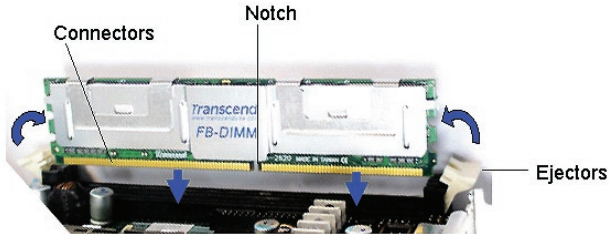


Figure 3-1: How to Install FB-DIMM

1. Position the FB-DIMM memory over the memory slot. Be sure the notch on the memory align with the memory slot.
2. Press down the memory evenly until the ejectors snap into the lock position.

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3.3 Tested Memory Reference List

Type	P/N Number	Size	Vendor
240pins 512MB DDR2 FB-DIMM Module PC2-5300 CL5	78.96G99.404	512 MB	Apacer
240pins 1GB DDR2 667 FB-DIMM Module (Reg & ECC & DDR667)	TS128MFB72V6J-T	1 GB	Tran-scend
240pins 2GB DDR2 677 FB-DIMM Module (Reg & ECC & DDR667)	TS256MFB72V6J-T	2 GB	Tran-scend

3.4 Installing CPU and CPU Cooler

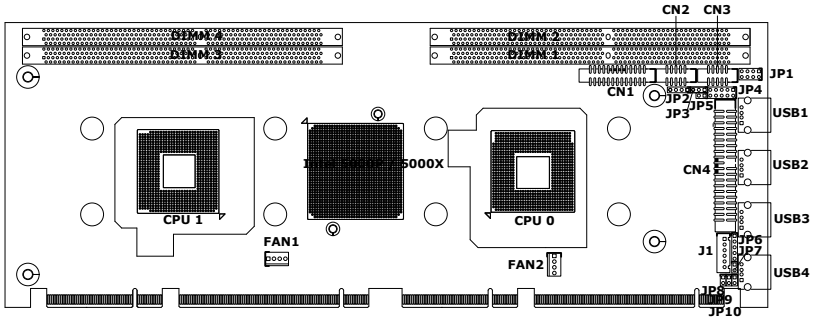


Figure 3-3: Installing CPU

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3.5 CPU support list

Dual-Core Intel® Xeon® Processor 5100 Series for Dual-Processor Embedded Computing							
Processor Name	Product Number	Core Speed	L2 Cache	Front-Side Bus Speed	Thermal Design Power	Tcase	Package
Dual-Core Intel® Xeon® processor LV 5138 Δ	HH80556JH0464M	2.13 GHz	4 MB	1066 MHz	35 W	70.8° C (nominal)	LGA 771
Dual-Core Intel® Xeon® processor LV 5148 Δ	HH80556JJ0534M	2.33 GHz	4 MB	1333 MHz	40 W	58° C	LGA 771
Dual-Core Intel® Xeon® processor LV 5128 Δ	HH80556JH0364M	1.86 GHz	4 MB	1066 MHz	40 W	58° C	LGA 771
Dual-Core Intel® Xeon® processor 5140 Δ	HH80556KJ0534M	2.33 GHz	4 MB	1333 MHz	65 W	65° C	LGA 771
Dual-Core Intel® Xeon® processor 5130 Δ	HH80556KJ0414M	2.0 GHz	4 MB	1333 MHz	65 W	65° C	LGA 771

Quad-Core Intel® Xeon® Processor 5300 Series

3.6 Passive Backplane Support List

NEXCOM provides PICMG 1.3 compliant 4U backplanes to fit most project needs. The 4U backplanes include two 14-slot NBP 14111, NBP 14210, and one 20-slot NBP 20016. All backplanes are compliant with PICMG 1.3 for greater reliability and compatibility with product from other manufactures. See blow for available backplanes and type.

PEAK 8920VL2 Compatible Backplane Table

Models	Slots	SHB	PCIe x16	PCIe x8	PCIe x4	PCIe x1	PCI	PCI-X
NBP14111 (P/N:1N01411100X0)	14	1	1	0	0	0	3	8
NBP14210 (P/N:79N1421000X0)	14	1	1	0	1	0	10	0
NBP20016 (P/N:1N02001600X0)	20	1	0	0	0	0	0	16

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Chapter 4 AMI BIOS Setup

4.1 About the BIOS

The BIOS (Basic Input and Output System) program is a menu driven utility that allow you to make changes to the system configuration and tailor the system to suit your individual needs. The BIOS is a ROM-based configuration utility that displays the system's configuration status and provides a tool to set system parameters. When the system is turned off, these parameters are saved in non-volatile battery backed-up CMOS RAM. When the system is turned back on, the system is configured with the values saved in CMOS.

With easy-to-use pull down menus, you can configure items such as: Hard drives, diskette drives, and peripherals. You can also configure Video display type, display options, and password protection from unauthorized use. The Power management features in the BIOS intimately affect how the computer performs. Therefore, it is important to understand all the Setup options, and select the appropriate settings.

4.2 When to Run BIOS

The BIOS program should be modified in the following

conditions:

- Changing of the system configuration
- Detecting configuration error by the system, and you are prompted to make changes to the BIOS program
- Resetting the system clock
- Redefining the communication ports to prevent any conflicts
- Making changes to the Power Management configuration
- Changing the password or making other changes to the security setup

Making the inappropriate BIOS setting may cause the system failure to function properly. Be sure to modified the setting with caution.

Load Failsafe Defaults to restore the manufacture setting.

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4.3 Entering Setup

When the system is powered on the BIOS will enter the Power-On Self Test (POST) routines. These routines perform various diagnostic checks; if anenor is encountered the error will be reported in one of tow different ways:

- If the error occars before th edisplay device is initaialized, a series of beeps will be tranamitted.
- If the error occurs afer the display device is initialized, the screen willdisplay the error message.

Powering on the computer and immediately pressing <Del> allows you to emtter setup. Amother way to enter setup is to power n the computer and wait for the following message during the POST:

TO ENTER SETUP BEFORE BOOT

PRESS <CTRL + ALT + DEL> KEY

Press the <Del> key or press the <Ctrl>, <Alt>, and <Esc> keys to enter Setup:

4.4 The Main Menu

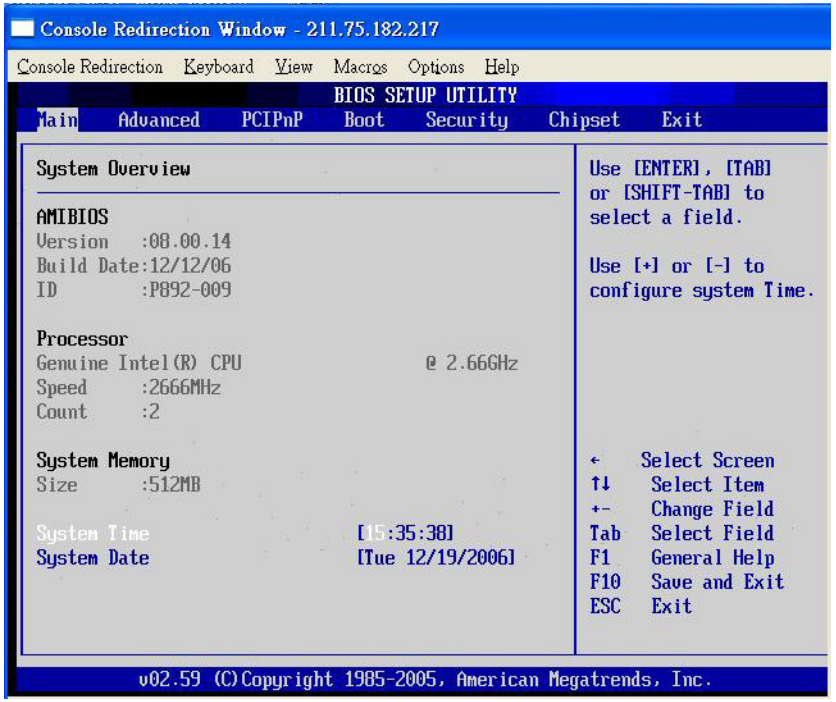


Figure 4-1: BIOS Setup Utility Main Menu

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4.5 Advanced BIOS Features

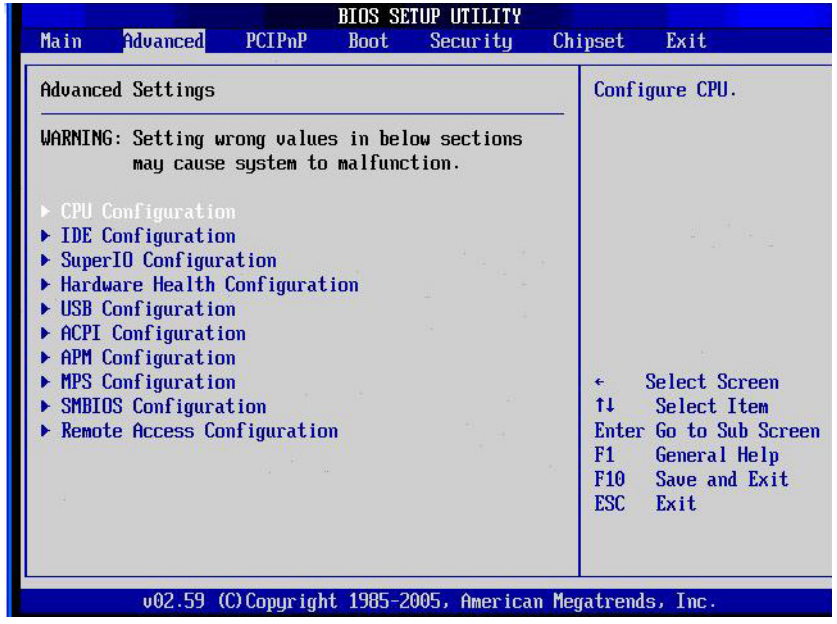


Figure 4-2: BIOS – Advanced BIOS Features

4.6 Chipset Features



Figure 4-3: BIOS –Chipset Features

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4.7 Power Management Setup/APM

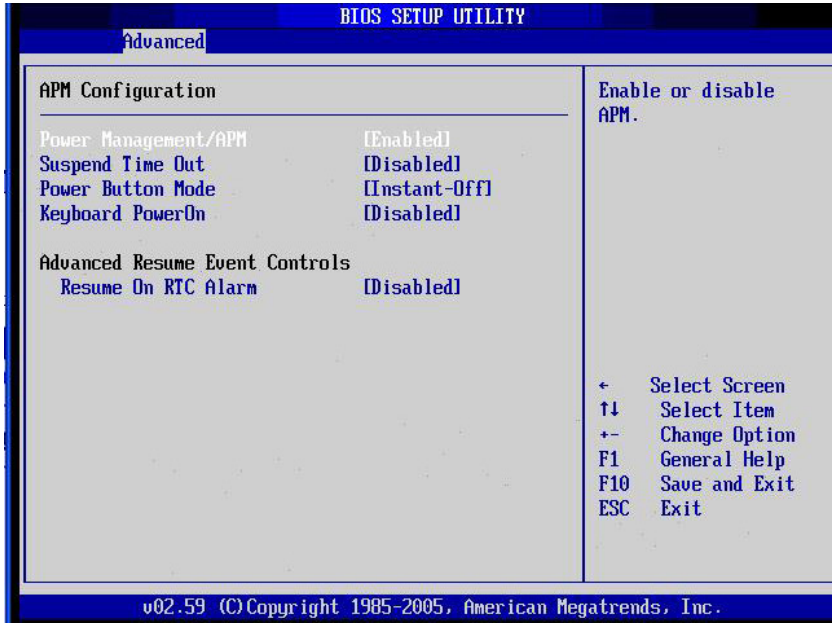
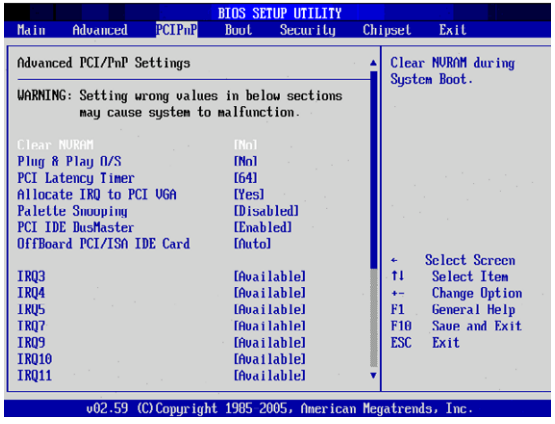


Figure 4-4: BIOS – Power Management Setup

4.8 PnP/PCI Configurations



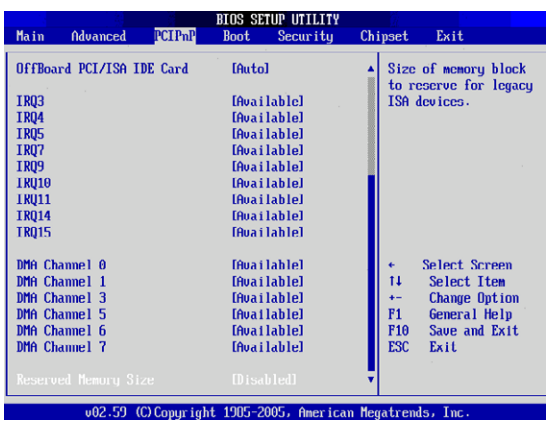
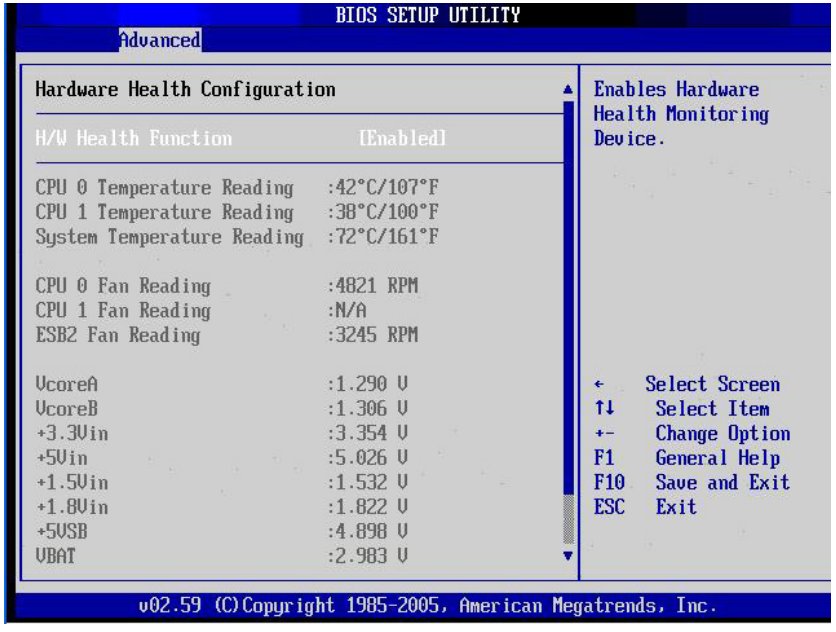


Figure 4-5: BIOS – PnP/PCI Configurations

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4.9 Advanced PC Health / Hardware Health Status



4.10 Set Password/Security

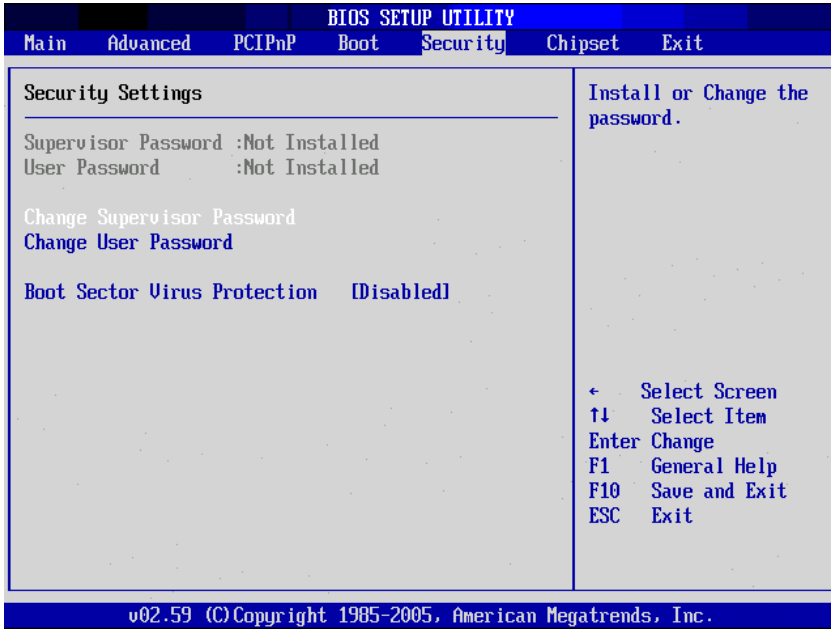
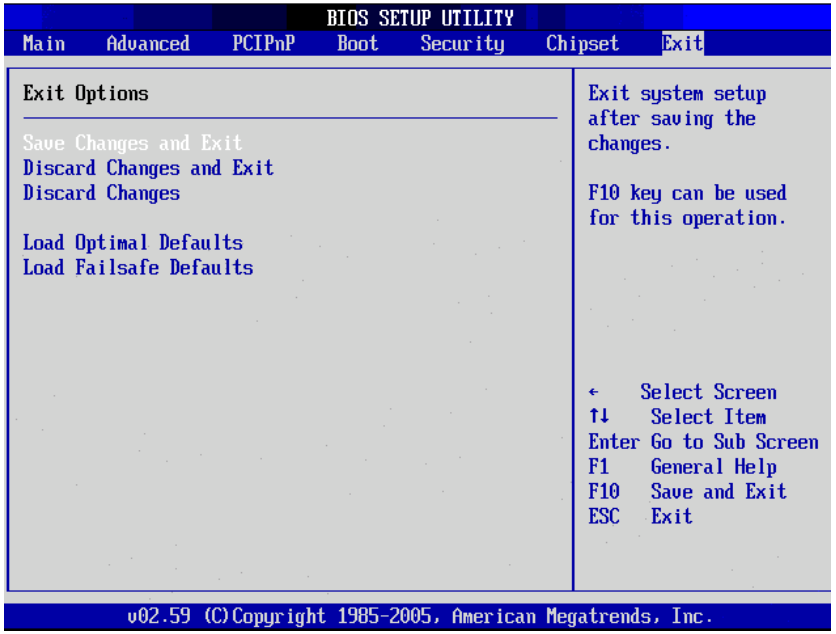


Figure 4-6: Advanced PC Health / Hardware Health Status

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4.11 Save & Exit Setup



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Appendix A Watchdog Timer

A.1 Watchdog Timer Working Procedure

Watchdog Timer (WDT) is a special hardware device that monitors the computer system during normal operation. WDT has a clock circuit that times down from a set number to zero. If a monitored item occurs before the timer reaches zero, WDT resets and counts down again. If for some reason the monitored item doesn't occur before the timer reaches zero, WDT performs an action, such as a diagnostic operation (rebooting the computer).

You must enter timer values into WDT Configuration Register (Write the control value to the Configuration Port), and clear WDT counter (read the Configuration Port).

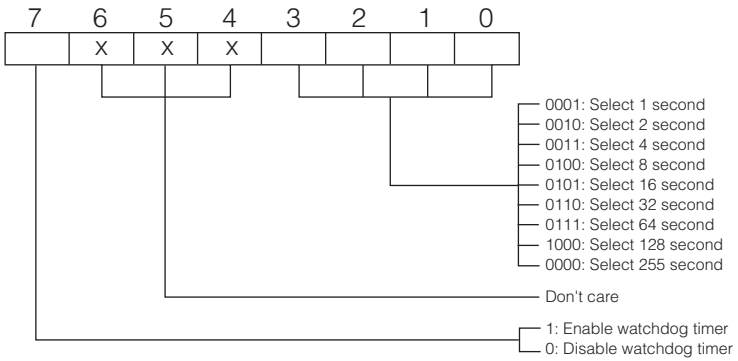
Table A-1: Watchdog Timer Character and Function

WDT Configuration port	F2	Default at F2
Watch Dog Timer	Disabled	1. Default at disabled
	Enabled	2. Enabled for user's programming
WDT Active Time	1 sec 2 sec 4 sec 8 sec 16 sec 32 sec 64 sec 128 sec 255 sec	

A.2 Watchdog Timer Control Register

Table A-2: Control Register Bit Definition

The Watchdog Timer Control Register controls the WDT working mode. Write the value to the WDT Configuration Port. The following table describes the Control Register bit definition:



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A.3 Watchdog Timer Programming Procedure

Table A-3: WDT Control Register Initial Value

Power On or Reset the System

The initial value of WDT Control Register (D7~D0) is zero (0), when power is on or the system has been reset. The following table indicates the initial value of WDT (00000000b):

Bit	Value	Mean
7	0	Disable Watchdog Timer
3, 2, 1, 0	0000	Select 255 second

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Clear the WDT

WDT counter interval cannot be longer than the preset time, otherwise, WDT sends a reset signal to the system. The following is an example of clearing the WDT program in Intel 8086 assembly language.

```
;(Clear the WDT)
Mov dx, F2h  ;Setting the WDT configuration port
In   al, dx
```

Note: Before running WDT, you must clear WDT to ensure that the initial value is zero.

WDT Control Register

Note: This register writes to WDT configuration port.

Set WDT Control Register to control the WDT working mode. The initial value of WDT Control Register is shown as follows:

```
;(Setting the WDT Control Register as AL)
Mov al, 0h  ;Setting initial value=0 for the WDT Control Register
```

Follow these instructions to set the register:

1. Select the time-out intervals of WDT (decide the values of D3, D2, D1, D0 in F2)

Example: If D3~D0 = 0, the time-out interval is 255 seconds.

```
AND        al, 10000000b ; Setting the time-out interval as 255 second.
```

2. Enable or Disable WDT (decide D7 value in F2)

i.e. D7=0, Disables WDT

```
AND        al, 01111111b ; Disable the WDT
```

i.e. D7=1, Enables WDT

```
OR         al, 10000000b ; Enable the WDT
```

After finishing the above settings, you must output the Control Register's value to WDT Configuration Port. Then WDT will start according to the above settings.

```
MOV        dx, F2h ; Setting WDT Configuration Port
OUT        dx, al ; Output the Control Register Value
```

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Appendix B GP I/O Programming

GPIO Programming Guide

It provides definitions for the four GPI/O pins in the PEAK8920. GPI/O (General Purpose Input/Output) pins are provided for custom system design.

JP4

Pin 4	Pin 6	Pin 8	Pin 10	Pin 3	Pin 5	Pin 7	Pin 9
GPIO10	GPIO11	GPIO12	GPIO13	GPIO14	GPIO15	GPIO16	GPIO17

GPIO sample code:

;###

;MSB LSB

GPIO17	GPIO16	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10

;###

;###

;Enable Configuration mode.

;###

out 2eh, 87h

out 2eh, 87h

;###

;Select logical device (GPIO1).

;###

out 2eh, 07h

out 2fh, 07h

;###

; Select function General Purpose I/O Port

;###

out 2eh, 2Ah

out 2fh, 0ffh

;###

;Activate GPIO Function.

;###

out 2eh, 30h

out 2fh, 01h

;###

;CRF0 (GP10-GP17 I/O selection register. Default 0xFF)

;When set to a '1', respective GPIO port is programmed as an input port.

;When set to a '0', respective GPIO port is programmed as an output port.

;###

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```
out 2eh, 0f0h
out 2fh, 0fh        ;GPIO10-13 as intput pin , GPIO14-17 as output pin
;#######################################################
###############
```

;CRF1 (GP10-GP17 data register. Default 0x00)

```
;If a port is programmed to be an output port, then its respective bit
can be read/written.
;If a port is programmed to be an input port, then its respective bit
can only be read.
;#######################################################
###############
out 2eh, 0f1h
out 2fh, 0f0h; pull high GPIO14-17
//#####################################################
################
// Exit Configuration mode.
//#####################################################
################
out 2eh, 0aah
```

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