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NI 5402/5406 Specifications

14/16-Bit 20/40 MHz Arbitrary Function Generator

This document lists specifications for the NI PXI/PCI-5402/5406 arbitrary function generator. Unless otherwise noted, the following conditions were used for each specification:

- Analog filter enabled.
- Interpolation set to maximum allowed factor.
- Signals terminated with 50 Ω.
- Full operating temperature range.

Typical values are representative of an average unit operating at ambient temperatures of 15 °C to 35 °C. Specifications are subject to change without notice. For the most recent NI 5402/5406 specifications, visit `ni.com/manuals`.

To access all of the NI 5402/5406 documentation, including the *NI Signal Generators Getting Started Guide*, which contains functional descriptions of the NI 5402/5406 signals, navigate to **Start»All Programs»National Instruments»NI-FGEN»Documentation**.



Hot Surface If the NI 5402/5406 has been in use, it may exceed safe handling temperatures and cause burns. Allow the NI 5402/5406 to cool before removing it from the chassis.

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NATIONAL INSTRUMENTS

Waveform Characteristics
(CH 0 Analog Output, Front Panel Connector)

Specification	Value	Comments
Number of Channels	1	—
Connector	BNC	—
Output Voltage Characteristics		
DAC Resolution	14 bits (**NI 5402**) 16 bits (**NI 5406**)	—
Maximum Voltage	± 5 V (AC_{pk} + DC)	—
Amplitude and Offset		
Amplitude Range	5.64 mV_{pk-pk} to 10 V_{pk-pk} (50 Ω load) 11.28 mV_{pk-pk} to 20 V_{pk-pk} (High impedance load)	NI-FGEN compensates for user-specified resistive loads.
Amplitude Resolution	3 digits	—
Offset Range	Square waveforms: ± 50% of Amplitude Range All other waveforms: ± 5 V	Output limited by Maximum Voltage specification.
Accuracy		
AC Amplitude Accuracy	±1.0% of Amplitude ± 1 mV	50 kHz sine wave.
Offset Accuracy	± 0.5% of Offset ± 2 mV ± 0.5% of Amplitude	High impedance load.
Output Characteristics		
Output Impedance	Selectable 50 Ω nominal or 75 Ω nominal	—
Output Enable	Selectable	When disabled, CH 0 output is terminated with a 1 W resistor with a value equal to the selected Output Impedance.

Specification	Value			Comments
Maximum Output Overload	The CH 0 output can be connected to a 50 Ω, ±12 V source without sustaining any damage. No damage occurs if the CH 0 output is shorted to ground indefinitely.			—
Waveform Summing	Outputs of multiple NI 5402/5406 signal generators can be connected together.			—
Frequency Resolution	0.355 µHz			—
Phase Adjustment	–180° to +180°			—
Digital Interpolation Filter	Selectable Finite Impulse Response (FIR) filter. Available interpolation factors are 2 or 4.			—
Analog Filter	Selectable 7-pole elliptical filter			—
Maximum Frequencies for Common Functions				
Function	**NI PXI/ PCI-5402**	**NI PXI/ PCI-5406**	Maximum Sample Rate	—
Sine	20 MHz	40 MHz	400 MS/s	
Square	20 MHz	40 MHz	400 MS/s	
Ramp	1 MHz	5 MHz	100 MS/s	
Triangle	1 MHz	5 MHz	100 MS/s	
User-Defined	20 MHz	40 MHz	400 MS/s	Interpolation set to 4.
Noise	—	—	100 MS/s	—

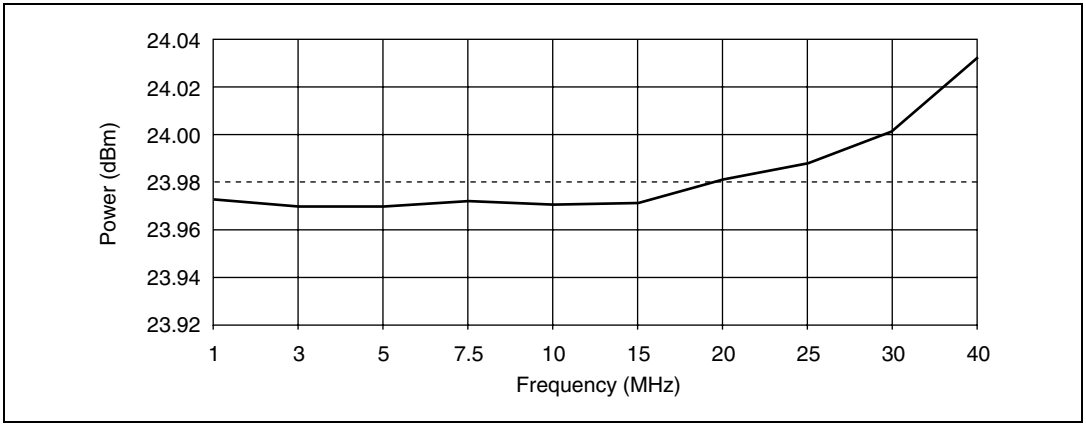


Figure 1. Nominal Passband Flatness, Expected Voltage 10 V_{pk-pk} (23.98 dBm)

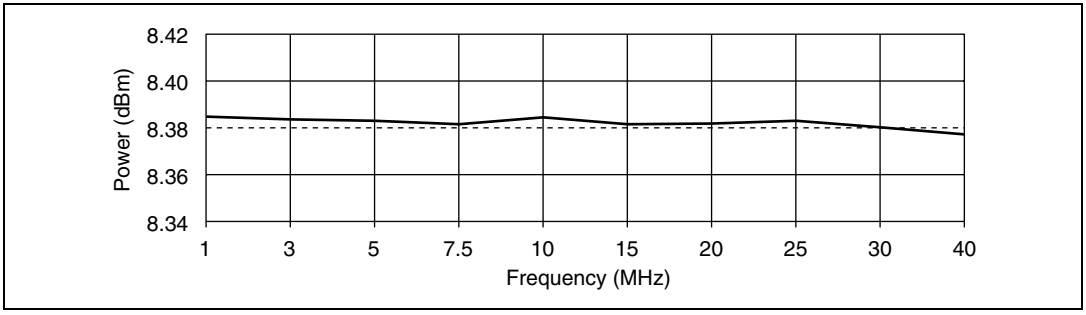


Figure 2. Nominal Passband Flatness, Expected Voltage 1.66 V_{pk-pk} (8.38 dBm)

Note Figures 1 and 2 were acquired with the Rohde & Schwarz NRVS Power Meter using the NRV-Z51 Thermal Power Sensor.

Specification	Value	Comments
Sine Waves		
Passband Flatness	±0.4 dB (± 5%)	Relative to 50 kHz
Spurious-Free Dynamic Range (SFDR) with Harmonics	–50 dBc (< 10 MHz) –45 dBc (**NI 5402**: 10 MHz to 20 MHz) (**NI 5406**: 10 MHz to 40 MHz)	Typical. Measured from DC to 50 MHz. Also called harmonic distortion.
Spurious-Free Dynamic Range (SFDR) without Harmonics	**NI 5402**: –70 dBc **NI 5406**: –70 dBc (< 20 MHz) –60 dBc (20 MHz to 40 MHz)	Typical. Measured from DC to 50 MHz.

Specification	Value		Comments
Total Harmonic Distortion (THD)	≤1.66 V_{pk-pk}	>1.66 V_{pk-pk}	Includes the 2nd through the 6th harmonics. * Typical
DC to 1 MHz	–60 dBc*	–58 dBc*	
NI 5402: 1 MHz to 20 MHz	–41 dBc	–32 dBc	
NI 5406: 1 MHz to 40 MHz	–41 dBc	–32 dBc	
Signal to Noise and Distortion (SINAD)	≤1.66 V_{pk-pk}	>1.66 V_{pk-pk}	Measured from DC to 50 MHz.
DC to 1 MHz	58 dBc	58 dBc	
NI 5402: 1 MHz to 20 MHz	41 dBc	32 dBc	
NI 5406: 1 MHz to 40 MHz	41 dBc	32 dBc	
Average Noise Density	–114 dBm/Hz		—
Phase Noise Density	100 Hz: –100 dBc/Hz 1 kHz: –110 dBc/Hz 10 kHz: –120 dBc/Hz		Sine wave at 10 MHz.
Jitter (RMS)	< 4.0 ps rms		Integrated from 100 Hz to 100 kHz. Sine wave at 10 MHz.
Notes: 1. Spectral characteristics may degrade when offset is applied. 2. Spectral characteristics at low amplitudes are limited by a –148 dBm/Hz noise floor. 3. Output amplitude of –1 dBFS is used for all spectral specifications.			
Square Waves			
Pulse Response	Rise/Fall Time	Aberration (undershoot/ overshoot)	—
	< 12 ns	< 5%	

Specification	Value	Comments
Duty Cycle	20% to 80% (< 10 MHz) **NI 5402**: 50% (10 MHz to 20 MHz) **NI 5406**: 50% (10 MHz to 40 MHz)	You can adjust duty cycle from 20 to 80% at higher frequencies, but the signal integrity degrades. For better waveforms at these duty cycles, use SYNC OUT.
Jitter (RMS)	0.01% of period + 500 ps (typical, < 2 MHz) 0.1% of period + 70 ps (≥2 MHz)	Integrated from 100 Hz to 100 kHz.
User-Defined		
Waveform Size	16,384 samples	—

Frequency List Mode

Specification	Value	Comments
Frequency Steps	1 to 9,999	—
Step Duration	1 ms to 21 sec	—

Sample Clock
(Internal 100 MHz VCXO)

Specification	Value	Comments
Clock Source	Onboard VCXO	Refer to the *Phase-Locked Loop (PLL) Reference Clock* section.
Frequency Accuracy	±25 ppm	PLL Reference source set to “None”.
Interpolation	1 (off), 2, or 4	Applicable to user-defined waveform modes.

Specification	Value			Comments
Sample Clock Exporting				
Exported Sample Clock Destinations	1. SYNC OUT/PFI 0, PFI 1(BNC connectors) 2. **NI PXI-5402/5406**—PXI_Trig<0..7> (backplane connector) **NI PCI-5402/5406**—RTSI<0..6>			Exported Sample Clocks can be divided by integer K ($1 \leq K \leq 4{,}194{,}304$).
Exported Sample Clock Destinations	Maximum Frequency	Jitter (Typical)	Duty Cycle	Integrated from 100 Hz to 100 kHz.
SYNC OUT/PFI 0, PFI 1	100 MHz	PFI 0: 6 ps rms PFI 1: 12 ps rms	25% to 65%	
PXI_Trig<0..7>	20 MHz	—	—	
RTSI<0..7>	20 MHz	—	—	

Phase-Locked Loop (PLL) Reference Clock

Specification	Value	Comments
Sources	1. REF IN (BNC connector) 2. **NI PXI-5402/5406**—PXI_CLK10 (backplane connector) **NI PCI-5402/5406**—RTSI_7 (RTSI_CLK) 3. None	The PLL Reference Clock provides the reference frequency for the phase-locked loop.
Frequency Accuracy	When you use the PLL (items 1 and 2 above), the frequency accuracy of the NI 5402/5406 is solely dependent on the frequency accuracy of the PLL Reference Clock Source.	If the PLL Reference source is set to “None”, refer to Sample Clock Frequency Accuracy.
Lock Time	Typical: 70 ms, Maximum: 200 ms	—
Frequency Range	5 MHz to 20 MHz in 1 MHz steps To guarantee locking, the PLL Reference Clock Frequency must be accurate to ±50 ppm.	Default of 10 MHz.

Specification	Value	Comments
Allowed Duty Cycle Range	40% to 60%	—
Exported PLL Reference Clock Destinations	1. SYNC OUT/PFI 0, PFI 1(BNC connectors) 2. **NI PXI-5402/5406**—PXI_Trig<0..6> (backplane connector) **NI PCI-5402/5406**—RTSI<0..6>	—

REF IN
(Reference Clock Input, Front Panel Connector)

Specification	Value	Comments
Connector	BNC	—
Direction	Input	—
Input Voltage Range	Sine wave: 0.63 V_{pk-pk} to 2.8 V_{pk-pk} into 50 Ω (0 dBm to +13 dBm) Square wave: 0.2 V_{pk-pk} to 2.8 V_{pk-pk} into 50 Ω	—
Maximum Input Overload	±10 V (AC_{pk} + DC)	—
Input Impedance	50 Ω	—
Input Coupling	AC	—

SYNC OUT/PFI 0 and PFI 1
(Programmable Function Interface, Front Panel Connectors)

Specification	Value	Comments
Connectors	Two BNC	—
Direction	Bi-directional	—
Frequency Range	DC to 100 MHz	—
As an Input (Trigger)		
Destination	Start Trigger	—
Maximum Input Overload	–2 V to +7 V (AC_{pk} + DC)	—
V_{IH}	2.0 V	—
V_{IL}	0.8 V	—
Input Impedance	1 kΩ	—
As an Output (Event)		
Sources	1. Sample Clock divided by integer K ($1 \le K \le 4{,}194{,}304$) 2. PLL Reference Clock 3. Exported Start Trigger (Out Start Trigger) 4. SYNC OUT	—
Output Impedance	50 Ω	—
Maximum Output Overload	–2 V to +7 V (AC_{pk} + DC)	—
V_{OH}	Minimum: 2.9 V (high impedance load), 1.4 V (50 Ω load)	Output drivers are +3.3 V TTL compatible.
V_{OL}	Maximum: 0.2 V (high impedance load), 0.2 V (50 Ω load)	
Rise/Fall Time (20% to 80%)	≤2.0 ns	Load of 10 pF

Sync

Specification	Value	Comments
Sync Duty Cycle	20% to 80%	—
Jitter (RMS)	0.01% of period + 500 ps (typical, < 2 MHz) 0.1% of period + 70 ps (≥ 2 MHz)	Integrated from 100 Hz to 100 kHz.

Start Trigger

Specification	Value	Comments
Sources	1. SYNC OUT/PFI 0, PFI 1(BNC connectors) 2. **NI PXI-5402/5406**—PXI_Trig<0..7> (backplane connector) **NI PCI-5402/5406**—RTSI<0..7> 3. **NI PXI-5402/5406**—PXI Star Trigger (backplane connector) 4. Software (use function call) 5. Immediate (does not wait for a trigger)—Default	—
Modes	1. Single 2. Continuous 3. Stepped 4. Burst	Refer to **NI Signal Generators Help»Devices» NI 5402/5406»NI <bus> -5402/5406»Waveform Generation»Frequency List»Trigger Modes**.
Edge Detection	Rising, falling, level high, level low	—
Minimum Pulse Width	25 ns	Refer to t_{s1} at **NI Signal Generators Help»Devices» NI 5402/5406»NI <bus> -5402/5406»Triggering» Trigger Timing**.

<table>
<tr><th>Specification</th><th colspan="2">Value</th><th>Comments</th></tr>
<tr><td rowspan="4">Delay from Start Trigger to CH 0 Analog Output</td><td>Waveform</td><td>Delay (typical)</td><td rowspan="4">Refer to t_{s2} at NI Signal Generators Help»Devices» NI 5402/5406»NI <bus> -5402/5406»Triggering» Trigger Timing.</td></tr>
<tr><td>Sine</td><td>1,100 ns</td></tr>
<tr><td>Square</td><td>1,100 ns + 0.5% of period</td></tr>
<tr><td>All Others</td><td>900 ns</td></tr>
<tr><td colspan="4">Start Trigger Exporting</td></tr>
<tr><td>Destinations</td><td colspan="2">1. SYNC OUT/PFI 0, PFI 1 (BNC Connectors)
2. NI PXI-5402/5406—PXI_Trig<0..6> (backplane connector)
NI PCI-5402/5406—RTSI<0..6></td><td>—</td></tr>
<tr><td>Delay</td><td colspan="2">65 ns (typical)</td><td rowspan="2">Refer to t_{s3} and t_{s4} at NI Signal Generators Help»Devices» NI 5402/5406»NI <bus> -5402/5406»Triggering» Trigger Timing.</td></tr>
<tr><td>Pulse Width</td><td colspan="2">> 150 ns</td></tr>
</table>

Calibration

Specification	Value	Comments
Self-Calibration	An onboard, 24-bit ADC and precision voltage reference are used to calibrate the gain and offset. Square waveform duty cycle is also calibrated. The self-calibration is initiated by the user through the software and takes approximately 105 seconds to complete.	—
External Calibration	The External Calibration calibrates the VCXO, voltage reference, self-calibration ADC, flatness, gain, and offset. Appropriate constants are stored in nonvolatile memory.	Also known as factory calibration.
Calibration Interval	Specifications valid within 2 years of External Calibration.	—
Warm-up Time	15 minutes	—

Power

Specification	Value	Comments
+3.3 VDC	1.4 A	—
+5 VDC	See Figure 3.	
+12 VDC	0.11 A	
–12 VDC	0.01 A	
Total Power	17.6 W	

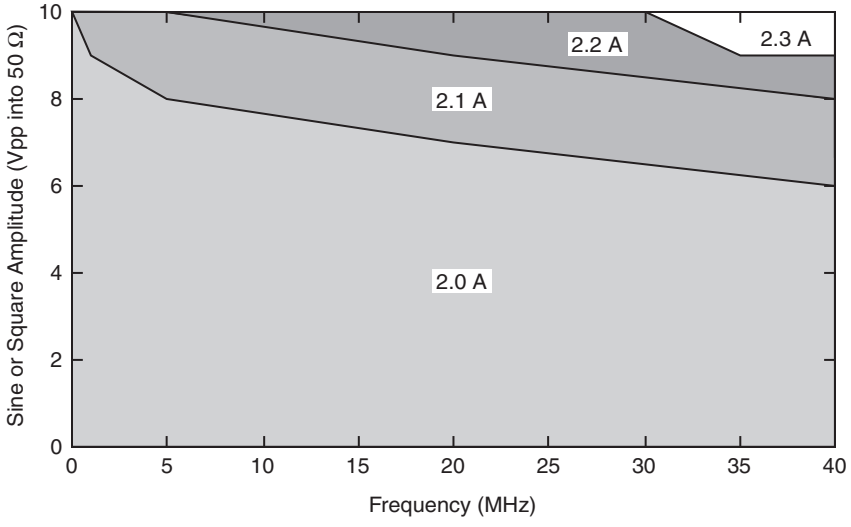


Figure 3. 5 V Current Versus Frequency and Amplitude

Software

Specification	Value	Comments
Driver Software	NI-FGEN 2.4 or later version. NI-FGEN is an IVI-compliant driver that allows you to configure, control, and calibrate the NI 5402/5406. NI-FGEN provides application programming interfaces for many development environments.	—
Application Software	NI-FGEN provides programming interfaces for the following application development environments: • LabVIEW • LabWindows™/CVI™ • Measurement Studio • Microsoft Visual C/C++ • Microsoft Visual Basic	—
Soft Front Panel/ Interactive Configuration	The FGEN Soft Front Panel supports interactive control of the NI 5402/5406. The FGEN Soft Front Panel is included on the NI-FGEN driver CD. Measurement & Automation Explorer (MAX) provides interactive configuration and test tools for the NI 5402/5406. MAX is also included on the NI-FGEN CD. You can use the NI 5402/5406 with NI SignalExpress.	—

Environment

NI PXI-5402/5406 Environment

Note To ensure that the NI PXI-5402/5406 cools effectively, follow the guidelines in the *Maintain Forced-Air Cooling Note to Users* included in the NI 5402/5406 kit. The NI PXI-5402/5406 is intended for indoor use only.

Specifications	Value	Comments
Operating Temperature	0 ºC to +55 ºC when installed in an NI PXI chassis, except for the following: 0 ºC to +45 ºC when installed in an NI PXI-101*X* or NI PXI-1000/B chassis. Meets IEC-60068-2-1 and IEC-60068-2-2.	—
Storage Temperature	–25 ºC to +85 ºC. Meets IEC-60068-2-1 and IEC-60068-2-2.	—
Operating Relative Humidity	10% to 90%, noncondensing. Meets IEC-60068-2-56.	—
Storage Relative Humidity	5% to 95%, noncondensing. Meets IEC-60068-2-56.	—
Operating Shock	30 g, half-sine, 11 ms pulse. Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	Spectral and jitter specifications could degrade.
Storage Shock	50 g, half-sine, 11 ms pulse. Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	—
Operating Vibration	5 Hz to 500 Hz, 0.31 g_{rms}. Meets IEC-60068-2-64.	Spectral and jitter specifications could degrade.
Storage Vibration	5 Hz to 500 Hz, 2.46 g_{rms}. Meets IEC-60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.	—
Altitude	2,000 m maximum (at 25 °C ambient temperature)	—
Pollution Degree	2	—

NI PCI-5402/5406 Environment

Note To ensure that the NI PCI-5402/5406 cools effectively, follow the guidelines in the *Maintain Forced-Air Cooling Note to Users* included in the NI 5402/5406 kit. Also, to maximize airflow and extend the life of the device, leave any adjacent PCI slots empty. The NI PCI-5402/5406 is intended for indoor use only.

Specifications	Value	Comments
Operating Temperature	0 ºC to +45 ºC. Meets IEC-60068-2-1 and IEC-60068-2-2.	—
Storage Temperature	–25 ºC to +85 ºC. Meets IEC-60068-2-1 and IEC-60068-2-2.	—
Operating Relative Humidity	10% to 90%, noncondensing. Meets IEC-60068-2-56.	—
Storage Relative Humidity	5% to 95%, noncondensing. Meets IEC-60068-2-56.	—
Storage Shock	50 g, half-sine, 11 ms pulse. Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	—
Storage Vibration	5 Hz to 500 Hz, 2.46 g_{rms}. Meets IEC-60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.	—
Altitude	2,000 m maximum (at 25 °C ambient temperature)	—
Pollution Degree	2	—

Safety, Electromagnetic Compatibility, and CE Compliance

Specification	Value	Comments
Safety	The NI 5402/5406 is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use: IEC 61010-1, EN 61010-1 UL 61010-1 CAN/CSA-C22.2 No. 61010-1	—
Note: For UL and other safety certifications, refer to the product label or visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.		
Emissions	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz	—
Immunity	EN 61326:1997 + A2:2001, Table 1	—
EMC/EMI	CE, C-Tick, and FCC Part 15 (Class A) Compliant **Notes**: 1. This device is not intended for, and is restricted from, use in residential areas. 2. For EMC compliance, operate this device with shielded cabling. 3. When connected to other test objects, this product may cause radio interference. If this occurs, you may be required to take adequate measures to reduce the interference.	—
This product meets the essential requirements of applicable European Directives as amended for CE marking, as follows:		
Low-Voltage Directive (safety)	73/23/EEC	—
Electromagnetic Compatibility Directive (EMC)	89/336/EEC	—
Note: Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.		

Physical

Specification	Value		Comments
Dimensions	NI PXI-5402/5406	NI PCI-5402/5406	—
	3U, One Slot, PXI/cPCI Module 21.6 × 2.0 × 13.0 cm (8.5 × 0.8 × 5.1 inches)	34.1 × 2.0 × 10.7 cm (13.4 × 0.8 × 4.2 inches)	
Weight	351 g (12.4 oz)	420 g (14.8 oz)	—
Front Panel Connectors			
Label	Function(s)	Connector Type	—
CH 0	Analog Output	BNC (female)	
REF IN	PLL reference clock input	BNC (female)	
SYNC OUT/PFI 0	Trigger input, sample clock output, exported trigger output, PLL reference clock output, and SYNC OUT	BNC (female)	
PFI 1	Trigger input, sample clock output, exported trigger output, PLL reference clock output, and SYNC OUT	BNC (female)	
NI PXI-5402/5406 Only—Front Panel LED Indicators			
Label	Function		For more information, refer to the *NI Signal Generators Help.*
ACCESS LED	The ACCESS LED indicates the status of the PCI bus and the interface from the NI 5402/5406 to the controller.		
ACTIVE LED	The ACTIVE LED indicates the status of the onboard generation hardware of the NI 5402/5406.		

Where to Go for Support

The National Instruments Web site is your complete resource for technical support. At ni.com/support you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from NI Application Engineers.

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