DAQ

6034E/6035E User Manual

Multifunction I/O Boards for PCI, PXI, and CompactPCI Bus Computers

NATIONAL INSTRUMENTS™

July 1999 Edition
Part Number 322339A-01

Worldwide Technical Support and Product Information

`www.natinst.com`

National Instruments Corporate Headquarters

11500 North Mopac Expressway   Austin, Texas 78759-3504   USA   Tel: 512 794 0100

Worldwide Offices

Australia 03 9879 5166, Austria 0662 45 79 90 0, Belgium 02 757 00 20, Brazil 011 284 5011,
Canada (Ontario) 905 785 0085, Canada (Québec) 514 694 8521, China 0755 3904939, Denmark 45 76 26 00,
Finland 09 725 725 11, France 01 48 14 24 24, Germany 089 741 31 30, Hong Kong 2645 3186,
India 91805275406, Israel 03 6120092, Italy 02 413091, Japan 03 5472 2970, Korea 02 596 7456,
Mexico (D.F.) 5 280 7625, Mexico (Monterrey) 8 357 7695, Netherlands 0348 433466, Norway 32 27 73 00,
Singapore 2265886, Spain (Madrid) 91 640 0085, Spain (Barcelona) 93 582 0251, Sweden 08 587 895 00,
Switzerland 056 200 51 51, Taiwan 02 2377 1200, United Kingdom 01635 523545

For further support information, see the *Technical Support Resources* appendix. To comment on the documentation, send e-mail to `techpubs@natinst.com`.

Important Information

Warranty

The 6034E and 6035E boards are warranted against defects in materials and workmanship for a period of one year from the date of shipment, as evidenced by receipts or other documentation. National Instruments will, at its option, repair or replace equipment that proves to be defective during the warranty period. This warranty includes parts and labor.

The media on which you receive National Instruments software are warranted not to fail to execute programming instructions, due to defects in materials and workmanship, for a period of 90 days from date of shipment, as evidenced by receipts or other documentation. National Instruments will, at its option, repair or replace software media that do not execute programming instructions if National Instruments receives notice of such defects during the warranty period. National Instruments does not warrant that the operation of the software shall be uninterrupted or error free.

A Return Material Authorization (RMA) number must be obtained from the factory and clearly marked on the outside of the package before any equipment will be accepted for warranty work. National Instruments will pay the shipping costs of returning to the owner parts which are covered by warranty.

National Instruments believes that the information in this document is accurate. The document has been carefully reviewed for technical accuracy. In the event that technical or typographical errors exist, National Instruments reserves the right to make changes to subsequent editions of this document without prior notice to holders of this edition. The reader should consult National Instruments if errors are suspected. In no event shall National Instruments be liable for any damages arising out of or related to this document or the information contained in it.

EXCEPT AS SPECIFIED HEREIN, NATIONAL INSTRUMENTS MAKES NO WARRANTIES, EXPRESS OR IMPLIED, AND SPECIFICALLY DISCLAIMS ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. CUSTOMER'S RIGHT TO RECOVER DAMAGES CAUSED BY FAULT OR NEGLIGENCE ON THE PART OF NATIONAL INSTRUMENTS SHALL BE LIMITED TO THE AMOUNT THERETOFORE PAID BY THE CUSTOMER. NATIONAL INSTRUMENTS WILL NOT BE LIABLE FOR DAMAGES RESULTING FROM LOSS OF DATA, PROFITS, USE OF PRODUCTS, OR INCIDENTAL OR CONSEQUENTIAL DAMAGES, EVEN IF ADVISED OF THE POSSIBILITY THEREOF. This limitation of the liability of National Instruments will apply regardless of the form of action, whether in contract or tort, including negligence. Any action against National Instruments must be brought within one year after the cause of action accrues. National Instruments shall not be liable for any delay in performance due to causes beyond its reasonable control. The warranty provided herein does not cover damages, defects, malfunctions, or service failures caused by owner's failure to follow the National Instruments installation, operation, or maintenance instructions; owner's modification of the product; owner's abuse, misuse, or negligent acts; and power failure or surges, fire, flood, accident, actions of third parties, or other events outside reasonable control.

Copyright

Trademarks

ComponentWorks™, CVI™, DAQ-STC™, LabVIEW™, Measure™, MITE™, `natinst.com`™, NI-DAQ™, RTSI™, SCXI™, and VirtualBench™ are trademarks of National Instruments Corporation.

Product and company names mentioned herein are trademarks or trade names of their respective companies.

WARNING REGARDING MEDICAL AND CLINICAL USE OF NATIONAL INSTRUMENTS PRODUCTS

National Instruments products are not designed with components and testing for a level of reliability suitable for use in or in connection with surgical implants or as critical components in any life support systems whose failure to perform can reasonably be expected to cause significant injury to a human. Applications of National Instruments products involving medical or clinical treatment can create a potential for death or bodily injury caused by product failure, or by errors on the part of the user or application designer. Because each end-user system is customized and differs from National Instruments testing platforms and because a user or application designer may use National Instruments products in combination with other products in a manner not evaluated or contemplated by National Instruments, the user or application designer is ultimately responsible for verifying and validating the suitability of National Instruments products whenever National Instruments products are incorporated in a system or application, including, without limitation, the appropriate design, process and safety level of such system or application.

Contents

About This Manual

Chapter 1
Introduction

Chapter 2
Installation and Configuration

Chapter 3
Hardware Overview

Chapter 4
Signal Connections

Chapter 5 Calibration

Appendix A Specifications

Appendix B Custom Cabling and Optional Connectors

Appendix C Common Questions

Appendix D Technical Support Resources

Glossary

Index

Figures

Tables

About This Manual

The 6034 and 6035 E Series devices are high-performance multifunction analog, digital, and timing I/O devices for PCI, PXI, and CompactPCI bus computers. Supported functions include analog input, analog output, digital I/O, and timing I/O.

This manual describes the electrical and mechanical aspects of the PCI-6034E, PCI-6035E, and PXI-6035E devices from the E Series product line and contains information concerning their operation and programming.

Conventions Used in This Manual

The following conventions are used in this manual:

<> — Angle brackets containing numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DBIO<3..0>.

♦ — The ♦ symbol indicates that the text following it applies only to a specific product, a specific operating system, or a specific software version.

This icon denotes a note, which alerts you to important information.

This icon to the left of bold italicized text denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.

bold — Bold text denotes items that you must select or click on in the software, such as menu items and dialog box options. Bold text also denotes parameter names.

italic — Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.

`monospace` — Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.

CompactPCI — Refers to the core specification defined by the PCI Industrial Computer Manufacturer’s Group (PICMG)

NI-DAQ — Refers to the NI-DAQ driver software for PC compatible computers unless otherwise noted.

PC — Refers to all PC AT series computers with PCI or PXI bus unless otherwise noted.

PXI — Stands for PCI eXtensions for Instrumentation. PXI is an open specification that builds off the CompactPCI specification by adding instrumentation-specific features.

Related Documentation

The following documents contain information you may find helpful:

- *DAQ-STC Technical Reference Manual*
- National Instruments Application Note 025, *Field Wiring and Noise Considerations for Analog Signals*
- *PCI Local Bus Specification Revision 2.1*
- *PICMG CompactPCI 2.0 Revision 2.1*
- *PXI Bus Specification Revision 1.0*

The following National Instruments manual contains detailed information for the register-level programmer:

- *PCI E Series Register-Level Programmer Manual*

  This manual is available from National Instruments by request. You should not need the register-level programmer manual if you are using National Instruments driver or application software. Using NI-DAQ, ComponentWorks, LabVIEW, LabWindows/CVI, Measure, or VirtualBench software is easier than the low-level programming described in the register-level programmer manual.

1 Introduction

This chapter describes the 6034E and 6035E devices, lists what you need to get started, gives unpacking instructions, and describes the optional software and equipment.

Features of the 6034E and 6035E

Thank you for buying a National Instruments 6034E or 6035E device. The 6035E features 16 channels (eight differential) of 16-bit analog input, two channels of 12-bit analog output, a 68-pin connector, and eight lines of digital I/O. The 6034E is identical to the 6035E, except that it does not have analog output channels.

These devices use the National Instruments DAQ-STC system timing controller for time-related functions. The DAQ-STC consists of three timing groups that control analog input, analog output, and general-purpose counter/timer functions. These groups include a total of seven 24-bit and three 16-bit counters and a maximum timing resolution of 50 ns. The DAQ-STC makes possible such applications as buffered pulse generation, equivalent time sampling, and seamless changing of the sampling rate.

With other DAQ devices, you cannot easily synchronize several measurement functions to a common trigger or timing event. These devices have the Real-Time System Integration (RTSI) bus to solve this problem. In a PCI system, the RTSI bus consists of the National Instruments RTSI bus interface and a ribbon cable to route timing and trigger signals between several functions on as many as five DAQ devices in your computer. In a PXI system, the RTSI bus consists of the National Instruments RTSI bus interface and the PXI trigger signals on the PXI backplane to route timing and trigger signals between several functions on as many as seven DAQ devices in your system.

These devices can interface to an SCXI system—the instrumentation front end for plug-in DAQ devices—so that you can acquire analog signals from thermocouples, RTDs, strain gauges, voltage sources, and current sources. You can also acquire or generate digital signals for communication and control.

Using PXI with CompactPCI

Using PXI compatible products with standard CompactPCI products is an important feature provided by *PXI Specification, Revision 1.0*. If you use a PXI compatible plug-in card in a standard CompactPCI chassis, you will be unable to use PXI-specific functions, but you can still use the basic plug-in card functions. For example, the RTSI bus on your PXI E Series device is available in a PXI chassis, but not in a CompactPCI chassis.

The CompactPCI specification permits vendors to develop sub-buses that coexist with the basic PCI interface on the CompactPCI bus. Compatible operation is not guaranteed between CompactPCI devices with different sub-buses nor between CompactPCI devices with sub-buses and PXI. The standard implementation for CompactPCI does not include these sub-buses. Your PXI E Series device will work in any standard CompactPCI chassis adhering to *PICMG CompactPCI 2.0 R2.1* core specification.

PXI specific features are implemented on the J2 connector of the CompactPCI bus. Table 3-3 lists the J2 pins used by your PXI E Series device. Your PXI device is compatible with any Compact PCI chassis with a sub-bus that does not drive these lines. Even if the sub-bus is capable of driving these lines, the PXI device is still compatible as long as those pins on the sub-bus are disabled by default and not ever enabled. Damage may result if these lines are driven by the sub-bus.

What You Need to Get Started

To set up and use your device, you will need the following:

❑ One of the following devices:
- PCI-6034E
- PCI-6035E
- PXI-6035E

❑ *6034E/6035E User Manual*

❑ One of the following software packages and documentation:
- ComponentWorks
- LabVIEW for Windows
- LabWindows/CVI for Windows

- Measure
- NI-DAQ for PC Compatibles
- VirtualBench

❑ Your computer equipped with one of the following:

- PCI bus for a PCI device
- PXI or CompactPCI chassis and controller for a PXI device

Note Read Chapter 2, *Installation and Configuration*, before installing your device. Always install your software before installing your device.

Unpacking

Your device is shipped in an antistatic package to prevent electrostatic damage to the device. Electrostatic discharge can damage several components on the device. To avoid such damage in handling the device, take the following precautions:

- Ground yourself via a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of your computer chassis before removing the device from the package.
- Remove the device from the package and inspect the device for loose components or any other sign of damage. Notify National Instruments if the device appears damaged in any way. Do *not* install a damaged device into your computer.
- *Never* touch the exposed pins of connectors.

Software Programming Choices

You have several options to choose from when programming your National Instruments DAQ and SCXI hardware. You can use National Instruments application software, NI-DAQ, or register-level programming.

National Instruments Application Software

ComponentWorks contains tools for data acquisition and instrument control built on NI-DAQ driver software. ComponentWorks provides a higher-level programming interface for building virtual instruments through standard OLE controls and DLLs. With ComponentWorks, you can use all of the configuration tools, resource management utilities, and interactive control utilities included with NI-DAQ.

LabVIEW features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW. The LabVIEW Data Acquisition VI Library is functionally equivalent to NI-DAQ software.

LabWindows/CVI features interactive graphics, state-of-the-art user interface, and uses the ANSI standard C programming language. The LabWindows/CVI Data Acquisition Library, a series of functions for using LabWindows/CVI with National Instruments DAQ hardware, is included with the NI-DAQ software kit. The LabWindows/CVI Data Acquisition Library is functionally equivalent to the NI-DAQ software.

VirtualBench features virtual instruments that combine DAQ products, software, and your computer to create a stand-alone instrument with the added benefit of the processing, display, and storage capabilities of your computer. VirtualBench instruments load and save waveform data to disk in the same forms that can be used in popular spreadsheet programs and word processors.

Using ComponentWorks, LabVIEW, LabWindows/CVI, or VirtualBench software will greatly reduce the development time for your data acquisition and control application.

NI-DAQ Driver Software

The NI-DAQ driver software is included at no charge with all National Instruments DAQ hardware. NI-DAQ is not packaged with SCXI or accessory products, except for the SCXI-1200. NI-DAQ has an extensive library of functions that you can call from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation (timed D/A conversion), digital I/O, counter/timer operations, SCXI, RTSI, self-calibration, messaging, and acquiring data to extended memory.

NI-DAQ has both high-level DAQ I/O functions for maximum ease of use and low-level DAQ I/O functions for maximum flexibility and performance. Examples of high-level functions are streaming data to disk or acquiring a certain number of data points. An example of a low-level function is writing directly to registers on the DAQ device. NI-DAQ does not sacrifice the performance of National Instruments DAQ devices because it lets multiple devices operate at their peak.

NI-DAQ also internally addresses many of the complex issues between the computer and the DAQ hardware such as programming interrupts and DMA controllers. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Whether you are using conventional programming languages or National Instruments application software, your application uses the NI-DAQ driver software, as illustrated in Figure 1-1.

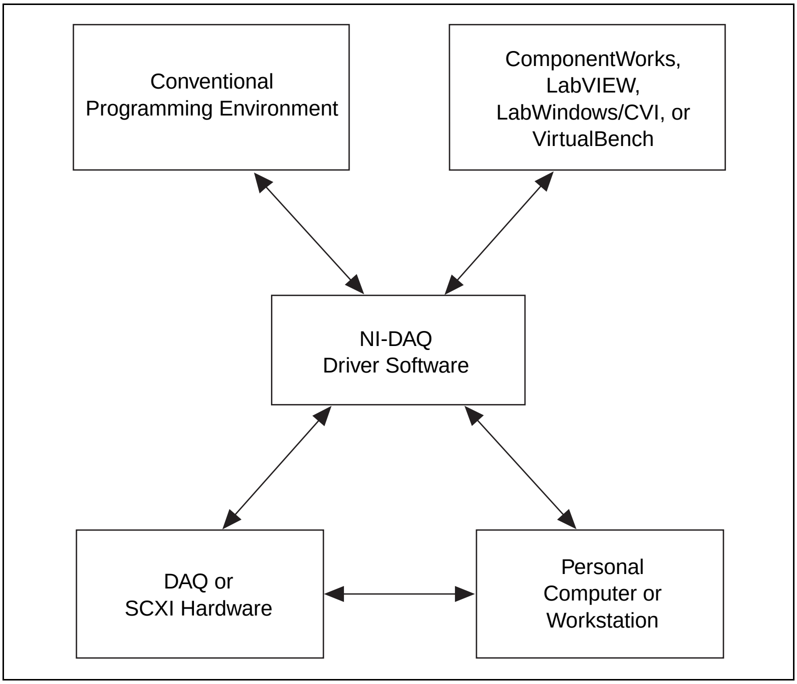


Figure 1-1. The Relationship between the Programming Environment, NI-DAQ, and Your Hardware

Register-Level Programming

The final option for programming any National Instruments DAQ hardware is to write register-level software. Writing register-level programming software can be very time-consuming and inefficient, and is not recommended for most users.

Even if you are an experienced register-level programmer, using NI-DAQ or application software to program your National Instruments DAQ hardware is easier than, and as flexible as, register-level programming, and can save weeks of development time.

Optional Equipment

National Instruments offers a variety of products to use with your device, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies, shielded and ribbon
- Connector blocks, shielded and unshielded screw terminals
- RTSI bus cables
- SCXI modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output. With SCXI you can condition and acquire up to 3,072 channels.
- Low channel count signal conditioning modules, devices, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample and hold, and relays

For more information about these products, refer to the National Instruments catalogue or Web site or call the office nearest you.

2

Installation and Configuration

This chapter explains how to install and configure your 6034E or 6035E.

Software Installation

Caution You should install your software before you install your device.

If you are using LabVIEW, LabWindows/CVI, other National Instruments application software packages, or the NI-DAQ driver software, refer to the appropriate release notes. After you have installed your application software, refer to your NI-DAQ release notes and follow the instructions given there for your operating system and application software package.

If you are a register-level programmer, refer to the *PCI E Series Register-Level Programmer Manual* and the *DAQ-STC Technical Reference Manual* for software configuration information.

Hardware Installation

Note Install your software before you install your device.

After installing your software, you are ready to install your hardware. Your device will fit in any 5 V expansion slot in your computer. However, to achieve best noise performance, leave as much room as possible between your device and other devices. The following are general installation instructions. Consult your computer user manual or technical reference manual for specific instructions and warnings.

♦ PCI Installation

1. Turn off and unplug your computer.
2. Remove the top cover of your computer.
3. Remove the expansion slot cover on the back panel of the computer.

4. Touch any metal part of your computer chassis to discharge any static electricity that might be on your clothes or body.
5. Insert the device into a 5 V PCI slot. Gently rock the device to ease it into place. It may be a tight fit, but *do not force* the device into place.
6. Screw the mounting bracket of the device to the back panel rail of the computer.
7. Visually verify the installation.
8. Replace the top cover of your computer.
9. Plug in and turn on your computer.

- PXI Installation

1. Turn off and unplug your computer.
2. Choose an unused PXI slot in your system. For maximum performance, the device has an onboard DMA controller that can only be used if the device is installed in a slot that supports bus arbitration, or bus master cards. National Instruments recommends installing the device in such a slot. The PXI specification requires all slots to support bus master cards, but the CompactPCI specification does not. If you install in a CompactPCI non-master slot, you must disable the device onboard DMA controller using software.
3. Remove the filler panel for the slot you have chosen.
4. Touch any metal part of your computer chassis to discharge any static electricity that might be on your clothes or body.
5. Insert the device into a 5 V PXI slot. Use the injector/ejector handle to fully insert the device into the chassis.
6. Screw the front panel of the device to the front panel mounting rail of the system.
7. Visually verify the installation.
8. Plug in and turn on your computer.

The device is installed. You are now ready to configure your hardware and software.

Hardware Configuration

Due to the National Instruments standard architecture for data acquisition and standard bus specifications, these devices are completely software-configurable. You must perform two types of configuration on the devices—bus-related and data acquisition-related configuration.

The PCI devices are fully compatible with the industry-standard *PCI Local Bus Specification Revision 2.1*. The PXI device is fully compatible with the *PXI Specification Revision 1.0*. These specifications let your computer automatically set the device base memory address and interrupt channel with no user interaction.

You can modify data acquisition-related configuration settings, such as analog input range and mode, through application-level software. Refer to Chapter 3, *Hardware Overview*, for more information about the various settings available for your device. These settings are changed and configured through software after you install your device. Refer to your software documentation for configuration instructions.

3

Hardware Overview

This chapter presents an overview of the hardware functions on your device.

Figure 3-1 shows a block diagram for the 6034E and 6035E.

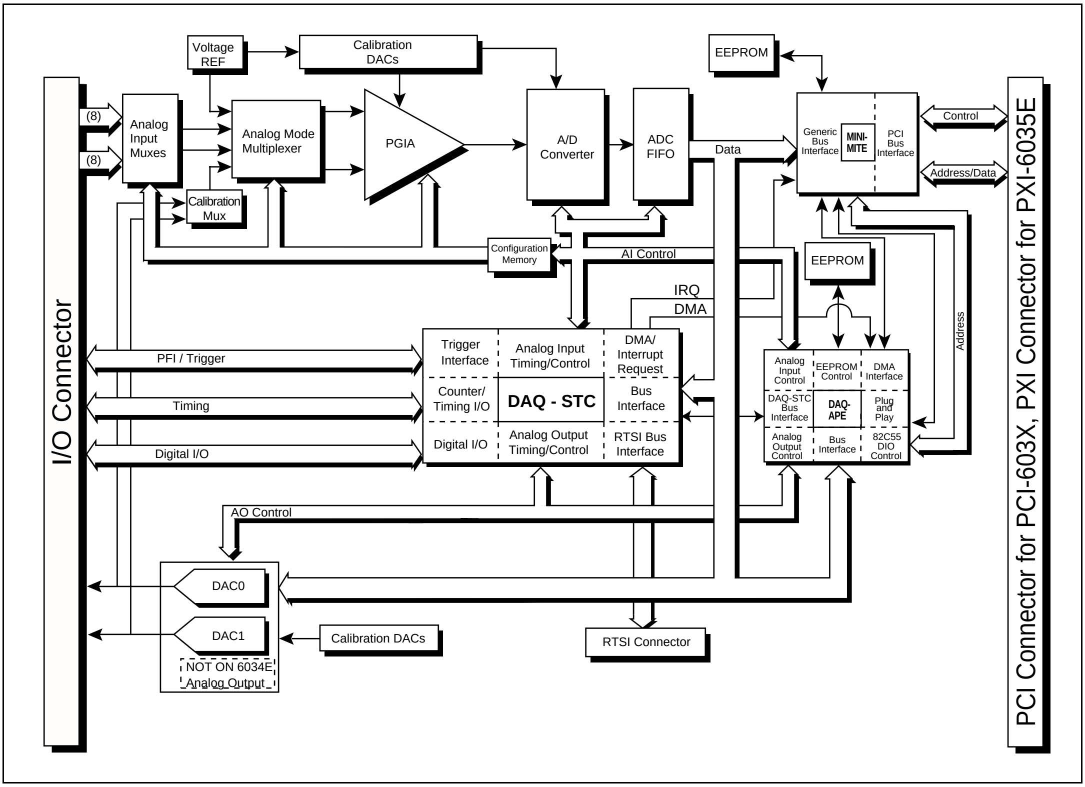


Figure 3-1. 6034E and 6035E Block Diagram

Analog Input

The analog input section of each device is software configurable. The following sections describe in detail each of the analog input settings.

Input Mode

The devices have three different input modes—nonreferenced single-ended (NRSE) input, referenced single-ended (RSE) input, and differential (DIFF) input. The single-ended input configurations provide up to 16 channels. The DIFF input configuration provides up to eight channels. Input modes are programmed on a per channel basis for multimode scanning. For example, you can configure the circuitry to scan 12 channels—four differentially-configured channels and eight single-ended channels. Table 3-1 describes the three input configurations.

Table 3-1. Available Input Configurations

Configuration	Description
DIFF	A channel configured in DIFF mode uses two analog input lines. One line connects to the positive input of the device's programmable gain instrumentation amplifier (PGIA), and the other connects to the negative input of the PGIA.
RSE	A channel configured in RSE mode uses one analog input line, which connects to the positive input of the PGIA. The negative input of the PGIA is internally tied to analog input ground (AIGND).
NRSE	A channel configured in NRSE mode uses one analog input line, which connects to the positive input of the PGIA. The negative input of the PGIA connects to analog input sense (AISENSE).

For diagrams showing the signal paths of the three configurations, refer to the *Analog Input Signal Overview* section in Chapter 4, *Signal Connections*.

Input Range

The devices have a bipolar input range that changes with the programmed gain. Each channel may be programmed with a unique gain of 0.5, 1.0, 10, or 100 to maximize the 16-bit analog-to-digital converter (ADC) resolution. With the proper gain setting, you can use the full resolution of the ADC to measure the input signal. Table 3-2 shows the input range and precision according to the gain used.

Table 3-2. Measurement Precision

Gain	Input Range	Precision *
0.5	–10 to +10 V	305.2 μV
1.0	–5 to +5 V	152.6 μV
10.0	–500 to +500 mV	15.3 μV
100.0	–50 to +50 mV	1.53 μV

*The value of 1 LSB of the 16-bit ADC; that is, the voltage increment corresponding to a change of one count in the ADC 16-bit count.

Note: See Appendix A, *Specifications*, for absolute maximum ratings.

Multichannel Scanning Considerations

The devices can scan multiple channels at the same maximum rate as their single-channel rate; however, pay careful attention to the settling times for each of the devices. No extra settling time is necessary between channels as long as the gain is constant and source impedances are low. Refer to Appendix A, *Specifications*, for a complete listing of settling times for each of the devices.

When scanning among channels at various gains, the settling times may increase. When the PGIA switches to a higher gain, the signal on the previous channel may be well outside the new, smaller range. For instance, suppose a 4 V signal is connected to channel 0 and a 1 mV signal is connected to channel 1, and suppose the PGIA is programmed to apply a gain of one to channel 0 and a gain of 100 to channel 1. When the multiplexer switches to channel 1 and the PGIA switches to a gain of 100, the new full-scale range is ±50 mV.

The approximately 4 V step from 4 V to 1 mV is 4,000% of the new full-scale range. It may take as long as 100 µs for the circuitry to settle to 1 LSB after such a large transition. In general, this extra settling time is not needed when the PGIA is switching to a lower gain.

Settling times can also increase when scanning high-impedance signals due to a phenomenon called *charge injection*, where the analog input multiplexer injects a small amount of charge into each signal source when that source is selected. If the impedance of the source is not low enough, the effect of the charge—a voltage error—will not have decayed by the time the ADC samples the signal. For this reason, keep source impedances under 1 kΩ to perform high-speed scanning.

Due to the previously described limitations of settling times resulting from these conditions, multiple-channel scanning is not recommended unless sampling rates are low enough or it is necessary to sample several signals as nearly simultaneously as possible. The data is much more accurate and channel-to-channel independent if you acquire data from each channel independently (for example, 100 points from channel 0, then 100 points from channel 1, then 100 points from channel 2, and so on.)

Analog Output

♦ 6035E only

These devices supply two channels of 12-bit analog output voltage at the I/O connector. The bipolar range is fixed at ±10 V. Data written to the digital-to-analog converter (DAC) will be interpreted as two's complement format.

Analog Output Glitch

In normal operation, a DAC output will glitch whenever it is updated with a new value. The glitch energy differs from code to code and appears as distortion in the frequency spectrum.

Digital I/O

The devices contain eight lines of digital I/O (DIO<0..7>) for general-purpose use. You can individually software-configure each line for either input or output. At system startup and reset, the digital I/O ports are all high impedance.

The hardware up/down control for general-purpose counters 0 and 1 are connected onboard to DIO6 and DIO7, respectively. Thus, you can use DIO6 and DIO7 to control the general-purpose counters. The up/down control signals are input only and do not affect the operation of the DIO lines.

Timing Signal Routing

The DAQ-STC chip provides a flexible interface for connecting timing signals to other devices or external circuitry. Your device uses the RTSI bus to interconnect timing signals between devices, and the Programmable Function Input (PFI) pins on the I/O connector to connect the device to external circuitry. These connections are designed to enable the device to both control and be controlled by other devices and circuits.

There are a total of 13 timing signals internal to the DAQ-STC that can be controlled by an external source. These timing signals can also be controlled by signals generated internally to the DAQ-STC, and these selections are fully software-configurable. Figure 3-2 shows an example of the signal routing multiplexer controlling the CONVERT* signal.

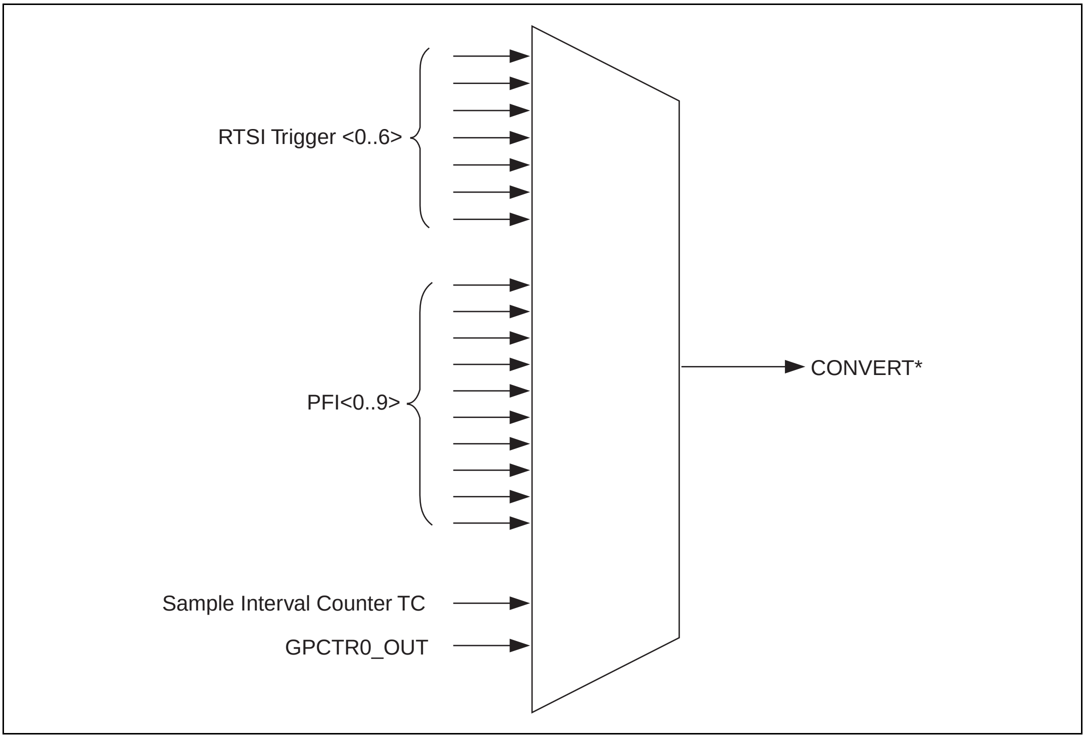


Figure 3-2. CONVERT* Signal Routing

This figure shows that CONVERT* can be generated from a number of sources, including the external signals RTSI<0..6> and PFI<0..9> and the internal signals Sample Interval Counter TC and GPCTR0_OUT.

Many of these timing signals are also available as outputs on the RTSI pins, as indicated in the *RTSI Triggers* section in this chapter, and on the PFI pins, as indicated in Chapter 4, *Signal Connections*.

Programmable Function Inputs

Ten PFI pins are available on the device connector as PFI<0..9> and are connected to the device's internal signal routing multiplexer for each timing signal. Software can select any one of the PFI pins as the external source for a given timing signal. It is important to note that any of the PFI pins can be used as an input by any of the timing signals and that multiple timing signals can use the same PFI simultaneously. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications.

You can also individually enable each of the PFI pins to output a *specific* internal timing signal. For example, if you need the UPDATE* signal as an output on the I/O connector, software can turn on the output driver for the PFI5/UPDATE* pin.

Device and RTSI Clocks

Many device functions require a frequency timebase to generate the necessary timing signals for controlling A/D conversions, DAC updates, or general-purpose signals at the I/O connector.

These devices can use either its internal 20 MHz timebase or a timebase received over the RTSI bus. In addition, if you configure the device to use the internal timebase, you can also program the device to drive its internal timebase over the RTSI bus to another device that is programmed to receive this timebase signal. This clock source, whether local or from the RTSI bus, is used directly by the device as the primary frequency source. The default configuration at startup is to use the internal timebase without driving the RTSI bus timebase signal. This timebase is software selectable.

♦ PXI-6035E

The RTSI clock connects to other devices through the PXI trigger bus on the PXI backplane. The RTSI clock signal uses the PXI trigger <7> line for this connection.

RTSI Triggers

The seven RTSI trigger lines on the RTSI bus provide a very flexible interconnection scheme for any device sharing the RTSI bus. These bidirectional lines can drive any of eight timing signals onto the RTSI bus and can receive any of these timing signals. This signal connection scheme is shown in Figure 3-3 for PCI devices and Figure 3-4 for PXI devices.

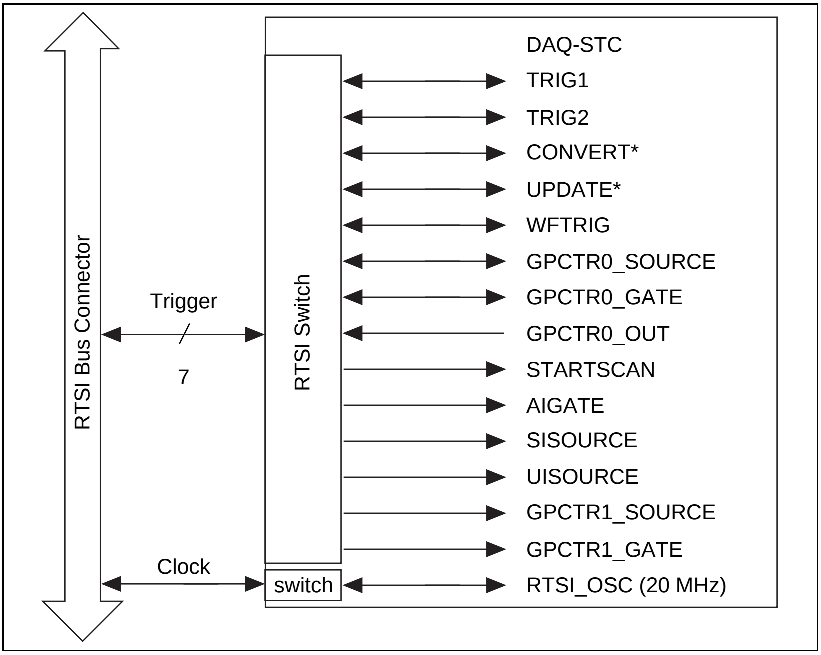


Figure 3-3. PCI RTSI Bus Signal Connection

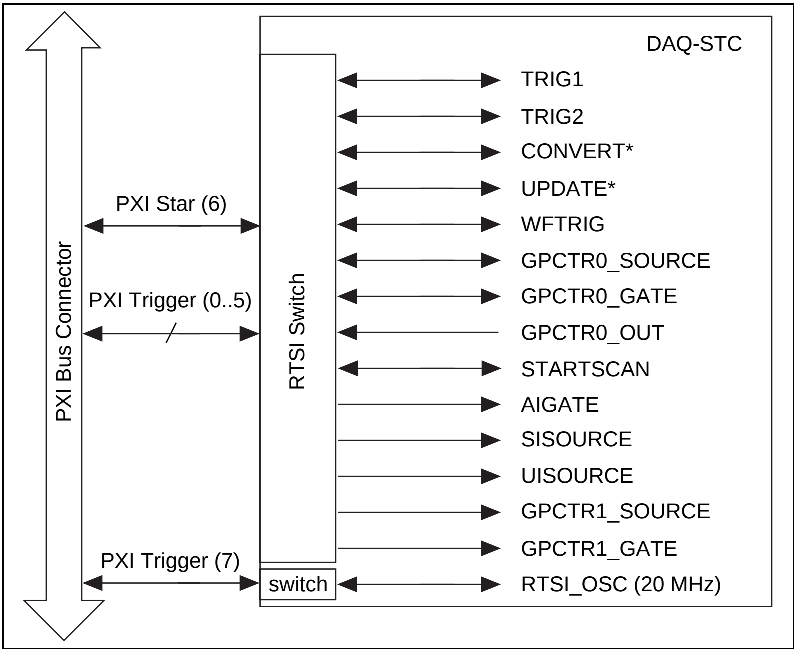


Figure 3-4. PXI RTSI Bus Signal Connection

Table 3-3 lists the name and number of pins used by the PXI-6035E.

Table 3-3. Pins Used by PXI E Series Device

PXI E Series Signal	PXI Pin Name	PXI J2 Pin Number
RTSI<0..5>	PXI Trigger<0..5>	B16, A16, A17, A18, B18, C18
RTSI 6	PXI Star	D17
RTSI Clock	PXI Trigger 7	E16
Reserved	LBL<0..3>	C20, E20, A19, C19
Reserved	LBR<0..12>	A21, C21, D21, E21, A20, B20, E15, A3, C3, D3, E3, A2, B2

Refer to the *Timing Connections* section of Chapter 4, *Signal Connections*, for a description of the signals shown in Figures 3-3 and 3-4.

4 Signal Connections

This chapter describes how to make input and output signal connections to your device via the I/O connector.

The I/O connector for the devices has 68 pins that you can connect to 68-pin accessories with the SH6868 shielded cable or the R6868 ribbon cable. You can connect your device to 50-pin signal accessories with the SH6850 shielded cable or R6850 ribbon cable.

Caution Connections that exceed any of the maximum ratings of input or output signals on the devices can damage the device and the computer. Maximum input ratings for each signal are given in the *Protection* column of Table 4-2. National Instruments is *not* liable for any damages resulting from such signal connections.

I/O Connector

Figure 4-1 shows the pin assignments for the 68-pin I/O connector. Refer to Appendix B, *Custom Cabling and Optional Connectors*, for pin assignments of the optional 50- and 68-pin connectors. A signal description follows the figures.

ACH8	34	68	ACH0
ACH1	33	67	AIGND
AIGND	32	66	ACH9
ACH10	31	65	ACH2
ACH3	30	64	AIGND
AIGND	29	63	ACH11
ACH4	28	62	AISENSE
AIGND	27	61	ACH12
ACH13	26	60	ACH5
ACH6	25	59	AIGND
AIGND	24	58	ACH14
ACH15	23	57	ACH7
DAC0OUT[1]	22	56	AIGND
DAC1OUT[1]	21	55	AOGND
RESERVED	20	54	AOGND
DIO4	19	53	DGND
DGND	18	52	DIO0
DIO1	17	51	DIO5
DIO6	16	50	DGND
DGND	15	49	DIO2
+5 V	14	48	DIO7
DGND	13	47	DIO3
DGND	12	46	SCANCLK
PFI0/TRIG1	11	45	EXTSTROBE*
PFI1/TRIG2	10	44	DGND
DGND	9	43	PFI2/CONVERT*
+5 V	8	42	PFI3/GPCTR1_SOURCE
DGND	7	41	PFI4/GPCTR1_GATE
PFI5/UPDATE*	6	40	GPCTR1_OUT
PFI6/WFTRIG	5	39	DGND
DGND	4	38	PFI7/STARTSCAN
PFI9/GPCTR0_GATE	3	37	PFI8/GPCTR0_SOURCE
GPCTR0_OUT	2	36	DGND
FREQ_OUT	1	35	DGND

[1] Not available on the 6034E

Figure 4-1. I/O Connector Pin Assignment for the 6034E/6035E

Table 4-1 shows the I/O connector signal descriptions for the 6034E and 6035E.

Table 4-1. I/O Connector Signal Descriptions

Signal Name	Reference	Direction	Description
AIGND	—	—	Analog Input Ground—These pins are the reference point for single-ended measurements in RSE configuration and the bias current return point for differential measurements. All three ground references—AIGND, AOGND, and DGND—are connected together on your device.
ACH<0..15>	AIGND	Input	Analog Input Channels 0 through 15—Each channel pair, ACH<*i*, *i*+8> (*i* = 0..7), can be configured as either one differential input or two single-ended inputs.
AISENSE	AIGND	Input	Analog Input Sense—This pin serves as the reference node for any of channels ACH <0..15> in NRSE configuration.
DAC0OUT[1]	AOGND	Output	Analog Channel 0 Output—This pin supplies the voltage output of analog output channel 0.
DAC1OUT[1]	AOGND	Output	Analog Channel 1 Output—This pin supplies the voltage output of analog output channel 1.
AOGND	—	—	Analog Output Ground—The analog output voltages are referenced to this node. All three ground references—AIGND, AOGND, and DGND—are connected together on your device.
DGND	—	—	Digital Ground—This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply. All three ground references—AIGND, AOGND, and DGND—are connected together on your device.
DIO<0..7>	DGND	Input or Output	Digital I/O signals—DIO6 and 7 can control the up/down signal of general-purpose counters 0 and 1, respectively.
+5 V	DGND	Output	+5 VDC Source—These pins are fused for up to 1 A of +5 V supply. The fuse is self-resetting.
SCANCLK	DGND	Output	Scan Clock—This pin pulses once for each A/D conversion in scanning mode when enabled. The low-to-high edge indicates when the input signal can be removed from the input or switched to another signal.
EXTSTROBE*	DGND	Output	External Strobe—This output can be toggled under software control to latch signals or trigger events on external devices.

Table 4-1. I/O Connector Signal Descriptions (Continued)

Signal Name	Reference	Direction	Description
PFI0/TRIG1	DGND	Input	PFI0/Trigger 1—As an input, this is one of the Programmable Function Inputs (PFIs). PFI signals are explained in the *Timing Connections* section later in this chapter.
		Output	As an output, this is the TRIG1 (AI Start Trigger) signal. In posttrigger data acquisition sequences, a low-to-high transition indicates the initiation of the acquisition sequence. In pretrigger applications, a low-to-high transition indicates the initiation of the pretrigger conversions.
PFI1/TRIG2	DGND	Input	PFI1/Trigger 2—As an input, this is one of the PFIs.
		Output	As an output, this is the TRIG2 (AI Stop Trigger) signal. In pretrigger applications, a low-to-high transition indicates the initiation of the posttrigger conversions. TRIG2 is not used in posttrigger applications.
PFI2/CONVERT*	DGND	Input	PFI2/Convert—As an input, this is one of the PFIs.
		Output	As an output, this is the CONVERT* (AI Convert) signal. A high-to-low edge on CONVERT* indicates that an A/D conversion is occurring.
PFI3/GPCTR1_SOURCE	DGND	Input	PFI3/Counter 1 Source—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR1_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 1.
PFI4/GPCTR1_GATE	DGND	Input	PFI4/Counter 1 Gate—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR1_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 1.
GPCTR1_OUT	DGND	Output	Counter 1 Output—This output is from the general-purpose counter 1 output.
PFI5/UPDATE*	DGND	Input	PFI5/Update—As an input, this is one of the PFIs.
		Output	As an output, this is the UPDATE* (AO Update) signal. A high-to-low edge on UPDATE* indicates that the analog output primary group is being updated for the 6035E.

Table 4-1. I/O Connector Signal Descriptions (Continued)

Signal Name	Reference	Direction	Description
PFI6/WFTRIG	DGND	Input Output	PFI6/Waveform Trigger—As an input, this is one of the PFIs. As an output, this is the WFTRIG (AO Start Trigger) signal. In timed analog output sequences, a low-to-high transition indicates the initiation of the waveform generation.
PFI7/STARTSCAN	DGND	Input Output	PFI7/Start of Scan—As an input, this is one of the PFIs. As an output, this is the STARTSCAN (AI Scan Start) signal. This pin pulses once at the start of each analog input scan in the interval scan. A low-to-high transition indicates the start of the scan.
PFI8/GPCTR0_SOURCE	DGND	Input Output	PFI8/Counter 0 Source—As an input, this is one of the PFIs. As an output, this is the GPCTR0_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 0.
PFI9/GPCTR0_GATE	DGND	Input Output	PFI9/Counter 0 Gate—As an input, this is one of the PFIs. As an output, this is the GPCTR0_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 0.
GPCTR0_OUT	DGND	Output	Counter 0 Output—This output is from the general-purpose counter 0 output.
FREQ_OUT	DGND	Output	Frequency Output—This output is from the frequency generator output.

* Indicates that the signal is active low

[1] Not available on the 6034E

Table 4-2 shows the I/O signal summary for the 6034E and 6035E.

Table 4-2. I/O Signal Summary

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..15>	AI	100 GΩ in parallel with 100 pF	25/15	—	—	—	±200 pA
AISENSE	AI	100 GΩ in parallel with 100 pF	25/15	—	—	—	±200 pA
AIGND	AO	—	—	—	—	—	—
DAC0OUT (6035E only)	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	10 V/µs	—
DAC1OUT (6035E only)	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	10 V/µs	—
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
VCC	DO	0.1 Ω	Short-circuit to ground	1A fused	—	—	—
DIO<0..7>	DIO	—	V_{CC} +0.5	13 at (V_{CC} –0.4)	24 at 0.4	1.1	50 kΩ pu
SCANCLK	DO	—	—	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI1/TRIG2	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu

Table 4-2. I/O Signal Summary (Continued)

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
PFI8/GPCTR0_SOURCE	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{CC}–0.4)	5 at 0.4	1.5	50 kΩ pu

AI = Analog Input DIO = Digital Input/Output pu = pullup
AO = Analog Output DO = Digital Output

Note: The tolerance on the 50 kΩ pullup and pulldown resistors is very large. Actual value may range between 17 kΩ and 100 kΩ.

Analog Input Signal Overview

The analog input signals for these devices are ACH<0..15>, ASENSE, and AIGND. Connection of these analog input signals to your device depends on the type of input signal source and the configuration of the analog input channels you are using. This section provides an overview of the different types of signal sources and analog input configuration modes. More specific signal connection information is provided in the *Analog Input Signal Connections* section.

Types of Signal Sources

When configuring the input channels and making signal connections, you must first determine whether the signal sources are floating or ground-referenced.

Floating Signal Sources

A floating signal source is not connected in any way to the building ground system but, rather, has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolators, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source. You must tie the ground reference of a floating signal to your device analog input ground to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats out of the common-mode input range.

Ground-Referenced Signal Sources

A ground-referenced signal source is connected in some way to the building system ground and is, therefore, already connected to a common ground point with respect to the device, assuming that the computer is plugged into the same power system. Nonisolated outputs of instruments and devices that plug into the building power system fall into this category.

The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV but can be much higher if power distribution circuits are not properly connected. If a grounded signal source is improperly measured, this difference may appear as an error in the measurement. The connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

Analog Input Modes

You can configure your device for one of three input modes: nonreferenced single ended (NRSE), referenced single ended (RSE), and differential (DIFF). With the different configurations, you can use the PGIA in different ways. Figure 4-2 shows a diagram of your device PGIA.

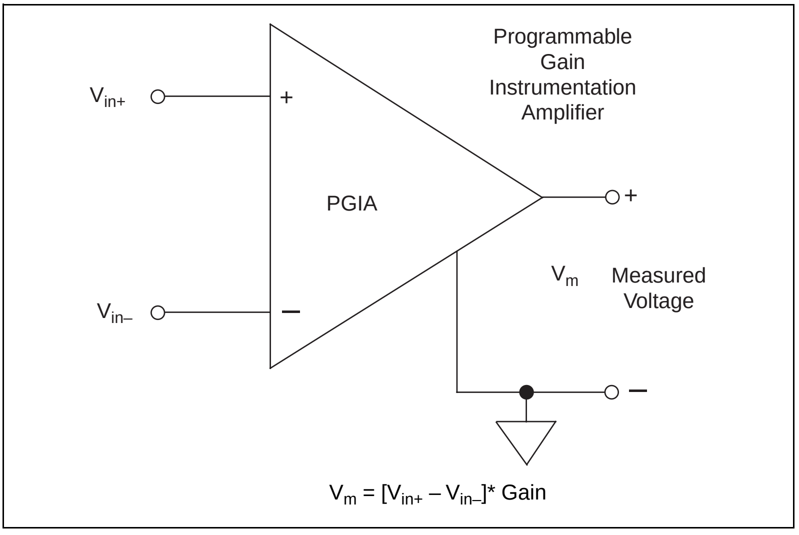


Figure 4-2. Programmable Gain Instrumentation Amplifier (PGIA)

In single-ended mode (RSE and NRSE), signals connected to ACH<0..15> are routed to the positive input of the PGIA. In differential mode, signals connected to ACH<0..7> are routed to the positive input of the PGIA, and signals connected to ACH<8..15> are routed to the negative input of the PGIA.

Caution Exceeding the differential and common-mode input ranges distorts your input signals. Exceeding the maximum input voltage rating can damage the device and the computer. National Instruments is *not* liable for any damages resulting from such signal connections. The maximum input voltage ratings are listed in the *Protection* column of Table 4-2.

In NRSE mode, the AISENSE signal is connected internally to the negative input of the PGIA when their corresponding channels are selected. In DIFF and RSE modes, AISENSE is left unconnected.

AIGND is an analog input common signal that is routed directly to the ground tie point on the devices. You can use this signal for a general analog ground tie point to your device if necessary.

The PGIA applies gain and common-mode voltage rejection and presents high input impedance to the analog input signals connected to your device. Signals are routed to the positive and negative inputs of the PGIA through input multiplexers on the device. The PGIA converts two input signals to a signal that is the difference between the two input signals multiplied by the gain setting of the amplifier. The amplifier output voltage is referenced to the ground for the device. Your device A/D converter (ADC) measures this output voltage when it performs A/D conversions.

You must reference all signals to ground either at the source device or at the device. If you have a floating source, you should reference the signal to ground by using the RSE input mode or the DIFF input configuration with bias resistors, see the *Differential Connections for Nonreferenced or Floating Signal Sources* section in this chapter. If you have a grounded source, you should not reference the signal to AIGND. You can avoid this reference by using DIFF or NRSE input configurations.

Analog Input Signal Connections

The following sections discuss the use of single-ended and differential measurements and recommendations for measuring both floating and ground-referenced signal sources.

Figure 4-3 summarizes the recommended input configuration for both types of signal sources.

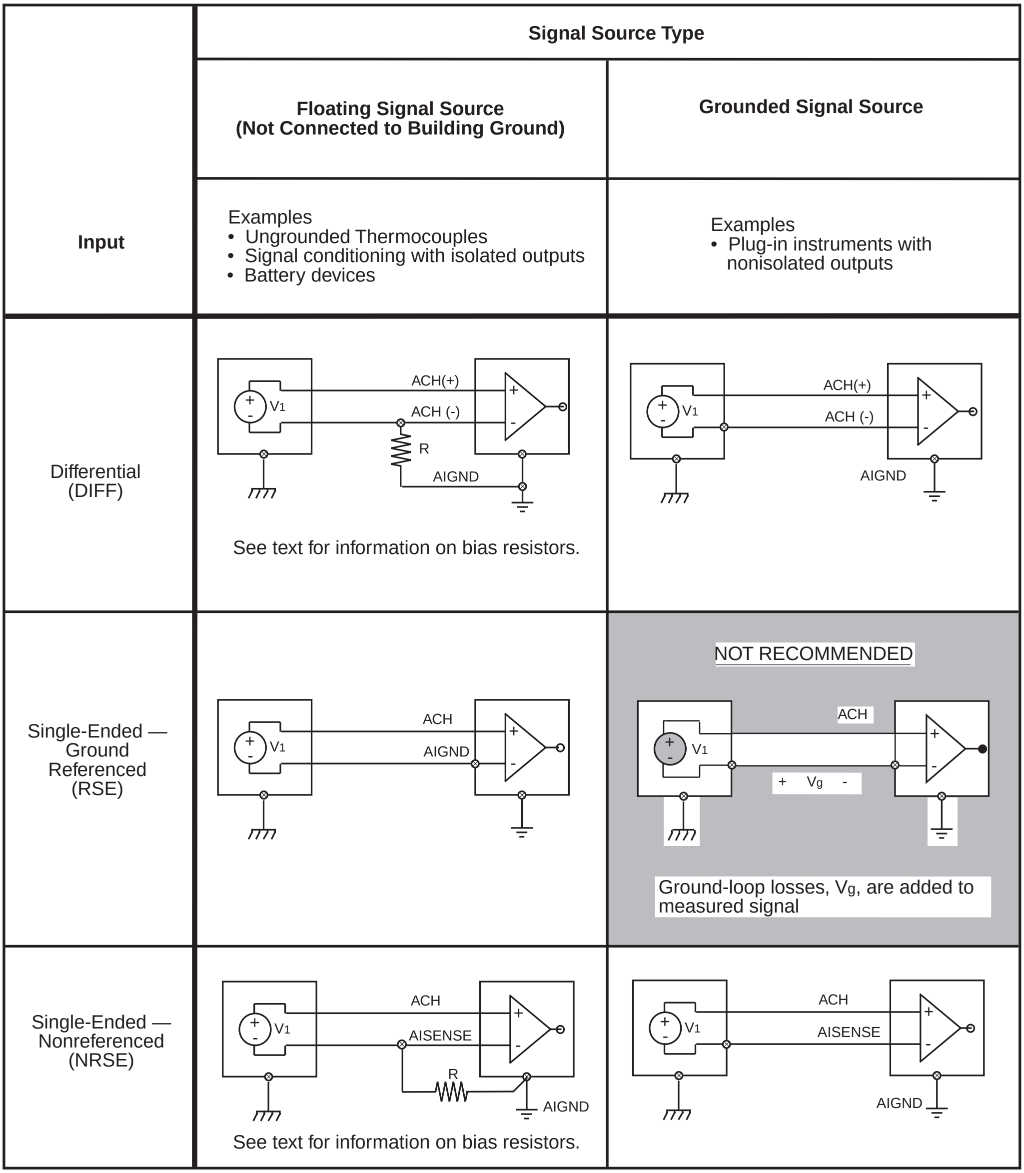


Figure 4-3. Summary of Analog Input Connections

Differential Connection Considerations (DIFF Input Configuration)

A differential connection is one in which the analog input signal has its own reference signal or signal return path. These connections are available when the selected channel is configured in DIFF input mode. The input signal is tied to the positive input of the PGIA, and its reference signal, or return, is tied to the negative input of the PGIA.

When you configure a channel for differential input, each signal uses two multiplexer inputs—one for the signal and one for its reference signal. Therefore, with a differential configuration for every channel, up to eight analog input channels are available.

You should use differential input connections for any channel that meets any of the following conditions:

- The input signal is low level (less than 1 V).
- The leads connecting the signal to the device are greater than 10 ft (3 m).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce picked up noise and increase common-mode noise rejection. Differential signal connections also allow input signals to float within the common-mode limits of the PGIA.

Differential Connections for Ground-Referenced Signal Sources

Figure 4-4 shows how to connect a ground-referenced signal source to a channel on the device configured in DIFF input mode.

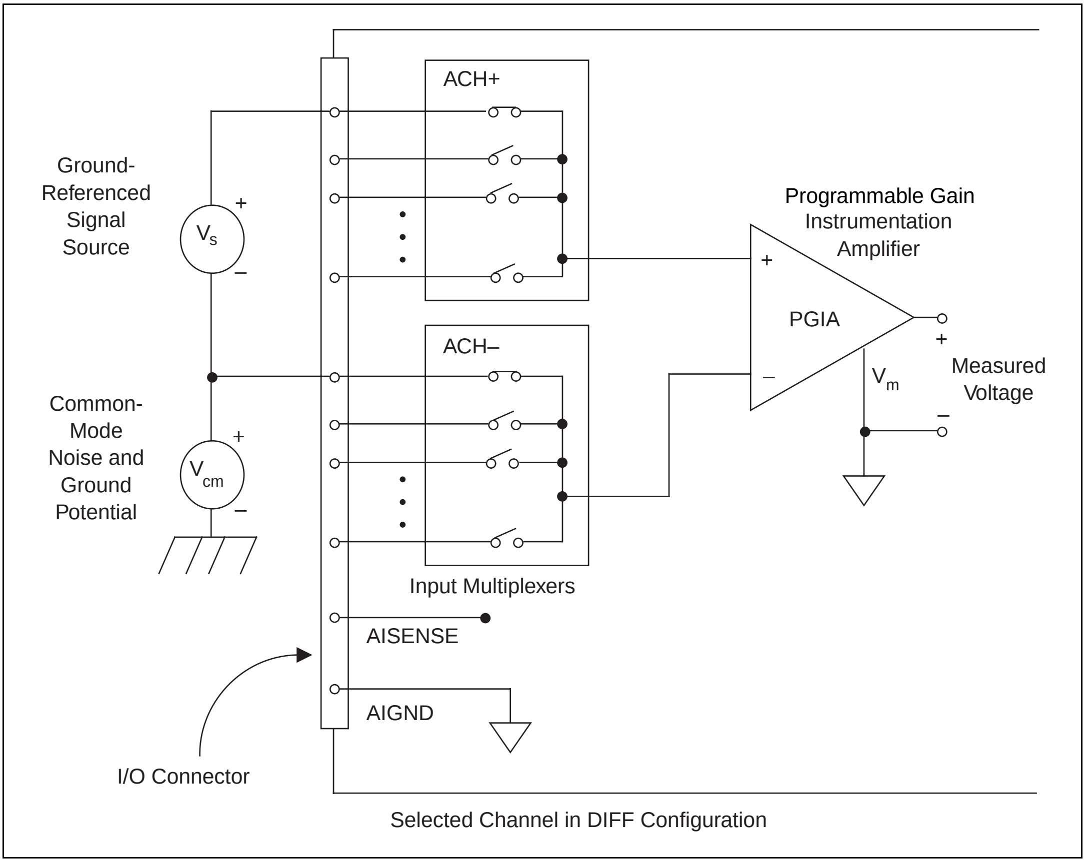


Figure 4-4. Differential Input Connections for Ground-Referenced Signals

With this type of connection, the PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the device ground, shown as V_{cm} in Figure 4-4.

Differential Connections for Nonreferenced or Floating Signal Sources

Figure 4-5 shows how to connect a floating signal source to a channel configured in DIFF input mode.

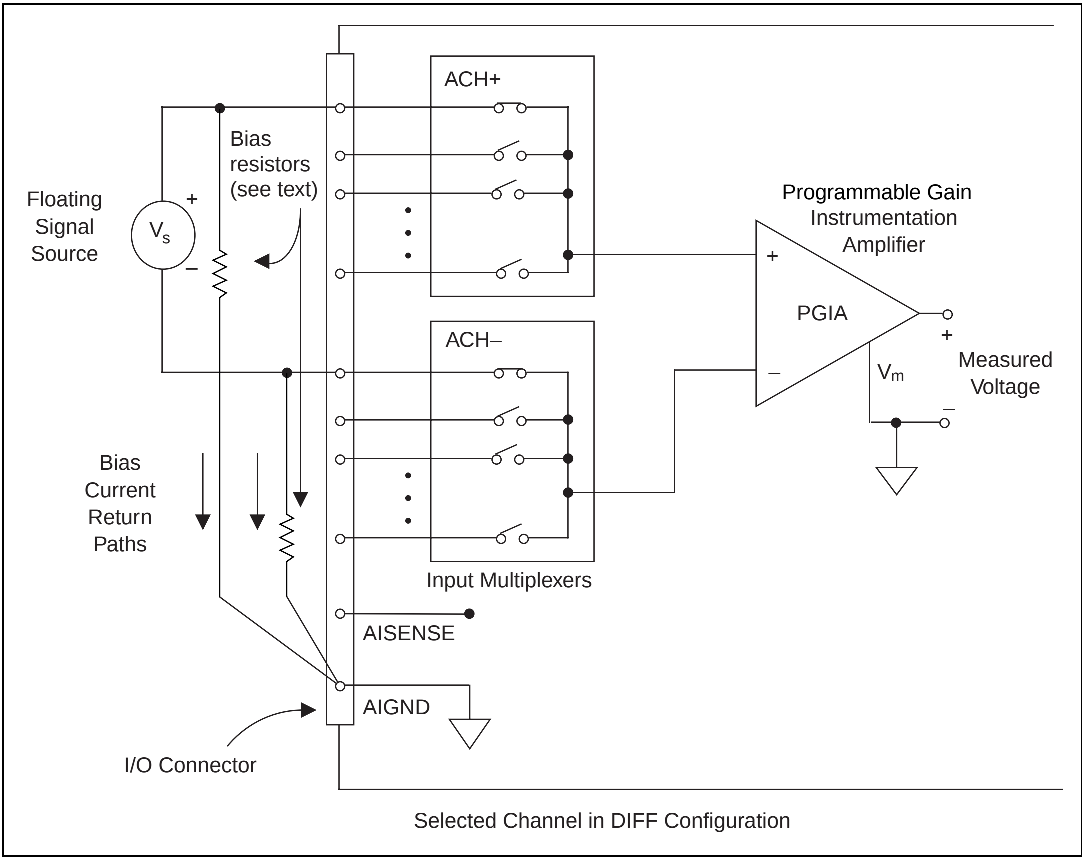


Figure 4-5. Differential Input Connections for Nonreferenced Signals

Figure 4-5 shows two bias resistors connected in parallel with the signal leads of a floating signal source. If you do not use the resistors and the source is truly floating, the source is not likely to remain within the common-mode signal range of the PGIA. The PGIA will then saturate, causing erroneous readings.

You must reference the source to AIGND. The easiest way is to connect the positive side of the signal to the positive input of the PGIA and connect the negative side of the signal to AIGND as well as to the negative input of the PGIA, without any resistors at all. This connection works well for DC-coupled sources with low source impedance (less than 100 Ω).

However, for larger source impedances, this connection leaves the differential signal path significantly out of balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line because it is connected to ground. Hence, this noise appears as a differential-mode signal instead of a common-mode signal, and the PGIA does not reject it. In this case, instead of directly connecting the negative line to AIGND, connect it to AIGND through a resistor that is about 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance, so that about the same amount of noise couples onto both connections, yielding better rejection of electrostatically coupled noise. Also, this configuration does not load down the source (other than the very high input impedance of the PGIA).

You can fully balance the signal path by connecting another resistor of the same value between the positive input and AIGND, as shown in Figure 4-5. This fully balanced configuration offers slightly better noise rejection but has the disadvantage of loading the source down with the series combination (sum) of the two resistors. If, for example, the source impedance is 2 kΩ and each of the two resistors is 100 kΩ, the resistors load down the source with 200 kΩ and produce a –1% gain error.

Both inputs of the PGIA require a DC path to ground in order for the PGIA to work. If the source is AC coupled (capacitively coupled), the PGIA needs a resistor between the positive input and AIGND. If the source has low impedance, choose a resistor that is large enough not to significantly load the source but small enough not to produce significant input offset voltage as a result of input bias current (typically 100 kΩ to 1 MΩ). In this case, you can tie the negative input directly to AIGND. If the source has high output impedance, you should balance the signal path as previously described using the same value resistor on both the positive and negative inputs; you should be aware that there is some gain error from loading down the source.

Single-Ended Connection Considerations

A single-ended connection is one in which the device analog input signal is referenced to a ground that can be shared with other input signals. The input signal is tied to the positive input of the PGIA, and the ground is tied to the negative input of the PGIA.

When every channel is configured for single-ended input, up to 16 analog input channels are available.

You can use single-ended input connections for any input signal that meets the following conditions:

- The input signal is high level (greater than 1 V).
- The leads connecting the signal to the device are less than 10 ft (3 m).
- The input signal can share a common reference point with other signals.

DIFF input connections are recommended for greater signal integrity for any input signal that does not meet the preceding conditions.

Using your software, you can configure the channels for two different types of single-ended connections—RSE configuration and NRSE configuration. The RSE configuration is used for floating signal sources; in this case, the device provides the reference ground point for the external signal. The NRSE input configuration is used for ground-referenced signal sources; in this case, the external signal supplies its own reference ground point and the device should not supply one.

In single-ended configurations, more electrostatic and magnetic noise couples into the signal connections than in differential configurations. The coupling is the result of differences in the signal path. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two conductors.

Single-Ended Connections for Floating Signal Sources (RSE Configuration)

Figure 4-6 shows how to connect a floating signal source to a channel configured for RSE mode.

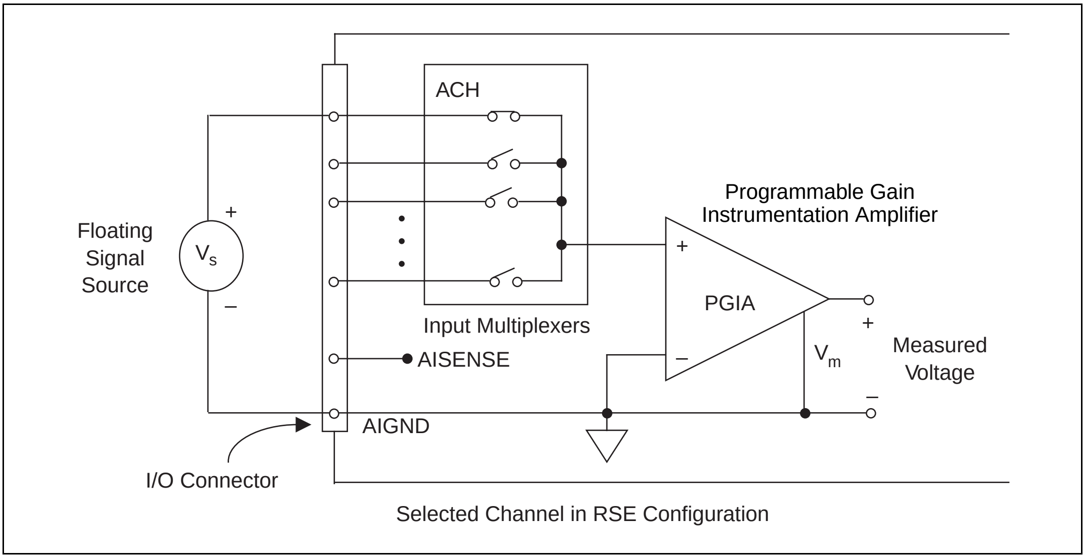


Figure 4-6. Single-Ended Input Connections for Nonreferenced or Floating Signals

Single-Ended Connections for Grounded Signal Sources (NRSE Configuration)

To measure a grounded signal source with a single-ended configuration, you must configure your device in the NRSE input configuration. The signal is then connected to the positive input of the PGIA, and the signal local ground reference is connected to the negative input of the PGIA. The ground point of the signal should, therefore, be connected to the AISENSE pin. Any potential difference between the device ground and the signal ground appears as a common-mode signal at both the positive and negative inputs of the PGIA, and this difference is rejected by the amplifier. If the input circuitry of a device were referenced to ground, in this situation as in the RSE input configuration, this difference in ground potentials would appear as an error in the measured voltage.

Figure 4-7 shows how to connect a grounded signal source to a channel configured for NRSE mode.

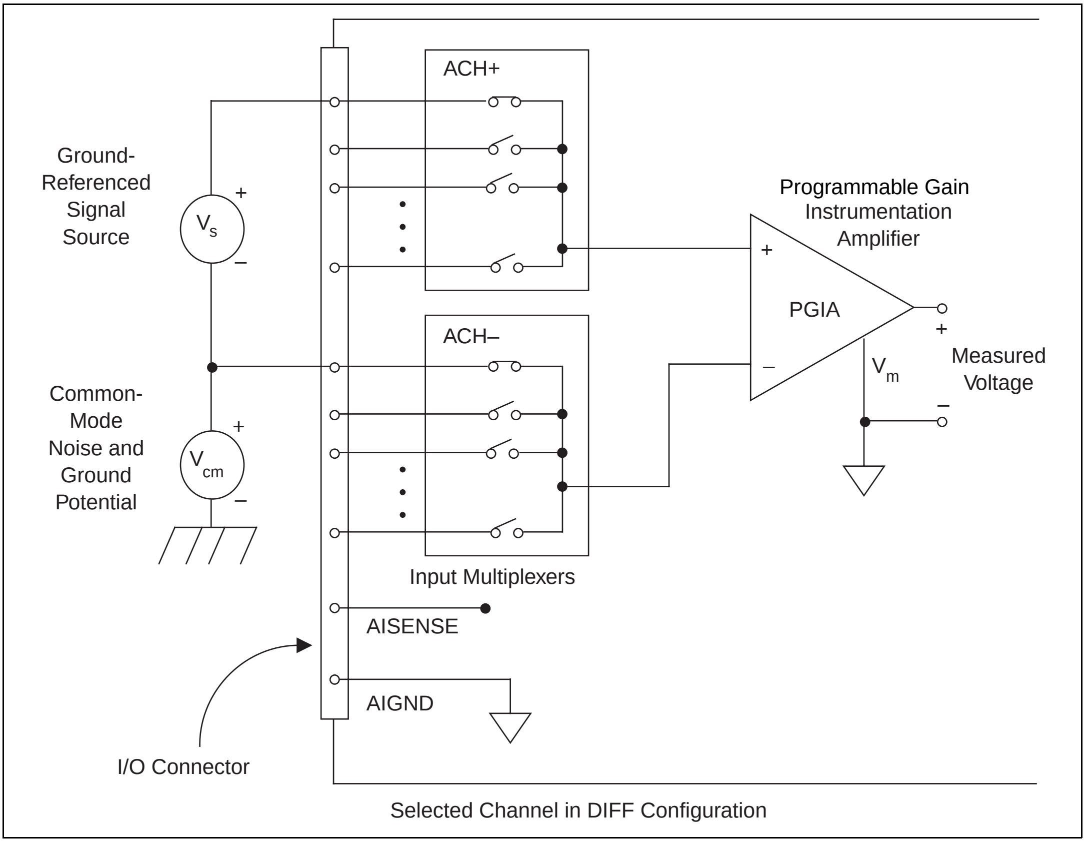


Figure 4-7. Single-Ended Input Connections for Ground-Referenced Signals

Common-Mode Signal Rejection Considerations

Figures 4-4 and 4-7 show connections for signal sources that are already referenced to some ground point with respect to the device. In these cases, the PGIA can reject any voltage caused by ground potential differences between the signal source and the device. In addition, with differential input connections, the PGIA can reject common-mode noise pickup in the leads connecting the signal sources to the device. The PGIA can reject common-mode signals as long as $V+_{in}$ and $V-_{in}$ (input signals) are both within ±11 V of AIGND.

Analog Output Signal Connections

- ♦ 6035E

The analog output signals are DAC0OUT, DAC1OUT, and AOGND. DAC0OUT and DAC1OUT are not available on the 6034E.

DAC0OUT is the voltage output signal for analog output channel 0. DAC1OUT is the voltage output signal for analog output channel 1.

AOGND is the ground reference signal for both analog output channels and the external reference signal.

Figure 4-8 shows how to make analog output connections to your device.

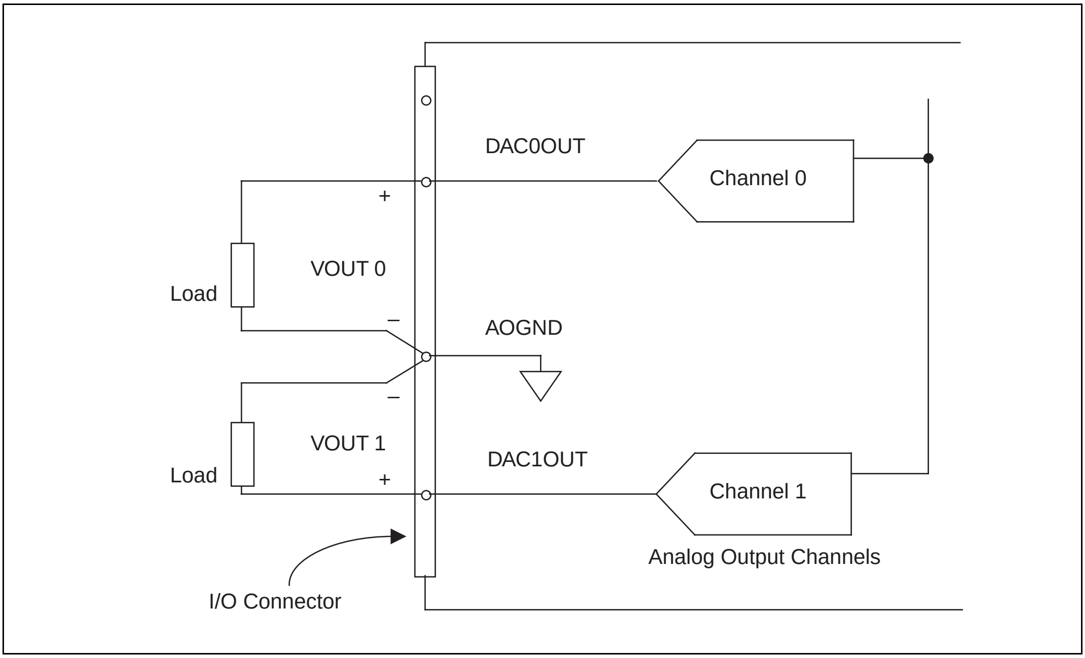


Figure 4-8. Analog Output Connections

Digital I/O Signal Connections

The 6034E and 6035E both have digital I/O signals DIO<0..7> and DGND. DIO<0..7> are the signals making up the DIO port, and DGND is the ground reference signal for the DIO port. You can program all lines individually to be inputs or outputs. Figure 4-9 shows signal connections for three typical digital I/O applications.

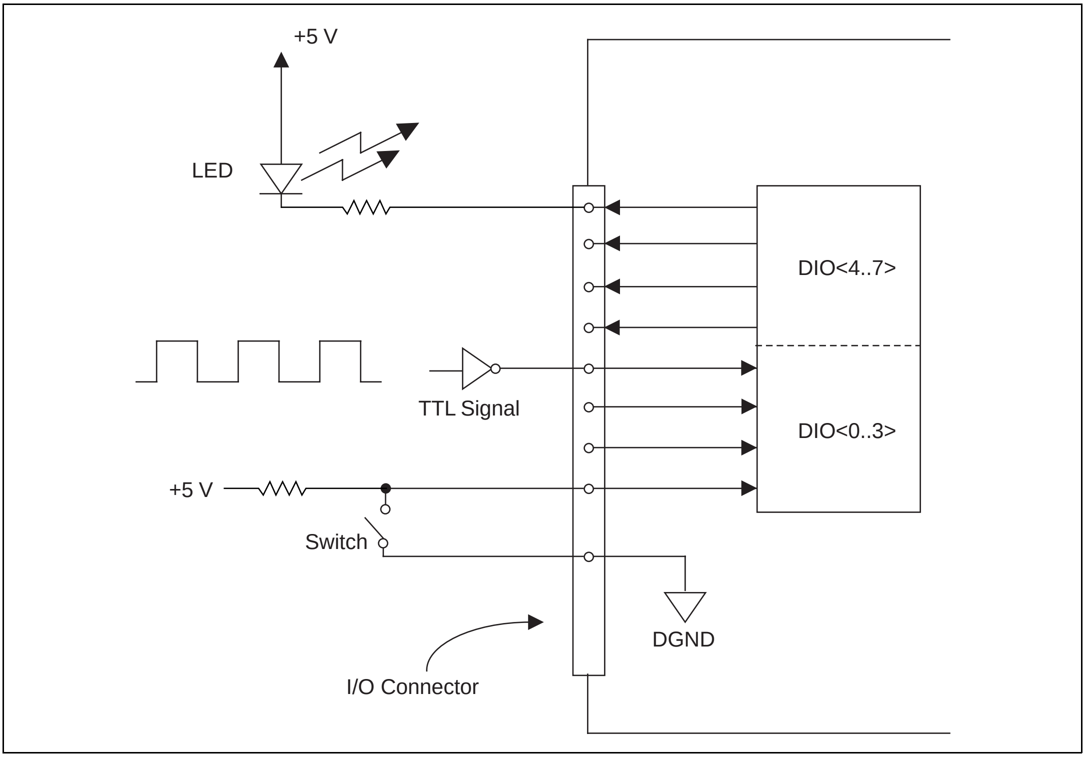


Figure 4-9. Digital I/O Connections

Figure 4-9 shows DIO<0..3> configured for digital input and DIO<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states such as the state of the switch shown in the figure. Digital output applications include sending TTL signals and driving external devices such as the LED shown in the figure.

Power Connections

Two pins on the I/O connector supply +5 V from the computer power supply via a self-resetting fuse. The fuse will reset automatically within a few seconds after the overcurrent condition is removed. These pins are referenced to DGND and can be used to power external digital circuitry. The power rating is +4.65 to +5.25 VDC at 1 A.

Caution Under no circumstances should you connect these +5 V power pins directly to analog or digital ground or to any other voltage source on the device or any other device. Doing so can damage the device and the computer. National Instruments is *not* liable for damages resulting from such a connection.

Timing Connections

Caution Exceeding the maximum input voltage ratings, which are listed in Table 4-2, can damage the device and the computer. National Instruments is *not* liable for any damages resulting from such signal connections.

All external control over the timing of your device is routed through the 10 programmable function inputs labeled PFI<0..9>. These signals are explained in detail in the section, *Programmable Function Input Connections*. These PFIs are bidirectional; as outputs they are not programmable and reflect the state of many DAQ, waveform generation, and general-purpose timing signals. There are five other dedicated outputs for the remainder of the timing signals. As inputs, the PFI signals are programmable and can control any DAQ, waveform generation, and general-purpose timing signals.

The DAQ signals are explained in the *DAQ Timing Connections* section later in this chapter. The waveform generation signals are explained in the *Waveform Generation Timing Connections* section later in this chapter. The general-purpose timing signals are explained in the *General-Purpose Timing Signal Connections* section in this chapter.

All digital timing connections are referenced to DGND. This reference is demonstrated in Figure 4-10, which shows how to connect an external TRIG1 source and an external CONVERT* source to two PFI pins.

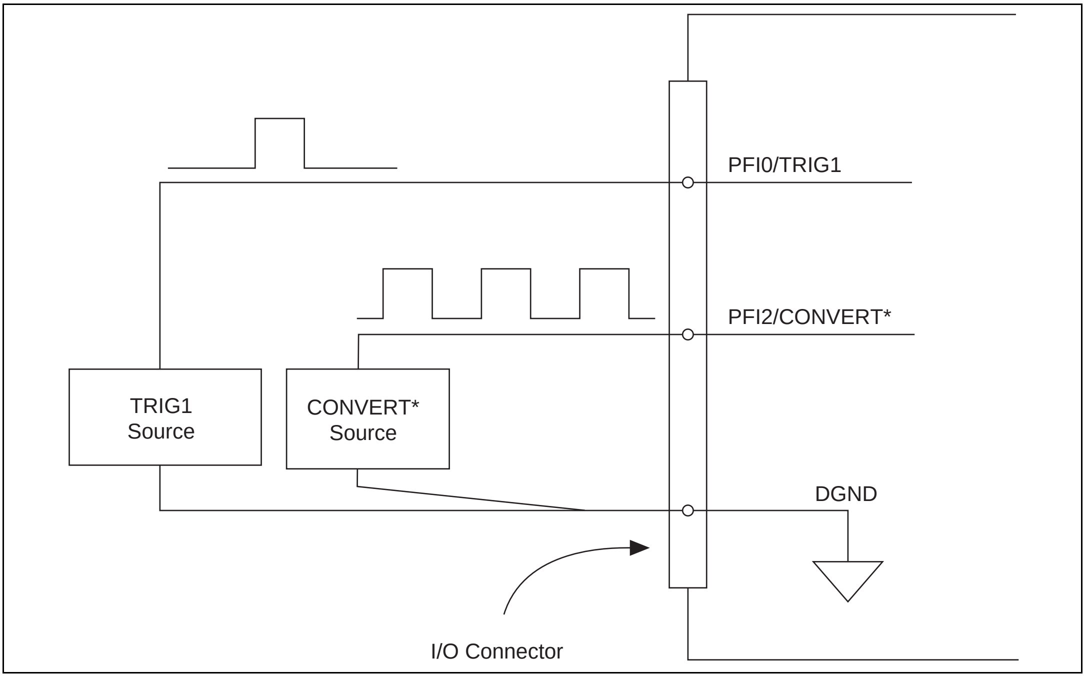


Figure 4-10. Timing I/O Connections

Programmable Function Input Connections

There are a total of 13 internal timing signals that you can externally control from the PFI pins. The source for each of these signals is software-selectable from any of the PFIs when you want external control. This flexible routing scheme reduces the need to change the physical wiring to the device I/O connector for different applications requiring alternative wiring.

You can individually enable each of the PFI pins to output a specific internal timing signal. For example, if you need the CONVERT* signal as an output on the I/O connector, software can turn on the output driver for the PFI2/CONVERT* pin. Be careful not to drive a PFI signal externally when it is configured as an output.

As an input, you can individually configure each PFI pin for edge or level detection and for polarity selection, as well. You can use the polarity selection for any of the 13 timing signals, but the edge or level detection will depend upon the particular timing signal being controlled. The detection requirements for each timing signal are listed within the section that discusses that individual signal.

In edge-detection mode, the minimum pulse width required is 10 ns. This applies for both rising-edge and falling-edge polarity settings. There is no maximum pulse-width requirement in edge-detect mode.

In level-detection mode, there are no minimum or maximum pulse-width requirements imposed by the PFIs themselves, but there may be limits imposed by the particular timing signal being controlled. These requirements are listed later in this chapter.

DAQ Timing Connections

The DAQ timing signals are SCANCLK, EXTSTROBE*, TRIG1, TRIG2, STARTSCAN, CONVERT*, AIGATE, and SISOURCE. Posttriggered data acquisition allows you to view only data that is acquired after a trigger event is received. A typical posttriggered DAQ sequence is shown in Figure 4-11. Pretriggered data acquisition allows you to view data that is acquired before the trigger of interest in addition to data acquired after the trigger. Figure 4-12 shows a typical pretriggered DAQ sequence. The description for each signal shown in these figures is included later in this chapter.

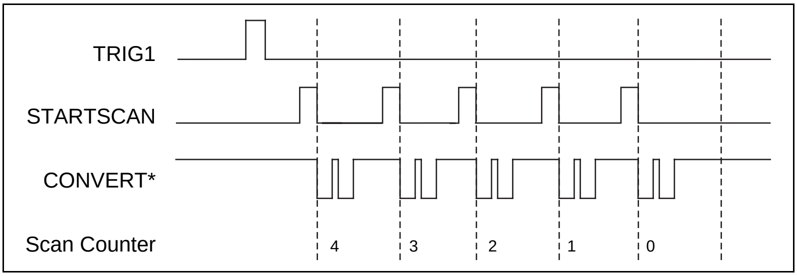


Figure 4-11. Typical Posttriggered Acquisition

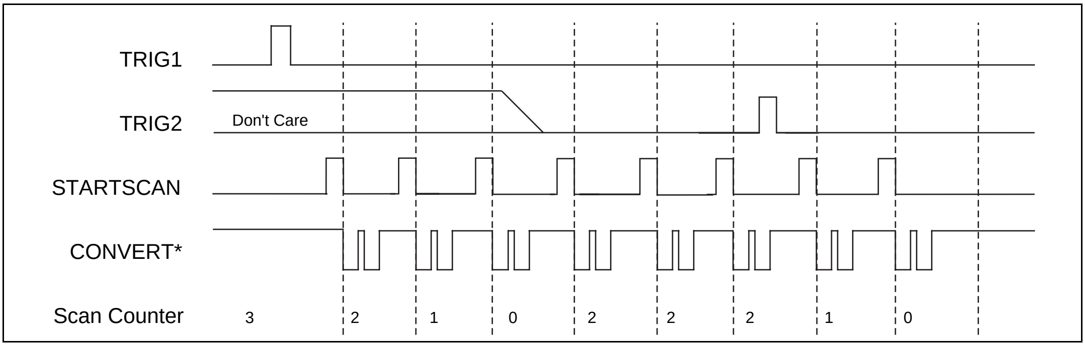


Figure 4-12. Typical Pretriggered Acquisition

SCANCLK Signal

SCANCLK is an output-only signal that generates a pulse with the leading edge occurring approximately 50 to 100 ns after an A/D conversion begins. The polarity of this output is software-selectable but is typically configured so that a low-to-high leading edge can clock external analog input multiplexers indicating when the input signal has been sampled and can be removed. This signal has a 400 to 500 ns pulse width and is software-enabled. Figure 4-13 shows the timing for the SCANCLK signal.

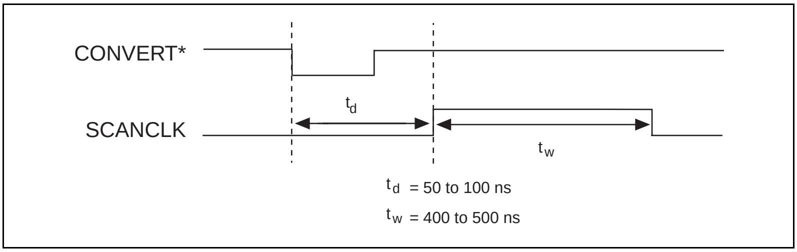


Figure 4-13. SCANCLK Signal Timing

EXTSTROBE* Signal

EXTSTROBE* is an output-only signal that generates either a single pulse or a sequence of eight pulses in the hardware-strobe mode. An external device can use this signal to latch signals or to trigger events. In the single-pulse mode, software controls the level of the EXTSTROBE* signal. A 10 µs and a 1.2 µs clock are available for generating a sequence of eight pulses in the hardware-strobe mode. Figure 4-14 shows the timing for the hardware-strobe mode EXTSTROBE* signal.

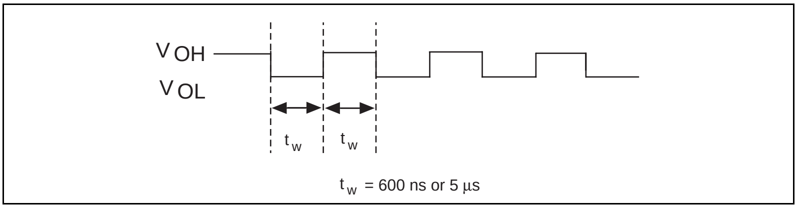


Figure 4-14. EXTSTROBE* Signal Timing

TRIG1 Signal

Any PFI pin can externally input the TRIG1 signal, which is available as an output on the PFI0/TRIG1 pin. Refer to Figures 4-11 and 4-12 for the relationship of TRIG1 to the DAQ sequence.

As an input, the TRIG1 signal is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG1 and configure the polarity selection for either rising or falling edge. The selected edge of the TRIG1 signal starts the data acquisition sequence for both posttriggered and pretriggered acquisitions.

As an output, the TRIG1 signal reflects the action that initiates a DAQ sequence. This is true even if the acquisition is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-15 and 4-16 show the input and output timing requirements for the TRIG1 signal.

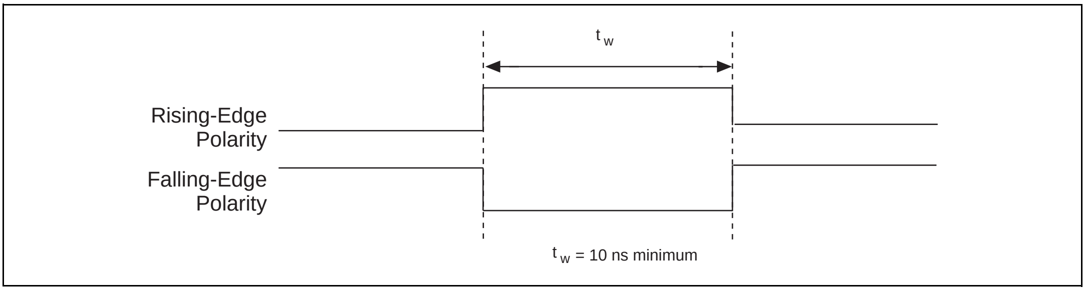


Figure 4-15. TRIG1 Input Signal Timing

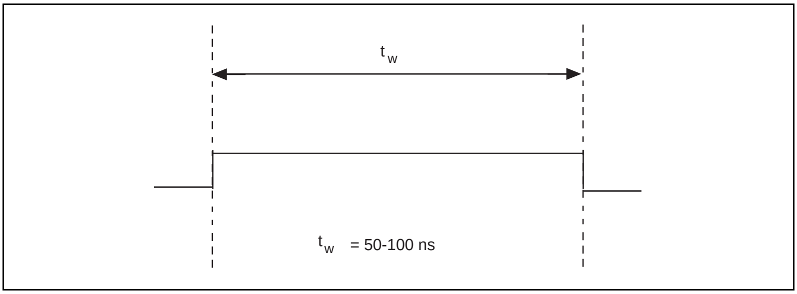


Figure 4-16. TRIG1 Output Signal Timing

The device also uses the TRIG1 signal to initiate pretriggered DAQ operations. In most pretriggered applications, the TRIG1 signal is generated by a software trigger. Refer to the TRIG2 signal description for a complete description of the use of TRIG1 and TRIG2 in a pretriggered DAQ operation.

TRIG2 Signal

Any PFI pin can externally input the TRIG2 signal, which is available as an output on the PFI1/TRIG2 pin. Refer to Figure 4-12 for the relationship of TRIG2 to the DAQ sequence.

As an input, the TRIG2 signal is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG2 and configure the polarity selection for either rising or falling edge. The selected edge of the TRIG2 signal initiates the posttriggered phase of a pretriggered acquisition sequence. In pretriggered mode, the TRIG1 signal initiates the data acquisition. The scan counter indicates the minimum number of scans before TRIG2 can be recognized. After the scan counter decrements to zero, it is loaded with the number of posttrigger scans to acquire while the acquisition continues. The device ignores the TRIG2 signal if it is asserted prior to the scan counter decrementing to zero. After the selected edge of TRIG2 is received, the device will acquire a fixed number of scans and the acquisition will stop. This mode acquires data both before and after receiving TRIG2.

As an output, the TRIG2 signal reflects the posttrigger in a pretriggered acquisition sequence. This is true even if the acquisition is being externally triggered by another PFI. The TRIG2 signal is not used in posttriggered data acquisition. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-17 and 4-18 show the input and output timing requirements for the TRIG2 signal.

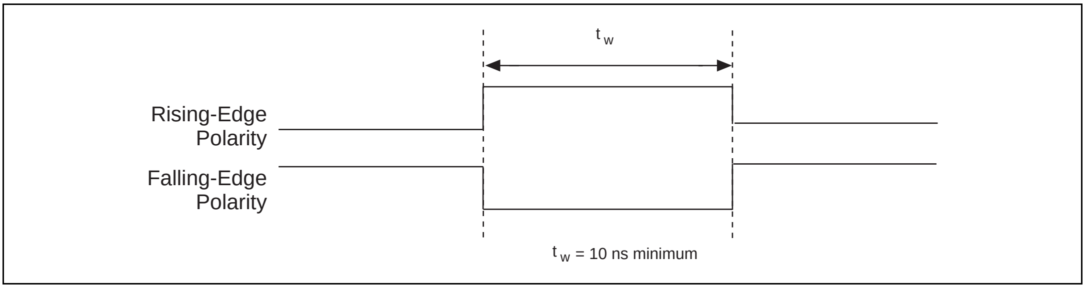


Figure 4-17. TRIG2 Input Signal Timing

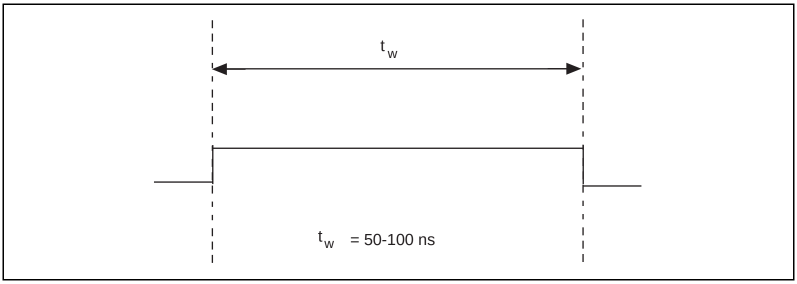


Figure 4-18. TRIG2 Output Signal Timing

STARTSCAN Signal

Any PFI pin can externally input the STARTSCAN signal, which is available as an output on the PFI7/STARTSCAN pin. Refer to Figures 4-11 and 4-12 for the relationship of STARTSCAN to the DAQ sequence.

As an input, the STARTSCAN signal is configured in the edge-detection mode. You can select any PFI pin as the source for STARTSCAN and configure the polarity selection for either rising or falling edge. The selected edge of the STARTSCAN signal initiates a scan. The sample interval counter starts if you select internally triggered CONVERT*.

As an output, the STARTSCAN signal reflects the actual start pulse that initiates a scan. This is true even if the starts are being externally triggered by another PFI. You have two output options. The first is an active high pulse with a pulse width of 50 to 100 ns, which indicates the start of the scan. The second action is an active high pulse that terminates at the start of the last conversion in the scan, which indicates a scan in progress. STARTSCAN will be deasserted t_{off} after the last conversion in the scan is initiated. This output is set to tri-state at startup.

Figures 4-19 and 4-20 show the input and output timing requirements for the STARTSCAN signal.

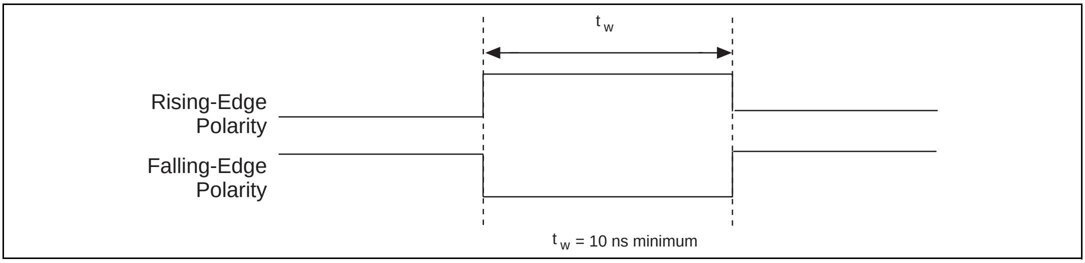


Figure 4-19. STARTSCAN Input Signal Timing

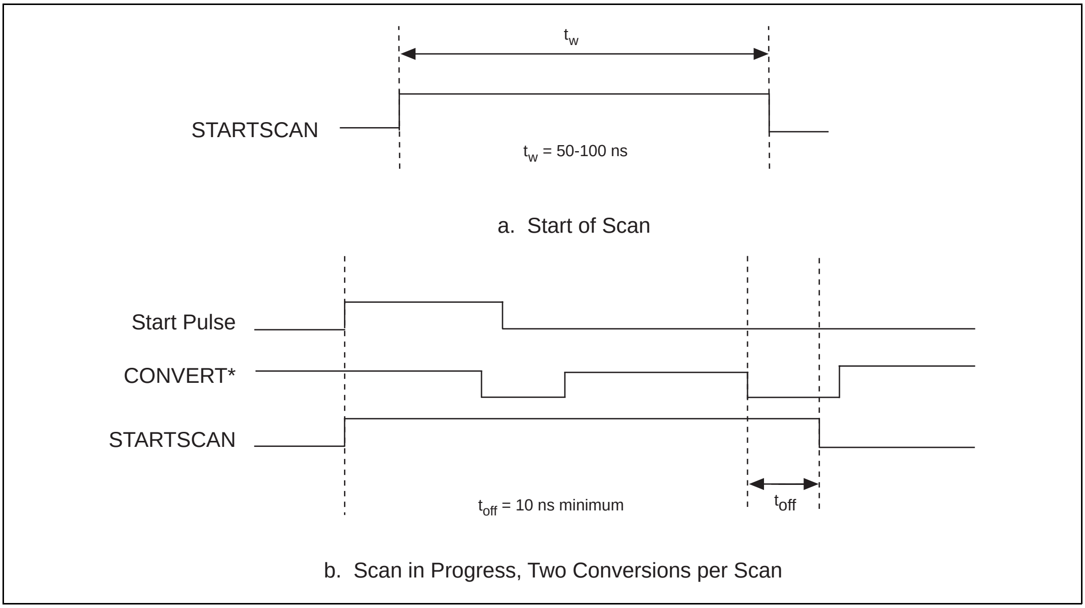


Figure 4-20. STARTSCAN Output Signal Timing

The CONVERT* pulses are masked off until the device generates the STARTSCAN signal. If you are using internally generated conversions, the first CONVERT* appears when the onboard sample interval counter reaches zero. If you select an external CONVERT*, the first external pulse after STARTSCAN generates a conversion. The STARTSCAN pulses should be separated by at least one scan period.

A counter on your device internally generates the STARTSCAN signal unless you select some external source. This counter is started by the TRIG1 signal and is stopped either by software or by the sample counter.

Scans generated by either an internal or external STARTSCAN signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

CONVERT* Signal

Any PFI pin can externally input the CONVERT* signal, which is available as an output on the PFI2/CONVERT* pin.

Refer to Figures 4-11 and 4-12 for the relationship of CONVERT* to the DAQ sequence.

As an input, the CONVERT* signal is configured in the edge-detection mode. You can select any PFI pin as the source for CONVERT* and configure the polarity selection for either rising or falling edge. The selected edge of the CONVERT* signal initiates an A/D conversion.

The ADC switches to hold mode within 60 ns of the selected edge. This hold-mode delay time is a function of temperature and does not vary from one conversion to the next. CONVERT* pulses should be separated by at least 5 µs (200 kHz sample rate)

As an output, the CONVERT* signal reflects the actual convert pulse that is connected to the ADC. This is true even if the conversions are being externally generated by another PFI. The output is an active low pulse with a pulse width of 50 to 150 ns. This output is set to tri-state at startup.

Figures 4-21 and 4-22 show the input and output timing requirements for the CONVERT* signal.

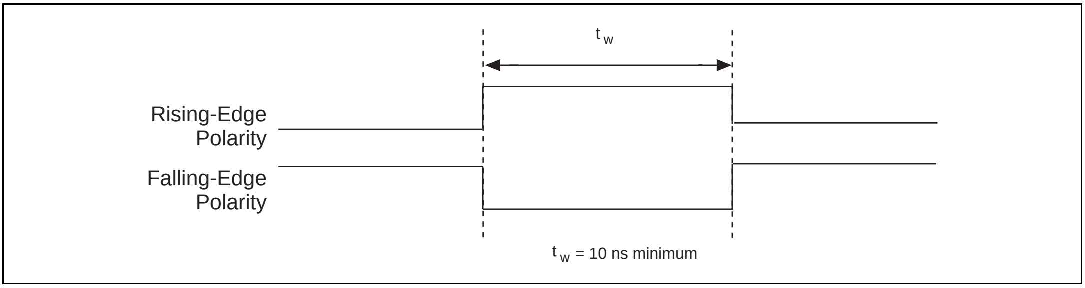


Figure 4-21. CONVERT* Input Signal Timing

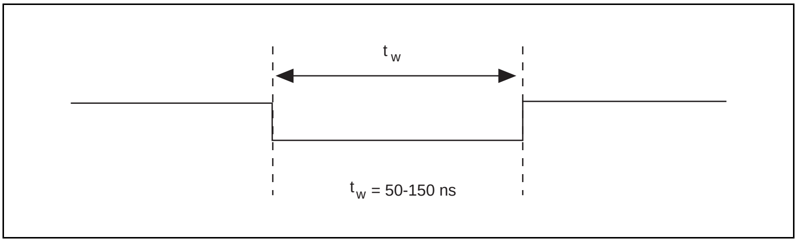


Figure 4-22. CONVERT* Output Signal Timing

The sample interval counter on the device normally generates the CONVERT* signal unless you select some external source. The counter is started by the STARTSCAN signal and continues to count down and reload itself until the scan is finished. It then reloads itself in preparation for the next STARTSCAN pulse.

A/D conversions generated by either an internal or external CONVERT* signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

AIGATE Signal

Any PFI pin can externally input the AIGATE signal, which is not available as an output on the I/O connector. The AIGATE signal can mask off scans in a DAQ sequence. You can configure the PFI pin you select as the source for the AIGATE signal in either the level-detection or edge-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

In the level-detection mode if AIGATE is active, the STARTSCAN signal is masked off and no scans can occur. In the edge-detection mode, the first active edge disables the STARTSCAN signal, and the second active edge enables STARTSCAN.

The AIGATE signal can neither stop a scan in progress nor continue a previously gated-off scan; in other words, once a scan has started, AIGATE does not gate off conversions until the beginning of the next scan and, conversely, if conversions are being gated off, AIGATE does not gate them back on until the beginning of the next scan.

SISOURCE Signal

Any PFI pin can externally input the SISOURCE signal, which is not available as an output on the I/O connector. The onboard scan interval counter uses the SISOURCE signal as a clock to time the generation of the STARTSCAN signal. You must configure the PFI pin you select as the source for the SISOURCE signal in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase generates the SISOURCE signal unless you select some external source. Figure 4-23 shows the timing requirements for the SISOURCE signal.

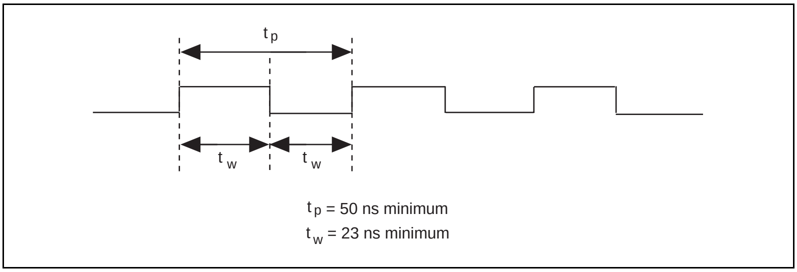


Figure 4-23. SISOURCE Signal Timing

Waveform Generation Timing Connections

The analog group defined for your device is controlled by WFTRIG, UPDATE*, and UISOURCE.

WFTRIG Signal

Any PFI pin can externally input the WFTRIG signal, which is available as an output on the PFI6/WFTRIG pin.

As an input, the WFTRIG signal is configured in the edge-detection mode. You can select any PFI pin as the source for WFTRIG and configure the polarity selection for either rising or falling edge. The selected edge of the WFTRIG signal starts the waveform generation for the DACs. The update interval (UI) counter is started if you select internally generated UPDATE*.

As an output, the WFTRIG signal reflects the trigger that initiates waveform generation. This is true even if the waveform generation is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-24 and 4-25 show the input and output timing requirements for the WFTRIG signal.

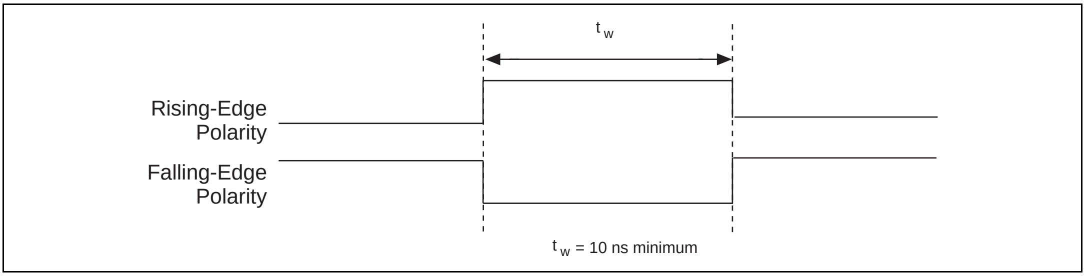


Figure 4-24. WFTRIG Input Signal Timing

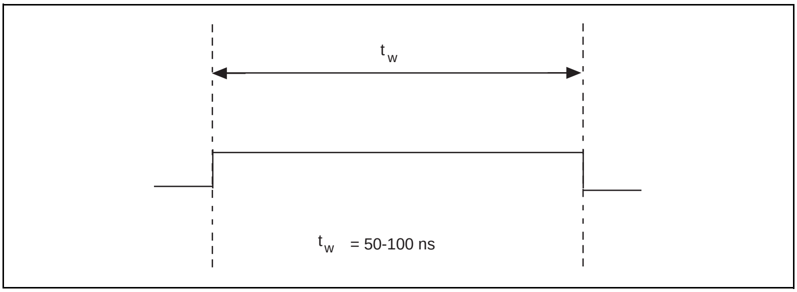


Figure 4-25. WFTRIG Output Signal Timing

UPDATE* Signal

Any PFI pin can externally input the UPDATE* signal, which is available as an output on the PFI5/UPDATE* pin.

As an input, the UPDATE* signal is configured in the edge-detection mode. You can select any PFI pin as the source for UPDATE* and configure the polarity selection for either rising or falling edge. The selected edge of the UPDATE* signal updates the outputs of the DACs. In order to use UPDATE*, you must set the DACs to posted-update mode.

As an output, the UPDATE* signal reflects the actual update pulse that is connected to the DACs. This is true even if the updates are being externally generated by another PFI. The output is an active low pulse with a pulse width of 300 to 350 ns. This output is set to tri-state at startup.

Figures 4-26 and 4-27 show the input and output timing requirements for the UPDATE* signal.

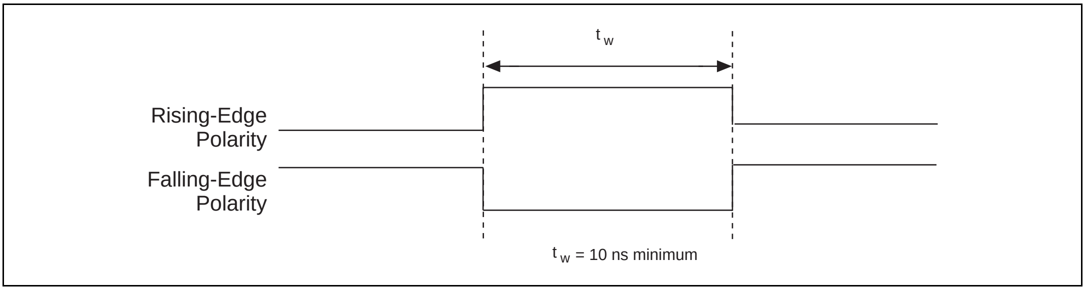


Figure 4-26. UPDATE* Input Signal Timing

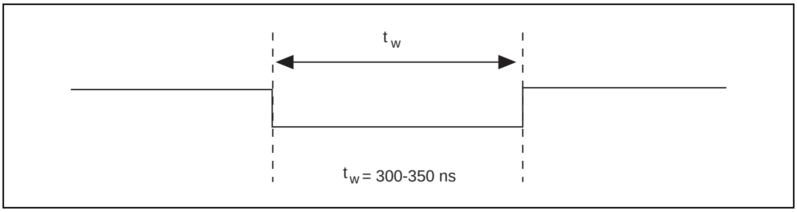


Figure 4-27. UPDATE* Output Signal Timing

The DACs are updated within 100 ns of the leading edge. Separate the UPDATE* pulses with enough time that new data can be written to the DAC latches.

The device UI counter normally generates the UPDATE* signal unless you select some external source. The UI counter is started by the WFTRIG signal and can be stopped by software or the internal Buffer Counter. D/A conversions generated by either an internal or external UPDATE* signal do not occur when gated by the software command register gate.

UISOURCE Signal

Any PFI pin can externally input the UISOURCE signal, which is not available as an output on the I/O connector. The UI counter uses the UISOURCE signal as a clock to time the generation of the UPDATE* signal. You must configure the PFI pin you select as the source for the UISOURCE signal in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low. Figure 4-28 shows the timing requirements for the UISOURCE signal.

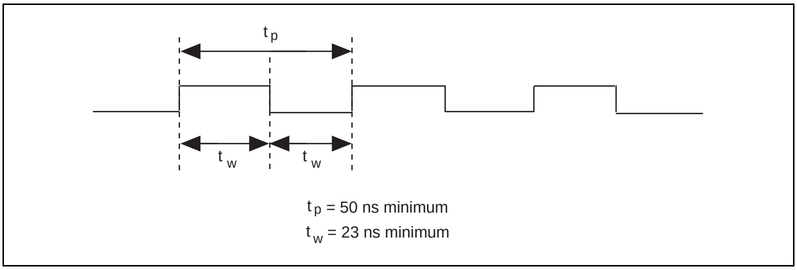


Figure 4-28. UISOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase normally generates the UISOURCE signal unless you select some external source.

General-Purpose Timing Signal Connections

The general-purpose timing signals are GPCTR0_SOURCE, GPCTR0_GATE, GPCTR0_OUT, GPCTR0_UP_DOWN, GPCTR1_SOURCE, GPCTR1_GATE, GPCTR1_OUT, GPCTR1_UP_DOWN, and FREQ_OUT.

GPCTR0_SOURCE Signal

Any PFI pin can externally input the GPCTR0_SOURCE signal, which is available as an output on the PFI8/GPCTR0_SOURCE pin.

As an input, the GPCTR0_SOURCE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, the GPCTR0_SOURCE signal reflects the actual clock connected to general-purpose counter 0. This is true even if another PFI is externally inputting the source clock. This output is set to tri-state at startup.

Figure 4-29 shows the timing requirements for the GPCTR0_SOURCE signal.

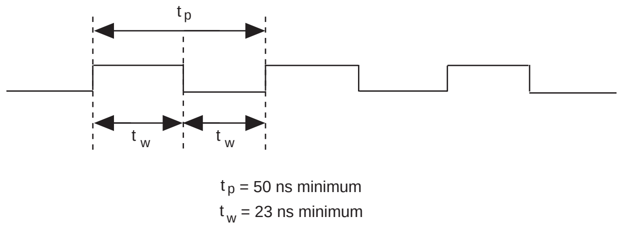


Figure 4-29. GPCTR0_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR0_SOURCE signal unless you select some external source.

GPCTR0_GATE Signal

Any PFI pin can externally input the GPCTR0_GATE signal, which is available as an output on the PFI9/GPCTR0_GATE pin.

As an input, the GPCTR0_GATE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform actions such as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, the GPCTR0_GATE signal reflects the actual gate signal connected to general-purpose counter 0. This is true even if the gate is being externally generated by another PFI. This output is set to tri-state at startup. Figure 4-30 shows the timing requirements for the GPCTR0_GATE signal.

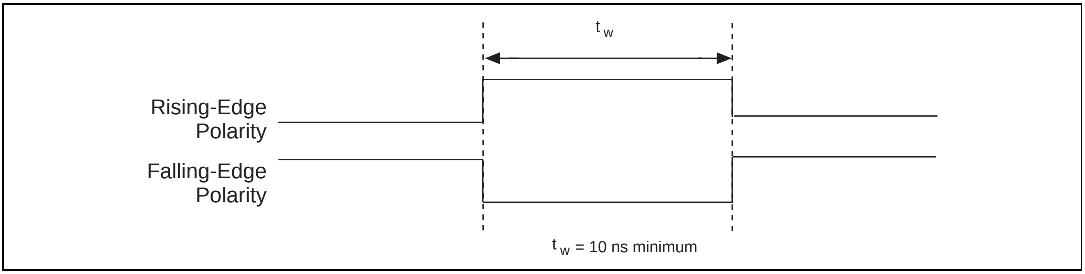


Figure 4-30. GPCTR0_GATE Signal Timing in Edge-Detection Mode

GPCTR0_OUT Signal

This signal is available only as an output on the GPCTR0_OUT pin. The GPCTR0_OUT signal reflects the terminal count (TC) of general-purpose counter 0. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software-selectable for both options. This output is set to tri-state at startup. Figure 4-31 shows the timing of the GPCTR0_OUT signal.

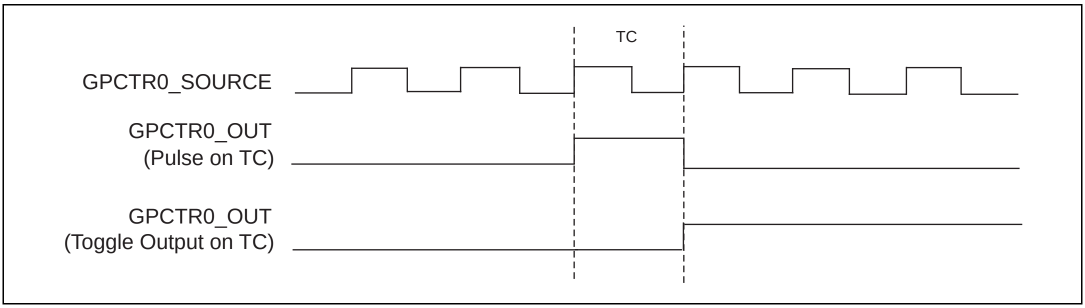


Figure 4-31. GPCTR0_OUT Signal Timing

GPCTR0_UP_DOWN Signal

This signal can be externally input on the DIO6 pin and is not available as an output on the I/O connector. The general-purpose counter 0 will count down when this pin is at a logic low and count up when it is at a logic high. You can disable this input so that software can control the up-down functionality and leave the DIO6 pin free for general use.

GPCTR1_SOURCE Signal

Any PFI pin can externally input the GPCTR1_SOURCE signal, which is available as an output on the PFI3/GPCTR1_SOURCE pin.

As an input, the GPCTR1_SOURCE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR1_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, the GPCTR1_SOURCE monitors the actual clock connected to general-purpose counter 1. This is true even if the source clock is being externally generated by another PFI. This output is set to tri-state at startup.

Figure 4-32 shows the timing requirements for the GPCTR1_SOURCE signal.

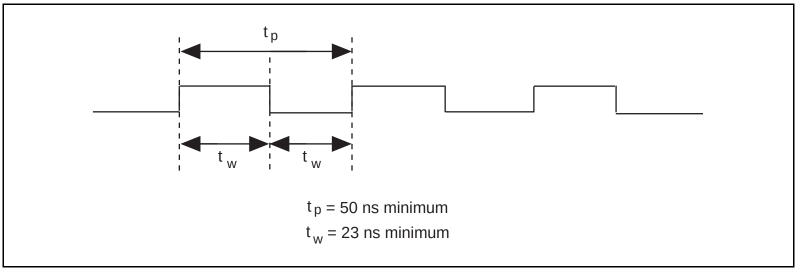


Figure 4-32. GPCTR1_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR1_SOURCE unless you select some external source.

GPCTR1_GATE Signal

Any PFI pin can externally input the GPCTR1_GATE signal, which is available as an output on the PFI4/GPCTR1_GATE pin.

As an input, the GPCTR1_GATE signal is configured in edge-detection mode. You can select any PFI pin as the source for GPCTR1_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform such actions as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, the GPCTR1_GATE signal monitors the actual gate signal connected to general-purpose counter 1. This is true even if the gate is being externally generated by another PFI. This output is set to tri-state at startup. Figure 4-33 shows the timing requirements for the GPCTR1_GATE signal.

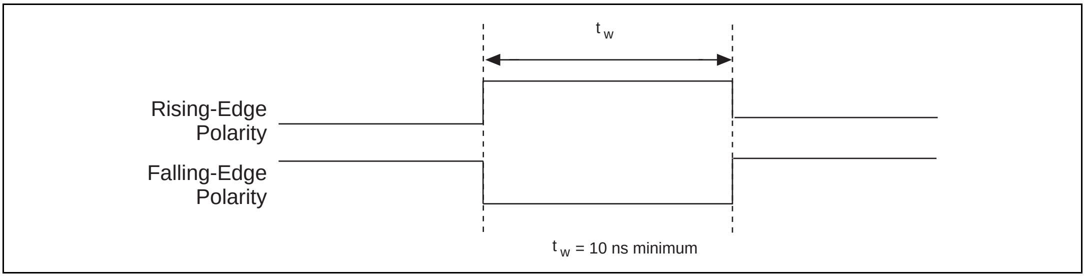


Figure 4-33. GPCTR1_GATE Signal Timing in Edge-Detection Mode

GPCTR1_OUT Signal

This signal is available only as an output on the GPCTR1_OUT pin. The GPCTR1_OUT signal monitors the TC device general-purpose counter 1. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software-selectable for both options. This output is set to tri-state at startup. Figure 4-34 shows the timing requirements for the GPCTR1_OUT signal.

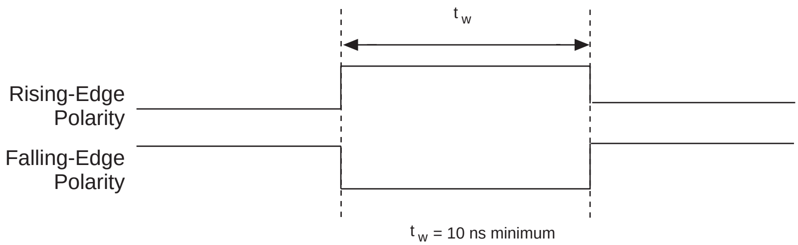
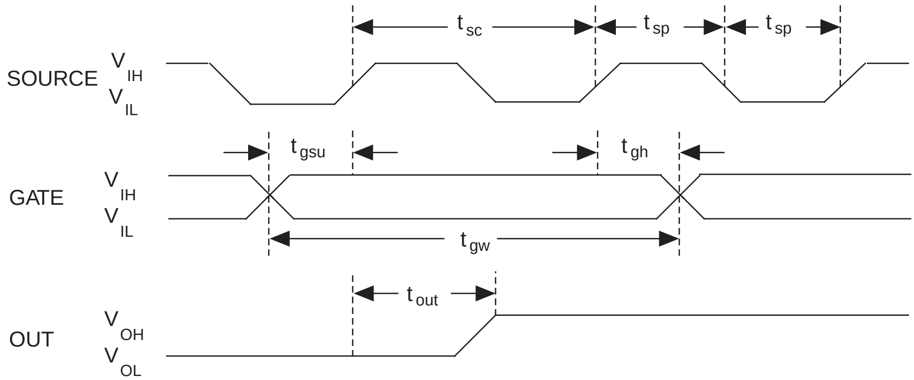


Figure 4-34. GPCTR1_OUT Signal Timing

GPCTR1_UP_DOWN Signal

This signal can be externally input on the DIO7 pin and is not available as an output on the I/O connector. General-purpose counter 1 counts down when this pin is at a logic low and counts up at a logic high. This input can be disabled so that software can control the up-down functionality and leave the DIO7 pin free for general use. Figure 4-35 shows the timing requirements for the GATE and SOURCE input signals and the timing specifications for the OUT output signals of your device.



Source Clock Period	t_{sc}	50 ns minimum
Source Pulse Width	t_{sp}	23 ns minimum
Gate Setup Time	t_{gsu}	10 ns minimum
Gate Hold Time	t_{gh}	0 ns minimum
Gate Pulse Width	t_{gw}	10 ns minimum
Output Delay Time	t_{out}	80 ns maximum

Figure 4-35. GPCTR Timing Summary

The GATE and OUT signal transitions shown in Figure 4-35 are referenced to the rising edge of the SOURCE signal. This timing diagram assumes that the counters are programmed to count rising edges. The same timing diagram, but with the source signal inverted and referenced to the falling edge of the source signal, would apply when the counter is programmed to count falling edges.

The GATE input timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated signals on your device. Figure 4-35 shows the GATE signal referenced to the rising edge of a source signal. The gate must be valid (either high or low) for at least 10 ns before the rising or falling edge of a source signal for the gate to take effect at that source edge, as shown by t_{gsu} and t_{gh} in Figure 4-35. The gate signal is not required to be held after the active edge of the source signal.

If you use an internal timebase clock, the gate signal cannot be synchronized with the clock. In this case, gates applied close to a source edge take effect either on that source edge or on the next one. This arrangement results in an uncertainty of one source clock period with respect to unsynchronized gating sources.

The OUT output timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated clock signals on the devices. Figure 4-35 shows the OUT signal referenced to the rising edge of a source signal. Any OUT signal state changes occur within 80 ns after the rising or falling edge of the source signal.

FREQ_OUT Signal

This signal is available only as an output on the FREQ_OUT pin. The device frequency generator outputs the FREQ_OUT pin. The frequency generator is a 4-bit counter that can divide its input clock by the numbers 1 through 16. The input clock of the frequency generator is software-selectable from the internal 10 MHz and 100 kHz timebases. The output polarity is software-selectable. This output is set to tri-state at startup.

Field Wiring Considerations

Environmental noise can seriously affect the accuracy of measurements made with your device if you do not take proper care when running signal wires between signal sources and the device. The following recommendations apply mainly to analog input signal routing to the device, although they also apply to signal routing in general.

Minimize noise pickup and maximize measurement accuracy by taking the following precautions:

- Use differential analog input connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect analog input signals to the device. With this type of wire, the signals attached to the CH+ and CH– inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.
- Route signals to the device carefully. Keep cabling away from noise sources. The most common noise source in a computer based data acquisition system is the video monitor. Separate the monitor from the analog signals as much as possible.

The following recommendations apply for all signal connections to your device:

- Separate device signal lines from high-current or high-voltage lines. These lines can induce currents in or voltages on the device signal lines if they run in parallel paths at a close distance. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel, or run the lines at right angles to each other.
- Do not run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

For more information, refer to the application note, *Field Wiring and Noise Consideration for Analog Signals*, available from National Instruments.

5 Calibration

This chapter discusses the calibration procedures for your device. If you are using the NI-DAQ device driver, that software includes calibration functions for performing all of the steps in the calibration process.

Calibration refers to the process of minimizing measurement and output voltage errors by making small circuit adjustments. For these devices, these adjustments take the form of writing values to onboard calibration DACs (CalDACs).

Some form of device calibration is required for all but the most forgiving applications. If you do not calibrate your device, your signals and measurements could have very large offset, gain, and linearity errors.

Three levels of calibration are available to you and described in this chapter. The first level is the fastest, easiest, and least accurate, whereas the last level is the slowest, most difficult, and most accurate.

Loading Calibration Constants

Your device is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the values that were written to the CalDACs to achieve calibration in the factory—are stored in the onboard nonvolatile memory (EEPROM). Because the CalDACs have no memory capability, they do not retain calibration information when the device is unpowered. Loading calibration constants refers to the process of loading the CalDACs with the values stored in the EEPROM. NI-DAQ software determines when this is necessary and does it automatically. If you are not using NI-DAQ, you must load these values yourself.

In the EEPROM there is a user-modifiable calibration area in addition to the permanent factory calibration area. This means that you can load the CalDACs with values either from the original factory calibration or from a calibration that you subsequently performed.

This method of calibration is not very accurate because it does not take into account the fact that the device measurement and output voltage errors can vary with time and temperature. It is better to self-calibrate when the device is installed in the environment in which it will be used.

Self-Calibration

Your device can measure and correct for almost all of its calibration-related errors without any external signal connections. Your National Instruments software provides a self-calibration method. This self-calibration process, which generally takes less than a minute, is the preferred method of assuring accuracy in your application. Initiate self-calibration to minimize the effects of any offset, gain, and linearity drifts, particularly those due to warmup.

Immediately after self-calibration, the only significant residual calibration error could be gain error due to time or temperature drift of the onboard voltage reference. This error is addressed by external calibration, which is discussed in the following section. If you are interested primarily in relative measurements, you can ignore a small amount of gain error, and self-calibration should be sufficient.

External Calibration

Your device has an onboard calibration reference to ensure the accuracy of self-calibration. Its specifications are listed in Appendix A, *Specifications*. The reference voltage is measured at the factory and stored in the EEPROM for subsequent self-calibrations. This voltage is stable enough for most applications, but if you are using your device at an extreme temperature or if the onboard reference has not been measured for a year or more, you may wish to externally calibrate your device.

An external calibration refers to calibrating your device with a known external reference rather than relying on the onboard reference. Redetermining the value of the onboard reference is part of this process and the results can be saved in the EEPROM, so you should not have to perform an external calibration very often. You can externally calibrate your device by calling the NI-DAQ calibration function.

To externally calibrate your device, be sure to use a very accurate external reference. The reference should be several times more accurate than the device itself.

Other Considerations

The CalDACs adjust the gain error of each analog output channel by adjusting the value of the reference voltage supplied to that channel. This calibration mechanism is designed to work only with the internal 10 V reference. Thus, in general, it is not possible to calibrate the analog output gain error when using an external reference. In this case, it is advisable to account for the nominal gain error of the analog output channel either in software or with external hardware. See Appendix A, *Specifications*, for analog output gain error information.

A

Specifications

This appendix lists the specifications of the 6034E and 6035E devices. These specifications are typical at 25 °C unless otherwise noted.

Analog Input

Input Characteristics

Number of channels .... 16 single-ended or 8 differential (software-selectable per channel)

Type of ADC.. Successive approximation

Resolution .... 16 bits, 1 in 65,536

Sampling rate .... 200 kS/s guaranteed

Input signal ranges .... Bipolar only

Device Gain (Software-Selectable)	**Range**
0.5	±10 V
1	±5 V
10	±500 mV
100	±50 mV

Input coupling .... DC

Max working voltage
(signal + common mode) .... Each input should remain within ±11 V of ground

Overvoltage protection

	Powered On	Powered Off
ACH<0..15>	±25 V	±15V
AISENSE	±25 V	±15V

FIFO buffer size.....................................512 samples

Data transfers..DMA, interrupts, programmed I/O

DMA modes ....Scatter-gather (Single transfer, demand transfer)

Configuration memory size ....512 words

Accuracy Information

Nominal Range (V)		Absolute Accuracy							Relative Accuracy	
		% of Reading			Offset	Noise + Quantization (µV)		Temp Drift	Resolution (µV)	
Positive FS	Negative FS	24 Hours	90 Days	1 Year	(µV)	Single Pt.	Averaged	(%/°C)	Theoretical	Averaged
10	–10	0.0496	0.0516	0.0538	±1591	±885	±77.9	0.0010	305.2	102.5
5	–5	0.0146	0.0166	0.0188	±806	±443	±38.9	0.0005	152.6	51.26
0.5	–0.5	0.0496	0.0516	0.0538	±99.5	±53.4	±4.76	0.0010	15.26	6.273
0.05	–0.05	0.0496	0.0516	0.0538	±28.9	±26.4	±2.57	0.0010	1.526	3.380

Note: Accuracies are valid for measurements following an internal E Series calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings. Measurement accuracies are listed for operational temperatures within ± 1 °C of internal calibration temperature and ±10 °C of external or factory calibration temperature.

Transfer Characteristics

Relative accuracy .... ±1.5 LSB typ, ±3.0 LSB max

DNL .... ±0.5 LSB typ, ±1.0 LSB max

No missing codes .... 16 bits, guaranteed

Offset error

- Pregain error after calibration .... ±1.0 μV max
- Pregain error before calibration ...... ±2.92 mV max
- Postgain error after calibration .... ±305 μV max
- Postgain error before calibration..... ±70.3 mV max

Gain error (relative to calibration reference)

- After calibration (gain = 1) .... ±74 ppm of reading max
- Before calibration .... ±18,900 ppm of reading max
- Gain ≠ 1 with gain error adjusted to 0 at gain = 1 .... ±300 ppm of reading max

Amplifier Characteristics

Input impedance

- Normal powered on .... 100 GΩ in parallel with 100 pF
- Powered off..................................... 820 Ω
- Overload.. 820 Ω

Input bias current .... ±200 pA

Input offset current................................ ±100 pA

CMRR (DC to 60 Hz)

- Gain 0.5, 1.0.................................... 85 dB
- Gain 10, 100.................................... 96 dB

Dynamic Characteristics

Bandwidth

Signal	Bandwidth
Small (–3 dB)	413 kHz
Large (1% THD)	490 kHz

Settling time for full-scale step

Gain 100 ....±4 LSB, 5 µs typ

Gain 0.5, 1, 10 ....±2 LSB, 5 µs max

System noise (LSBrms, including quantization)

Gain	LSBrms
0.5, 1.0	0.8
10	1.0
100	5.6

Crosstalk ....DC to 100 kHz

Adjacent channels............................–75 dB

Other channels ....≤–90 dB

Stability

Recommended warm-up time.................15 min.

Offset temperature coefficient

Pregain..±20 µV/°C

Postgain ....±175 µV/°C

Gain temperature coefficient ....±20 ppm/°C

Analog Output

♦ 6035E only

Output Characteristics

Number of channels .... 2 voltage

Resolution .... 12 bits, 1 in 4,096

Max update rate
- DMA .... 10 kHz, system dependent
- Interrupts... 1 kHz, system dependent

Type of DAC... Double buffered, multiplying

FIFO buffer size .... none

Data transfers .... DMA, interrupts, programmed I/O

DMA modes.. Scatter-gather (Single transfer, demand transfer)

Accuracy Information

Nominal Range (V)		Absolute Accuracy				
		% of Reading			Offset	Temp Drift
Positive FS	Negative FS	24 Hours	90 Days	1 Year	(mV)	(%/ °C)
10	–10	0.0177	0.0197	0.0219	± 5.933	0.0005

Transfer Characteristics

Relative accuracy (INL)
- After calibration.............................. ±0.3 LSB typ, ±0.5 LSB max
- Before calibration .... ±4 LSB max

DNL
- After calibration.............................. ±0.3 LSB typ, ± 1.0 LSB max
- Before calibration .... ±3 LSB max

Monotonicity ....12 bits, guaranteed after calibration

Offset error

After calibration..............................±1.0 mV max

Before calibration ....±200 mV max

Gain error (relative to internal reference)

After calibration..............................±0.01% of output max

Before calibration ....±0.75% of output max

Voltage Output

Range ....± 10 V

Output coupling ....DC

Output impedance..................................0.1 Ω max

Current drive..±5 mA max

Protection..Short-circuit to ground

Power-on state (steady state) ....±200 mV

Initial power-up glitch

Magnitude.......................................±1.1 V

Duration.. 2.0 ms

Power reset glitch

Magnitude.......................................±2.2 V

Duration.. 4.2 µs

Dynamic Characteristics

Settling time for full-scale step..............10 µs to ±0.5 LSB accuracy

Slew rate ....10 V/µs

Noise..200 µVrms, DC to 1 MHz

Midscal transition glitch

Magnitude.......................................±12 mV

Duration.. 2.0 µs

Stability

Offset temperature coefficient .... ±50 µV/°C

Gain temperature coefficient.................. ±25 ppm/°C

Digital I/O

Number of channels .... 8 input/output

Compatibility .... TTL/CMOS

DIO<0..7>

Digital logic levels

Level	**Min**	**Max**
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V
Input low current (V_{in} = 0 V)	—	–320 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Power-on state .... Input (High-Z), 50 kΩ pull up to +5 VDC

Data transfers .... Programmed I/O

Timing I/O

Number of channels .... 2 up/down counter/timers, 1 frequency scaler

Resolution

Counter/timers .... 24 bits

Frequency scalers............................ 4 bits

Compatibility .... TTL/CMOS

Base clocks available

Counter/timers ....20 MHz, 100 kHz

Frequency scalers ....10 MHz, 100 kHz

Base clock accuracy...............................±0.01%

Max source frequency............................20 MHz

Min source pulse duration ....10 ns in edge-detect mode

Min gate pulse duration ....10 ns in edge-detect mode

Data transfers ....DMA, interrupts, programmed I/O

DMA modes ....Scatter-gather (Single transfer, demand transfer)

Triggers

Digital Trigger

Compatibility ....TTL

Response ....Rising or falling edge

Pulse width ....10 ns min

RTSI

Trigger lines...7

Calibration

Recommended warm-up time................15 minutes

Interval...1 year

External Calibration reference...............> 6 and < 10 V

Onboard calibration reference

- Level .... 5.000 V (±3.5 mV) (actual value stored in EEPROM)
- Temperature coefficient .... ±5 ppm/°C max
- Long-term stability .... ±15 ppm/ $\sqrt{1,000\ h}$

Power Requirement

+5 VDC (±5%)...................................... 0.9 A

☞ **Note** Excludes power consumed through V_{cc} available at the I/O connector.

Power available at I/O connector........... +4.65 to +5.25 VDC at 1 A

Physical

Dimensions (not including connectors)

- PCI devices .... 17.5 by 10.6 cm (6.9 by 4.2 in.)
- PXI devices.................................... 16.0 by 10.0 cm (6.3 by 3.9 in.)

I/O connector... 68-pin male SCSI-II type

Operating Environment

Ambient temperature.............................. 0 to 55 °C

Relative humidity.................................. 10% to 90% noncondensing

♦ PXI-6035E only

Functional Shock.................................... MIL-T-28800 E Class 3 (per Section 4.5.5.4.1) Half-sine shock pulse, 11 ms duration, 30 g peak, 30 shocks per face

Operational random vibration .... 5 to 500 Hz, 0.31 g_{rms}, 3 axes

Storage Environment

Ambient temperature ....–20 to 70 °C

Relative humidity ....5% to 95% noncondensing

♦ PXI-6035E only

Non-operational random vibration ....5 to 500 Hz, 2.5 g_{rms}, 3 axes

☞ **Note** Random vibration profiles were developed in accordance with MIL-T-28800E and MIL-STD-810E Method 514. Test levels exceed those recommended in MIL-STD-810E for Category 1, Basic Transportation.

B

Custom Cabling and Optional Connectors

This appendix describes the various cabling and connector options for the devices.

Custom Cabling

National Instruments offers cables and accessories for you to prototype your application or to use if you frequently change device interconnections.

If you want to develop your own cable, however, the following guidelines may be useful:

- For the analog input signals, shielded twisted-pair wires for each analog input pair yield the best results, assuming that you use differential inputs. Tie the shield for each signal pair to the ground reference at the source.
- You should route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

The following list gives recommended part numbers for connectors that mate to the I/O connector on your device.

Mating connectors and a backshell kit for making custom 68-pin cables are available from National Instruments (part number 776832-01)

Honda 68-position, solder cup, female connector (part number PCS-E68FS). Honda backshell (part number PCS-E68LKPA).

Optional Connectors

Figure B-1 shows the pin assignments for the 68-pin E Series connector. This connector is available when you use the SH6868 or R6868 cable assemblies.

ACH8	34	68	ACH0
ACH1	33	67	AIGND
AIGND	32	66	ACH9
ACH10	31	65	ACH2
ACH3	30	64	AIGND
AIGND	29	63	ACH11
ACH4	28	62	AISENSE
AIGND	27	61	ACH12
ACH13	26	60	ACH5
ACH6	25	59	AIGND
AIGND	24	58	ACH14
ACH15	23	57	ACH7
DAC0OUT[1]	22	56	AIGND
DAC1OUT[1]	21	55	AOGND
RESERVED	20	54	AOGND
DIO4	19	53	DGND
DGND	18	52	DIO0
DIO1	17	51	DIO5
DIO6	16	50	DGND
DGND	15	49	DIO2
+5 V	14	48	DIO7
DGND	13	47	DIO3
DGND	12	46	SCANCLK
PFI0/TRIG1	11	45	EXTSTROBE*
PFI1/TRIG2	10	44	DGND
DGND	9	43	PFI2/CONVERT*
+5 V	8	42	PFI3/GPCTR1_SOURCE
DGND	7	41	PFI4/GPCTR1_GATE
PFI5/UPDATE*	6	40	GPCTR1_OUT
PFI6/WFTRIG	5	39	DGND
DGND	4	38	PFI7/STARTSCAN
PFI9/GPCTR0_GATE	3	37	PFI8/GPCTR0_SOURCE
GPCTR0_OUT	2	36	DGND
FREQ_OUT	1	35	DGND

[1] Not available on the 6034E

Figure B-1. 68-Pin E Series Connector Pin Assignments

Figure B-2 shows the pin assignments for the 50-pin E Series connector. This connector is available when you use the SH6850 or R6850 cable assemblies.

AIGND	1	2	AIGND
ACH0	3	4	ACH8
ACH1	5	6	ACH9
ACH2	7	8	ACH10
ACH3	9	10	ACH11
ACH4	11	12	ACH12
ACH5	13	14	ACH13
ACH6	15	16	ACH14
ACH7	17	18	ACH15
AISENSE	19	20	DAC0OUT[1]
DAC1OUT[1]	21	22	RESERVED
AOGND	23	24	DGND
DIO0	25	26	DIO4
DIO1	27	28	DIO5
DIO2	29	30	DIO6
DIO3	31	32	DIO7
DGND	33	34	+5 V
+5 V	35	36	SCANCLK
EXTSTROBE*	37	38	PFI0/TRIG1
PFI1/TRIG2	39	40	PFI2/CONVERT*
PFI3/GPCTR1_SOURCE	41	42	PFI4/GPCTR1_GATE
GPCTR1_OUT	43	44	PFI5/UPDATE*
PFI6/WFTRIG	45	46	PFI7/STARTSCAN
PFI8/GPCTR0_SOURCE	47	48	PFI9/GPCTR0_GATE
GPCTR0_OUT	49	50	FREQ_OUT

[1] Not available on the 6034E

Figure B-2. 50-Pin E Series Connector Pin Assignments

C

Common Questions

This appendix contains a list of commonly asked questions and their answers relating to usage and special features of your device.

General Information

What is the DAQ-STC?

The DAQ-STC is the System Timing Control application-specific integrated circuit (ASIC) designed by National Instruments and is the backbone of the E Series devices. The DAQ-STC contains seven 24-bit counters and three 16-bit counters. The counters are divided into the following three groups:

- Analog input—two 24-bit, two 16-bit counters
- Analog output—three 24-bit, one 16-bit counters
- General-purpose counter/timer functions—two 24-bit counters

The groups can be configured independently with timing resolutions of 50 ns or 10 µs. With the DAQ-STC, you can interconnect a wide variety of internal timing signals to other internal blocks. The interconnection scheme is quite flexible and completely software configurable. New capabilities such as buffered pulse generation, equivalent time sampling, and seamless changing of the sampling rate are possible.

What does sampling rate mean to me?

It means that this is the fastest you can acquire data on your device and still achieve accurate results. For example, these devices have a sampling rate of 200 kS/s. This sampling rate is aggregate: one channel at 200 kS/s or two channels at 100 kS/s per channel illustrates the relationship.

What type of 5 V protection do the devices have?

The devices have 5 V lines equipped with a self-resetting 1 A fuse.

Installation and Configuration

How do I set the base address for a my device?

The base address of your device is assigned automatically through the PCI/PXI bus protocol. This assignment is completely transparent to you.

What jumpers should I be aware of when configuring my E Series device?

The E Series devices are jumperless and switchless.

Which National Instruments document should I read first to get started using DAQ software?

Your NI-DAQ or application software release notes documentation is always the best starting place.

What version of NI-DAQ must I have to use my 6034E/6035E?

You must have *NI-DAQ for PC Compatibles* version 6.6 or higher.

Analog Input and Output

I'm using my device in differential analog input mode and I have connected a differential input signal, but my readings are random and drift rapidly. What's wrong?

Check your ground reference connections. Your signal may be referenced to a level that is considered *floating* with reference to the device ground reference. Even if you are in differential mode, the signal *must* still be referenced to the same ground level as the device reference. There are various methods of achieving this while maintaining a high common-mode rejection ratio (CMRR). These methods are outlined in Chapter 4, *Signal Connections*.

I'm using the DACs to generate a waveform, but I discovered with a digital oscilloscope that there are glitches on the output signal. Is this normal?

When it switches from one voltage to another, any DAC produces glitches due to released charges. The largest glitches occur when the most significant bit (MSB) of the D/A code switches. You can build a lowpass deglitching filter to remove some of these glitches, depending on the frequency and nature of your output signal.

Can I synchronize a one-channel analog input data acquisition with a one-channel analog output waveform generation on my PCI E Series device?

Yes. One way to accomplish this is to use the waveform generation timing pulses to control the analog input data acquisition. To do this, follow steps 1 through 4 below, in addition to the usual steps for data acquisition and waveform generation configuration.

1. Enable the PFI5 line for output, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_PFI_5, ND_OUT_UPDATE, ND_HIGH_TO_LOW)`.
   - If you are using LabVIEW, invoke Route Signal VI with signal name set to PFI5 and signal source set to AO Update.
2. Set up data acquisition timing so that the timing signal for A/D conversion comes from PFI5, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_IN_CONVERT, ND_PFI_5, ND_HIGH_TO_LOW)`.
   - If you are using LabVIEW, invoke AI Clock Config VI with clock source code set to PFI pin, high to low, and clock source string set to 5.
3. Initiate analog input data acquisition, which will start only when the analog output waveform generation starts.
4. Initiate analog output waveform generation.

Timing and Digital I/O

What types of triggering can be hardware-implemented on my device?

Digital triggering is hardware-supported on every device.

Will the counter/timer applications that I wrote previously work with the DAQ-STC?

If you are using NI-DAQ with LabVIEW, some of your applications drawn using the CTR VIs will still run. However, there are many differences in the counters between the E Series and other devices; the counter numbers are different, timebase selections are different, and the DAQ-STC counters are 24-bit counters (unlike the 16-bit counters on devices without the DAQ-STC).

If you are using the NI-DAQ language interface or LabWindows/CVI, the answer is no, the counter/timer applications that you wrote previously will not work with the DAQ-STC. You must use the GPCTR functions; ICTR and CTR functions will not work with the DAQ-STC. The GPCTR functions have the same capabilities as the ICTR and CTR functions, plus more, but you must rewrite the application with the GPCTR function calls.

I'm using one of the general-purpose counter/timers on my device, but I do not see the counter/timer output on the I/O connector. Why?

If you are using the NI-DAQ language interface or LabWindows/CVI, you must configure the output line to output the signal to the I/O connector. Use the `Select_Signal` call in NI-DAQ to configure the output line. By default, all timing I/O lines except EXTSTROBE* are tri-stated.

What are the PFIs and how do I configure these lines?

PFIs are Programmable Function Inputs. These lines serve as connections to virtually all internal timing signals.

If you are using the NI-DAQ language interface or LabWindows/CVI, use the `Select_Signal` function to route internal signals to the I/O connector, route external signals to internal timing sources, or tie internal timing signals together.

If you are using NI-DAQ with LabVIEW and you want to connect external signal sources to the PFI lines, you can use AI Clock Config, AI Trigger Config, AO Clock Config, AO Trigger and Gate Config, CTR Mode Config, and CTR Pulse Config advanced level VIs to indicate which function the connected signal will serve. Use the Route Signal VI to enable the PFI lines to output internal signals.

Caution If you enable a PFI line for output, do not connect any external signal source to it; if you do, you can damage the device, the computer, and the connected equipment.

What are the power-on states of the PFI and DIO lines on the I/O connector?

At system power-on and reset, both the PFI and DIO lines are set to high impedance by the hardware. This means that the device circuitry is not actively driving the output either high or low. However, these lines may have pull-up or pull-down resistors connected to them as shown in Table 4-2. These resistors weakly pull the output to either a logic high or logic low state. For example, DIO(0) will be in the high impedance state after power on, and Table 4-2 shows that there is a 50 kΩ pull-up resistor. This pull-up resistor will set the DIO(0) pin to a logic high when the output is in a high impedance state.

D

Technical Support Resources

This appendix describes the comprehensive resources available to you in the Technical Support section of the National Instruments Web site and provides technical support telephone numbers for you to use if you have trouble connecting to our Web site or if you do not have internet access.

NI Web Support

To provide you with immediate answers and solutions 24 hours a day, 365 days a year, National Instruments maintains extensive online technical support resources. They are available to you at no cost, are updated daily, and can be found in the Technical Support section of our Web site at `www.natinst.com/support`.

Online Problem-Solving and Diagnostic Resources

- **KnowledgeBase**—A searchable database containing thousands of frequently asked questions (FAQs) and their corresponding answers or solutions, including special sections devoted to our newest products. The database is updated daily in response to new customer experiences and feedback.
- **Troubleshooting Wizards**—Step-by-step guides lead you through common problems and answer questions about our entire product line. Wizards include screen shots that illustrate the steps being described and provide detailed information ranging from simple getting started instructions to advanced topics.
- **Product Manuals**—A comprehensive, searchable library of the latest editions of National Instruments hardware and software product manuals.
- **Hardware Reference Database**—A searchable database containing brief hardware descriptions, mechanical drawings, and helpful images of jumper settings and connector pinouts.
- **Application Notes**—A library with more than 100 short papers addressing specific topics such as creating and calling DLLs, developing your own instrument driver software, and porting applications between platforms and operating systems.

Software-Related Resources

- **Instrument Driver Network**—A library with hundreds of instrument drivers for control of standalone instruments via GPIB, VXI, or serial interfaces. You also can submit a request for a particular instrument driver if it does not already appear in the library.
- **Example Programs Database**—A database with numerous, non-shipping example programs for National Instruments programming environments. You can use them to complement the example programs that are already included with National Instruments products.
- **Software Library**—A library with updates and patches to application software, links to the latest versions of driver software for National Instruments hardware products, and utility routines.

Worldwide Support

National Instruments has offices located around the globe. Many branch offices maintain a Web site to provide information on local services. You can access these Web sites from `www.natinst.com/worldwide`.

If you have trouble connecting to our Web site, please contact your local National Instruments office or the source from which you purchased your National Instruments product(s) to obtain support.

For telephone support in the United States, dial 512 795 8248. For telephone support outside the United States, contact your local branch office:

Australia 03 9879 5166, Austria 0662 45 79 90 0, Belgium 02 757 00 20, Brazil 011 284 5011, Canada (Ontario) 905 785 0085, Canada (Québec) 514 694 8521, China 0755 3904939, Denmark 45 76 26 00, Finland 09 725 725 11, France 01 48 14 24 24, Germany 089 741 31 30, Hong Kong 2645 3186, India 91805275406, Israel 03 6120092, Italy 02 413091, Japan 03 5472 2970, Korea 02 596 7456, Mexico (D.F.) 5 280 7625, Mexico (Monterrey) 8 357 7695, Netherlands 0348 433466, Norway 32 27 73 00, Singapore 2265886, Spain (Madrid) 91 640 0085, Spain (Barcelona) 93 582 0251, Sweden 08 587 895 00, Switzerland 056 200 51 51, Taiwan 02 2377 1200, United Kingdom 01635 523545

Glossary

Prefix	Meanings	Value
p-	pico	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}
t-	tera-	10^{12}

Numbers/Symbols

%	percent
+	positive of, or plus
–	negative of, or minus
/	per
°	degree
Ω	ohm

A

A	amperes
A/D	analog-to-digital
AC	alternating current
ACH	analog input channel signal

ADC	analog-to-digital converter—an electronic device, often an integrated circuit, that converts an analog voltage to a digital number
ADC resolution	the resolution of the ADC, which is measured in bits. An ADC with 16 bits has a higher resolution, and thus a higher degree of accuracy, than a 12-bit ADC.
AI	analog input
AIGATE	analog input gate signal
AIGND	analog input ground signal
AISENSE	analog input sense signal
alias	a false lower frequency component that appears in sampled data acquired at too low a sampling rate
ANSI	American National Standards Institute
AO	analog output
AOGND	analog output ground signal
ASIC	Application-Specific Integrated Circuit—a proprietary semiconductor component designed and manufactured to perform a set of specific functions for a specific customer
asynchronous	(1) hardware—a property of an event that occurs at an arbitrary time, without synchronization to a reference clock (2) software—a property of a function that begins an operation and returns prior to the completion or termination of the operation

B

bandwidth	the range of frequencies present in a signal, or the range of frequencies to which a measuring device can respond
base address	a memory address that serves as the starting address for programmable registers. All other addresses are located by adding to the base address.
BIOS	Basic input/output system—BIOS functions are the fundamental level of any PC or compatible computer. BIOS functions embody the basic operations needed for successful use of the computer's hardware resources.

bipolar	a signal range that includes both positive and negative values (for example, –5 V to +5 V)
breakdown voltage	the voltage high enough to cause breakdown of optical isolation, semiconductors, or dielectric materials. *See also* working voltage.
bus	the group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. Examples of PC buses are the ISA and PCI bus.
bus master	a type of a plug-in device or controller with the ability to read and write devices on the computer bus

C

C	Celsius
CalDAC	calibration DAC
CH	channel—pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels.
channel clock	the clock controlling the time interval between individual channel sampling within a scan. Devices with simultaneous sampling do not have this clock.
CMRR	common-mode rejection ratio—a measure of an instrument's ability to reject interference from a common-mode signal, usually expressed in decibels (dB)
cold-junction compensation	a method of compensating for inaccuracies in thermocouple circuits
common-mode range	the input range over which a circuit can handle a common-mode signal
common-mode signal	any voltage present at the instrumentation amplifier inputs with respect to amplifier ground
conversion time	the time required, in an analog input or output system, from the moment a channel is interrogated (such as with a read instruction) to the moment that accurate data is available
CONVERT*	convert signal

counter/timer	a circuit that counts external pulses or clock pulses (timing)
crosstalk	an unwanted signal on one channel due to an input on a different channel
CTR	counter
current drive capability	the amount of current a digital or analog output channel is capable of sourcing or sinking while still operating within voltage range specifications
current sinking	the ability of a DAQ device to dissipate current for analog or digital output signals
current sourcing	the ability of a DAQ device to supply current for analog or digital output signals

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current
DAC0OUT	analog channel 0 output signal
DAC1OUT	analog channel 1 output signal
DAQ	data acquisition—(1) collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing; (2) collecting and measuring the same kinds of electrical signals with A/D and/or DIO devices plugged into a computer, and possibly generating control signals with D/A and/or DIO devices in the same computer
dB	decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: dB=20log10 V1/V2, for signals in volts
DC	direct current
DGND	digital ground signal
DIFF	differential mode

differential input	an analog input consisting of two terminals, both of which are isolated from computer ground, whose difference is measured
digital port	*See* port.
DIO	digital input/output
dithering	the addition of Gaussian noise to an analog input signal
DMA	direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
DNL	differential nonlinearity—a measure in least significant bit of the worst-case deviation of code widths from their ideal value of 1 LSB
DO	digital output
driver	software that controls a specific hardware device such as a DAQ device or a GPIB interface board

E

EEPROM	electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed
electrostatically coupled	propagating a signal by means of a varying electric field
external trigger	a voltage pulse from an external source that triggers an event such as A/D conversion
EXTSTROBE	external strobe signal

F

FIFO	first-in first-out memory buffer—the first data stored is the first data sent to the acceptor. FIFOs are often used on DAQ devices to temporarily store incoming or outgoing data until that data can be retrieved or output. For example, an analog input FIFO stores the results of A/D conversions until the data can be retrieved into system memory, a process that requires the servicing of interrupts and often the programming of the DMA controller. This process can take several milliseconds in some cases. During this time, data accumulates in the FIFO for future retrieval. With a larger FIFO, longer latencies can be tolerated. In the case of analog output, a FIFO permits faster update rates, because the waveform data can be stored on the FIFO ahead of time. This again reduces the effect of latencies associated with getting the data from system memory to the DAQ device.
filtering	a type of signal conditioning that allows you to filter unwanted signals from the signal you are trying to measure
floating signal sources	signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called nonreferenced signal sources. Some common example of floating signal sources are batteries, transformers, or thermocouples.
FREQ_OUT	frequency output signal
ft	feet

G

g	grams
gain	the factor by which a signal is amplified, sometimes expressed in decibels
gain accuracy	a measure of deviation of the gain of an amplifier from the ideal gain
GATE	gate signal
glitch	an unwanted momentary deviation from a desired signal
GPCTR	general purpose counter
GPCTR0_GATE	general purpose counter 0 gate signal
GPCTR0_OUT	general purpose counter 0 output signal

GPCTR0_SOURCE	general purpose counter 0 clock source signal
GPCTR0_UP_DOWN	general purpose counter 0 up down
GPCTR1_GATE	general purpose counter 1 gate signal
GPCTR1_OUT	general purpose counter 1 output signal
GPCTR1_SOURCE	general purpose counter 1 clock source signal
GPCTR1_UP_DOWN	general purpose counter 1 up down
GPIB	General Purpose Interface bus, synonymous with HP-IB. The standard bus used for controlling electronic instruments with a computer. Also called IEEE 488 bus because it is defined by ANSI/IEEE Standards 488-1978, 488.1-1987, and 488.2-1987.
grounded measurement system	*See* referenced single-ended configuration.

H

h	hour
half-power bandwidth	the frequency range over which a circuit maintains a level of at least –3 dB with respect to the maximum level
handshaked digital I/O	a type of digital acquisition/generation where a device or module accepts or transfers data after a digital pulse has been received. Also called latched digital I/O.
hex	hexadecimal
Hz	hertz—the number of scans read or updates written per second

I

I/O	input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces
I_{OH}	current, output high

I_{OL}	current, output low
in.	inches
INL	integral nonlinearity—a measure in LSB of the worst-case deviation from the ideal A/D or D/A transfer characteristic of the analog I/O circuitry
input bias current	the current that flows into the inputs of a circuit
input impedance	the resistance and capacitance between the input terminals of a circuit
input offset current	the difference in the input bias currents of the two inputs of an instrumentation amplifier
instrument driver	a set of high-level software functions that controls a specific GPIB, VXI, or RS-232 programmable instrument or a specific plug-in DAQ device. Instrument drivers are available in several forms, ranging from a function callable language to a virtual instrument (VI) in LabVIEW.
instrumentation amplifier	a circuit whose output voltage with respect to ground is proportional to the difference between the voltages at its two high impedance inputs
interrupt	a computer signal indicating that the CPU should suspend its current task to service a designated activity
interrupt level	the relative priority at which a device can interrupt
interval scanning	scanning method where there is a longer interval between scans than there is between individual channels comprising a scan
IRQ	interrupt request

K

k	kilo—the standard metric prefix for 1,000, or 10^3, used with units of measure such as volts, hertz, and meters
K	kilo—the prefix for 1,024, or 2^{10}, used with B in quantifying data or computer memory
kS	1,000 samples

L

LabVIEW	Laboratory Virtual Instrument Engineering Workbench—a program development application based on the programming language G and used commonly for test and measurement purposes
LED	light-emitting diode
library	a file containing compiled object modules, each comprised of one of more functions, that can be linked to other object modules that make use of these functions. NIDAQMSC.LIB is a library that contains NI-DAQ functions. The NI-DAQ function set is broken down into object modules so that only the object modules that are relevant to your application are linked in, while those object modules that are not relevant are not linked.
linearity	the adherence of device response to the equation R = KS, where R = response, S = stimulus, and K = a constant
LSB	least significant bit

M

MIO	multifunction I/O
MITE	MXI Interface to Everything—a custom ASIC designed by National Instruments that implements the PCI bus interface. The MITE supports bus mastering for high-speed data transfers over the PCI bus.
MS	million samples
MSB	most significant bit
mux	multiplexer—a switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel

N

NC	normally closed, or not connected
NI-DAQ	National Instruments driver software for DAQ hardware

noise	an undesirable electrical signal—Noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, soldering irons, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.
nonlatched digital I/O	a type of digital acquisition/generation where LabVIEW updates the digital lines or port states immediately or returns the digital value of an input line. Also called immediate digital I/O or non-handshaking.
nonreferenced signal sources	signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called floating signal sources. Some common example of nonreferenced signal sources are batteries, transformers, or thermocouples.
NRSE	nonreferenced single-ended mode—All measurements are made with respect to a common (NRSE) measurement system reference, but the voltage at this reference can vary with respect to the measurement system ground.

O

OUT	output pin—a counter output pin where the counter can generate various TTL pulse waveforms
output settling time	the amount of time required for the analog output voltage to reach its final value within specified limits
output slew rate	the maximum rate of change of analog output voltage from one level to another

P

PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 Mbytes/s.
peak to peak	a measure of signal amplitude; the difference between the highest and lowest excursions of the signal
PFI	programmable function input

PFI0/TRIG1	PFI0/trigger 1
PFI1/TRIG2	PFI1/trigger 2
PFI2/CONVERT*	PFI2/convert
PFI3/GPCTR1_ SOURCE	PFI3/general purpose counter 1 source
PFI4/GPCTR1_GATE	PFI4/general purpose counter 1 gate
PFI5/UPDATE*	PFI5/update
PFI6/WFTRIG	PFI6/waveform trigger
PFI7/STARTSCAN	PFI7/start of scan
PFI8/GPCTR0_ SOURCE	PFI8/general purpose counter 0 source
PFI9/GPCTR0_GATE	PFI9/general purpose counter 0 gate
PGIA	programmable gain instrumentation amplifier
Plug and Play devices	devices that do not require DIP switches or jumpers to configure resources on the devices—also called switchless devices
port	(1) a communications connection on a computer or a remote controller (2) a digital port, consisting of four or eight lines of digital input and/or output
posttriggering	the technique used on a DAQ device to acquire a programmed number of samples after trigger conditions are met
PPI	programmable peripheral interface
ppm	parts per million
pretriggering	the technique used on a DAQ device to keep a continuous buffer filled with data, so that when the trigger conditions are met, the sample includes the data leading up to the trigger condition
pts	points
pu	pullup

pulse trains	multiple pulses
pulsed output	a form of counter signal generation by which a pulse is outputted when a counter reaches a certain value

Q

quantization error	the inherent uncertainty in digitizing an analog value due to the finite resolution of the conversion process

R

RAM	random-access memory
real time	a property of an event or system in which data is processed as it is acquired instead of being accumulated and processed at a later time
referenced single-ended configuration	RSE—all measurements are made with respect to a common reference measurement system or a ground. Also called grounded measurement system.
relative accuracy	a measure in LSB of the accuracy of an ADC. It includes all non-linearity and quantization errors. It does not include offset and gain errors of the circuitry feeding the ADC.
resolution	the smallest signal increment that can be detected by a measurement system. Resolution can be expressed in bits, in proportions, or in percent of full scale. For example, a system has 12-bit resolution, one part in 4,096 resolution, and 0.0244% of full scale.
ribbon cable	a flat cable in which the wires are lined up, not bunched together
rise time	the difference in time between the 10% and 90% points of a system's step response
rms	root mean square—the square root of the average value of the square of the instantaneous signal amplitude; a measure of signal amplitude
RSE	*see* referenced single-ended configuration

RTSI bus	real-time system integration bus—the National Instruments timing bus that connects DAQ devices directly, for precise synchronization of functions. For PCI devices, the connection is made by means of connectors on top of the device. For PXI devices, the connection is made across the PXI trigger bus.

S

s	seconds
S	samples
S/H	sample-and-hold—a circuit that acquires and stores an analog voltage on a capacitor for a short period of time
S/s	samples per second—used to express the rate at which a DAQ device samples an analog signal
sample counter	the clock that counts the output of the channel clock, in other words, the number of samples taken. On devices with simultaneous sampling, this counter counts the output of the scan clock and hence the number of scans.
scan	one or more analog or digital input samples. Typically, the number of input samples in a scan is equal to the number of channels in the input group. For example, one pulse from the scan clock produces one scan which acquires one new sample from every analog input channel in the group.
scan clock	the clock controlling the time interval between scans.
scan rate	the number of scans per second. For example, a scan rate of 10 Hz means sampling each channel 10 times per second.
SCXI	Signal Conditioning eXtensions for Instrumentation—the National Instruments product line for conditioning low-level signals within an external chassis near sensors so only high-level signals are sent to DAQ devices in the noisy PC environment
SE	single-ended—a term used to describe an analog input that is measured with respect to a common ground
self-calibrating	a property of a DAQ device that has an extremely stable onboard reference and calibrates its own A/D and D/A circuits without manual adjustments by the user

sensor	a device that responds to a physical stimulus (heat, light, sound, pressure, motion, flow, and so on), and produces a corresponding electrical signal
settling time	the amount of time required for a voltage to reach its final value within specified limits
Shannon Sampling Theorem	a law of sampling theory stating that if a continuous bandwidth-limited signal contains no frequency components higher than half the frequency at which it is sampled, then the original signal can be recovered without distortion
signal conditioning	the manipulation of signals to prepare them for digitizing
SISOURCE	SI counter clock signal
SNR	signal-to-noise ratio—the ratio of the overall rms signal level to the rms noise level, expressed in decibels
software trigger	a programmed event that triggers an event such as data acquisition
software triggering	a method of triggering in which you simulate an analog trigger using software. Also called conditional retrieval.
SOURCE	source signal
SS	simultaneous sampling—a property of a system in which each input or output channel is digitized or updated at the same instant
STARTSCAN	start scan signal
STC	system timing controller
synchronous	(1) hardware—a property of an event that is synchronized to a reference clock (2) software—a property of a function that begins an operation and returns only when the operation is complete

T

TC	terminal count—the highest value of a counter
T/H	track-and-hold—a circuit that tracks an analog voltage and holds the value on command

THD	total harmonic distortion—the ratio of the total rms signal due to harmonic distortion to the overall rms signal, in decibel or a percentage
THD+N	signal-to-THD plus noise—the ratio in decibels of the overall rms signal to the rms signal of harmonic distortion plus noise introduced
throughput rate	the data, measured in bytes/s, for a given continuous operation, calculated to include software overhead
transducer	*See* sensor
transfer rate	the rate, measured in bytes/s, at which data is moved from source to destination after software initialization and set up operations; the maximum rate at which the hardware can operate
TRIG	trigger signal
trigger	any event that causes or starts some form of data capture
TTL	transistor-transistor logic—a digital circuit composed of bipolar transistors wired in a certain manner.

U

UI	update interval
unipolar	a signal range that is always positive (for example, 0 to +10 V)
UISOURCE	update interval counter clock signal
update	the output equivalent of a scan. One or more analog or digital output samples. Typically, the number of output samples in an update is equal to the number of channels in the output group. For example, one pulse from the update clock produces one update which sends one new sample to every analog output channel in the group.
update rate	the number of output updates per second

V

V	volts
Vcc	positive supply voltage

VDC	volts direct current
V_{IH}	volts, input high
V_{IL}	volts, input low
V_{in}	volts in
V_m	measured voltage
V_{OH}	volts, output high
V_{OL}	volts, output low
V_{ref}	reference voltage
Vrms	volts, root mean square
VI	virtual instrument—(1) a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument (2) a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program

W

waveform	multiple voltage readings taken at a specific sampling rate
WFTRIG	waveform generation trigger signal
working voltage	the highest voltage that should be applied to a product in normal use, normally well under the breakdown voltage for safety margin. *See also* breakdown voltage.

Index

Numbers

A

B

C

D

E

F

G

H

I

L

M

N

O

P

Q

R

S

T

U

V

W