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AT-A2150
User Manual

Dynamic Signal Acquisition Board for the PC AT

August 1993 Edition

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Preface

This manual describes the mechanical and electrical aspects of the AT-A2150 and contains information concerning its operation and programming. The AT-A2150 is a dynamic signal acquisition board and is a member of the National Instruments AT Series of PC AT I/O channel expansion boards for the IBM PC AT and compatible computers.

Organization of This Manual

The *AT-A2150 User Manual* is organized as follows:

- Chapter 1, *Introduction*, describes the AT-A2150, lists the contents of your AT-A2150 kit, describes the optional software and optional equipment, and explains how to unpack the AT-A2150.
- Chapter 2, *Configuration and Installation*, explains board configuration, installation of the AT-A2150 into the PC, signal connections to the board, and cabling considerations.
- Chapter 3, *Theory of Operation*, contains a functional overview of the AT-A2150 and explains the operation of each functional unit making up the AT-A2150.
- Chapter 4, *Programming*, discusses programming the AT-A2150 and describes the AT-A2150 control and status registers in detail. This chapter includes the AT-A2150 register address map, a detailed description of each register, and a functional programming description.
- Chapter 5, *Calibration Procedures*, discusses the calibration procedures for the AT-A2150 analog input circuitry.
- Appendix A, *Specifications*, lists the specifications of the AT-A2150.
- Appendix B, *Connectors,* describes the pinout and signal names for the I/O connector and the RTSI connector on the AT-A2150.
- Appendix C, *MSM82C53 Data Sheet*, contains the *MSM82C53 Programmable Interval Timer* (Oki Semiconductor) data sheet. This counter/timer is used on the AT-A2150.
- Appendix D, *Customer Communication*, contains forms for you to complete to facilitate communication with National Instruments concerning our products.
- The *Index* contains an alphabetical list of key terms and topics used in this manual, including the page where each one can be found.

Conventions Used in This Manual

The following conventions are used in this manual:

AT-A2150	AT-A2150 refers to the AT-A2150C and AT-A2150S boards unless otherwise stated.
italic	Italic text denotes emphasis, a cross reference, or an introduction to a key concept.
`monospace`	Text in this font denotes variables or routines.
NI-DAQ	NI-DAQ is used throughout this manual to refer to the NI-DAQ software for DOS/Windows/LabWindows unless otherwise noted.
PC	PC refers to the IBM PC AT and compatible computers.

Abbreviations

The following metric system prefixes are used with abbreviations for units of measure in this manual:

Prefix	Meaning	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}

The following abbreviations are used in this manual:

A	amperes
C	Celsius
dB	decibels
°	degrees
F	farads
hex	hexadecimal
Hz	hertz
I_{IH}	current, input high
I_{IL}	current, input low
I_{OH}	current, output high
I_{OL}	current, output low
in.	inches

M	megabytes of memory
Ω	ohms
%	percent
rms	root mean square
sec	seconds
V	volts
V_{IH}	volts, input high
V_{IL}	volts, input low
V_{OH}	volts, output high
V_{OL}	volts, output low
Vrms	volts, root mean square

Acronyms

The following acronyms are used in this manual:

AC	alternating current
A/D	analog-to-digital
ADC	A/D converter
BCD	binary-coded decimal
DC	direct current
DIP	dual inline package
DMA	direct memory access
DNL	differential nonlinearity
DSP	digital signal processing
EDAQ	end-of-data acquisition
EISA	Extended Industry Standard Architecture
FIFO	first-in-first-out
IMD	intermodulation distortion
I/O	input/output
LSB	least significant bit
MSB	most significant bit
RTSI	Real-Time System Integration
SCXI	Signal Conditioning eXtensions for Instrumentation
TC	terminal count
THD	total harmonic distortion
TTL	transistor-transistor logic
VDC	volts direct current

Related Documentation

The following document contains information that you may find helpful as you read this manual:

- *IBM Personal Computer AT Technical Reference* manual

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix D, *Customer Communication*, at the end of this manual.

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Chapter 1
Introduction

This chapter describes the AT-A2150, lists the contents of your AT-A2150 kit, describes the optional software and optional equipment, and explains how to unpack the AT-A2150.

The AT-A2150 is a dynamic signal acquisition board for the PC. The board has four channels of 16-bit, simultaneously sampled analog input with 64-times oversampling delta-sigma modulating ADCs and digital antialiasing filters for extremely high-accuracy data acquisition. The ADCs can be run at conversion rates of up to 51.2 kHz. The interface to the AT bus includes 256-word FIFO buffers for smooth data flow out of the board.

The AT-A2150 can interface to the National Instruments RTSI bus, which includes a serial data link directly to and from other National Instruments AT Series boards, such as the AT-DSP2200 digital signal processing board. With the RTSI bus, sampling clock synchronization is possible between multiple AT-A2150 boards for simultaneous sampling on more than four channels.

The AT-A2150 is useful for digitizing signals with bandwidths of 22 kHz or less. The antialiasing filters on the input ensure that signals are acquired with extremely high fidelity. Applications include audio signal processing and analysis, audio workstations, acoustics and speech research, sonar, and audio frequency test and measurement.

There are two models of the AT-A2150. The AT-A2150C is designed for full audio band measurements and for signal processing applications and is equipped with crystal oscillators for standard digital audio and digital signal processing frequencies. The AT-A2150S is designed for speech and voiceband measurements and comes with crystal oscillators for speech applications. (For more information about these frequencies, see Tables 3-1 and 3-2 in Chapter 3, *Theory of Operation*.) In this manual, AT-A2150 refers to the AT-A2150C and the AT-A2150S unless otherwise stated.

Figure 1-1 shows the AT-A2150 board.

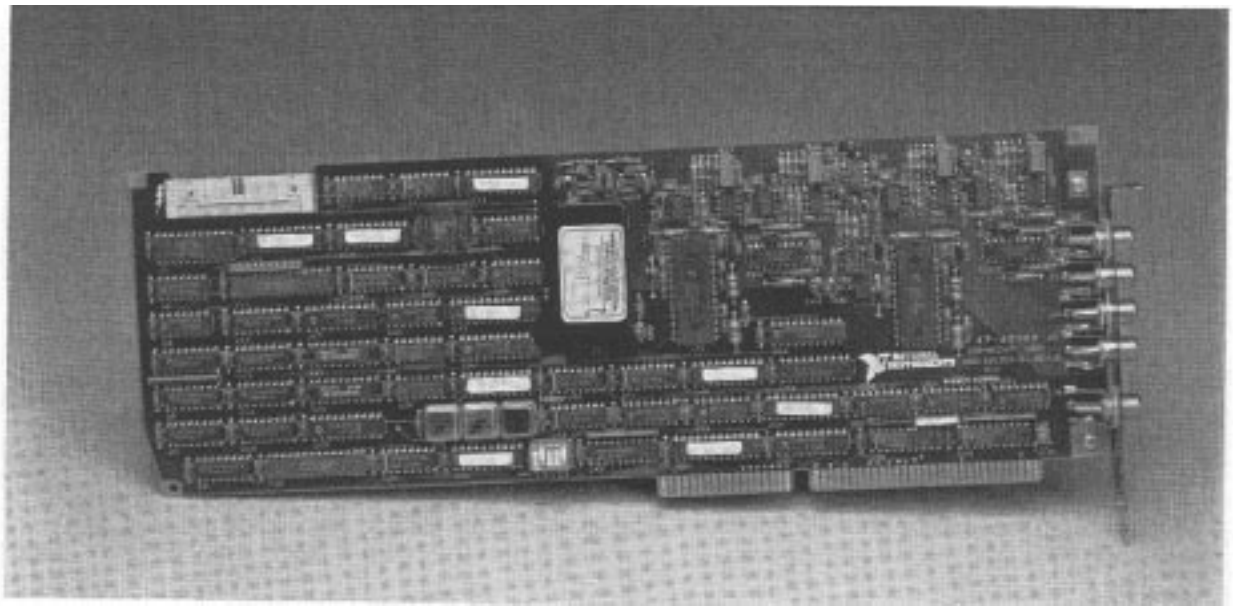


Figure 1-1. AT-A2150 Board

What Your Kit Should Contain

Each version of the AT-A2150 board has a different part number and kit part number, listed as follows.

Kit Name	Kit Part Number	Kit Component	Board Part Number
AT-A2150C	776493-01	AT-A2150C board	180350-01
AT-A2150S	776493-02	AT-A2150S board	180350-02

The board part number is printed on your board along the top edge on the component side. You can identify which version of the AT-A2150 board you have by looking up the part number in the preceding table.

In addition to the board, each version of the AT-A2150 kit contains the following components.

Kit Component	Part Number
AT-A2150 User Manual	320360-01
NI-DAQ software for DOS/Windows/LabWindows, with manuals	776250-01
NI-DAQ Software Reference Manual for DOS/Windows/LabWindows	320498-01
NI-DAQ Function Reference Manual for DOS/Windows/LabWindows	320499-01

If your kit is missing any of the components or if you received the wrong version, contact National Instruments.

Your AT-A2150 is shipped with the NI-DAQ software for DOS/Windows/LabWindows. NI-DAQ has a library of functions that can be called from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation, digital I/O, counter/timer, SCXI, RTSI, and self-calibration. NI-DAQ maintains a consistent software interface among its different versions so you can switch between platforms with minimal modifications to your code. NI-DAQ comes with language interfaces for Professional BASIC, Turbo Pascal, Turbo C, Turbo C++, Borland C++, and Microsoft C for DOS; and Visual Basic, Turbo Pascal, Microsoft C with SDK, and Borland C++ for Windows. NI-DAQ software is on high-density 5.25 in. and 3.5 in. diskettes.

Optional Software

This manual contains complete instructions for directly programming the AT-A2150. Normally, however, you should not need to read the low-level programming details in the user manual because the NI-DAQ software package for controlling the AT-A2150 is included with the board. Using NI-DAQ is quicker and easier than and as flexible as using the low-level programming described in Chapter 4, *Programming*.

You can use the AT-A2150 with LabVIEW for Windows or LabWindows for DOS. LabVIEW and LabWindows are innovative program development software packages for data acquisition and control applications. LabVIEW uses graphical programming, whereas LabWindows enhances Microsoft C and QuickBASIC. Both packages include extensive libraries for data acquisition, instrument control, data analysis, and graphical data presentation.

Part numbers for these software packages are listed in the following table.

Software	Part Number
LabVIEW for Windows	776670-01
LabWindows	
Standard package	776473-01
Advanced Analysis Library	776474-01
Standard package with the Advanced Analysis Library	776475-01

Optional Equipment

Equipment	Part Number
Type RCA1 single cable	
3 ft	181341-03
6 ft	181341-06
Type RCA2 dual cable	
3 ft	181342-03
6 ft	181342-06

Equipment	Part Number
AT-DSP2200 board	
with 64 Kwords of memory	776597-01
with 128 Kwords of memory	776597-02
with 384 Kwords of memory	776597-03
with 256 Kwords of memory	776597-04
AT Series RTSI bus cables for	
Two boards	776249-02
Three boards	776249-03
Four boards	776249-04
Five boards	776249-05

Unpacking

Your AT-A2150 is shipped in an antistatic plastic package to prevent electrostatic damage to the board. Several components on the board can be damaged by electrostatic discharge. To avoid such damage in handling the board, take the following precautions:

- Touch the plastic package to a metal part of your computer chassis before removing the board from the package.
- Remove the board from the package and inspect the board for loose components or any other sign of damage. Notify National Instruments if the board appears damaged in any way. *Do not* install a damaged board into your computer.

Chapter 2
Configuration and Installation

This chapter explains board configuration, installation of the AT-A2150 into the PC, signal connections to the board, and cabling considerations.

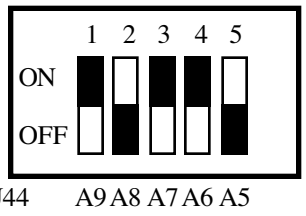
Board Configuration

The AT-A2150 contains one DIP switch to configure the AT bus interface setting. The DIP switch is shown in the parts locator diagram in Figure 2-1 and is used to set the base I/O address.

AT Bus Interface

The AT-A2150 is configured at the factory to use a base I/O address of hex 120. This setting (shown in Table 2-1) is suitable for most systems. However, if your system has other hardware at this base I/O address, you need to change these settings on the AT-A2150 (as described in the following pages) or on the other hardware. Record your settings in the *AT-A2150 Hardware and Software Configuration Form* in Appendix D, *Customer Communication*.

Table 2-1. AT-A2150 Factory-Set Switch Settings

Base I/O Address	Hex 120 (factory setting)	 (The black side indicates the side of the switch that is pushed down.)

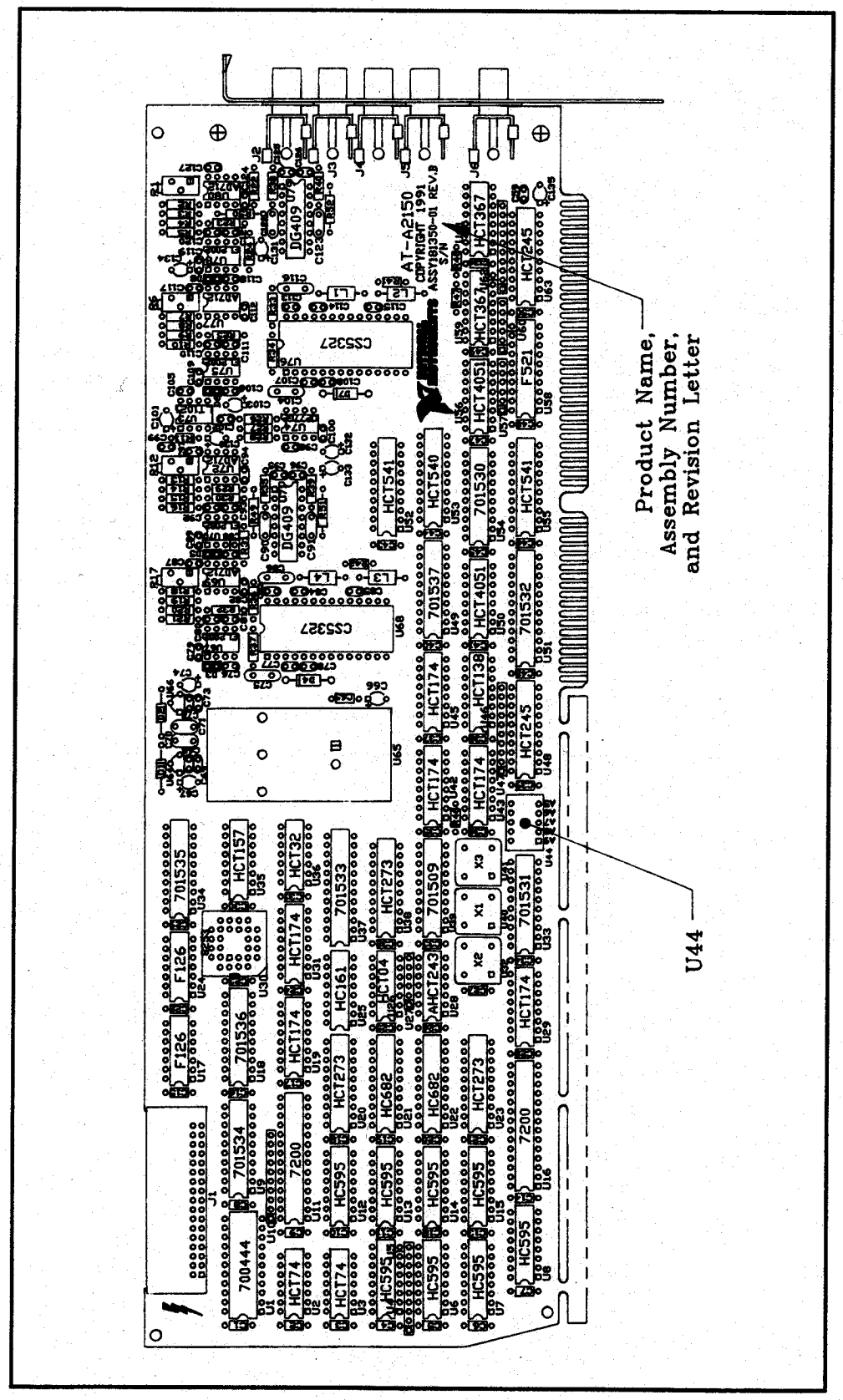


Figure 2-1. AT-A2150 Parts Locator Diagram

Base I/O Address Selection

The base I/O address for the AT-A2150 is determined by the switches at position U44 (see Figure 2-1). The switches are set at the factory for the base I/O address hex 120. This factory setting is used by National Instruments software packages as the default base I/O address value for the AT-A2150. The AT-A2150 uses the I/O address space hex 120 through 13F with the factory setting.

Note: Verify that this space is not already used by other equipment installed in your computer. If any equipment in your computer uses this base I/O address space, change the base I/O address of the AT-A2150 or of the other device. If you change the AT-A2150 base I/O address, make a corresponding change to any software packages you use with the AT-A2150. Table 2-2 lists the default settings of other National Instruments products for the PC. For more information about the I/O address of your PC, refer to the technical reference manual for your computer.

Each switch in U44 corresponds to one of the address lines A9 through A5. Press the side marked OFF to select a binary value of one for the corresponding address bit. Press the other side of the switch to select a binary value of zero for the corresponding address bit. Figure 2-2 shows two possible switch settings. The shaded portion indicates the side of the switch that is pressed down.

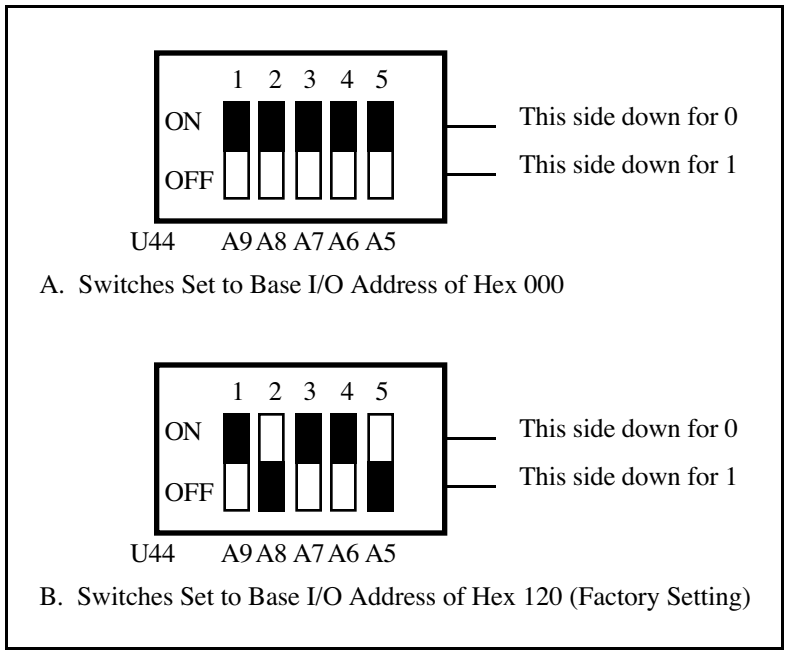


Figure 2-2. Example Base I/O Address Switch Settings

The five LSBs of the address (A4 through A0) are decoded by the AT-A2150 to select the appropriate AT-A2150 register. To change the base I/O address, remove the plastic cover on U44, press each switch to the desired position, verify that each switch is completely pressed down, and replace the plastic cover. Make a note of the new AT-A2150 base I/O address for use when configuring the AT-A2150 software (a form is included for you in Appendix D). Table 2-3 lists the possible switch settings, the corresponding base I/O address, and the base I/O address space used for that setting.

Table 2-2. Default Settings of National Instruments Products for the PC

Board	DMA Channel	Interrupt Level	Base I/O Address
AT-A2150	None*	None*	120 hex
AT-AO-6/10	Channel 5	Lines 11, 12	1C0 hex
AT-DIO-32F	Channels 5, 6	Lines 11, 12	240 hex
AT-DSP2200	None*	None*	120 hex
AT-GPIB	Channel 5	Line 11	2C0 hex
AT-MIO-16	Channels 6, 7	Line 10	220 hex
AT-MIO-16D	Channels 6, 7	Lines 5, 10	220 hex
AT-MIO-16F-5	Channels 6, 7	Line 10	220 hex
AT-MIO-16X	None*	None*	220 hex
AT-MIO-64F-5	None*	None*	220 hex
GPIB-PCII	Channel 1	Line 7	2B8 hex
GPIB-PCIIA	Channel 1	Line 7	02E1 hex
GPIB-PCIII	Channel 1	Line 7	280 hex
Lab-PC	Channel 3	Line 5	260 hex
PC-DIO-24	None	Line 5	210 hex
PC-DIO-96	None	Line 5	180 hex
PC-LPM-16	None	Line 5	260 hex
PC-TIO-10	None	Line 5	1A0 hex

* These settings are software configurable and are disabled at startup time.

Table 2-3. Switch Settings with Corresponding Base I/O Address and Base I/O Address Space

Switch Setting A9 A8 A7 A6 A5	Base I/O Address (hex)	Base I/O Address Space Used (hex)
0 0 0 0 0	000	000 - 01F *
0 0 0 0 1	020	020 - 03F *
0 0 0 1 0	040	040 - 05F *
0 0 0 1 1	060	060 - 07F *
0 0 1 0 0	080	080 - 09F *
0 0 1 0 1	0A0	0A0 - 0BF *
0 0 1 1 0	0C0	0C0 - 0DF *
0 0 1 1 1	0E0	0E0 - 0FF *
0 1 0 0 0	100	100 - 11F
0 1 0 0 1	120	120 - 13F
0 1 0 1 0	140	140 - 15F
0 1 0 1 1	160	160 - 17F
0 1 1 0 0	180	180 - 19F
0 1 1 0 1	1A0	1A0 - 1BF
0 1 1 1 0	1C0	1C0 - 1DF
0 1 1 1 1	1E0	1E0 - 1FF *
1 0 0 0 0	200	200 - 21F *
1 0 0 0 1	220	220 - 23F
1 0 0 1 0	240	240 - 25F
1 0 0 1 1	260	260 - 27F *
1 0 1 0 0	280	280 - 29F
1 0 1 0 1	2A0	2A0 - 2BF *
1 0 1 1 0	2C0	2C0 - 2DF *
1 0 1 1 1	2E0	2E0 - 2FF *
1 1 0 0 0	300	300 - 31F *
1 1 0 0 1	320	320 - 33F
1 1 0 1 0	340	340 - 35F
1 1 0 1 1	360	360 - 37F *
1 1 1 0 0	380	380 - 39F *
1 1 1 0 1	3A0	3A0 - 3BF *
1 1 1 1 0	3C0	3C0 - 3DF *
1 1 1 1 1	3E0	3E0 - 3FF *

Note: Base I/O address values hex 000 through 0FF are reserved for system use. Base I/O address values hex 100 through 3FF are available on the I/O channel. Also, addresses marked with an asterisk (*) may be reserved depending on the system and should be avoided. Please refer to the *IBM Personal Computer AT Technical Reference* manual for additional information about the I/O space available to expansion cards.

Analog Input Configuration

Analog input channel coupling (AC or DC) is software programmable and is discussed in Chapter 4, *Programming*.

Installation

The AT-A2150 can be installed in any available 16-bit expansion slot (AT style) in your computer. However, to achieve best noise performance, you should leave as much room as possible between the AT-A2150 and other boards and hardware. The AT-A2150 *does not* work if installed in an 8-bit expansion slot (PC style). After you have made any necessary changes, verified, and recorded the switch settings (a form is included in Appendix D), you are ready to install the AT-A2150. The following are general installation instructions, but consult the user manual or technical reference manual of your PC for specific instructions and warnings.

1. Turn off your computer.
2. Remove the top cover or access port to the I/O channel.
3. Remove the expansion slot cover on the back panel of the computer.
4. Insert the AT-A2150 into a 16-bit slot. It may be a tight fit, but do not force the board into place.
5. If you want to connect AT Series boards to each other, attach a RTSI cable to the RTSI connectors at this time.
6. Screw the mounting bracket of the AT-A2150 to the back panel rail of the computer.
7. Check the installation.
8. Replace the cover.

The AT-A2150 board is installed and ready for operation.

Signal Connections

This section contains specifications and connection instructions for the I/O signals on the AT-A2150 I/O connector.

I/O Connector Description

Figure 2-3 shows the signal assignments for the AT-A2150 I/O connector. This connector is located on the back panel of the AT-A2150 board and is accessible at the rear of the PC after the board has been properly installed. The connector consists of five RCA-type phono jacks and accepts standard RCA-type phono plugs.

Warning: Connections that exceed any of the maximum ratings of input or output signals on the AT-A2150 can result in damage to the AT-A2150 board and to the PC, including connections of any power signals to ground and vice versa. The description of each

signal in this section includes information about maximum input or output ratings. National Instruments is not liable for any damages resulting from incorrect signal connections.

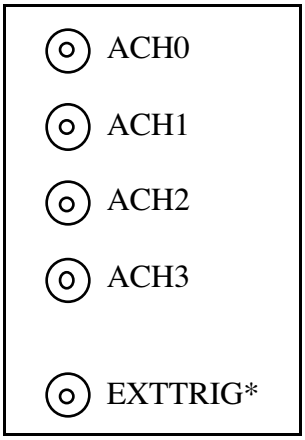


Figure 2-3. AT-A2150 I/O Connector Signal Assignments

Signal Connection Descriptions

Table 2-4 lists the signal descriptions for the AT-A2150 I/O connector.

Table 2-4. I/O Connector Signal Descriptions

Signal Name	Description
ACH0	Analog input Channel 0
ACH1	Analog input Channel 1
ACH2	Analog input Channel 2
ACH3	Analog input Channel 3
EXTTRIG*	External digital trigger to start a conversion sequence

Analog Input Signal Connections

The following ratings apply to inputs ACH<0..3>:

Input signal range	±2.828 V (2 Vrms)
Maximum input voltage rating	±20 V powered on or off

Exceeding the input signal range does not damage the input circuitry as long as the maximum input voltage rating of ±20 V is not exceeded.

Warning: Exceeding the input signal range results in distorted input signals. Exceeding the maximum input voltage rating can result in damage to the AT-A2150 board and to the PC. National Instruments is not liable for any damages resulting from incorrect signal connections.

Cabling Considerations

When you are connecting signal sources to the AT-A2150, use high-quality coaxial cables with low resistance and thorough shielding whenever possible. Sources should be floating, although this is not always possible. The analog grounds on the AT-A2150 are internally connected to the computer's ground, which in turn is connected to earth ground through the chassis and power connections. If a signal source is also grounded, then a large ground loop is set up when the signal source is connected to the board. This condition sometimes induces a large amount of unwanted noise in the signal (especially 60-Hz noise) and should be avoided whenever possible. Some signal sources have provisions for floating the output ground, which significantly cleans up the signal.

Digital Signal Connections

The digital trigger line (EXTTRIG*) is bidirectional, which means it can be used both to input and output a digital trigger signal. When EXTTRIG* is not being driven by the board, the line appears as an input at the I/O connector. When EXTTRIG* is being driven by the board, the line appears as a TTL output.

The following specifications and ratings apply to the digital trigger line.

Absolute maximum voltage input rating:	+5.75 V with respect to DGND -0.5 V with respect to DGND

Digital input specifications (referenced to DGND):

V_{IH} input logic high voltage	2 V minimum
V_{IL} input logic low voltage	0.8 V maximum
I_{IH} input current load, logic high input voltage	10 μA maximum
I_{IL} input current load, logic low input voltage	-10 μA maximum

Digital output specifications (referenced to DGND):

V_{OH} output logic high voltage	2.4 V minimum
V_{OL} output logic low voltage	0.5 V maximum
I_{OH} high-level output current	-3.2 mA
I_{OL} low-level output current	24 mA

A data acquisition operation can be initiated by an external trigger applied to the EXTTRIG* input or by a software trigger. Notice that the ADC operates in a free running mode; therefore, the hardware or software triggering actually controls storage of the conversion data. Figure 2-4 shows the timing requirements for the EXTTRIG* signal.

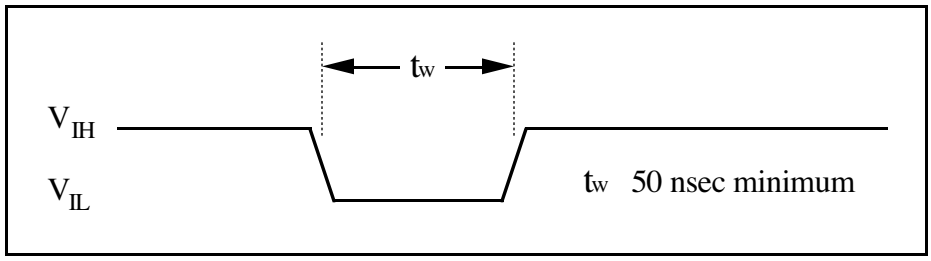


Figure 2-4. Timing Requirements for the EXTTRIG* Signal

A hardware trigger can be generated in one of three ways: a TTL-level trigger (high-to-low transition) from an external source applied at the EXTTRIG* signal on the I/O connector, a trigger generated from the internal level-and-slope detection circuit, and a trigger received over the RTSI bus. The hardware trigger can initiate three of the four available data acquisition modes: posttrigger mode, pretrigger mode, and delayed trigger mode. The fourth mode is the no-hardware trigger mode. In posttrigger mode, the A/D conversion data storage in the FIFO is initiated after a hardware trigger or a software trigger. This storage is terminated after a programmed count expires. In pretrigger mode, A/D conversion data storage in the FIFO is started via software. The counter, however, is not started until a hardware trigger. A/D conversion data storage is disabled after the programmed count expires. Thus, conversion data both before and after the trigger is obtained. In delayed trigger mode, A/D conversion data storage in the FIFO is initiated after a programmable delay from the hardware trigger or a software trigger. The A/D conversion data storage is disabled after a programmed count expires.

Chapter 3
Theory of Operation

This chapter contains a functional overview of the AT-A2150 and explains the operation of each functional unit making up the AT-A2150.

Functional Overview

Figure 3-1 is a block diagram of the AT-A2150.

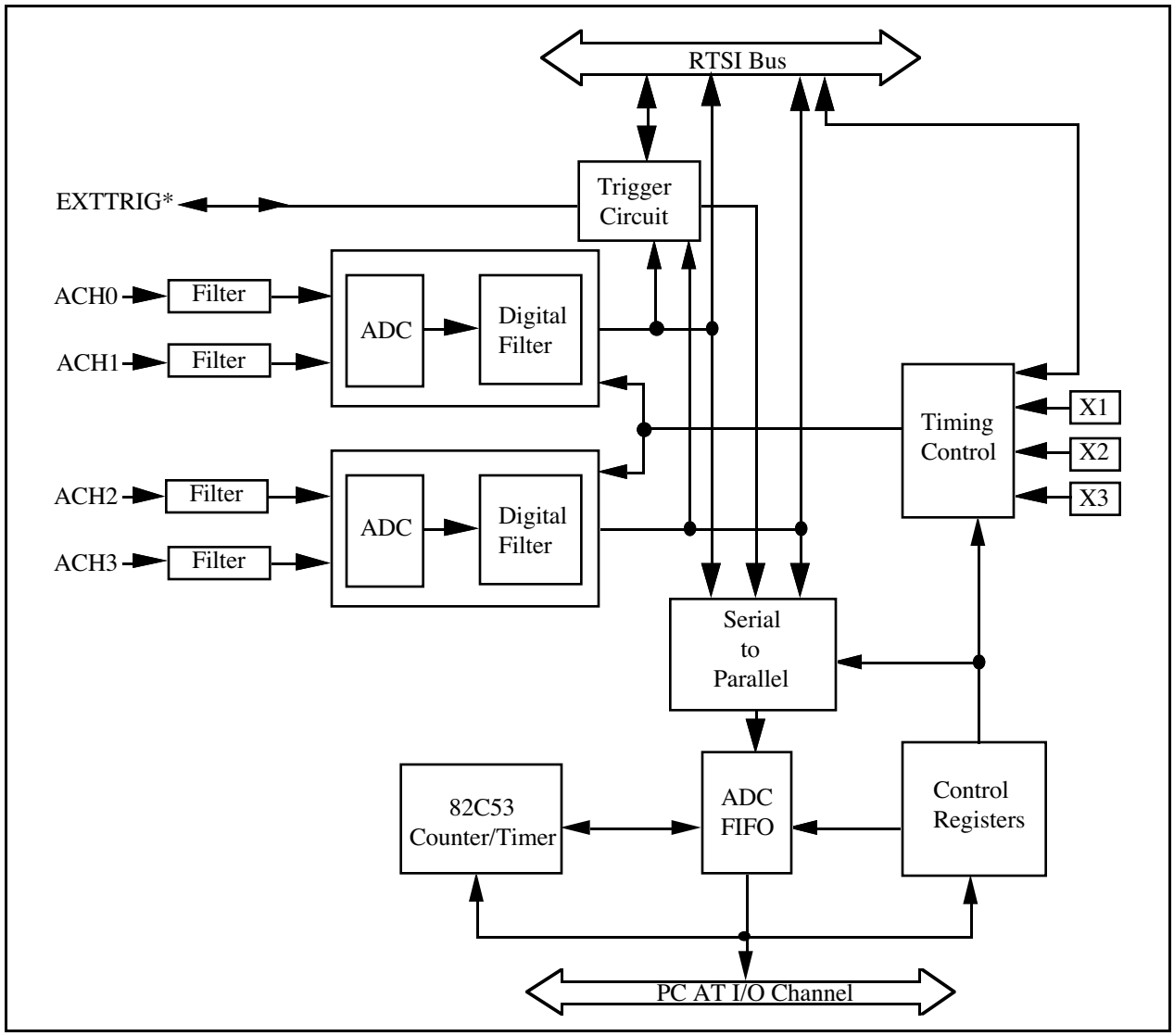


Figure 3-1. AT-A2150 Block Diagram

The following are the major components making up the AT-A2150:

- PC I/O channel interface circuitry
- Analog input circuitry
- Trigger circuitry
- RTSI bus interface circuitry

The internal data and control buses interconnect these components. The theory of operation of each of these components is explained in the remainder of this chapter.

PC I/O Channel Interface Circuitry

The AT-A2150 board is a full-size, 16-bit, PC I/O channel adapter. The PC I/O channel consists of a 24-bit address bus, a 16-bit data bus, a DMA arbitration bus, interrupt lines, and several control and support signals. The components making up the AT-A2150 PC I/O channel interface circuitry are shown in Figure 3-2.

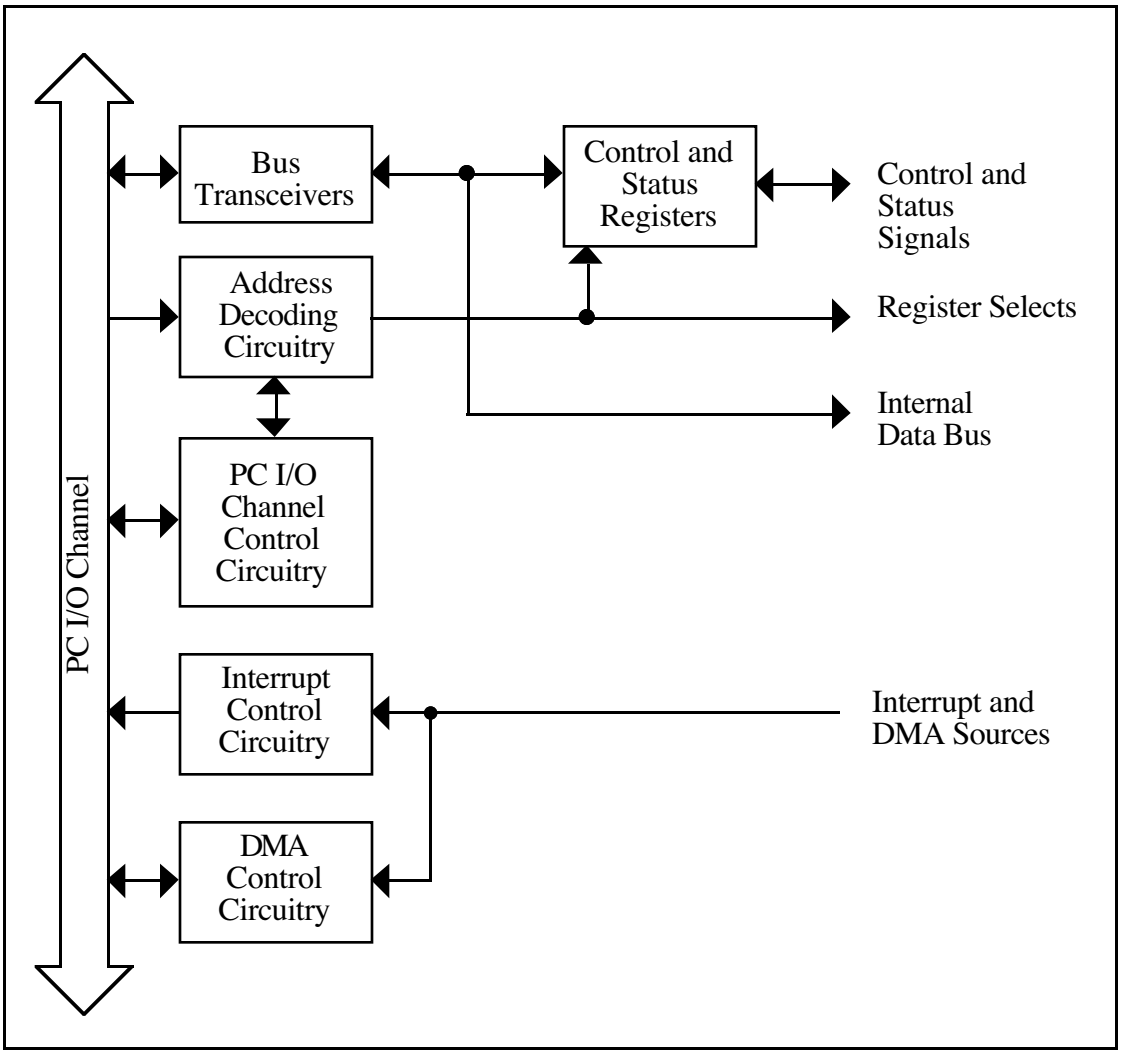


Figure 3-2. PC I/O Channel Interface Circuitry Block Diagram

Address Decoder

The PC I/O channel has 24 address lines; the AT-A2150 uses ten of these lines to decode the board address. Therefore, the board address range is hex 000 to 3FF. Address lines SA5 through SA9 are used to generate the board enable signal. SA0 through SA4 are used to select the onboard registers.

Bus Transceivers

The bus transceivers control the sending and receiving of the data lines to and from the PC I/O channel.

PC I/O Channel Control Circuitry

This circuitry monitors and transmits the PC I/O channel control and support signals. The control signals identify transfers as read or write, memory or I/O, and 8-bit or 16-bit. A support signal is returned to the PC I/O channel from the AT-A2150 to indicate the size of the current data transfer.

Control and Status Registers

The AT-A2150 has several control registers and a status register. Six 16-bit control registers (Analog Input Config, Trigger Config, Level Trigger Data, A/D FIFO Start, A/D FIFO Reset, and Interrupt/DMA Control) are used to program all of the I/O modes of the AT-A2150. The other control registers are used to configure three onboard counters, the RTSI bus trigger lines, the RTSI bus serial data lines, and to clear certain DMA status bits. The 16-bit status register contains DMA and interrupt signal status information. Refer to Chapter 4, *Programming*, for additional information about these registers.

Interrupt Control Circuitry

The interrupt control circuitry routes any enabled interrupts to the selected interrupt request lines. Eleven interrupt request lines are available for use by the AT-A2150: IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, and IRQ15. With the interrupt requests, which are tri-state output signals, the AT-A2150 board can share the interrupt lines with other devices. The AT-A2150 generates interrupts in the following situations:

- When data is available or the FIFO is half full (depending on the FIFO flag selected in the Interrupt/DMA Control Register)
- When a data acquisition operation completes
- When a DMA TC pulse is received

Each one of these interrupts is individually enabled and cleared. See Chapter 4, *Programming*, for additional information about programming with interrupts.

DMA Control Circuitry

The A/D FIFO can be assigned a DMA channel for 16-bit data transfer. This channel has a DMA enable bit, DMAEN. When DMA is enabled and the FIFO has data available to be read, the AT-A2150 sends a DMA request. DMA Channels 5 through 7 of the PC I/O channel are available for such transfers. If running on an EISA machine, DMA Channels 0 through 3 are also available as 16-bit DMA channels.

Analog Input Circuitry

The AT-A2150 has four identical analog input channels, which are grouped in pairs of two. An analog input channel is illustrated in Figure 3-3.

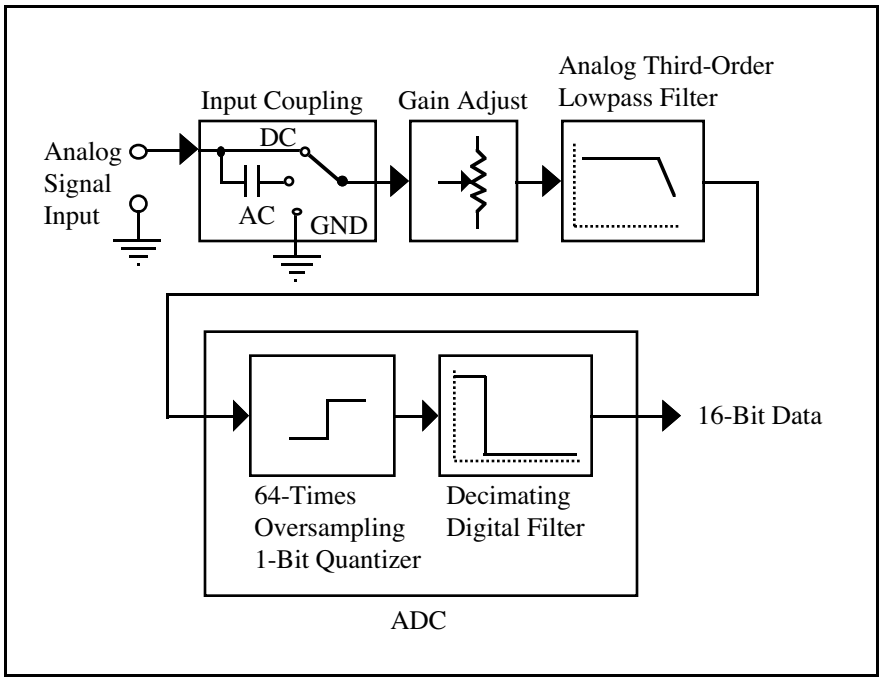


Figure 3-3. Analog Input Channel Block Diagram

The AT-A2150 analog input circuitry simultaneously converts four bandlimited analog signals to 16-bit two's complement digital signals. Both channels have an input range of ±2.828 V, or 2 Vrms full scale. Each of the input channels has input coupling selection, gain adjustment circuitry, an analog antialiasing filter, a 64-times oversampling ADC, and a digital antialiasing filter.

There are two models of the AT-A2150. The AT-A2150C is designed for full audio band measurements and for signal processing applications and is equipped with crystal oscillators for standard digital audio and digital signal processing frequencies. The AT-A2150S is designed for speech and voiceband measurements and comes with crystal oscillators for speech applications.

The AT-A2150 has room for three crystals, which are referred to as *X1*, *X2*, and *X3*. A total of 16 sample rates are derived from these crystals. *X1* is divided by both 768 and 1,152, producing two timebases. *X2* and *X3* are each divided by 384 to produce the other two timebases. These timebases are the fastest sample rates on the board. Each of these timebases is divided by 2, 4, and 8 to produce 12 more sample rates from which to choose. The specific sample rates available are listed in Tables 3-1 and 3-2. F_u is a user-defined sample rate produced from *X3* on the AT-A2150S. F_u can range from 8 kHz to 51.2 kHz, which means that *X3* can range from 3.072 MHz to 19.6608 MHz. Notice that because $F_u/8$ is available, the total range of available sample rates extends down to 1 kHz. Also, because the cutoff frequency of the analog lowpass filter is 31 kHz on the AT-A2150S, significant frequency response rolloff and phase distortion may appear above 10 kHz, thus sample rates above 20 kHz are not recommended for the AT-A2150S. To obtain custom crystals for *X3*, contact National Instruments.

Table 3-1. AT-A2150C Sample Rates

X 1 **36.864 MHz**		***X 2*** **16.9344 MHz**	***X 3*** **19.6608 MHz**
48 kHz	32 kHz	44.1 kHz	51.2 kHz
24 kHz	16 kHz	22.05 kHz	25.6 kHz
12 kHz	8 kHz	11.025 kHz	12.8 kHz
6 kHz	4 kHz	5.5125 kHz	6.4 kHz

Table 3-2. AT-A2150S Sample Rates

X 1 **18.432 MHz**		***X 2*** **7.68 MHz**	***X 3*** **F_u * 384**
24 kHz	16 kHz	20 kHz	F_u
12 kHz	8 kHz	10 kHz	$F_u/2$
6 kHz	4 kHz	5 kHz	$F_u/4$
3 kHz	2 kHz	2.5 kHz	$F_u/8$

Input Coupling

The AT-A2150 has a software-programmed switch that selects whether a capacitor is placed in the signal path. If the switch is set for DC, the capacitor is bypassed, and any DC offset present in the source signal being used is passed to the ADC. The DC configuration is preferred because it places one less component in the signal path and thus has higher fidelity. This configuration is recommended if the signal source has only small amounts of offset voltage (less than ±25 mV) or if the source already has AC (capacitive) coupling. If the source has a significant amount of unwanted offset (or bias voltage), however, you must set the switch for AC coupling to take full advantage of the ±2.828-V input signal range. Using AC coupling results in a drop in the low frequency response of the analog input. The -3 dB cutoff frequency is approximately 8.8 Hz, but the -0.01 dB cutoff frequency, for instance, is considerably higher at approximately 180 Hz. Using AC coupling also results in a broadband gain drop of about 0.009 dB from DC coupling. The input coupling switch is also used to connect the input circuitry to ground instead of to the signal source. This connection is usually made during offset calibration, which is described in Chapter 4, *Programming*, and Chapter 5, *Calibration Procedures*.

Calibration

The AT-A2150 has calibration adjustments. The offset for each channel is nulled (calibrated to zero) digitally. The gain for each channel is calibrated by adjusting a trimpot at the top of the circuit board. This trimpot has an approximately ±3.5% (±0.3 dB) gain adjustment range for each channel. For complete calibration instructions, see Chapter 5, *Calibration Procedures*.

Antialias Filtering

A sampling system (such as an ADC) can only represent signals of limited bandwidth. Specifically, a sampler sampling at rate f_s can only represent signals with a maximum frequency of $f_s/2$. This maximum frequency is known as the *Nyquist frequency*. If a signal is input to the sampling system with frequency components that exceed the Nyquist frequency, then the sampler cannot distinguish parts of this signal from some signals with frequencies less than the Nyquist frequency.

For example, suppose a sampler (such as an ADC) is sampling at 1,000 Hz. If a 400-Hz sine wave is input, then the resulting samples accurately represent a 400-Hz sine wave. However, if a 600-Hz sine wave is input, then the resulting samples again represent a 400-Hz sine wave (this time inaccurately) because this signal exceeds the Nyquist frequency (500 Hz) by 100 Hz. In fact, any sine wave with a frequency greater than 500 Hz that is input is represented incorrectly as a signal between 0 Hz and 500 Hz. The apparent frequency of this sine wave is the absolute value of the difference between the frequency of the input signal and the closest integer multiple of 1,000 Hz (the sampling rate). Therefore, if a 2,325-Hz sine wave is input, its apparent frequency is calculated as follows:

2,325 - (2)(1,000) = 325 Hz

If a 3,975-Hz sine wave is input, its apparent frequency is calculated as follows:

(4)(1,000) - 3,975 = 25 Hz

The process by which these higher frequency signals are modulated by the sampler back into the 0-Hz to 500-Hz baseband is called *aliasing*.

If the signal in the previous example is not a sine wave, the signal may have many components (harmonics) that lie above the Nyquist frequency. If present, these harmonics are erroneously aliased back into the baseband and added to the parts of the signal that are sampled accurately, producing a distorted sampled data set. Only those signals that can be accurately represented should be input to the sampler. All frequency components of such signals lie below the Nyquist frequency. To make sure that only those signals go into the sampler, a lowpass filter is applied to signals before they reach the sampler. The AT-A2150 has complete antialiasing filters.

Included on the AT-A2150 are two stages of antialias filtering in each input channel–an analog filter and a digital filter. The analog filter is a third-order lowpass Butterworth filter. On the AT-A2150C, it has a cutoff of 80 kHz and a rejection of greater than 90 dB at 3 MHz. On the AT-A2150S, the analog filter has a cutoff of 31 kHz and a rejection of greater than 90 dB at 1 MHz. Because its cutoff is significantly higher than the data sample rate, the analog filter has an extremely flat frequency response in the bandwidth of interest and has very little phase error.

The analog filter precedes the analog sampler, which operates at 64 times the selected sample rate (3.072 MHz in the case of a 48-kHz sample rate) and is actually a 1-bit ADC. The 1-bit, 64-times oversampled data the analog sampler produces is passed on to a digital antialiasing filter that is built into the ADC chip. This filter also has extremely flat frequency response and zero phase error, but its cutoff (about 0.45 times the sample rate) is extremely sharp, so the rejection at and above the Nyquist frequency (0.5 times the sample rate) is greater than 85 dB. The output stage of the digital filter resamples the higher frequency data stream at the output data rate, producing 16-bit digital samples.

With the AT-A2150 filters, you have the complete antialiasing protection needed to sample signals accurately. The digital filter in each channel passes only signal components with frequencies that lie below the Nyquist frequency or within one Nyquist bandwidth of multiples of 64 times the sample rate. The analog filter in each channel rejects possible aliases (mostly noise) from signals that lie near these multiples. The frequency response of the AT-A2150 input circuitry is shown in Figure 3-4 and Figure 3-5.

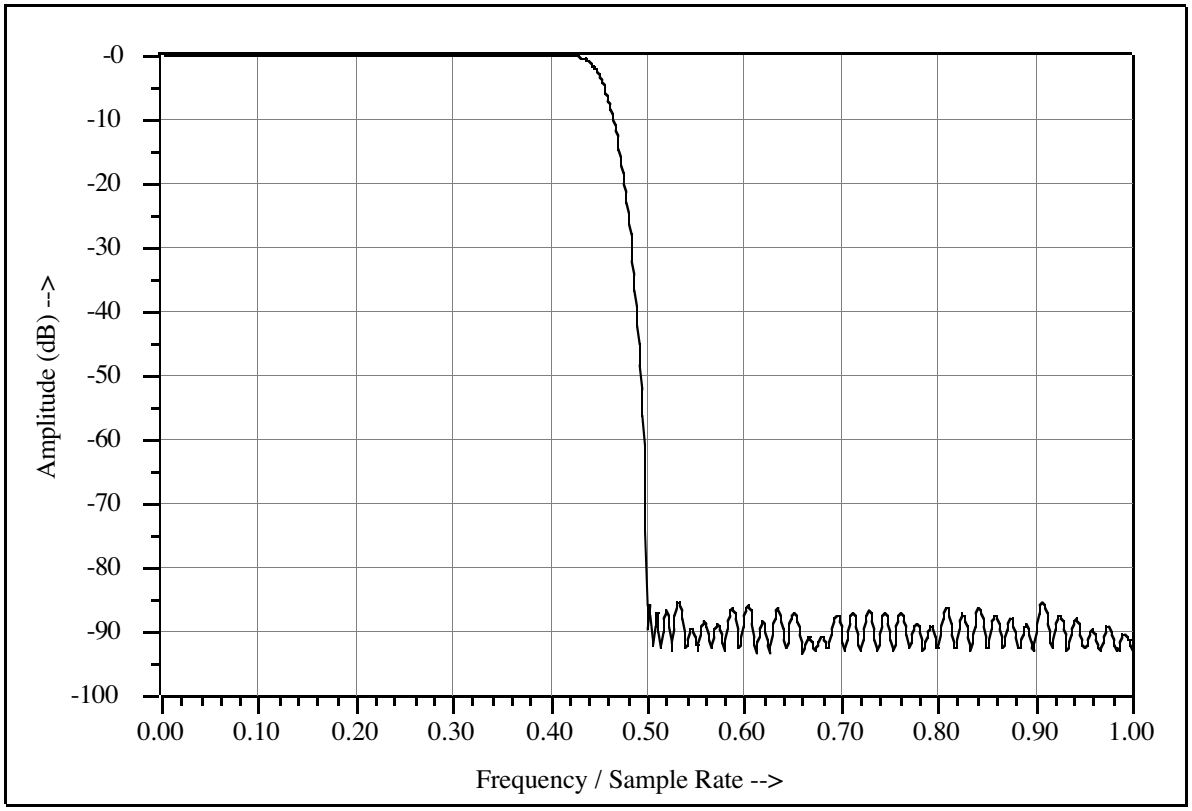


Figure 3-4. Input Frequency Response

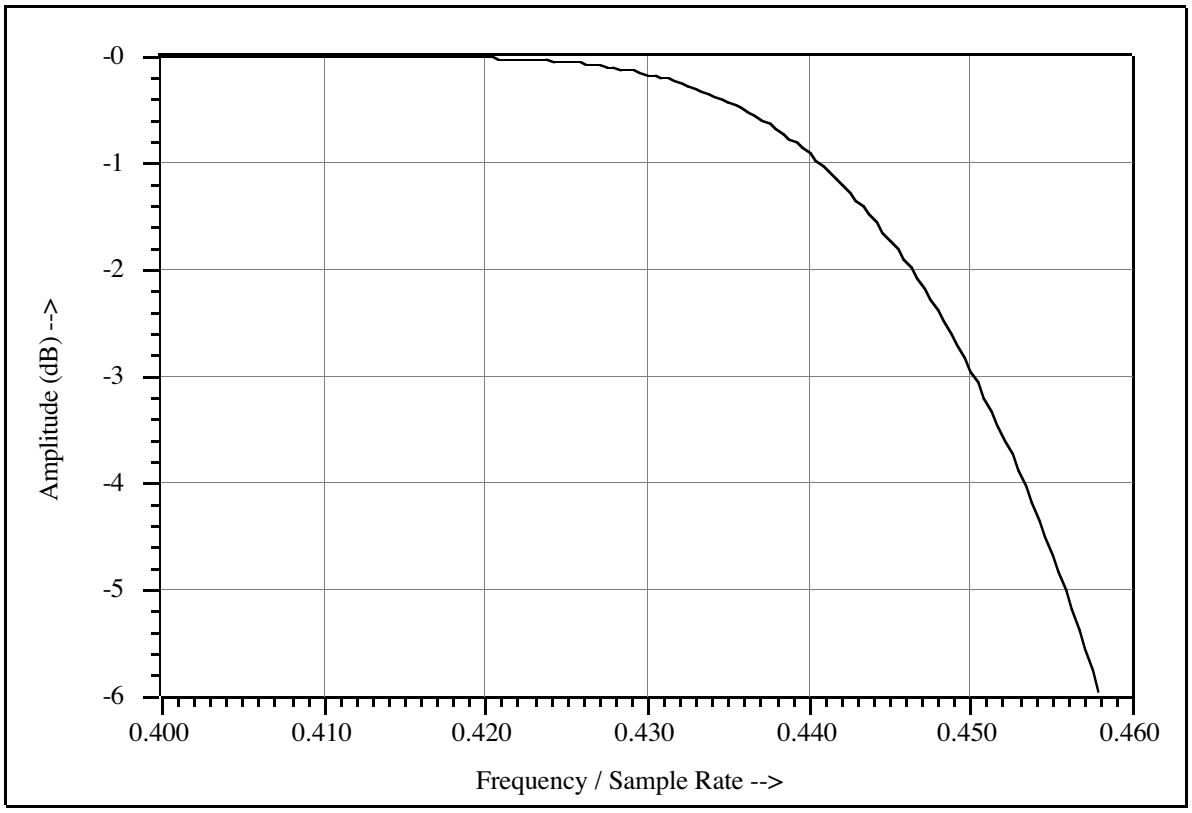


Figure 3-5. Input Frequency Response Near the Cutoff

Because the ADC samples at 64 times the data rate, frequency components above 32 times the data rates can alias. The digital filter rejects most of the frequency range over which this aliasing can occur. However, the filter can do nothing about components that lie close to 64 times the data rate, 128 times the data rate, and so on, because it cannot distinguish these components from components in the baseband (0 Hz to the Nyquist frequency). If, for instance, the sample rate is 48 kHz and a signal component lies within 24 kHz of 64 ∗ 48 kHz or 3.072 MHz, then this signal is aliased into the passband region of the digital filter and is not attenuated. The purpose of the analog filter is to remove these higher frequency components near multiples of the oversampling rate before they get to the sampler and the digital filter. While the frequency response of the digital filter scales in proportion to the sample rate, the frequency response of the analog filter remains fixed. The response of the filter is optimized to give the most high-frequency alias rejection while having the flattest in-band frequency response. Because this filter is third order, its rolloff is rather slow. This means that while the filter has good alias rejection for high sample rates, it does not have as good rejection at lower sample rates. The data sample rates, oversample rates, and analog filter rejection at the oversample rates are tabulated in Tables 3-3 and 3-4. The rejections listed in these tables apply only near the oversample frequency for the given sample rate. For frequencies not near multiples of the oversample rate, the rejection is better than -85 dB.

Table 3-3. AT-A2150C Alias Rejection at the Oversample Rate

Data Sample Rate	Oversample Rate	Alias Rejection
51.2 kHz	3.2768 MHz	-97 dB
48 kHz	3.072 MHz	-95 dB
44.1 kHz	2.8224 MHz	-93 dB
32 kHz	2.048 MHz	-84 dB
25.6 kHz	1.6384 MHz	-79 dB
24 kHz	1.536 MHz	-77 dB
22.05 kHz	1.4112 MHz	-75 dB
16 kHz	1.024 MHz	-66 dB
12.8 kHz	0.8192 MHz	-60 dB
12 kHz	0.768 MHz	-59 dB
11.025 kHz	0.7056 MHz	-57 dB
8 kHz	0.512 MHz	-48 dB
6.4 kHz	0.4096 MHz	-42 dB
6 kHz	0.384 MHz	-41 dB
5.5125 kHz	0.3528 MHz	-39 dB
4 kHz	0.256 MHz	-30 dB

Table 3-4. AT-A2150S Alias Rejection at the Oversample Rate

Data Sample Rate	Oversample Rate	Alias Rejection
24 kHz	1.536 MHz	-103 dB
20 kHz	1.280 MHz	-98 dB
16 kHz	1.024 MHz	-93 dB
12 kHz	0.768 MHz	-85 dB
10 kHz	0.64 MHz	-80 dB
8 kHz	0.512 MHz	-75 dB
6 kHz	0.384 MHz	-67 dB
5 kHz	0.32 MHz	-62 dB
4 kHz	0.256 MHz	-57 dB
3 kHz	0.192 MHz	-49 dB
2.5 kHz	0.16 MHz	-44 dB
2 kHz	0.128 MHz	-38 dB

There is a form of aliasing that no filter can prevent. When a waveform exceeds the range of the ADC, it is said to be *clipped*. When clipping occurs, the ADC assumes the closest value in its digital range to the actual value of the signal, which is always either -32,768 or +32,767. Clipping nearly always results in an abrupt change in the slope of the signal and causes the corrupted digital data to have high-frequency energy. This energy is spread throughout the frequency spectrum, and because the clipping occurs *after* the antialiasing filters, the energy is aliased (chaotically) back into the baseband. The remedy for this problem is simple: don't allow the signal to exceed the 2-Vrms range. Figures 3-6 and 3-7 show the spectrums of 2.1 Vrms and 2.0 Vrms, respectively,

2.962 kHz sine waves digitized at 48 kHz. The signal-to-THD+noise ratio is 35 dB for the clipped waveform and 92 dB for the properly ranged waveform. Notice that aliases of all the harmonics due to clipping appear in Figure 3-6.

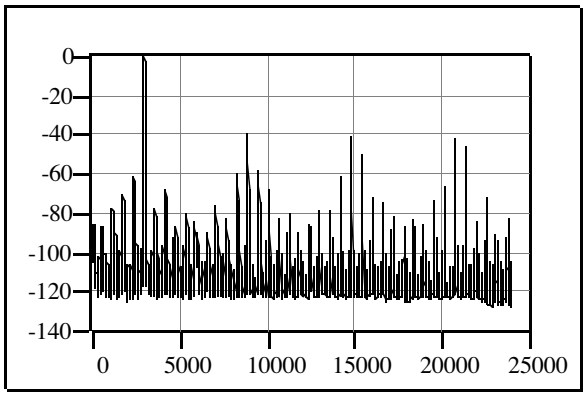


Figure 3-6. Clipped Signal

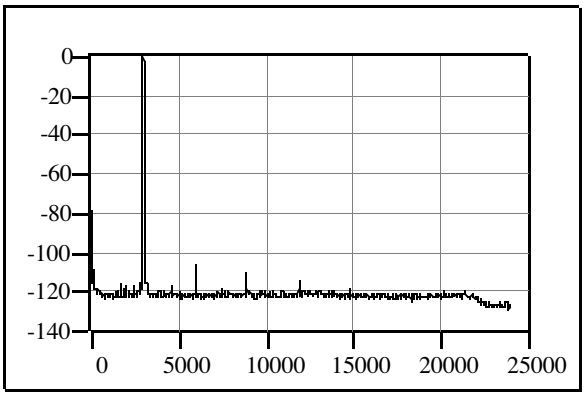


Figure 3-7. Proper Signal

The ADC

The AT-A2150 ADCs use a method of A/D conversion known as delta-sigma modulation. If the data rate is 48 kHz, each ADC actually samples its input signal at 3 MHz (64 times the data rate) and produces 1-bit samples that are applied to the digital filter. This filter then expands the data to 16 bits, rejects signal components greater than 24 kHz (the Nyquist frequency), and resamples the data at the more conventional rate of 48 kHz. Although a 1-bit quantizer introduces a large amount of quantization error to the signal, the 1-bit, 3-MHz samples from the ADC carry all the information used to produce 16-bit samples at 48 kHz. The delta-sigma ADC achieves this conversion from high speed to high resolution by adding a large amount of random noise to the signal so that the resulting quantization noise, although large, is restricted to frequencies above 24 kHz. This noise is uncorrelated with the input signal and is almost completely rejected by the digital filter. The resulting output of the filter is a bandlimited signal with a dynamic range of over 93 dB. One of the advantages of using a delta-sigma ADC is that it uses a 1-bit DAC as an internal reference, while most 16-bit ADCs use 16-bit resistor-network DACs or capacitor-network DACs. As a result, the delta-sigma ADC is free from the kind of differential nonlinearity (DNL) that is inherent in most high-resolution ADCs. This lack of DNL is especially beneficial when the ADC is converting low-level signals, where noise and distortion are directly affected by converter DNL.

Coding

The ADCs on the AT-A2150 produce two's complement 16-bit binary data. When 0 V is input, the ADC returns the code 0000 hex, plus or minus some noise. When +2.828 V is input, the ADC returns the code 7FFF hex (approximately), and when -2.828 V is input, the ADC returns the code 8000 hex (approximately). The full-scale range of the input circuitry is 2 Vrms (5.657 V peak-to-peak).

Data Transfer

The AT-A2150 uses a FIFO for storing the A/D conversion data. The A/D FIFO is 16 bits wide and 256 words deep. The A/D FIFO serves as a buffer to the ADC and can collect up to 256 16-bit A/D conversion values. With this capability, software or DMA latency can range up to 64 times the sample interval for four-channel data acquisition, 128 times the sample interval for two-channel acquisition, or 256 times the sample interval for single-channel acquisition.

The A/D FIFO generates a signal that indicates when the FIFO contains A/D conversion data. The state of this signal can be read from the AT-A2150 Status Register. This signal can also be used to generate a DMA request signal or an interrupt. The A/D FIFO also generates a signal that indicates when the FIFO is at least half full. The state of this signal can also be read in the AT-A2150 Status Register. An interrupt can be generated by this signal instead of by the data available (at least one word) flag. The FlagSel bit in the Interrupt/DMA Control Register determines which signal generates this interrupt. See Chapter 4, *Programming*, for additional information about programming with interrupts.

The A/D conversion data can also be sent serially over the RTSI bus to other National Instruments boards such as the AT-DSP2200 digital signal processing board, for further processing. Data transfer over the RTSI bus is completely independent of the AT bus.

Trigger Circuitry

The AT-A2150 can be triggered to start a data acquisition sequence from one of four possible sources. These sources are listed as follows:

- Software trigger
- TTL-level trigger from an external source applied at EXTTRIG* on the I/O connector
- Trigger generated from the internal level-and-slope detection trigger circuit
- Trigger received over the RTSI bus from another AT Series board

In addition to these triggering capabilities, the AT-A2150 can be programmed to drive the EXTTRIG* signal on the I/O connector with the trigger generated from the internal level-and-slope detection circuit or with the trigger received over the RTSI bus.

The signal source for the level-and-slope detection circuit is programmable and can be any of the four analog input channels. The level-and-slope detection circuit is implemented digitally and contains a programmable hysteresis window. The hysteresis window defines the sensitivity of the level-and-slope detection circuit. The digital output words from the ADC must cross the upper and lower hysteresis window thresholds, V_U and V_L, to activate the level-and-slope detection circuit. The digital value of the analog signal must cross the lower threshold followed by the upper threshold for positive-slope triggering. For negative-slope triggering, the digital value of the analog signal must cross the upper threshold followed by the lower threshold. Both hysteresis window thresholds correspond to the eight most significant bits of the 16-bit conversion value from the selected analog input channel. Therefore, the resolution of the level-and-slope detection circuit is eight bits. Figure 3-8 shows a plot of the transfer function of the level-and-slope trigger circuit for positive-slope triggering. Because HWTrig* is a negative logic signal, a trigger is generated on a high-to-low transition of HWTrig*.

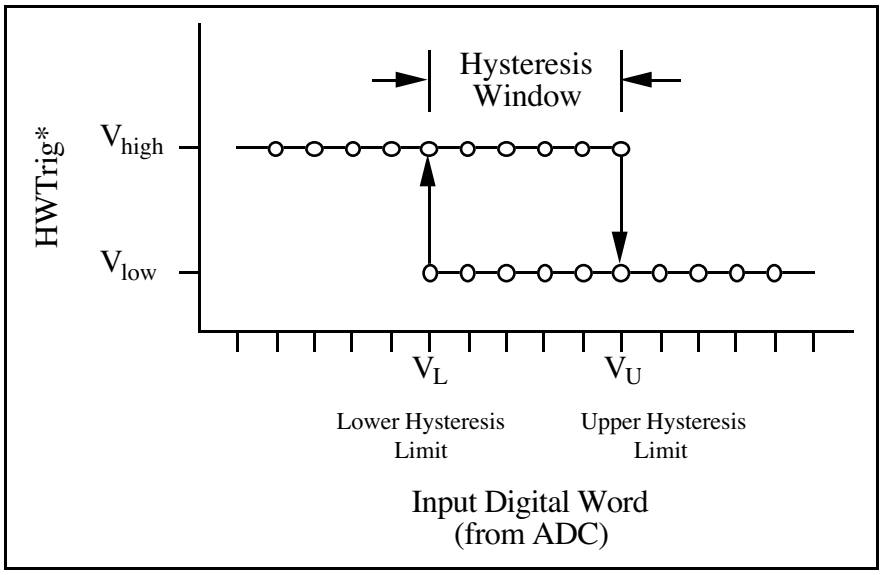


Figure 3-8. Transfer Function of Level-and-Slope Trigger Circuit

RTSI Bus Interface Circuitry

The AT-A2150 is interfaced to the National Instruments RTSI bus. The RTSI bus has a clock line, seven trigger lines, and four serial data links. All National Instruments AT Series data acquisition boards with RTSI bus connectors can be wired together inside the PC to share these signals. A block diagram of the RTSI bus interface circuitry is shown in Figure 3-9.

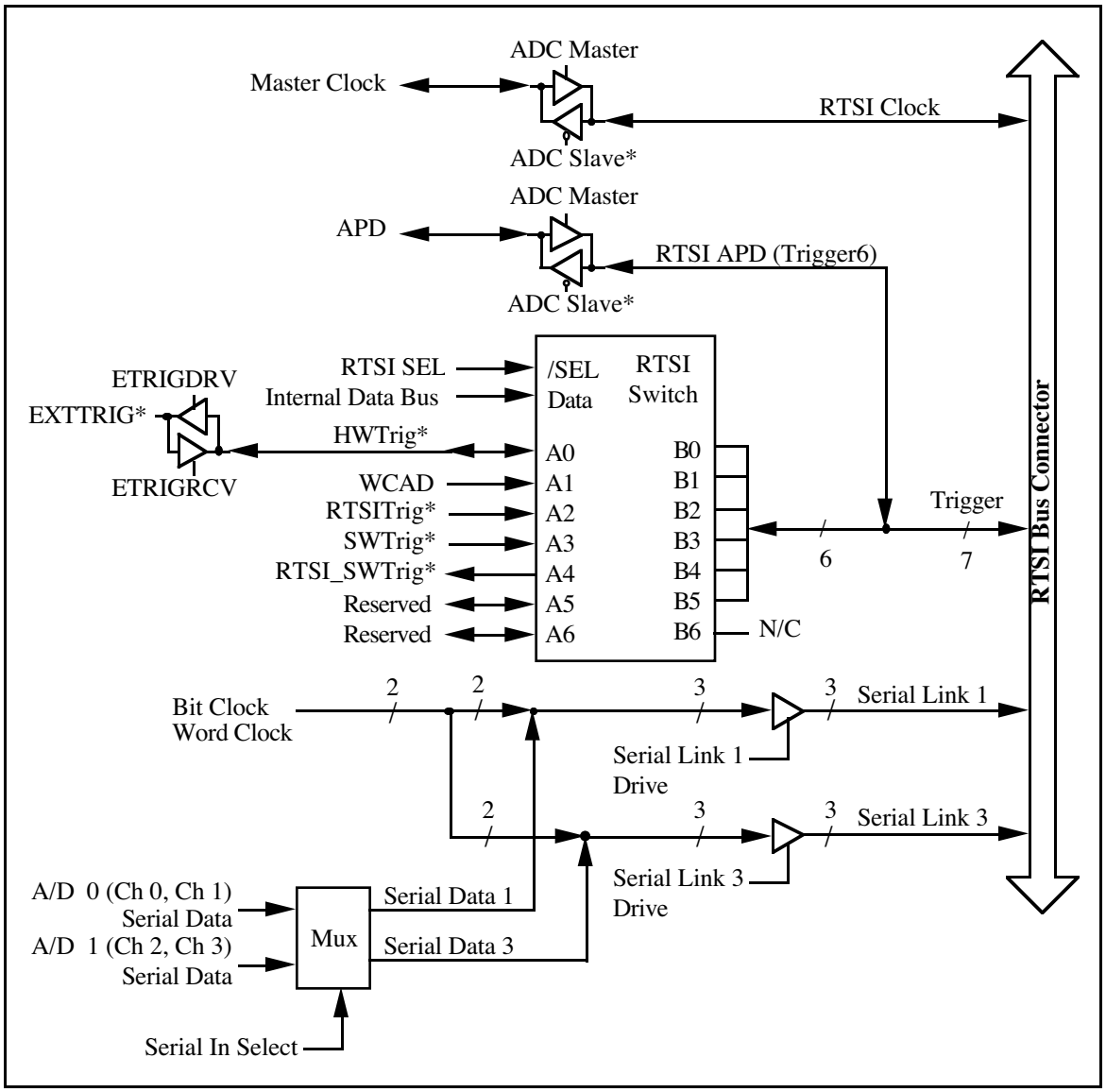


Figure 3-9. RTSI Bus Interface Circuitry Block Diagram

Figure 3-9 shows the RTSI clock drivers, the RTSI switch, and the two serial links. These drivers and the RTSI switch route AT-A2150 signals to and from the RTSI Bus.

The RTSI switch is a National Instruments custom-integrated circuit that acts as a 7x7 crossbar switch. Pins B<5..0> are connected to the six RTSI bus trigger lines. The seventh line in the RTSI bus trigger lines, B6 (Trigger6), is used on the AT-A2150 in conjunction with another signal for multiple-board sampling clock synchronization. Pins A<2..0> are connected to three signals on the board. Other pins on the A side are reserved. The RTSI switch can drive any of the signals at pins A<2..0> onto any one or more of the six RTSI bus trigger lines and can drive any of the six trigger line signals onto any one or more of the pins A<6..0>. With this capability, a completely flexible signal interconnection scheme is possible for any AT Series board sharing the RTSI bus. The RTSI switch is programmed via its select and data inputs.

On the AT-A2150 board, five signals are connected to pins A<4..0> of the RTSI switch. The signal HWTrig* is the final hardware trigger used for pretrigger, posttrigger, and delayed trigger modes and can originate from the EXTTRIG* signal receive circuitry, from the RTSI switch, or from the level-and-slope detection circuit. The signal labeled WCAD is the A/D sampling clock signal. RTSITrig* is a strobe generated by the AT bus interface and is used to test the hardware trigger functionality of the AT-A2150. RTSITrig* is also used to send a common hardware trigger generated by a single software strobe to multiple AT-A2150 boards connected via the RTSI bus. SWTrig* is a strobe generated by the AT bus interface when the A/D FIFO Start Register is written. The signal RTSI_SWTrig* can be received from the RTSI switch and effects the board in the same way as writing to the A/D FIFO Start Register in the various trigger modes. In this way one board can send a software trigger on SWTrig* and other boards can receive the trigger on RTSI_SWTrig* in order to synchronize triggering of multiple AT-A2150 boards connected via the RTSI bus.

In addition to the RTSI switch, the AT-A2150 can use a serial data link to transmit data from the AT-A2150 to other AT Series boards sharing the RTSI bus, such as the AT-DSP2200. For more information on the RTSI switch and the serial data link, see Chapter 4, *Programming*.

Chapter 4
Programming

This chapter discusses programming the AT-A2150 and describes the AT-A2150 control and status registers in detail. This chapter includes the AT-A2150 register address map, a detailed description of each register, and a functional programming description.

Note: If you plan to use a programming software package such as NI-DAQ or LabWindows with your AT-A2150 board, you do not need to read this chapter.

Register Map

The register map for the AT-A2150 is shown in Table 4-1. This table gives the register name, the register address, the type of the register (read-only, write-only, or read-and-write), and the size of the register in bits.

Table 4-1. AT-A2150 Register Map

Register Name (Hex)	Offset Address	Type	Size
Analog Input Register Group			
Analog Input Config Register	00	Write-only	16-bit
Trigger Config Register	02	Write-only	16-bit
Level Trigger Data Register	04	Write-only	16-bit
A/D FIFO Start Register	06	Write-only	16-bit
A/D FIFO Reset Register	08	Write-only	16-bit
A/D FIFO Data Register	10	Read-only	16-bit
Interrupt/DMA Register Group			
Status Register	12	Read-only	16-bit
Interrupt/DMA Control Register	12	Write-only	16-bit
DMA TC Interrupt Clear Register	0E	Write-only	16-bit
82C53 Counter/Timer Register Group			
Counter 0 Data Register	14	Read-and-write	8-bit
Counter 1 Data Register	15	Read-and-write	8-bit
Counter 2 Data Register	16	Read-and-write	8-bit
Counter Mode Register	17	Write-only	8-bit
RTSI Bus Register Group			
RTSI Switch Shift Register	18	Write-only	8-bit
RTSI Switch Strobe Register	19	Write-only	8-bit
Serial Data Link Control Register	1A	Write-only	16-bit
RTSI Trigger Register	0A	Write-only	16-bit

Register Sizes

Two different transfer sizes can be used for read-and-write operations with the PC: byte (8-bit), and word (16-bit). Table 4-1 shows the size of each AT-A2150 register. For example, reading the Status Register requires a 16-bit (word) read operation at the selected address, whereas writing to the RTSI Switch Shift Register requires an 8-bit (byte) write operation at the selected address.

Register Description

Table 4-1 divides the AT-A2150 registers into four register groups. A bit description of each of the registers making up these groups is included later in this chapter.

The Analog Input Register Group is used to control and read data from the two 16-bit, two-channel ADCs. The Interrupt/DMA Register Group can be used to enable the interrupt and/or DMA facility on the AT-A2150 and to obtain the status of the data acquisition process, the A/D offset calibration, and the DMA TC. The 82C53 Counter/Timer Register Group consists of four registers for the onboard 82C53 Counter/Timer integrated circuit. The registers in the RTSI Bus Register Group control RTSI bus signals.

Register Description Format

The remainder of the register description sections discuss each of the AT-A2150 registers in the order shown in Table 4-1. Each register group is introduced, followed by a detailed bit description of each register. The individual register description gives the address, type, word size, and bit map of the register, followed by a description of each bit.

The register bit map shows a diagram of the register with the MSB (bit 15 for a 16-bit register, bit 7 for an 8-bit register) shown on the left, and the LSB (bit 0) shown on the right. A rectangle is used to represent each bit. Each bit is labeled with a name inside its rectangle. An asterisk (*) after the bit name indicates that the bit is inverted (negative logic).

In many of the registers, several bits are labeled with a 0, indicating *reserved bits*. When a register is written, these bits must be set to zero.

In many of the registers, one or more bits are labeled with Xs, indicating *don't care* bits. When a register is read, these bits may appear set or cleared but should be ignored because they have no significance. When a register is written to, setting or clearing these bit locations has no effect on the AT-A2150 hardware.

The bit map field for some write-only registers states *not applicable, no bits used.* Writing to one of these registers causes some onboard event to occur, such as clearing the A/D FIFO circuitry. The data is ignored when writing to these registers; therefore, any bit pattern suffices.

Analog Input Register Group

The six registers making up the Analog Input Register Group control the analog input circuitry and are used for reading from the A/D FIFO. The Analog Input Config Register selects the input channel(s) to be read, the sampling rate, input coupling, and controls the calibration cycle. The Trigger Config Register controls the various trigger circuitry. The Level Trigger Data Register is used to specify the trigger level used for level triggering. Writing to the A/D FIFO Start Register acts as a software trigger to the A/D conversion storage circuitry. Writing to the A/D FIFO Reset Register resets the error bit in the Status Register and empties the A/D FIFO. Reading the A/D FIFO Data Register returns stored A/D conversion results.

Bit descriptions for the registers in the Analog Input Register Group are given on the following pages.

The Analog Input Config Register controls the input channel to be read, the sampling rate to be used, and input coupling (AC or DC).

Address: Base address + 00 (hex)

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
0	0	TEST	DPD	APD	AC/DC*1	AC/DC*0	CAL*1

7	6	5	4	3	2	1	0
CAL*0	CLKAD3	CLKAD2	CLKAD1	CLKAD0	ACH2	ACH1	ACH0

Bit	Name	Description
15-14	0	Reserved bits. These bits must be set to zero.
13	TEST	This bit places the ADC interface circuitry into a special test mode when it is high. This bit should be low for normal operation of the board.
12	DPD	Digital Power Down. If this bit is set high, the digital section of the ADC goes into power-down mode. Upon returning this bit to low, the ADC starts an offset calibration cycle. The calibration cycle takes 4,096 sampling periods.
11	APD	Analog Power Down. If this bit is set high, the analog section of the ADC goes into power-down mode. A high-to-low transition on this bit resets and synchronizes the ADC clock circuitry. This bit should first be set high and then set low once after startup.
10	AC/DC*1	This bit configures the analog input coupling for the second two input channels. If this bit is set high, the analog input on the second two channels (ACH2 and ACH3) is AC coupled. If this bit is set low, the analog input on the second two channels is DC coupled.
9	AC/DC*0	This bit configures the analog input coupling for the first two input channels. If this bit is set high, the analog input on the first two channels (ACH0 and ACH1) is AC coupled. If this bit is set low, the analog input on the first two channels is DC coupled.

Bit	Name	Description (continued)
8	CAL*1	This bit controls the input multiplexer to the second ADC. If this bit is set low, the inputs to the second ADC are grounded. If this bit is set high, the analog input signals ACH2 and ACH3 appear at the analog input to the second ADC. This bit is useful in offset calibration.
7	CAL*0	This bit controls the input multiplexer to the first ADC. If this bit is set low, the inputs to the first ADC are grounded. If this bit is set high, the analog input signals ACH0 and ACH1 appear at the analog input to the first ADC. This bit is useful in offset calibration.
6-3	CLKAD<3..0>	These four bits and the three crystal oscillators on the AT-A2150 control the sampling rate. Different versions of the AT-A2150 have different sets of crystal oscillators. The available sampling rates and the corresponding CLKAD bit patterns for the AT-A2150C are shown in the following table.

CLKAD<3..0>	Sampling Rate (kHz)
0000	32
0001	44.1
0010	48
0011	51.2
0100	16
0101	22.05
0110	24
0111	25.6
1000	8
1001	11.025
1010	12
1011	12.8
1100	4
1101	5.5125
1110	6
1111	6.4

Refer to Chapter 3, *Theory of Operation*, for more information about alias rejection near the oversampling rate for lower sampling rates.

Bit **Name** **Description (continued)**

The available sampling rates and the corresponding CLKAD bit patterns for the AT-A2150S are shown in the following table.

CLKAD<3..0>	Sampling Rate (kHz)
0000	16
0001	20
0010	24
0011	Fu
0100	8
0101	10
0110	12
0111	Fu/2
1000	4
1001	5
1010	6
1011	Fu/4
1100	2
1101	2.5
1110	3
1111	Fu/8

Fu refers to the sampling rate obtained by installing a user-supplied crystal oscillator in the empty slot on the AT-A2150S. Fu is related to the crystal frequency by the following expression:

$$Fu = \frac{X}{384}$$ where X is the crystal oscillator frequency

X can range from 3.072 MHz to 19.6608 MHz. Refer to Chapter 3, *Theory of Operation*, for more information about alias rejection near the oversampling rate for lower sampling rates.

2-0 ACH<2..0> These bits control which analog channel data is stored in the input FIFO. The following table shows the channels that correspond to each bit.

ACH<3..0>	Selected Channel
000	None
001	ACH0 through ACH3
010	ACH0 and ACH1
011	ACH2 and ACH3
100	ACH0
101	ACH1
110	ACH2
111	ACH3

Trigger Config Register

The Trigger Config Register controls the level-and-slope trigger circuitry control bits.

Address: Base address + 02 (hex)

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
0	0	0	0	TestData	TestClk	LTrigCh1	LTrigCh0

7	6	5	4	3	2	1	0
LTrigSlope	CLK0	Count32/16*	ExtTrigRcv	ExtTrigDrv	LTrigEn	TrigMode1	TrigMode0

Bit	Name	Description
15-12	0	Reserved bits. These bits must be set to zero.
11	TestData	This bit is the serial data for the ADC interface when bit 13, TEST, in the Analog Input Config Register is high. This bit is a don't care bit when TEST is low.
10	TestClk	This bit is the serial bit clock for the ADC interface when bit 13, TEST, in the Analog Input Config Register is high. This bit is a don't care bit when TEST is low.
9-8	LTrigCh<1..0>	These bits select the analog input channel used for level triggering.
7	LTrigSlope	This bit selects the slope used for level triggering. Low (0) selects positive slope. High (1) selects negative slope.
6	CLK0	This bit can be toggled to send clock pulses to sample Counter 0. Clocking sample Counter 0 is useful in testing the sample counter. This bit should be kept clear in all other write operations to the Trigger Config Register.
5	Count32/16*	This bit selects the sample counter size. If Count32/16* is set high, a 32-bit sample counter size is selected; that is, two 16-bit counters (Counters 0 and 1) are used for sample counting. In this mode, Counter 1 terminates the data acquisition. If Count32/16* is set low, a 16-bit sample counter size is selected; that is, only a single 16-bit counter (Counter 0) is used for sample counting. In this mode, Counter 0 terminates the data acquisition.
4	ExtTrigRcv	This bit controls whether the external digital trigger EXTTRIG* drives the internal trigger circuitry. If ExtTrigRcv is set high, the TTL digital signal on EXTTRIG* is applied to the internal triggering logic. If ExtTrigRcv is low, the input driver for EXTTRIG* is tri-stated.

Bit **Name** **Description (continued)**

3 ExtTrigDrv

This bit controls whether the external digital trigger EXTTRIG* is driven from the internal trigger circuitry. If ExtTrigDrv is set high, EXTTRIG* at the I/O connector becomes a digital output. If ExtTrigDrv is set low, the output driver for EXTTRIG* is tri-stated.

The following table lists the possible combinations and their effect on the I/O connector signal EXTTRIG*.

ExtTrigRcv	ExtTrigDrv	EXTTRIG*
0	0	EXTTRIG* is disconnected from the internal trigger logic.
1	0	Digital input. EXTTRIG* is used as the digital trigger source.
0	1	Digital output. EXTTRIG* reflects the state of the internal trigger.
1	1	Illegal. This combination should not be used.

2 LTrigEn

This bit controls whether the level detection circuitry drives the internal trigger. If set high, the level detection circuitry drives the internal trigger and is enabled. If set low, the level detection circuitry does not drive the internal trigger and is disabled.

1-0 TrigMode<1..0>

These bits control the various trigger modes: no hardware trigger, pretrigger, posttrigger, and delay trigger. The following table lists the type of triggering that corresponds to each mode.

TrigMode<1..0>	Selected Triggering
00	No hardware trigger
01	Pretrigger
10	Posttrigger
11	Delay trigger

In pretrigger mode, a hardware trigger terminates an ongoing data acquisition sequence. The termination can be programmed to occur at a given number of samples after the hardware trigger. Thus, data before and after the trigger can be captured. For more information on programming the sample counter, see the section *Programming Multiple A/D Conversions* later in this chapter.

Bit	Name	Description (continued)
1-0	TrigMode<1..0>	In posttrigger mode, data acquisition is terminated after a programmed number of samples have been acquired because a trigger (hardware or software) has occurred. For more information on programming the sample counter, see the section *Programming Multiple A/D Conversions* later in this chapter. In delay trigger mode, data acquisition is started after a programmable delay after the trigger (hardware or software). The delayed trigger data acquisition mode programming is described in *Programming Multiple A/D Conversions* later in this chapter.

Level Trigger Data Register

The Level Trigger Data Register controls the level-and-slope trigger circuitry detection levels.

Address: Base address + 04 (hex)

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
Level H7	Level H6	Level H5	Level H4	Level H3	Level H2	Level H1	Level H0

7	6	5	4	3	2	1	0
Level L7	Level L6	Level L5	Level L4	Level L3	Level L2	Level L1	Level L0

Bit	Name	Description
15-8	Level H<7..0>	These bits represent the upper value used for level triggering. (They constitute the 8 MSBs of a 16-bit word in which the 8 LSBs are not used by the trigger circuitry.)
7-0	Level L<7..0>	These bits represent the lower value used for level triggering. (They constitute the 8 MSBs of a 16-bit word in which the 8 LSBs are not used by the trigger circuitry.)

A/D FIFO Start Register

Writing to the A/D FIFO Start Register initiates buffering of the A/D conversion data by the A/D FIFOs.

Address: Base address + 06 (hex)

Type: Write-only

Word Size: 16-bit

Bit Map: Not applicable, no bits used

Note: Buffering of the A/D conversion data by the A/D FIFOs can be initiated in one of three ways: when the A/D FIFO Start Register is written to; when a falling edge is detected on the internal hardware trigger signal, HWTrig*; or when a falling edge is detected on the internal software trigger signal, RTSI_SWTrig*. The internal trigger signal is connected to pin A0 on the RTSI bus switch and can also be available on the I/O connector. See the Trigger Config Register for more information on driving and receiving the EXTTRIG* signal. Writing to this register generates a strobe on the SWTrig* line which is connected to pin A3 on the RTSI bus switch and can also be available on the I/O connector.

A/D FIFO Reset Register

Writing to the A/D FIFO Reset Register empties the A/D FIFO and resets the error flags associated with the A/D FIFO. The following events occur:

- The A/D FIFO is emptied.
- The overflow flag is cleared.
- Any pending A/D FIFO interrupt is cleared.
- Any pending A/D FIFO DMA request is unasserted.
- The trigger circuitry is reset.

Address: Base address + 08 (hex)

Type: Write-only

Word Size: 16-bit

Bit Map: Not applicable, no bits used

A/D FIFO Data Register

Reading the A/D FIFO Data Register returns the next A/D conversion value stored in the A/D FIFO. Whenever the A/D FIFO Data Register is read, the value read is removed from the A/D FIFO, thereby freeing space for another A/D conversion value to be stored. A value is stored in the A/D FIFO Data Register by the ADC whenever an A/D conversion is completed. If one-channel data buffering mode is selected in the Analog Input Config Register (ACH<2..0> = 100, 101, 110, or 111), each 16-bit word read from the A/D FIFO Data Register contains conversion data from that one channel. If two-channel data buffering mode is selected in the Analog Input Config Register (ACH<2..0> = 010 or 011), data from both channels is read in two 16-bit word read operations. If four-channel data buffering mode is selected in the Analog Input Config Register (ACH<2..0> = 001), data from all four channels is read in four 16-bit word read operations.

The A/D FIFO is emptied when all the values it contains are read. The Status Register should be read before the A/D FIFO Register is read. If the A/D FIFO contains at least one A/D conversion value, the DataAvail bit is set in the Status Register and the A/D FIFO Register can be read to retrieve a value. If the DataAvail bit is cleared, the A/D FIFO is empty, in which case reading the A/D FIFO Register returns meaningless information.

Address: Base address + 10 (hex)

Type: Read-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
15-0	D<15..0>	These bits are 16-bit A/D conversions from the channel(s) selected by the ACH<2..0> bits in the Analog Input Config Register. If the AT-A2150 is configured to store data from more than one analog input channel, the board requires multiple read operations from the A/D FIFO to obtain all the simultaneous samples. The data in the FIFO appears as given in the following table, according to the ACH<2..0> bits in the Analog Input Config Register.

Bit Name Description (continued)

ACH<3..0>	D<15..0>
000	None
001	Channel 0 Channel 1 Channel 2 Channel 3
010	Channel 0 Channel 1
011	Channel 2 Channel 3
100	Channel 0
101	Channel 1
110	Channel 2
111	Channel 3

Values read range from -32,768 to +32,767 decimal (8000 to 7FFF hex).

Interrupt/DMA Register Group

The three registers making up the Interrupt/DMA Register Group control and monitor the interrupt and DMA circuitry. The Status Register reports the status of the input FIFO and returns any errors found. The Interrupt/DMA Control Register controls the interrupt and DMA functions of the AT-A2150. The DMA TC Interrupt Clear Register is used to clear a DMA TC interrupt if one occurs.

Bit descriptions for the registers in the Interrupt/DMA Register Group are given on the following pages.

Status Register

The Status Register indicates the status of the A/D FIFOs and the associated error flags. Bits 5 through 0 pertain to A/D conversion.

Address: Base address +12 (hex)

Type: Read-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	X	X	BRD_ID1	BRD_ID0

7	6	5	4	3	2	1	0
DMATCIntr	INTR	DCal	EDAQ	OverFlow	DaqInProg	HalfFull*	DataAvail

Bit **Name** **Description**

15-10 X Don't care bits.

9-8 BRD_ID<1..0> The BRD_ID<1..0> bits indicate the specific kind of AT-A2150 board according to the following table.

BRD_ID<1..0>	Board Type
00	AT-A2150C
01	AT-A2150S
10	Reserved for future board type
11	Reserved for future board type

7 DMATCIntr This bit goes high when a DMA TC has occurred and the DMATCIntEn bit in the Interrupt/DMA Control Register is set high. This bit is cleared by a write to the DMA TC Interrupt Clear Register or by a hardware reset.

6 INTR This bit shows the overall state of interrupts generated by the AT-A2150 board. If this bit is high, the AT-A2150 is asserting an interrupt that has not yet been serviced. If this bit is low, no interrupt is pending. This bit is normally low. See the description of the Interrupt/DMA Control Register in this chapter for information on the three possible sources for an interrupt.

Bit	Name	Description (continued)
5	DCal	This bit is set high when the ADCs are performing an internal offset calibration cycle. DCal is set low at the end of the calibration cycle and can be used to determine the end of a calibration cycle.
4	EDAQ	This bit shows the state of the end-of-data acquisition (EDAQ) interrupt. If this bit is high, the AT-A2150 is asserting an end-of-data acquisition interrupt that has not yet been serviced. If this bit is low, no end-of-data acquisition interrupt is pending. This bit is normally low and is asserted if the EDAQIntEn bit in the Interrupt/DMA Control Register is set and the DaqInProg bit makes a high-to-low transition.
3	OverFlow	This bit indicates the status of the overflow flag. If this bit is set, an overflow has occurred in the current data acquisition sequence. An overflow occurs when data from the ADC is loaded into the FIFO faster than data is read from the FIFO. Thus, one or more conversion values in the data sequence have been lost.
2	DaqInProg	This bit indicates the status of data acquisition. If this bit is set, a data acquisition operation is in progress; that is, the A/D FIFOs are buffering the A/D conversion data.
1	HalfFull*	This bit reflects the status of the A/D FIFOs. If this bit is low, the A/D FIFO is at least half full and contains at least 128 16-bit words. If this bit is high, the A/D FIFO contains less than 128 words.
0	DataAvail	This bit reflects the status of the A/D FIFOs. If this bit is set, the A/D FIFO has at least one data value. If this bit is low, the A/D FIFO is empty.

Interrupt/DMA Control Register

The Interrupt/DMA Control Register controls the interrupt and DMA facility on the AT-A2150.

Address: Base address + 12 (hex)

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
0	0	0	DMADemEn	DMATCIntEn	EDAQIntEn	FlagSel	IntInEn

7	6	5	4	3	2	1	0
IntChan3	IntChan2	IntChan1	IntChan0	DMAEn	DMACh2	DMACh1	DMACh0

Bit	Name	Description
15-13	0	Reserved bits. These bits must be set to zero.
12	DMADemEn	DMA Demand Enable – Setting this bit on a Revision C or later AT-A2150 enables DMA demand mode to be used on the EISA bus. If you are not using a computer with an EISA bus, this bit should be cleared.
11	DMATCIntEn	Setting this bit allows an interrupt to be generated when a DMA TC occurs.
10	EDAQIntEn	This bit enables or disables generation of an end-of-data acquisition interrupt on the AT bus. If this bit is set, an IRQ*n* (where *n* is determined by IntChan<3..0>) is generated whenever the DaqInProg bit makes a high-to-low transition, meaning data acquisition has ended. If EDAQIntEn is set low, no end-of-data acquisition interrupt is generated on the AT bus. The EDAQ Interrupt can be cleared by writing to the A/D FIFO Reset Register.
9	FlagSel	This bit determines which of the two FIFO flags (HalfFull* or DataAvail) is used to generate interrupt requests. If this bit is set low, an interrupt request can be generated using the DataAvail flag. If this bit is set high, an interrupt request is generated using the HalfFull* flag of the FIFO. Setting FlagSel high is useful in reducing the interrupt frequency. This bit becomes a *don't care* bit if IntInEn is low and A/D FIFO interrupts are disabled.
8	IntInEn	This bit enables or disables generation of an interrupt from the A/D FIFOs. If IntInEn is set high and FlagSel is set low, an interrupt is generated whenever the A/D FIFO is not empty; that is, the A/D FIFO has at least one 16-bit word available. If IntInEn is set high and FlagSel is set high, an interrupt is generated whenever the A/D FIFO is more than half full and at least 128 16-bit words are

Bit Name Description (continued)

8 IntInEn available. The A/D FIFO interrupt is cleared by emptying the A/D FIFO if FlagSel is low. If FlagSel is high, the A/D FIFO interrupt is cleared by reading the A/D FIFO until the A/D FIFO is less than half full.

7-4 IntChan<3..0> These bits select the interrupt channel used by the AT-A2150.

IntChan<3..0>	Selected Channel
0000	Not a valid channel
0001	Not a valid channel
0010	Not a valid channel
0011	IRQ3
0100	IRQ4
0101	IRQ5
0110	IRQ6
0111	IRQ7
1000	Not a valid channel
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	Not a valid channel
1110	IRQ14
1111	IRQ15

3 DMAEn This bit enables DMA requests from the AT-A2150 on the DMA input channel selected by the DMACh<2..0> bits. A DMA request is generated whenever the A/D FIFO is not empty, that is, the A/D FIFO has at least one 16-bit word available, and the DMAEn bit is set high.

2-0 DMACh<2..0> These bits select the DMA channel on the AT bus for analog input.

DMACh<2..0>	Selected Channel
000	DMARQ0
001	DMARQ1
010	DMARQ2
011	DMARQ3
100	Not a valid channel
101	DMARQ5
110	DMARQ6
111	DMARQ7

DMA TC Interrupt Clear Register

The DMA TC Interrupt Clear Register is used to clear a DMA TC interrupt if one occurs.

Address: Base address + 0E (hex)

Type: Write-only

Word Size: 16-bit

Bit Map: Not applicable, no bits used

82C53 Counter/Timer Register Group

The four registers making up the 82C53 Counter/Timer Register Group access the onboard 82C53 Counter/Timers. The 82C53 has three counters that control onboard data acquisition.

The 82C53 has three independent, 16-bit counter registers and one 8-bit Mode Register. The Mode Register is used to set the mode of operation for each of the three counters.

Bit descriptions for the registers in the 82C53 Counter/Timer Register Group are given on the following pages.

Counter 0 Data Register

The Counter 0 Data Register is used for loading and reading back the contents of 82C53 Counter 0.

Address: Base address + 14 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7-0	D<7..0>	8-bit Counter 0 contents.

Counter 1 Data Register

The Counter 1 Data Register is used for loading and reading back the contents of 82C53 Counter 1.

Address: Base address + 15 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7-0	D<7..0>	8-bit Counter 1 contents.

Counter 2 Data Register

The Counter 2 Data Register is used for loading and reading back the contents of 82C53 Counter 2.

Address: Base address + 16 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
7-0	D<7..0>	8-bit Counter 2 contents.

Counter Mode Register

The Counter Mode Register determines the operation mode for each of the three counters on the 82C53 chip. The Counter Mode Register selects the counter involved, the read/load mode, the operation mode (that is, any of the six 82C53 operation modes), and the counting mode (binary or BCD counting).

The Counter Mode Register is an 8-bit register. Bit descriptions for each of these bits are given in Appendix C, *MSM82C53 Data Sheet*.

Address: Base address + 17 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Bit	Name	Description
7-6	SC<1..0>	Select Counter. These bits select which of the three counters are being programmed by this write operation.
5-4	RL<1..0>	Read/Load. These bits select the read/load mode for the counter involved.
3-1	M<2..0>	Mode. These bits select one of the six 82C53 operation modes for the counter selected.
0	BCD	BCD. This bit selects the counting mode, either binary or BCD counting.

These bits are described further in Appendix C, *MSM82C53 Data Sheet*.

RTSI Bus Register Group

With the four registers making up the RTSI Bus Register Group, you can program the RTSI bus interface circuitry for routing signals on the RTSI bus lines to and from AT-A2150 signals. You can also generate trigger signals useful for synchronizing and triggering multiple boards sharing the RTSI bus.

Bit descriptions of the registers making up the RTSI Bus Register Group are given on the following pages.

RTSI Switch Shift Register

The RTSI Switch Shift Register is written to in order to load the RTSI switch internal 56-bit control register with routing information for switching signals to and from the RTSI bus trigger lines. The RTSI Switch Shift Register is a 1-bit register and must be written to 56 times to shift the 56 bits into the internal register.

Address: Base address + 18 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	RSI

Bit	Name	Description
7-1	X	Don't care bits.
0	RSI	RTSI Switch Serial Input. This bit is the serial input to the RTSI switch. Each time the RTSI Switch Shift Register is written to, the value of this bit is shifted into the RTSI switch. See *Programming the RTSI Switch* later in this chapter for more information.

RTSI Switch Strobe Register

The RTSI Switch Strobe Register is written to in order to load the RTSI Switch Shift Register into the RTSI Switch Control Register, thereby updating the RTSI switch routing pattern. The RTSI Switch Strobe Register is written to after shifting the 56-bit routing pattern into the RTSI Switch Shift Register.

Address: Base address + 19 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map: Not applicable, no bits used

Serial Data Link Control Register

The Serial Data Link Control Register controls the serial data link and multiple-board synchronization-related signals that are sent over the RTSI bus.

Address: Base address + 1A (hex)

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	0
SLDSel	ADCMaster	ADCSlave	C30*/32C	0	0	A/D DRIVE 3	A/D DRIVE 1

Bit	Name	Description
15-8	0	Reserved bits. These bits must be set to zero.
7	SLDSel	This bit selects which ADC chip is routed to which serial data link. When SLDSel is low, ADC 0 is routed to Serial Link 1, and ADC 1 is routed to Serial Link 3. When SLDSel is high, ADC 0 is routed to Serial Link 3, and ADC 1 is routed to Serial Link 1.
6	ADCMaster	This bit is useful for synchronizing multiple AT-A2150 boards. When this bit is set high, the board drives its local master clock and a synchronization signal on the RTSI bus so the sampling on one or more AT-A2150 boards can be synchronized to the clock on this board.
5	ADCSlave	This bit is useful for synchronizing multiple AT-A2150 boards. When this bit is set high, the board receives the master clock and a synchronization signal on the RTSI bus from another AT-A2150 board. When this bit is set low, the board uses its local master clock.
4	C30*/32C	This bit selects the serial link format for either a TMS320C30 DSP chip (0) or a WEDSP32C DSP chip (1).
3-2	0	Reserved bits. These bits must be set to zero.
1	A/D DRIVE 3	This bit controls driving the serial communication group Serial Link 3 on the RTSI bus with the A/D data. Setting this bit high causes the AT-A2150 to drive the Serial Link 3 group lines onto the RTSI bus. Setting this bit low tri-states the Serial Link 3 group lines, so other boards can use the Serial Link 3 group.
0	A/D DRIVE 1	This bit controls driving the serial communication group Serial Link 1 on the RTSI bus with the A/D data. Setting this bit high causes the AT-A2150 to drive the Serial Link 1 group lines onto the RTSI bus. Setting this bit low tri-states the Serial Link 1 group lines, so other boards can use the Serial Link 1 group.

RTSI Trigger Register

The RTSI Trigger Register sends a trigger to the RTSI switch that can be routed to the RTSI trigger lines, TRIGGER<5..0>, and to the HWTrig* signal. This register can be used to send a common hardware trigger generated by a single software strobe to multiple AT-A2150 boards connected via the RTSI bus. This register can also be used to test the AT-A2150 hardware trigger capability.

Address: Base address + 0A (hex)

Type: Write-only

Word Size: 16-bit

Bit Map: Not applicable, no bits used

Programming Considerations

The following sections contain programming instructions for operating the circuitry on the AT-A2150. Programming the AT-A2150 involves writing to and reading from the various registers on the board. The programming instructions included here list the sequences of steps to take. These instructions are language independent; that is, you are instructed to write a value to a given register, to set or clear a bit in a given register, or to detect whether a given bit is set or cleared, but actual code is not presented.

Register Programming Considerations

Registers on the AT-A2150 are I/O mapped; so writing to a register involves storing a value in an I/O location. A register is read by reading an I/O location. Only I/O location read and write operations can be performed on the AT-A2150 registers. Mathematical or logical operations *cannot* be directly applied to the AT-A2150 registers. Attempting to do so results in unpredictable program behavior.

Several write-only registers on the AT-A2150 contain bits that control several independent pieces of the onboard circuitry. In the set or clear instructions, specific register bits should be set or cleared without changing the current state of the remaining bits in the register. However, writing to these registers affects all register bits simultaneously. You cannot read these registers to determine which bits have been set or cleared in the past; therefore, you should maintain a software copy of the write-only registers. This software copy can then be read to determine the status of the write-only registers. To change the state of a single bit without disturbing the remaining bits, set or clear the bit in the software copy and then write the software copy to the register.

Initializing the AT-A2150 Board

The AT-A2150 hardware initializes on startup in the following state:

All configuration registers (Analog Input Config Register, Trigger Config Register, Level Trigger Data Register, Interrupt/DMA Control Register, and Serial Data Link Control Register) are initialized to zero. This initialization configures the board as follows:

Analog input sampling rate:	32 kHz on the AT-A2150C, 16 kHz on the AT-A2150S
Analog input coupling:	Analog Ground
Data acquisition mode:	Software-triggered
RTSI serial data links:	Disabled (high impedance)
RTSI trigger lines:	Disabled (high impedance)
AT bus DMA lines:	Disabled (high impedance)
AT bus interrupt:	Disabled (high impedance)

The ADC initiates an offset calibration cycle upon startup with respect to analog ground. This calibration cycle takes 4,096 sampling interval periods (128 msec at 32 kHz, for example). The digital filter delay adds another 72 sampling interval periods (2.25 msec at 32 kHz, for example). Thus, valid A/D conversion data does not start until 130.25 msec after startup if the sampling rate is 32 kHz.

Performing an ADC Offset Calibration

The ADCs can initiate an internal offset calibration cycle under software control. During the offset calibration cycle, the digital section of the ADC measures and stores the value of the ADC input channels in registers. This stored value is subtracted from all future outputs. Because the ADC 0 input channels can be multiplexed between ground (AIGND) and the signal inputs (ACH0 and ACH1) via the CAL*0 bit in the Analog Input Config Register, the offset calibration cycle can use either AIGND or ACH0 and ACH1 inputs for calibration ground reference. Similarly, the ADC 1 input channels can be multiplexed between ground (AIGND) and the signal inputs (ACH2 and ACH3) via the CAL*1 bit in the Analog Input Config Register.

Use the following steps to perform an ADC offset calibration cycle.

1. The sampling rate should be selected first by writing to the Analog Input Config Register. See the Analog Input Config Register bit description earlier in this chapter for sampling rate bit patterns.

2. Set the CAL*0 bit in the Analog Input Config Register high or low depending on the offset calibration reference required. If offset calibration with reference to AIGND is desired, the CAL*0 bit should be set low. Setting the CAL*0 bit low switches the ADC input multiplexers to AIGND. If offset calibration is to be referenced to ACH0 and ACH1, respectively, for Channel 0 and Channel 1, the CAL*0 bit should be set high. This setting switches the ADC input multiplexers to the ACH0 and ACH1 signals. The CAL*1 bit in the Analog Input Config Register can be similarly set or cleared to select the offset calibration reference for ACH2 and ACH3.

3. Set the DPD bit high in the Analog Input Config Register.

4. Set the DPD bit low in the Analog Input Config Register. This setting initiates an offset calibration cycle. The offset calibration cycle takes 4,096 sampling intervals (85.3 msec at 48 kHz, for example) during which the DCal bit in the Status Register is set high. The DCal bit goes low at the end of the offset calibration cycle. Thus, this bit can be used to determine the end of the offset calibration cycle.

5. Set the CAL*0 and CAL*1 bits high. This setting switches the ADC input multiplexers to the external input signals ACH0, ACH1, ACH2, and ACH3.

6. Reset the A/D FIFO to ensure that the FIFO is cleared of any leftover data from the previous setup.

The normal operation of the ADC begins about 72 sampling intervals after the offset calibration cycle (about 1.5 msec at 48 kHz, for example). This extra delay is a result of the digital filter settling time.

Programming the Analog Input Circuitry

Programming the analog input circuitry for a single ADC read involves the following sequence of steps:

1. Select the analog input channel.

2. Enable the A/D FIFOs.

3. Read the A/D conversion result.

Each of these programming steps is discussed in detail as follows.

1. Select the analog input channel.

The analog input channel is selected by writing to the Analog Input Config Register. See the Analog Input Config Register bit description earlier in this chapter for analog input channel bit patterns. Set up the bits as given in the Analog Input Config Register bit description, and write to the Analog Input Config Register.

The Analog Input Config Register needs to be written to only when the analog input channel or input coupling bits need to be changed.

2. Enable the A/D FIFOs.

The ADCs on the AT-A2150 continuously sample at the rate set by the CLKAD<3..0> bits in the Analog Input Config Register. However, you must enable the input FIFOs to store the A/D conversion data in order to read the conversion data.

To enable the A/D FIFOs, complete the following:

- Clear the A/D FIFO by writing to the A/D FIFO Reset Register.
- Start buffering the conversion data in the FIFO by writing to the A/D FIFO Start Register.

3. Read the A/D conversion result.

A/D conversion results are obtained by reading the A/D FIFO Register. However, before you read the A/D FIFO, you must read the Status Register to determine whether the A/D FIFO contains any results.

To read the A/D conversion results, complete the following steps:

- Read the Status Register (16-bit read).
- If the DataAvail bit (bit 0) is set high, read the A/D FIFO Register to obtain the result.

Reading the A/D FIFO Register removes the A/D conversion result from the A/D FIFO.

Programming Multiple A/D Conversions

A sequence of timed A/D conversions is referred to in this manual as a *data acquisition operation*. Counter 0 and Counter 1 on the AT-A2150 are used as sample counters. A specified number of conversions is stored, after which the hardware terminates storing the conversion data. If a 16-bit count is required (less than 65,536 samples), only Counter 0 is used. If more than 65,535 samples are to be acquired, two 16-bit counters (Counters 0 and 1) are concatenated. Unlike many other data acquisition boards on which individual A/D conversions are timed or requested, the AT-A2150 is continuously running because of the way the digital filter works. Because the ADC runs off a clock that is independent of the digital circuitry, the period of time from when a single conversion or the beginning of a data acquisition sequence is requested or triggered to the time it actually occurs has an inherent uncertainty of up to one sample period.

Four triggering modes are available for a data acquisition operation: pretrigger mode, posttrigger mode, delay trigger mode, and software trigger mode. In pretrigger mode, a software trigger begins the data acquisition, but a hardware trigger begins the sample counter that terminates the data acquisition process. In posttrigger mode, either a software or a hardware trigger begins both the data acquisition process and the sample counter that terminates the process. In delay trigger mode, the the data acquisition and the sample counter start after a programmed delay from a software or hardware trigger. In software trigger mode, the data acquisition is both started and terminated by software. Notice that the digital filter delay in the ADC is 35.6 samples. This delay implies that the first ADC conversion stored in the serial input port in posttrigger mode corresponds to the value of the analog input signal 35.1 ± 0.5 sample periods before the trigger occurred. As a result, the posttrigger mode data contains 35 or 36 samples of pretriggered data. The one sample period uncertainty results from the ADC sample clock and the trigger signals being asynchronous. In the case of level-and-slope trigger, there is no pretrigger data from digital filter delay, because the level-and-slope trigger detection circuitry operates on data which has already passed through the digital filter. Data acquisition can be performed on a single channel, two channels simultaneously, or all four channels simultaneously.

The following programming steps are required for a data acquisition operation:

1. Reset the trigger circuit.
2. Select the analog input channel, sampling rate, and coupling.
3. Reset the A/D FIFO.
4. Program the sample counter.
5. Program the delay timer.
6. Configure the trigger circuit.
7. Apply a trigger.
8. Service the data acquisition operation.

Each of these programming steps is explained in detail as follows.

1. Reset the trigger circuit.

The trigger circuit is controlled by the Trigger Config Register. Write zero to this register to reset the trigger circuit. Writing zero ensures that the trigger circuit is in a known state.

2. Select the analog input channel, sampling rate, and coupling.

The analog input channel, sampling rate, and coupling are selected by writing to the Analog Input Config Register. See the Analog Input Config Register bit description earlier in this chapter for sampling rate, analog input channel, and coupling bit patterns. Either a single analog input channel, two channels, or all four channels can be selected at the same time. A delay of 72 sampling intervals should be used after a change in the sampling rate before valid data can be expected.

3. Reset the A/D FIFO.

The A/D FIFO can be cleared by writing to the A/D FIFO Reset Register. This reset also clears the triggering circuitry, the A/D FIFO overflow detection circuitry, and the EDAQ detection circuitry.

4. Program the sample counter.

The following sequence should be used to program the sample counter. Regardless of the triggering mode, count size refers to the number of 16-bit words stored in the FIFO *after* the trigger. Thus, for a single-channel data acquisition, *count size* equals the number of samples per channel, whereas for a two-channel data acquisition, count size equals the number of samples per channel multiplied by two. For four-channel data acquisition, count size equals the number of samples multiplied by four. Counter 0 is used as the sample counter for a 16-bit count size. Counter 0 and Counter 1 are concatenated to form a 32-bit counter for greater than 16-bit count size.

Sample Count Performed in Software

Use the following steps to disable the sample counter if sample counting is to be performed in software. In other words, the counter is not required to terminate storing the A/D conversions after a programmed number of conversions. Notice that the sample count must be performed by hardware for pretrigger data acquisition mode.

a. Clear the Count32/16* bit in the Trigger Config Register.

b. Write 30 (hex) to the Counter Mode Register (select Counter 0, Mode 0). This is an 8-bit write operation. This write sets the output of Counter 0 in a low state.

Sample Count Performed by Hardware

The sequence for programming the sample counter is slightly different depending on the count size.

Count Size 2 through 65,536. Use the following steps to program the sample counter for sample counts up to 65,536. The minimum possible sample count is two. At the end of the programmed sample count, the Counter 0 output (OUT0) goes high, which resets the DaqInProg flag in the Status Register and disables storage of further A/D conversion data in the A/D FIFO.

a. Clear the Count32/16* bit in the Trigger Config Register.

b. Write 30 (hex) to the Counter Mode Register (select Counter 0, Mode 0). This is an 8-bit write operation.

c. Write the least significant byte of *M*-1, where *M* is the count size, to the Counter 0 Data Register.

d. Write the most significant byte of *M*-1, where *M* is the count size, to the Counter 0 Data Register.

Count Size Greater than 65,536. Two counters (Counter 0 and Counter 1) are used for sample counts greater than 65,536. Counter 0 divides the sample conversion clock by a programmable number *N*. Counter 0 output is tied to the clock source of Counter 1 that counts this divided-down sample clock. Thus, counts greater than 65,536 are possible. However, the specified sample count must be a multiple of *N*. Use the following steps to program the sample counter for sample counts greater than 65,536. All writes to the Counter/Timer Register group are 8-bit write operations.

a. Set the Count32/16* bit in the Trigger Config Register.

b. Write 70 (hex) to the Counter Mode Register (select Counter 1, Mode 0).

c. Write the least significant byte of $\frac{M}{N}$, where *M* is the count size and *N* is the prescaler, to the Counter 1 Data Register.

d. Write the most significant byte of $\frac{M}{N}$, where *M* is the count size and *N* is the prescaler, to the Counter 1 Data Register.

e. Write 30 (hex) to the Counter Mode Register (select Counter 0, Mode 0). This write operation sets the output of Counter 0 low.

f. Write 38 (hex) to the Counter Mode Register (select Counter 0, Mode 4). This write operation sets the output of Counter 0 high.

g. Write 30 (hex) to the Counter Mode Register (select Counter 0, Mode 0). This write operation sets the output of Counter 0 low. The three writes in steps *e*, *f,* and *g* produce a pulse at the Counter 0 output that is tied to the clock input of Counter 1. Thus, a pulse is produced at the Counter 1 clock input that loads the Counter 1 Count Register in the Counter/Timer integrated circuit.

h. Write 34 (hex) to the Counter Mode Register (select Counter 0, Mode 2). This write operation sets up Counter 0 for use as a divide-by-*N* counter.

i. Write the least significant byte of *N*, where *N* is the prescaler, to the Counter 0 Data Register.

j Write the most significant byte of *N*, where *N* is the prescaler, to the Counter 0 Data Register.

5. Program the delay timer.

Counter/Timer 2 of the 82C53 System Timing Controller chip is used as a programmable delay timer for delay trigger mode data acquisition. Counter/Timer 2 is clocked by the ADC sample clock. Perform the following steps for programming the delay timer. If delay trigger mode data acquisition is not required, only step *a* must be performed.

a. Write B0 (hex) to the Counter Mode Register (select Counter 2, Mode 0). This is an 8-bit write operation.

b. Write the least significant byte of the delay count to the Counter 2 Data Register. This is an 8-bit write operation.

c. Write the most significant byte of the delay count to the Counter 2 Data Register. This is an 8-bit write operation.

d. Set the TrigMode<1..0> bits in the Trigger Config Register to enable the delayed trigger mode (11 binary). With the TrigMode<1..0> bits set, a trigger condition does not start data acquisition. The gate input of Counter 2 is set high instead, which enables the Counter/Timer 2. Data acquisition begins at the end of the programmed delay. The trigger condition depends on the trigger source being used.

Note: The actual delay = $D * \frac{1}{Fs}$, where *D* is the 16-bit delay count programmed in Counter 2 and *Fs* is the ADC sampling rate.

6. Configure the trigger circuit.

The AT-A2150 can be programmed to use one of four data acquisition trigger modes and one of four possible trigger sources. The four data acquisition modes are pretrigger data acquisition, posttrigger data acquisition, delay trigger data acquisition, and software trigger data acquisition. The four possible trigger sources are listed as follows:

- software trigger
- TTL-level trigger from an external source applied at the EXTTRIG* on the I/O connector
- trigger generated from the internal level-and-slope detection circuit
- trigger received over the RTSI bus

In the following discussion, the last three sources are referred to as *hardware* trigger sources.

Configuring the Trigger Circuit Mode

To configure the trigger circuit to the desired trigger mode, set the TrigMode<1..0> bits in the Trigger Config Register to the desired trigger mode code.

- Pretrigger data acquisition – In pretrigger mode, a software trigger begins the data acquisition, but a hardware trigger begins the sample counter that terminates the data acquisition process. For pretrigger data acquisition, set the TrigMode<1..0> bits in the Trigger Config Register to the appropriate value (01 binary).
- Posttrigger data acquisition – In posttrigger mode, either a software or a hardware trigger begins both the data acquisition process and the sample counter that terminates the process. For posttrigger data acquisition, set the TrigMode<1..0> bits in the Trigger Config Register to the appropriate value (10 binary).
- Delay trigger data acquisition – In delay trigger mode, the data acquisition and the sample counter start after a programmed delay from a software or hardware trigger. The sample counter terminates the data acquisition process. The delay programming sequence is described in step 5.

- Software trigger data acquisition – In software trigger mode, the data acquisition is both started and terminated by software. For software trigger data acquisition, set the TrigMode<1..0> bits in the Trigger Config Register to the appropriate value (00 binary).

Configuring the Trigger Circuit Source

To configure the trigger circuit to the desired trigger source, set the proper bits in the Trigger Config Register as described in the following paragraphs.

- Software trigger – No special steps must be taken to set up the AT-A2150 for a software trigger when the board is in the correct trigger mode.

- External trigger – Set the ExtTrigRcv bit high in the Trigger Config Register to enable the EXTTRIG* signal to drive the internal trigger circuit.

- Level-and-slope circuit trigger – Write the eight MSBs of the upper and lower level values to the Level Trigger Data Register. Write the slope and signal source to the Trigger Config Register. Also, set the LTrigEn bit high in the Trigger Config Register. A description of the level-and-slope circuit operation is given in Chapter 3, *Theory of Operation*. For example, to set the trigger value to 3FFF (hex) with no hysteresis, the trigger slope to positive slope, and the trigger signal source to Channel 0, using a 16-bit sample counter and posttrigger mode, write 3F3F (hex) to the Level Trigger Data Register and 0006 (hex) to the Trigger Config Register.

- RTSI trigger – Clear the ExtTrigRcv bit in the Trigger Config Register to ensure that the EXTTRIG* signal is not driving the HWTrig* signal. Program the RTSI switch to drive the signal HWTrig* from the selected trigger line. See *RTSI Bus Trigger Line Programming Considerations* later in this chapter for more information.

7. Apply a trigger.

The following section describes how each type of trigger source applies a trigger.

- Software trigger – Write any value to the A/D FIFO Start Register to generate a software trigger.

- External trigger – A TTL-level high-to-low transition on EXTTRIG* generates a hardware trigger when the AT-A2150 is configured to use the external trigger as its trigger source.

- Level-and-slope circuit trigger – The level-and-slope detection circuitry generates a hardware trigger when the AT-A2150 is configured to use the level-and-slope circuit as its trigger source. The digital value of the analog source signal must also cross both the high and low trigger thresholds as described in Chapter 3, *Theory of Operation*.

- RTSI trigger – A TTL-level high-to-low transition on the HWTrig* output from the RTSI switch generates a hardware trigger when the AT-A2150 is configured to use the RTSI trigger as its trigger source.

The four data acquisition triggering modes available on the AT-A2150 are triggered in the following ways.

- Pretrigger data acquisition – Write to the A/D FIFO Start Register to send a software trigger to the AT-A2150. This trigger starts the data acquisition sequence and sets the DaqInProg bit in the Status Register high. The sample counter starts counting after a hardware trigger is received by the AT-A2150. The DaqInProg bit goes low after the programmed sample count expires, inhibiting further conversion data storage in the A/D FIFO.

- Posttrigger data acquisition – A software or a hardware trigger starts the data acquisition sequence, sets the DaqInProg bit in the Status Register high, and starts the sample counter. The DaqInProg bit goes low after the programmed sample count expires, inhibiting further conversion data storage in the A/D FIFO.

- Delay trigger data acquisition – The delay trigger data acquisition starts the data acquisition, sets the DaqInProg bit in the Status Register high, and starts the sample counter after a programmed delay from the software or hardware trigger. The DaqInProg bit goes low after the programmed sample count expires, inhibiting further conversion data storage in the A/D FIFO.

- Software trigger data acquisition – The software trigger data acquisition is both started and terminated by software. Write to the A/D FIFO Start Register to start the data acquisition process and set the DaqInProg bit in the Status Register high. After the desired number of samples have been obtained (the sample count is also done by software), write to the A/D FIFO Reset Register to terminate the data acquisition and set the DaqInProg bit in the Status Register low.

8. Service the data acquisition operation.

When the data acquisition operation is started by applying a trigger, the operation must be serviced by reading the A/D FIFO Register every time an A/D conversion result becomes available. To service the operation, perform the following sequence until the desired number of conversion results have been read:

a. Read the Status Register (16-bit read).

b. If the DataAvail bit (bit 0) is set, read the A/D FIFO Register to obtain the result. If the HalfFull* bit (bit 1) is cleared, there are at least 128 words in the A/D FIFO. You can read the A/D FIFO 128 times before reading the Status Register again.

The DataAvail bit indicates whether one or more A/D conversion results are stored in the A/D FIFO. If the DataAvail bit is cleared, the A/D FIFO is empty and reading the A/D FIFO Register returns meaningless data.

Interrupts can also be used to service the data acquisition operation. This topic is discussed in the next section.

An overflow error condition can occur during a data acquisition operation. This error condition is reported through the Status Register and should be checked every time the Status Register is read to check the DataAvail bit or the HalfFull* bit.

An overflow condition occurs if more than 64 four-channel A/D conversions, 128 two-channel A/D conversions, or 256 single-channel A/D conversions have been stored in the A/D FIFO

without the A/D FIFO being read. In other words, the A/D FIFO is full and cannot accept any more data. This condition occurs if the software loop reading the A/D FIFO Register is not fast enough to keep up with the A/D conversion rate. When an overflow occurs, at least one A/D conversion result is lost. An overflow condition has occurred if the OverFlow bit in the Status Register is set.

The OverFlow bit in the Status Register is reset by writing to the A/D FIFO Reset Register.

Interrupt Programming

Interrupts can be used for servicing the A/D FIFO during a data acquisition operation. The IntInEn and FlagSel bits in the Interrupt/DMA Control Register enable and select the FIFO flag used for interrupts related to the A/D FIFO. The IntChan <3..0> bits in the Interrupt/DMA Control Register control which interrupt channel is selected for use by the AT-A2150.

Warning: Be very careful to select only an interrupt channel that is not already being used by another board on the AT bus. If a channel is selected improperly, interrupts do not function properly and damage can even result to the boards in use.

To use the conversion interrupt, set the IntInEn bit in the Interrupt/DMA Control Register after step 4 in the previous sequence. If the IntInEn bit is set high and FlagSel is set low, an interrupt is generated whenever the DataAvail bit in the Status Register is high. Emptying the A/D FIFO clears this interrupt condition. The A/D FIFO is emptied by reading its contents. If both the IntInEn bit and the FlagSel bit are set high, an interrupt is generated whenever the HalfFull* bit in the Status Register is low, that is, when the A/D FIFO is at least half full. Making the A/D FIFO less than half full clears this interrupt condition. The A/D FIFO is made half full by reading its contents. The half-full interrupt is used to reduce the interrupt frequency because the interrupt service routine is invoked at a much lower rate than the ADC sample rate. The half-full interrupt also reduces the use of the AT bus bandwidth because at least 128 words can be read from the A/D FIFO without polling the Status Register before each read from the A/D FIFO.

The AT-A2150 can also generate an interrupt at the end of a data acquisition operation. To use the end-of-data acquisition interrupt, set the EDAQIntEn bit in the Interrupt/DMA Control Register. If this bit is set, an interrupt is generated whenever the DaqInProg bit in the Status Register makes a high-to-low transition. This interrupt condition is cleared by writing to the A/D FIFO Reset Register.

The final way of generating interrupts is by the occurrence of a DMA TC. To use the DMA TC interrupt, set the DMATCIntEn bit in the Interrupt/DMA Control Register. If this bit is set, an interrupt is generated whenever a DMA TC for the AT-A2150 occurs. To clear this interrupt, write to the DMA TC Interrupt Clear Register.

Programming DMA Operations

DMA operations can be used for servicing the A/D FIFOs during a data acquisition operation. The DMA controller sends a TC when the value in its Count Register changes from hex 0000 to hex FFFF. See the *Interrupt Programming* section earlier in this chapter for information about generating an interrupt on the DMA TC.

The AT-A2150 can be programmed so that the A/D FIFO generates a DMA request signal every time the A/D FIFO is not empty.

To program the AT-A2150 for DMA operation, perform the following steps after the circuitry on the AT-A2150 is set up for a data acquisition operation and before the operation begins:

1. Program the DMA controller on the PC to service DMA requests from the AT-A2150 board. Refer to the *IBM Personal Computer AT Technical Reference* manual for additional information about programming the DMA controller.

2. Set the DMACh<2..0> bits in the Interrupt/DMA Control Register to the DMA channel to be used for the A/D FIFO. DMA Channels 5 through 7 can be used by the AT-A2150 in an AT bus computer. DMA Channels 0 through 3 and 5 through 7 can be used by the AT-A2150 in an EISA bus computer. DMA Channel 4 cannot be used by the AT-A2150 in any computer.

3. Set the DMAEn bit to enable DMA request generation on the DMA channel selected by DMACh<2..0>.

4. If you are using a computer with an EISA bus, want to use DMA demand mode, and have a Revision C or later AT-A2150, set the DMADemEn bit in the Interrupt/DMA Control Register. Do not set this bit if you are not using a computer with an EISA bus.

After completing these steps, the DMA controller automatically reads the A/D FIFO Register whenever an A/D conversion result is available and stores the result in a buffer in memory.

You need the following information to program the DMA controller:

- The target address is the program address of the memory buffer that is written to. Notice that the program address can be different from the physical address in a virtual memory environment. The DMA controller requires the physical address of the memory buffer.

- The transfer count is the desired number of 16-bit transfers.

- The transfer type is write transfer (write to target) for the A/D FIFO DMA channel.

- The data transfer mode is single-transfer mode.

- The target address bit should be set to increment.

RTSI Bus Trigger Line Programming Considerations

The RTSI switch connects signals on the AT-A2150 to six of the seven RTSI bus trigger lines. The RTSI switch has seven pins labeled A<6..0> connected to the AT-A2150, and seven pins labeled B<6..0>, six of which are connected to the six RTSI bus trigger lines. Table 4-2 shows the signals connected to each pin.

Table 4-2. RTSI Trigger Lines

RTSI Switch Pin	Signal Name	Signal Direction
A Side:		
A0	HWTrig*	Bidirectional
A1	WCAD	Output
A2	RTSITrig*	Output
A3	SWTrig*	Output
A4	RTSI_SWTrig	Input
A5	Reserved	Reserved
A6	Reserved	Reserved
B Side:		
B0	TRIGGER0	Bidirectional
B1	TRIGGER1	Bidirectional
B2	TRIGGER2	Bidirectional
B3	TRIGGER3	Bidirectional
B4	TRIGGER4	Bidirectional
B5	TRIGGER5	Bidirectional
B6	Not Used	N/A

Note: The signal directions given in Table 4-2 are with respect to the AT-A2150 board. For example, WCAD is an output from the board but an input to the RTSI switch.

AT-A2150 RTSI Signal Connection Considerations

The AT-A2150 has five signals connected to the seven A-side pins of the RTSI switch. HWTrig* is the digital trigger signal. This signal can be received from the RTSI bus, it can be received from the external hardware trigger circuitry, or it can be generated by the internal level-and-slope trigger circuit and sent from the board over the RTSI bus. WCAD is the ADC word clock. RTSITrig* is a signal that is generated by writing to the RTSI Trigger Register. This signal is useful in sending a common hardware trigger generated by a single software strobe to multiple AT-A2150 boards connected via the RTSI bus. SWTrig* is a strobe generated by the AT bus interface when the A/D FIFO Start Register is written. The signal RTSI_SWTrig* can be received from the RTSI switch and effects the board in the same way as writing to the A/D FIFO Start Register in the various trigger modes. In this way one board can send a software trigger on SWTrig* and other boards can receive the trigger on RTSI_SWTrig* in order to synchronize triggering of multiple AT-A2150 boards connected via the RTSI bus.

Programming the RTSI Switch

The RTSI switch can be programmed to connect any of the signals on the A side to any of the signals on the B side and vice versa. To program the switch, a 56-bit pattern is shifted into the RTSI switch by writing one bit at a time to the RTSI Switch Shift Register and then by writing to the RTSI Switch Strobe Register to load the pattern into the RTSI switch.

The 56-bit pattern is made up of two 28-bit patterns–one for each side (A and B) of the RTSI switch. The low-order 28 bits select the signal sources for the B-side pins. The high-order 28 bits select the signal sources for the A-side pins. Each of the 28-bit patterns are made up of seven 4-bit fields, one for each pin. The 4-bit field selects the signal source and the output enable for the pin. Figure 4-1 shows the bit map of the RTSI switch 56-bit pattern.

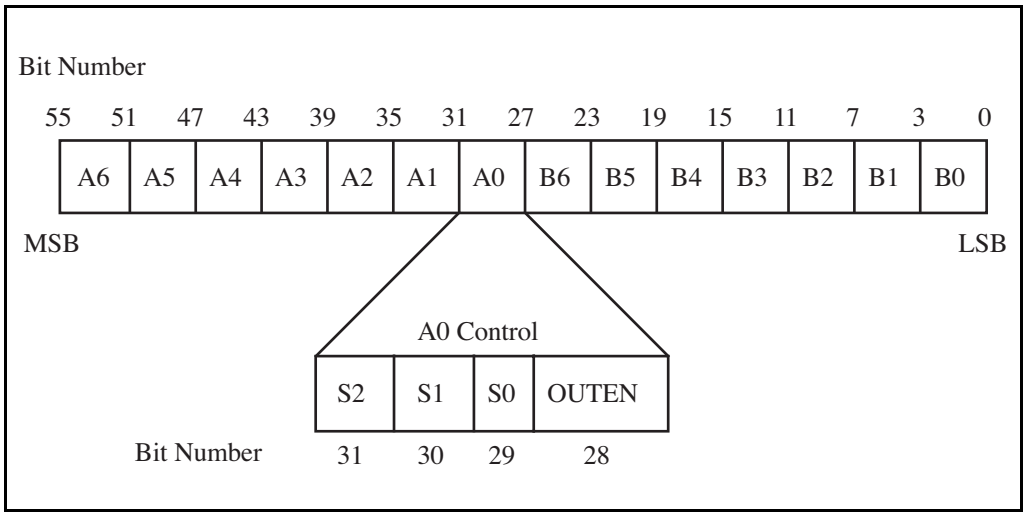


Figure 4-1. RTSI Switch Control Pattern

In Figure 4-1, the fields labeled A6 through A0 and B6 through B0 are the 4-bit control fields for each RTSI switch pin of the same name. The 4-bit control field for pin A0 is shown in Figure 4-1.

The bits labeled S2 through S0 are the signal source selection bits for the pin. One of seven source signals can be selected. Pins A6 through A0 can select any of the pins B6 through B0 as signal sources. Pins B6 through B0 can select any of the pins A6 through A0 as signal sources. For example, the pattern 011 for S2 through S0 in the A0 control field selects the signal connected to pin B3 as the signal source for pin A0.

The bit labeled OUTEN is the output enable bit for that pin. If the OUTEN bit is set, the pin is driven by the selected source signal (the pin acts as an output pin). If the OUTEN bit is cleared, the pin is not driven regardless of the source signal selected; instead, the pin can be used as an input pin.

To program the RTSI switch, complete these steps:

1. Calculate the 56-bit pattern based on the desired signal routing.

   a. Clear the OUTEN bit for all input pins and for all unused pins.

   b. Select the signal source pin for all output pins by setting bits S2 through S0 to the source pin number.

   c. Set the OUTEN bit for all output pins.

2. For $i = 0$ to 55, perform the following steps:

   a. Copy bit i of the 56-bit pattern to bit 0 of an 8-bit temporary variable.

   b. Write the temporary variable to the RTSI Switch Shift Register (8-bit write).

3. Write any value to the RTSI Switch Strobe Register (8-bit write). This operation loads the 56-bit pattern into the RTSI switch. At this point, the new signal routing takes effect.

The preceding step 2 can be completed by writing the low-order 8 bits of the 56-bit pattern to the RTSI Switch Shift Register, shifting the 56-bit pattern right once, and repeating this two-step operation a total of 56 times. Only bit 0 of the word written to the RTSI Switch Shift Register is used. The higher-order bits are ignored.

Synchronizing Multiple AT-A2150 Boards

The AT-A2150 uses two signals on the RTSI bus for sampling clock synchronization between two or more AT-A2150 boards. The sampling clock synchronization circuitry makes simultaneous sampling possible on more than four channels by using additional AT-A2150 boards. Perform the following steps to synchronize two or more AT-A2150 boards. Notice that the boards must first be connected via the RTSI bus for this operation.

1. Set the ADCMaster bit high and the ADCSlave bit low in the Serial Data Link Control Register on the master board. The AT-A2150 board that drives the sampling clock on the RTSI bus is referred to as the master board.

2. Set the ADCSlave bit high and the ADCMaster bit low in the Serial Data Link Control Register on the slave board(s). The board(s) receiving the sampling clock from the RTSI bus is (are) referred to as the slave board(s).

3. Set the APD bit high in the Analog Input Config Register on the master board.

4. Clear the APD bit in the Analog Input Config Register on the master board.

After the preceding sequence of steps is performed, the sampling rate on the slave board(s) is controlled by the sampling rate selected on the master board. In addition, the clock circuitry on the two boards is synchronized so that simultaneous sampling occurs on the two boards.

Chapter 5
Calibration Procedures

This chapter discusses the calibration procedures for the AT-A2150 analog input circuitry.

The AT-A2150 input circuitry is calibrated at the factory before shipment, and if the calibration is not disturbed, the circuitry is not likely to drift more than ±0.025 dB. However, if you need to recalibrate the board, the procedures are given in this chapter.

Calibration Equipment Requirements

For best measurement results, the AT-A2150 should be calibrated so that its absolute AC signal accuracy is within ±0.01 dB. According to standard practice, the equipment used to calibrate the AT-A2150 should be 10 times as accurate, that is, have ±0.001 dB (≈ ±0.01%) rated accuracy. However, calibration equipment with twice the accuracy of this class of acquisition system is usually acceptable. Twice the accuracy of the AT-A2150 is ±0.005 dB (≈ ±0.05%).

To calibrate the AT-A2150 board, you need a precision variable DC voltage source (usually a calibrator) with these attributes:

Accuracy	±250 μV standard ±1.25 mV sufficient
Range	±3 V
Resolution	100 μV

A calibration procedure using an AC source is not included in this manual. While it is possible, AC calibration is difficult. An AC signal source with greater than ±0.01 dB accuracy is not easy to obtain. Also, to calibrate this way, a sequence of data samples must be taken and their standard deviation computed. Unfortunately, accuracy of greater than ±0.01 dB is not possible unless very large sets of data are taken (greater than 10,000 samples) or more sophisticated root mean square computation algorithms are employed. As a result, DC calibration is recommended because it is easier and it results in very accurate AC calibration.

Calibration Trimpots

The AT-A2150 has four trimpots for calibration. The locations of these trimpots on the AT-A2150 are shown in Figure 5-1.

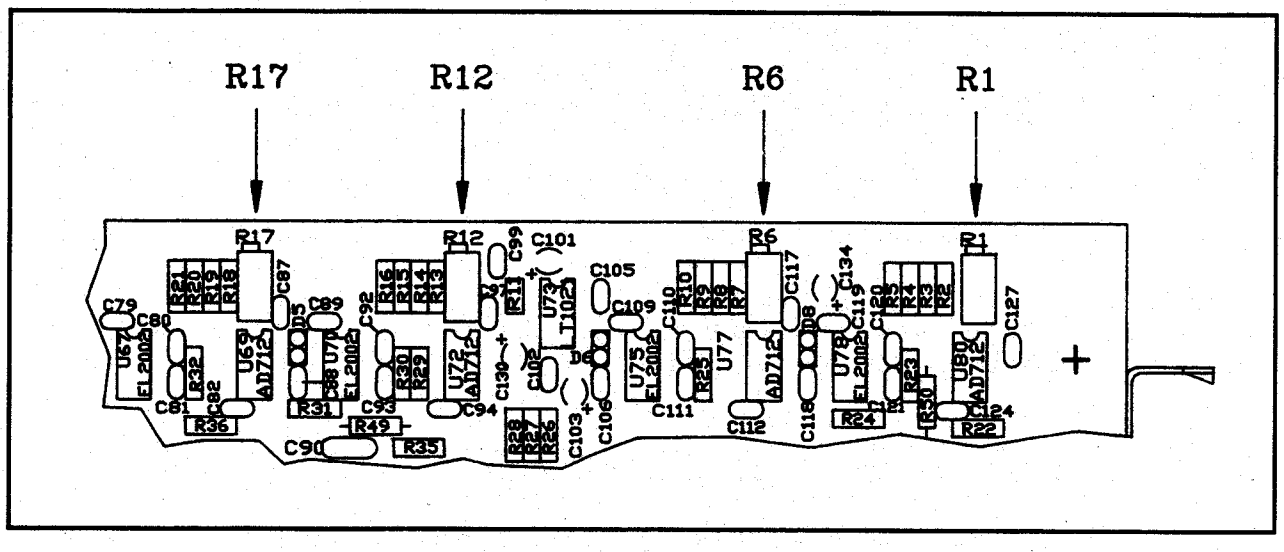


Figure 5-1. Calibration Trimpot Location Diagram

The four trimpots are as follows:

R1 – Gain trim, analog input Channel 0

R6 – Gain trim, analog input Channel 1

R12 – Gain trim, analog input Channel 2

R17 – Gain trim, analog input Channel 3

Analog Input Calibration Procedure

The AT-A2150 should warm up in the computer for approximately ten minutes before calibration is performed. Because they drift with temperature, the offset and gain should stabilize first. The following steps explain the analog input calibration procedure.

1. Calibrate the offset.

2. Calibrate the gain.

These steps are explained in detail as follows.

1. Calibrate the offset.

Offset should always be calibrated first because the gain calibration depends on offset. The offset is automatically nulled digitally instead of being calibrated by potentiometer (as is the gain). To null offset, execute the `A2150_Calibrate` routine if you are using NI-DAQ for DOS/Windows/LabWindows; otherwise follow the procedure given in *Performing an ADC Offset Calibration* in Chapter 4. After completion, the offset in each channel is within a few LSBs of zero.

2. Calibrate the gain.

For each channel, adjust the analog input gain by applying a voltage to the input. A convenient voltage to use is 2.500 V, which corresponds to an ADC reading of about 28,963 or 7123 (hex). Use the following steps to calibrate the gain:

a. Connect the calibration voltage (2.5 V) between the appropriate analog input and analog ground.

b. Select DC input coupling. Switch to DC coupling by setting the coupling switch to DC in the `MAI_Coupling` NI-DAQ for DOS/Windows routine or by setting the AC/DC* bit low in the Input Configuration Register (see Chapter 4, *Programming*, for more information).

c. Take analog input readings from the appropriate channel, and adjust the channel's trimpot until the ADC readings are within a few (< 5) LSBs of 28,963. Alternatively, average a number of readings (at least 100) and adjust the channel's trimpot until the average reading is near 28,963.09. The trimpots are listed in Table 5-1.

Table 5-1. Analog Channels and Corresponding Trimpots

Analog Channel	Trimpot Designation
0	R1
1	R6
2	R12
3	R17

Appendix A
Specifications

This appendix lists the specifications of the AT-A2150. These specifications are typical at 25° C, unless otherwise stated. The operating temperature range is 0° to 70° C.

Analog Input

Number of channels	4, single-ended, simultaneously sampled
Input impedance	460 kΩ in parallel with 75 pF
Input coupling	AC or DC
Resolution	16 bits
Signal range	±2.828 V (2 Vrms)
Maximum input voltage	±20 V (powered on or off)
Gain adjustment range	±3.5% (±0.3 dB)
Offset error (after calibration)	±15 LSB maximum ±5 LSB typical
Amplitude flatness	(see also Figure A-1)
AT-2150C	±0.025 dB maximum, DC to 20 kHz ±0.01 dB typical (48 kHz sampling rate)
AT-A2150S	±0.025 dB maximum, DC to 4 kHz ±0.01 dB typical (24 kHz sampling rate) ±0.05 dB, DC to 10 kHz AC coupling -3 dB cutoff at 8.8 Hz
Phase linearity	±0.5°, DC to 20 kHz
Interchannel phase	±1°, DC to 20 kHz (see also Figure A-2)
Signal delay (time from when signal enters analog input until sample data is latched into the FIFO)	35.6 sample periods, any sample rate
Total harmonic distortion (THD)	-95 dB for 0 dB input, DC to 22 kHz
Signal-to-THD+noise	90 dB for 0 dB input, DC to 22 kHz
Intermodulation distortion (IMD)	
48 kHz sample rate	
SMPTE (60 Hz, 7 kHz)	-85 dB
DIN (250 Hz, 8 kHz)	-85 dB
CCIF (14 kHz, 15 kHz)	-95 dB

Dynamic range (maximum signal-to-noise ratio)	93 dB
Crosstalk (channel separation)	-90 dB, DC to 22 kHz
Bandwidth (-3 dB)	0.45 times sampling rate
Sampling rates	
AT-A2150S	2, 2.5, 3, 4, 5, 6, 8, 10, 12, 16, 20, 24 kHz
AT-A2150C	4, 5.5125, 6, 6.4, 8, 11.025, 12, 12.8, 16, 22.05, 24, 25.6, 32, 44.1, 48, 51.2 kHz

Digital Trigger

Input level	TTL-compatible
Response	Falling edge
Minimum pulse width	50 nsec
Output level	TTL-compatible
High-level output current	-3.2 mA
Low-level output current	24.0 mA

Power Requirement (from PC AT I/O Channel)

Power consumption	1.5 A at +5 VDC

Physical

Board dimensions	13.25 in. by 4.5 in.
I/O connector	5 RCA phono jacks

Operating Environment

Component temperature	0° to 70° C
Relative humidity	5% to 90% noncondensing

Storage Environment

Temperature	-55° to 150° C
Relative humidity	5% to 90% noncondensing

Performance Plots

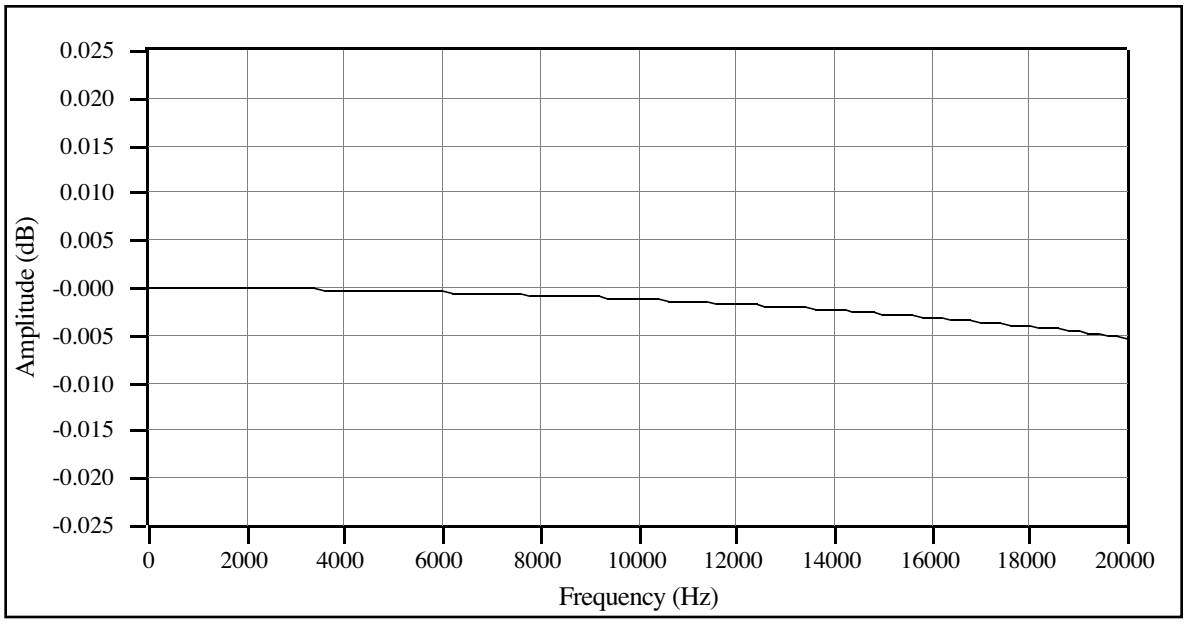


Figure A-1. Analog Input Frequency Response (Typical)

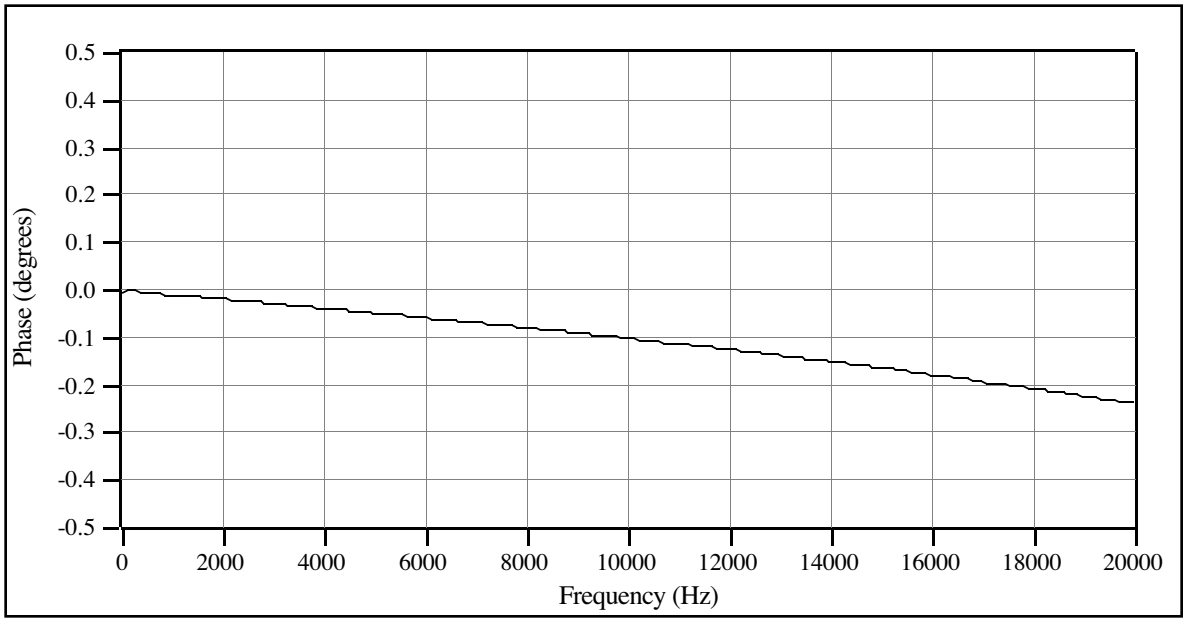


Figure A-2. Analog Input Interchannel Phase (Typical)

Appendix B
Connectors

This appendix describes the pinout and signal names for the I/O connector and the RTSI connector on the AT-A2150.

Figure B-1 shows the AT-A2150 I/O connector.

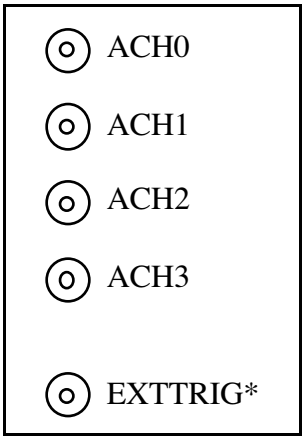


Figure B-1. AT-A2150 I/O Connector Signal Assignments

Detailed signal specifications are included in Chapter 2, *Configuration and Installation,* and in Appendix A, *Specifications*.

Figure B-2 shows the AT-A2150 RTSI connector.

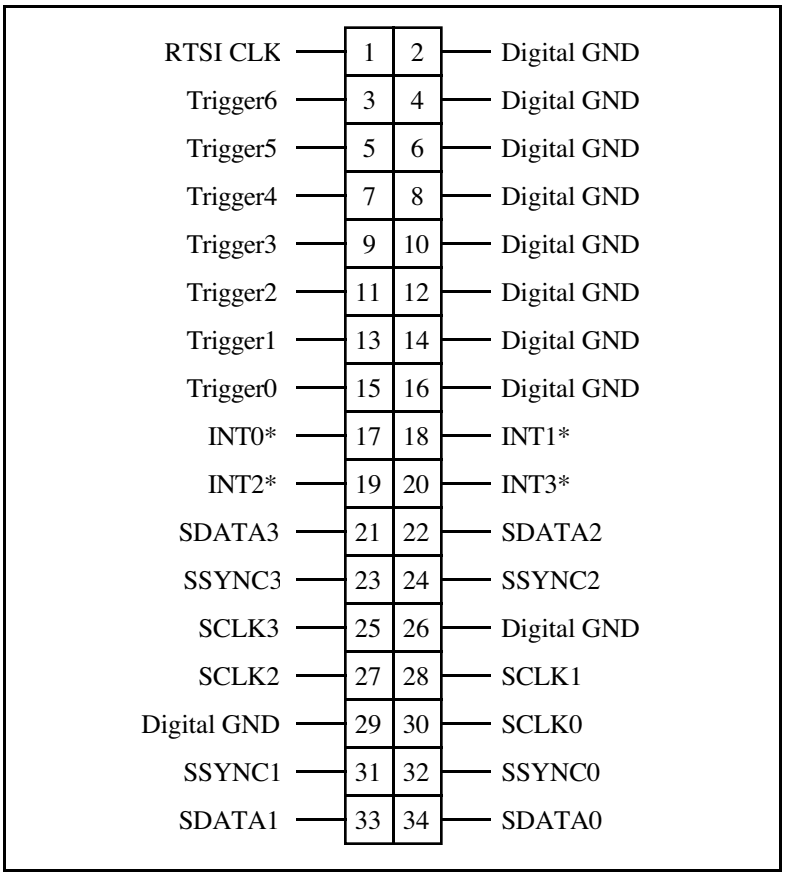


Figure B-2. AT-A2150 RTSI Connector Signal Assignments

Appendix C
MSM82C53 Data Sheet*

This appendix contains the *MSM82C53 Programmable Interval Timer* (Oki Semiconductor) data sheet. This counter/timer is used on the AT-A2150.

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Oki Semiconductor. *Microprocessor Data Book* 1990/1991.

OKI semiconductor

MSM82C53-2RS/GS/JS

CMOS PROGRAMMABLE INTERVAL TIMER

GENERAL DESCRIPTION

The MSM82C53-2RS/GS/JS are programmable universal timers designed for use in microcomputer systems. Based on silicon gate CMOS technology, it requires a standby current of only 100μA (max.) when the chip is in the nonselected state. During timer operation, power consumption is still very low with only 8 mA (max.) at 8 MHz of current required.

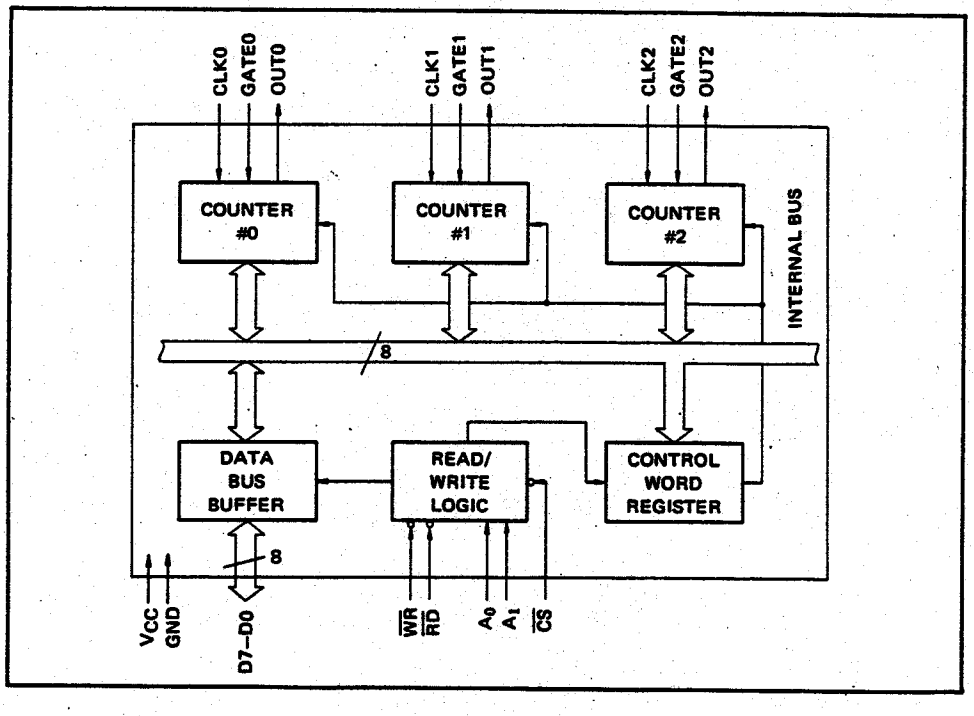
The devices consist of three independent counters, and can count up to a maximum of 8 MHz (MSM82C53-2) The timer features six different counter modes, and binary count/BCD count functions. Count values can be set in byte or word units, and all functions are freely programmable.

FEATURES

- Maximum operating frequency of 8 MHz (MSM82C53-2)
- High speed and low power consumption achieved through silicon gate CMOS technology.
- Completely static operation
- Three independent 16-bit down-counters
- 3V to 6V single power supply
- Six counter modes available for each counter
- Binary and decimal counting possible
- 24 pin Plastic DIP (DIP24-P-600)
- 28 pin PLCC (QFJ28-P-S450)
- 32 pin-V Plastic SOP (SSOP32-P-430-VK)

5

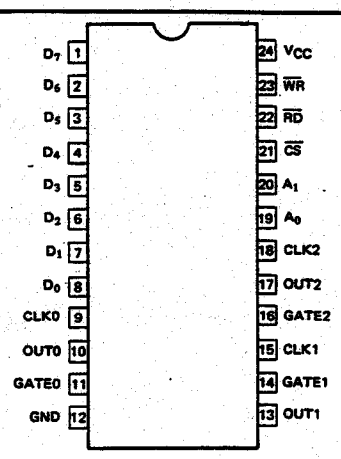
FUNCTIONAL BLOCK DIAGRAM



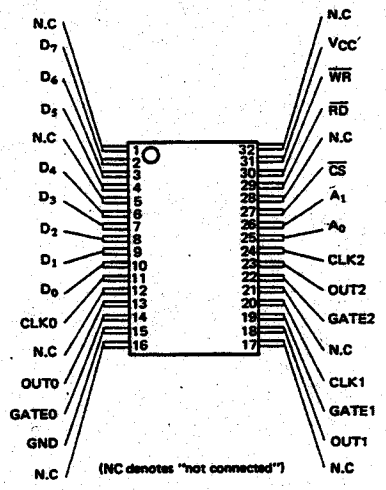
MSM82C53-2RS/GS/JS

PIN CONFIGURATION

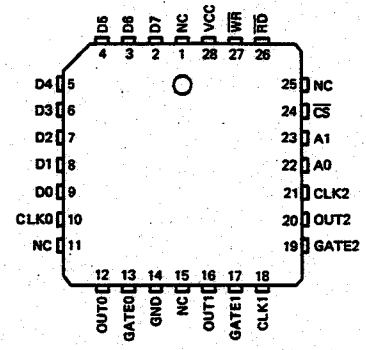
MSM82C53-2RS (Top View)
24 pin Plastic DIP



MSM82C53-2GS (Top View)
32 pin Plastic Small Outine Package



MSM82C53-2JS (Top View)
28 pin Plastic Leaded Chip Carrier



5

■ I/O-MSM82C53-2RS/GS/JS ■

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits			Unit
			MSM82C53-2RS	MSM82C53-2GS	MSM82C53-2JS	
Ssupply Voltage	V_{CC}	Respect to GND	−0.5 to +7			V
Input Voltage	V_{IN}		−0.5 to V_{CC} + 0.5			V
Output Voltage	V_{OUT}		−0.5 to V_{CC} + 0.5			V
Storage Temperature	T_{stg}		−55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	0.9	0.7	0.9	W

OPERATING RANGES

Parameter	Symbol	Limits	Conditions	Unit
Supply Voltage	V_{CC}	3 to 6	V_{IL} = 0.2V, V_{IH} = V_{CC} − 0.2V, operating frequency 2.6 MHz	V
Operating Temperature	T_{OP}	−40 to +85		°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL}	−0.3		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" Output Voltage	V_{OL}	I_{OL} = 4mA				0.45	V
"H" Output Voltage	V_{OH}	I_{OH} = −1mA		3.7			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$	V_{CC}=4.5V to 5.5V	−10		10	μA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$	Ta=−40°C to +85°C	−10		10	μA
Standby Supply Current	I_{CCS}	$\overline{CS} \geq V_{CC}$ −0.2V $V_{IH} \geq V_{CC}$ − 0.2V $V_{IL} \leq$ 0.2V				100	μA
Operating Supply Current	I_{CC}	t_{CLK} = 125 ns C_L = 0pF				8	mA

AC CHARACTERISTICS

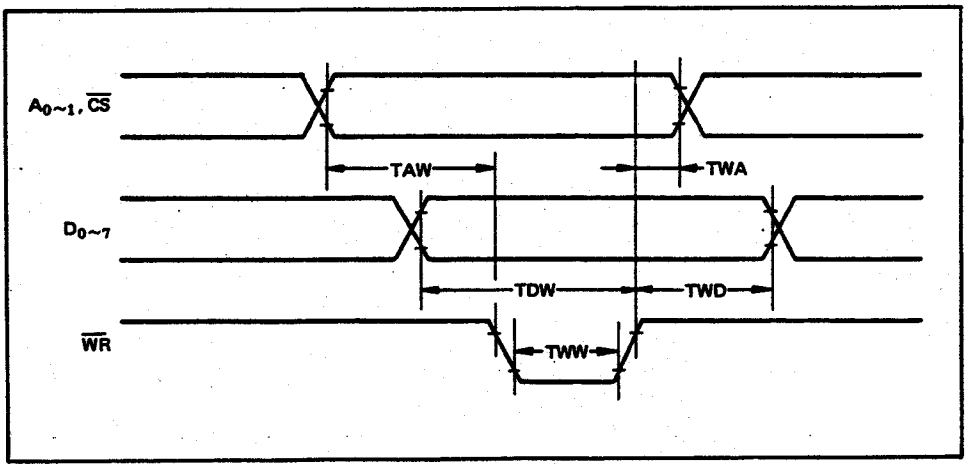
(V_{CC} = 4.5V ~ 5.5V, Ta = –40 ~ +85°C)

Parameter	Symbol	MSM82C53-2 Min.	MSM82C53-2 Max.	Unit	Conditions	
Address Set-up Time before reading	TAR	30		ns	Read cycle	C_L = 150pF
Address Hold Time after reading	TRA	0		ns		
Read Pulse Width	TRR	150		ns		
Read Recovery Time	TRVR	200		ns		
Address Set-up Time before writing	TAW	0		ns	Write cycle	
Address Hold Time after writing	TWA	20		ns		
Write Pulse Width	TWW	150		ns		
Data Input Set-up Time before writing	TDW	100		ns		
Data Input Hold Time after writing	TWD	20		ns		
Write Recovery time	TRVW	200		ns		
Clock Cycle Time	TCLK	125	D.C.	ns	Clock and gate timing	
Clock "H" Pulse Width	TPWH	60		ns		
Clock "L" Pulse Width	TPWL	60		ns		
"H" Gate Pulse Width	TGW	50		ns		
"L" Gate Pulse Width	TGL	50		ns		
Gate Input Set-up Time before clock	TGS	50		ns		
Gate Input Hold Time after clock	TGH	50		ns		
Output Delay Time after reading	TRD		120	ns	Delay time	
Output Floating Delay Time after reading	TDF	5	90	ns		
Output Delay Time after gate	TODG		120	ns		
Output Delay Time after clock	TOD		150	ns		
Output Delay Time after address	TAD		180	ns		

Note: Timing measured at V_L = 0.8V and V_H = 2.2V for both inputs and outputs.

TIME CHART

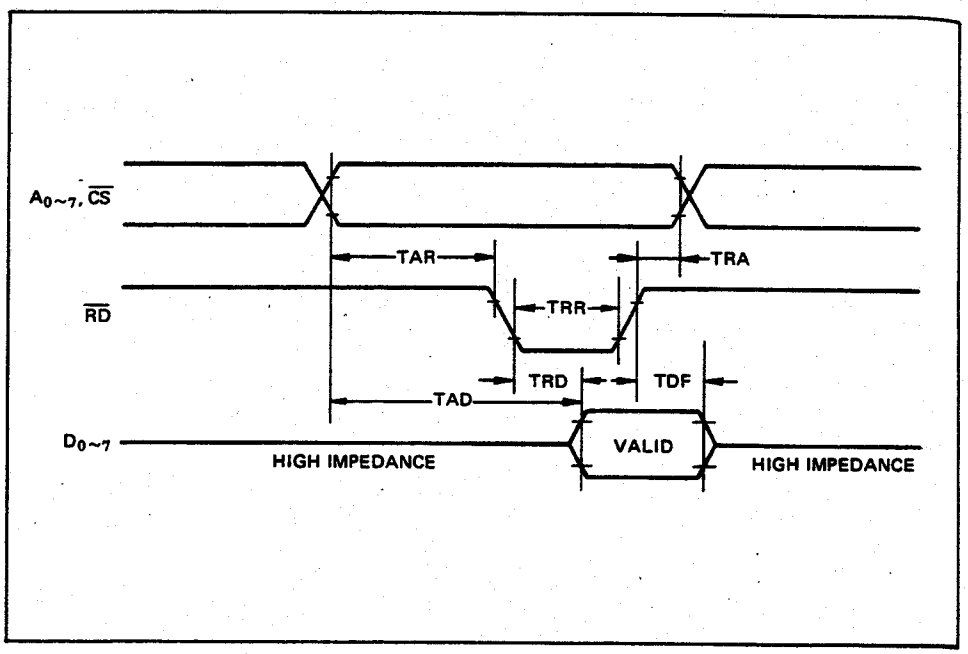
Write Timing



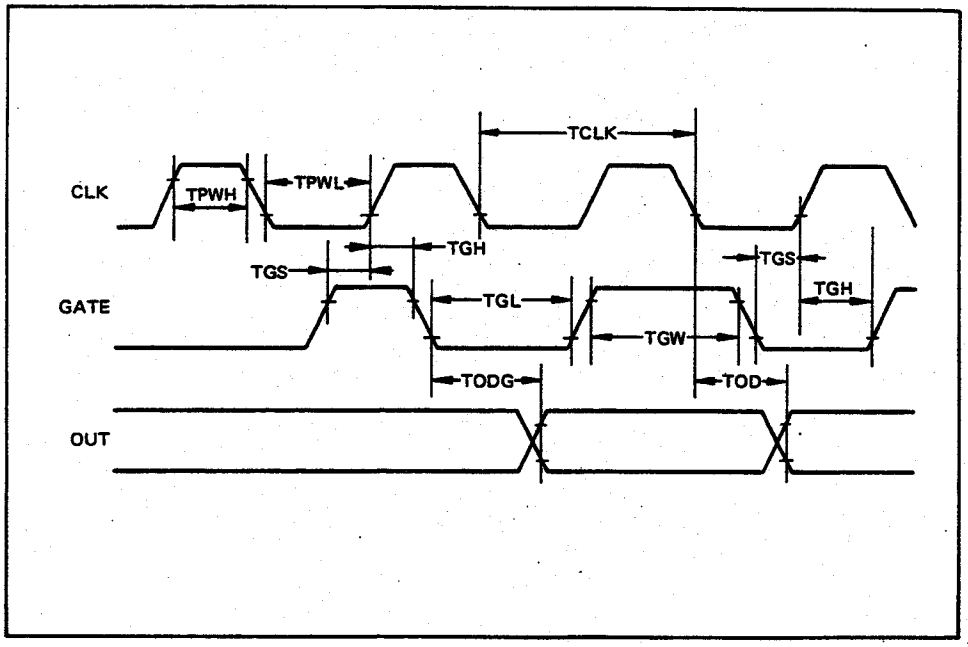
5

■ MSM82C53-2RS/GS/JS ■

Read Timing



Clock & Gate Timing



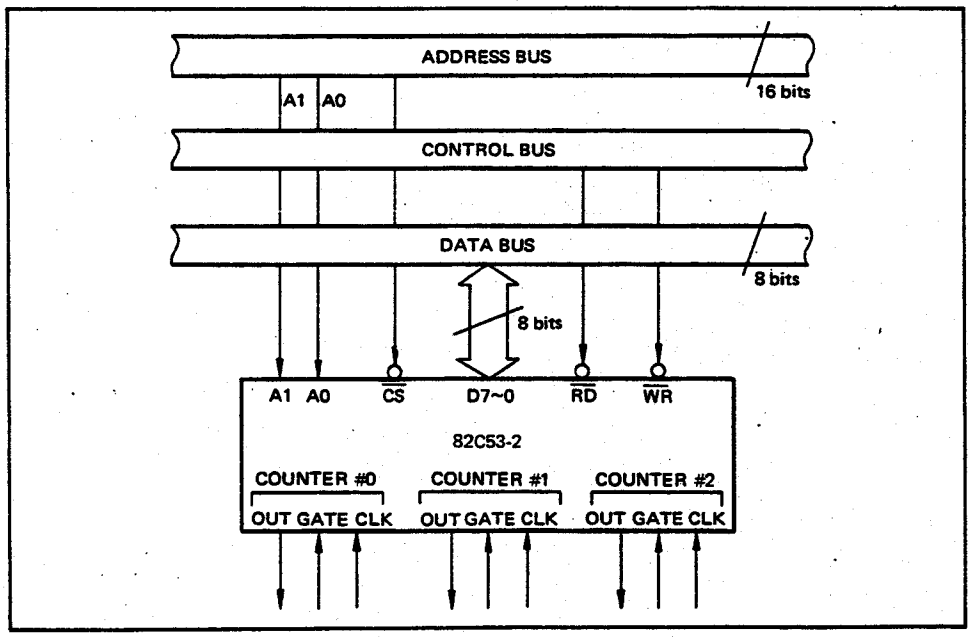
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DESCRIPTION OF PIN FUNCTIONS

Pin Symbol	Name	Input/output	Function
D7 ~ D0	Bidirectional data bus	Input/output	Three-state 8-bit bidirectional data bus used when writing control words and count values, and reading count values upon reception of $\overline{WR}$ and $\overline{RD}$ signals from CPU.
$\overline{CS}$	Chip select input	Input	Data transfer with the CPU is enabled when this pin is at low level. When at high level, the data bus (D_0 thru D_7) is switched to high impedance state where neither writing nor reading can be executed. Internal registers, however, remain unchanged.
$\overline{RD}$	Read input	Input	Data can be transferred from MSM82C53 to CPU when this pin is at low level.
$\overline{WR}$	Write input	Input	Data can be transferred from CPU to MSM82C53 when this pin is at low level.
A0, A1	Address input	Input	One of the three internal counters or the control word register is selected by A0/A1 combination. These two pins are normally connected to the two lower order bits of the address bus.
CLK0~2	Clock input	Input	Supply of three clock signals to the three counters incorporated in MSM82C53.
GATE0~2	Gate input	Input	Control of starting, interruption, and restarting of counting in the three respective counters in accordance to the set control word contents.
OUT0~2	Counter output	Output	Output of counter output waveform in accordance with the set mode and count value.

SYSTEM INTERFACING



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■ I/O-MSM82C53-2RS/GS/JS ■

DESCRIPTION OF BASIC OPERATIONS

Data transfers between the internal registers and the external data bus is outlined in the following table.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	Function
0	1	0	0	0	Data bus to counter #0 Writing
0	1	0	0	1	Data bus to counter #1 Writing
0	1	0	1	0	Data bus to counter #2 Writing
0	1	0	1	1	Data bus to control word register Writing
0	0	1	0	0	Data bus from counter #0 Reading
0	0	1	0	1	Data bus from counter #1 Reading
0	0	1	1	0	Data bus from counter #2 Reading
0	0	1	1	1	Data bus in high impedance status
1	x	x	x	x	
0	1	1	x	x	

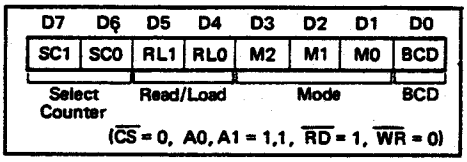
x denotes "not specified".

DESCRIPTION OF OPERATION

82C53 functions are selected by a control word from the CPU. In the required program sequence, the control word setting is followed by the count value setting and execution of the desired timer operation.

Control Word and Count Value Program

Each counter operation mode is set by control word programming. The control word format is outlined below.



- **Select Counter (SC0, SC1):** Selection of set counter

SC1	SC0	Set Contents
0	0	Counter #0 selection
0	1	Counter #1 selection
1	0	Counter #2 selection
1	1	Illegal combination

- **Read/Load (RL1, RL0):** Count value Reading/Loading format setting

RL1	RL0	Set Contents
0	0	Counter Latch operation
0	1	Reading/Loading of Least Significant byte (LSB)
1	0	Reading/Loading of Most Significant byte (MSB)
1	1	Reading/Loading of LSB followed by MSB

- **Mode (M2, M1, M0):** Operation waveform mode setting

M2	M1	M0	Set Contents
0	0	0	Mode 0 (Interrupt on Terminal Count)
0	0	1	Mode 1 (Programmable One-Shot)
x	1	0	Mode 2 (Rate Generator)
x	1	1	Mode 3 (Square Wave Generator)
1	0	0	Mode 4 (Software Triggered Strobe)
1	0	1	Mode 5 (Hardware Triggered Strobe)

x denotes "not specified".

- **BCD:** Operation count mode setting

BCD	Set Contents
0	Binary Count (16-bits Binary)
1	BCD Count (4-decades Binary Coded Decimal)

After setting Read/Load, Mode, and BCD in each counter as outlined above, next set the desired count value. (In some Modes, counting is started immediately after the count value has been written). This count value setting must conform with the Read/Load format set in advance. Note that the internal counters are reset to OOOOH during control word setting. The counter value (OOOOH) can.t be read.

If the two bytes (LSB and MSB) are written at this stage (RL0 and RL1 = 1,1), take note of the following precaution.

Although the count values may be set in the three counters in any sequence after the control word has been set in each counter, count values must be set consecutively in the LSB – MSB order in any one counter.

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I/O-MSM82C53-2RS/GS/JS

- **Example of control word and count value setting**

Counter #0: Read/Load LSB only, Mode 3, Binary count, count value 3H
Counter #1: Read/Load MSB only, Mode 5, Binary count, count value AA00H
Counter #2: Read/Load LSB and MSB, Mode 0, BCD count, count value 1234

```
MVI A, 1EH
OUT n3          Counter #0 control word setting
MVI A, 6AH
OUT n3          Counter #1 control word setting
MVI A, B1H
OUT n3          Counter #2 control word setting
MVI A, 03H
OUT n0          Counter #0 count value setting
MVI A, AAH
OUT n1          Counter #1 count value setting
MVI A, 34H
OUT n2          Counter #2 count value setting
MVI A, 12H      (LSB then MSB)
OUT n2
```

Note: n0: Counter #0 address
n1: Counter #1 address
n2: Counter #2 address
n3: Control word register address

- **The minimum and maximum count values which can be counted in each mode are listed below.**

Mode	Min.	Max.	Remarks
0	1	0	0 executes 10000H count (ditto in other modes)
1	1	0	
2	2	0	1 cannot be counted
3	2	1	1 executes 10001H count
4	1	0	
5	1	0	

Mode Definition

- **Mode 0 (terminal count)**

The counter output is set to "L" level by the mode setting. If the count value is then written in the counter with the gate input at "H" level (that is, upon completion of writing the MSB when there are two bytes), the clock input counting is started. When the terminal count is reached, the output is switched to "H" level and is maintained in this status until the control word and count value are set again.
Counting is interrupted if the gate input is switched to "L" level, and restarted when switched back to "H" level.
When Count Values are written during counting, the operation is as follows:

1 byte Read/Load.... When the new count value is written, counting is stopped immediately, and then restarted at the new count value by the next clock.

2-byte Read/Load.... When byte 1 (LSB) of the new count value is written, counting is stopped immediately. Counting is restarted at the new count value when byte 2 (MSB) is written.

- **Mode 1 (programmable one-shot)**

The counter output is switched to "H" level by the mode setting. Note that in this mode, counting is not started if only the count value is written. Since counting has to be started in this mode by using the leading edge of the gate input as a trigger, the counter output is switched to "L" level by the next clock after the gate input trigger. This "L" level status is maintained during the set count value, and is switched back to "H" level when the terminal count is reached.
Once counting has been started, there is no interruption until the terminal count is reached, even if the gate input is switched to "L" level in the meantime. And although counting continues even if a new count value is written during the counting, counting is started at the new count value if another trigger is applied by the gate input.

- **Mode 2 (rate generator)**

The counter output is switched to "H" level by the mode setting. When the gate input is at "H" level, counting is started by the next clock after the count value has been written. And if the gate input is at "L" level, counting is started by using the rising edge of the gate input as a trigger after the count value has been set.
An "L" level output pulse appears at the counter output during a single clock duration once every n clock inputs where n is the set count value. If a new count value is written during while counting is in progress, counting is started at the new count value following output of the pulse currently being counted. And if the gate input is switched to "L" level during counting, the counter output is forced to switch to "H" level, the counting being restarted by the rising edge of the gate input.

- **Mode 3 (square waveform rate generator)**

The counter output is switched to "H" level by the mode setting. Counting is started in the same way as described for mode 2 above.
The repeated square wave output appearing at the counter output contains half the number of counts as the set count value. If the set count value (n) is an odd number, the repeated square wave output consists of only (n + 1)/2 clock inputs at "H" level and (n – 1)/2 clock inputs at "L" level.
If a new count value is written during counting, the new count value is reflected immediately after the

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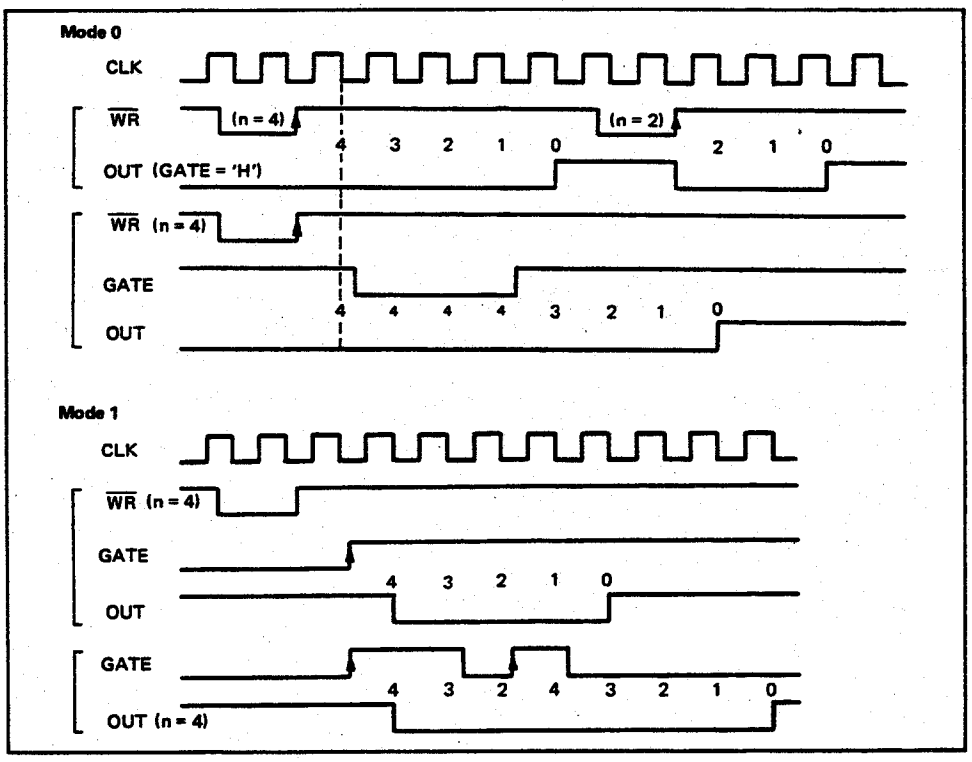
■ I/O-MSM82C53-2RS/GS/JS ■

change ("H" to "L" or "L" to "H") in the next counter output to be executed. The counting operation at the gate input is done the same as in mode 2.

- **Mode 4 (software trigger strobe)**
  The counter output is switched to "H" level by the mode setting. Counting is started in the same way as described for mode 0. A single "L" pulse equivalent to one clock width is generated at the counter output when the terminal count is reached.
  This mode differs from 2 in that the "L" level output appears one clock earlier in mode 2, and that pulses are not repeated in mode 4. Counting is stopped when the gate input is switched to "L" level, and restarted from the set count value when switched back to "H" level.

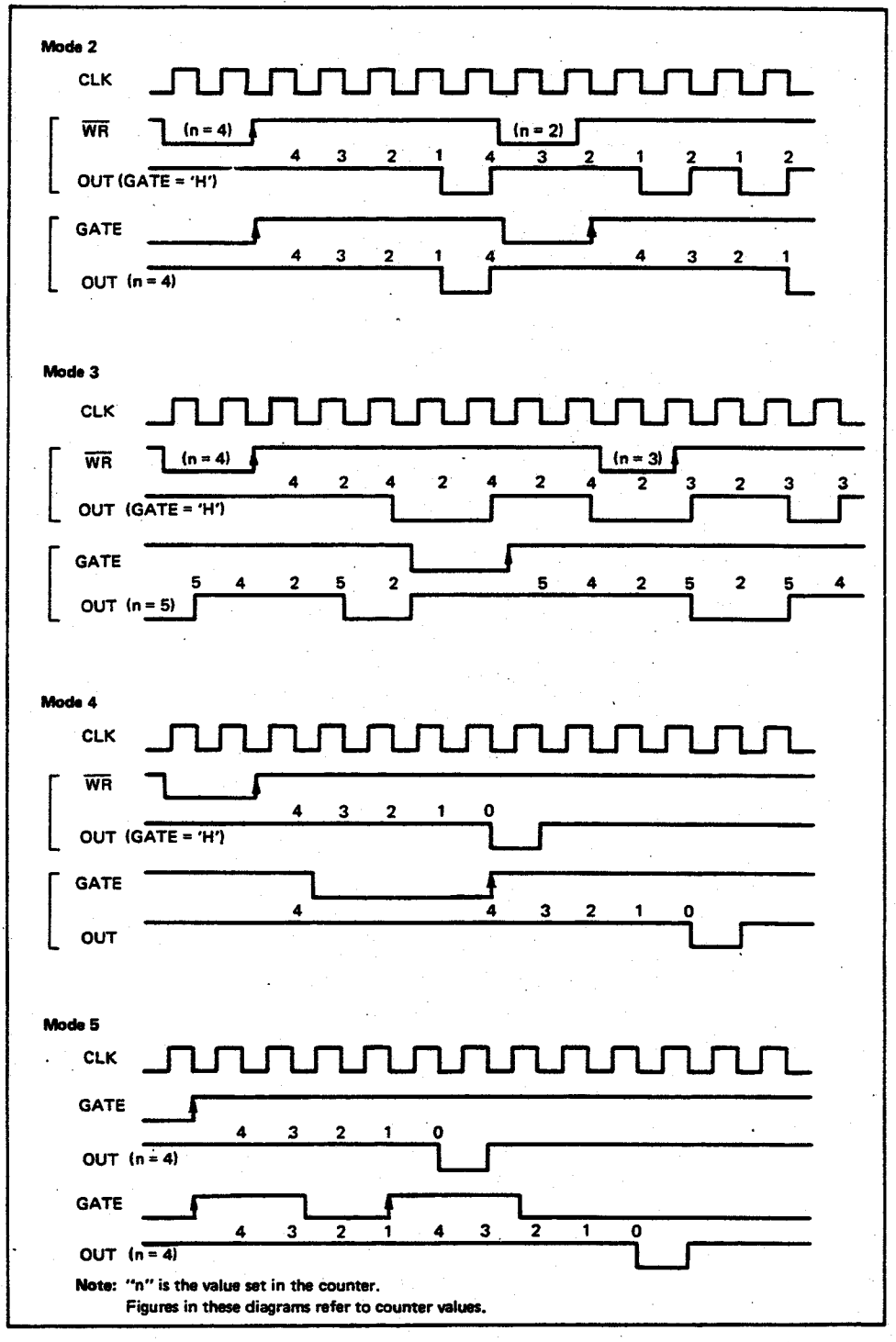
- **Mode 5 (hardware trigger strobe)**
  The counter output is switched to "H" level by the mode setting. Counting is started, and the gate input used, in the same way as in mode 1.
  The counter output is identical to the mode 4 output.
  The various roles of the gate input signals in the above modes are summarized in the following table.

Mode \ Gate	"L" Level Falling Edge	Rising Edge	"H" Level
0	Counting not possible		Counting possible
1		(1) Start of counting (2) Retriggering	
2	(1) Counting not possible (2) Counter output forced to "H" level	Start of counting	Counting possible
3	(1) Counting not possible (2) Counter output forced to "H" level	Start of counting	Counting possible
4	Counting not possible		Counting possible
5		(1) Start of counting (2) Retriggering	



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■ I/O-MSM82C53-2RS/GS/JS ■



Note: "n" is the value set in the counter.
Figures in these diagrams refer to counter values.

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■ I/O-MSM82C53-2RS/GS/JS ■

Reading of Counter Values

All 82C53 counting is down-counting, the counting being in steps of 2 in mode 3. Counter values can be read during counting by (1) direct reading, and (2) counter latching ("read on the fly").

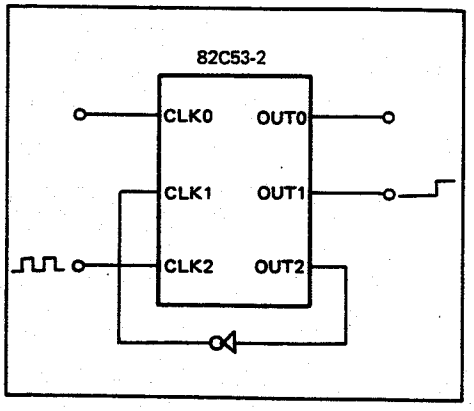
- **Direct reading**
  Counter values can be read by direct reading operations.
  Since the counter value read according to the timing of the $\overline{RD}$ and CLK signals is not guaranteed, it is necessary to stop the counting by a gate input signal, or to interrupt the clock input temporarily by an external circuit to ensure that the counter value is correctly read.

- **Counter latching**
  In this method, the counter value is latched by writing a counter latch command, thereby enabling a stable value to be read without effecting the counting in any way at all. An example of a counter latching program is given below.
  Counter latching executed for counter #1 (Read/Load 2-byte setting)

```
MVI A  01 00 xxxx
              └── Denotes counter latching
OUT n3 ──┬── Write in control word address (n3)
         └── The counter value at this point is latched
IN n1  ──┬── Reading of the LSB of the counter value latched from counter #1.
         └── n1: Counter #1 address
MOV B, A
IN n1  ──── Reading of MSB from counter #1.
MOV C, A
```

Example of Practical Application

- 82C53 used as a 32-bit counter.



Use counter #1 and counter #2

Counter #1: mode 0, upper order 16-bit counter value

Counter #2: mode 2, lower order 16-bit counter value

This setting enables counting up to a maximum of 2^{32}.

5

Appendix D
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Italy	02/48301892	02/48301915
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Operating system _____

Speed _____MHz RAM _____MB Display adapter _____

Mouse _____yes _____no Other adapters installed _____

Hard disk capacity _____MB Brand _____

Instruments used _____

National Instruments hardware product model _____ Revision _____

Configuration _____

National Instruments software product _____ Version _____

Configuration _____

The problem is _____

_____

_____

_____

_____

List any error messages _____

_____

_____

_____

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The following steps will reproduce the problem _____

_____

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