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DAQ

AT E Series User Manual

Multifunction I/O Devices for the PC AT

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Worldwide Technical Support and Product Information

ni.com

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Compliance

FCC/Canada Radio Frequency Interference Compliance*

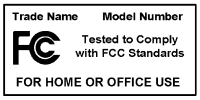
Determining FCC Class

The Federal Communications Commission (FCC) has rules to protect wireless communications from interference. The FCC places digital electronics into two classes. These classes are known as Class A (for use in industrial-commercial locations only) or Class B (for use in residential or commercial locations). Depending on where it is operated, this product could be subject to restrictions in the FCC rules. (In Canada, the Department of Communications (DOC), of Industry Canada, regulates wireless interference in much the same way.)

Digital electronics emit weak signals during normal operation that can affect radio, television, or other wireless products. By examining the product you purchased, you can determine the FCC Class and therefore which of the two FCC/DOC Warnings apply in the following sections. (Some products may not be labeled at all for FCC; if so, the reader should then assume these are Class A devices.)

FCC Class A products only display a simple warning statement of one paragraph in length regarding interference and undesired operation. Most of our products are FCC Class A. The FCC rules have restrictions regarding the locations where FCC Class A products can be operated.

FCC Class B products display either a FCC ID code, starting with the letters **EXN**, or the FCC Class B compliance mark that appears as shown here on the right.



Consult the FCC Web site at `http://www.fcc.gov` for more information.

FCC/DOC Warnings

This equipment generates and uses radio frequency energy and, if not installed and used in strict accordance with the instructions in this manual and the CE Mark Declaration of Conformity**, may cause interference to radio and television reception. Classification requirements are the same for the Federal Communications Commission (FCC) and the Canadian Department of Communications (DOC).

Changes or modifications not expressly approved by National Instruments could void the user's authority to operate the equipment under the FCC Rules.

Class A

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Canadian Department of Communications

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe A respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Class B

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Canadian Department of Communications

This Class B digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe B respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Compliance to EU Directives

Readers in the European Union (EU) must refer to the Manufacturer's Declaration of Conformity (DoC) for information** pertaining to the CE Mark compliance scheme. The Manufacturer includes a DoC for most every hardware product except for those bought for OEMs, if also available from an original manufacturer that also markets in the EU, or where compliance is not required as for electrically benign apparatus or cables.

To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by your product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

* Certain exemptions may apply in the USA, see FCC Rules §15.103 **Exempted devices**, and §15.105(c). Also available in sections of CFR 47.

** The CE Mark Declaration of Conformity will contain important supplementary information and instructions for the user or installer.

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About This Manual

This manual describes the electrical and mechanical aspects of each device in the AT E Series product line and contains information concerning their operation and programming. Unless otherwise noted, text applies to all devices in the AT E Series.

The AT E Series includes the following devices:

- AT-MIO-16E-1
- AT-MIO-16E-2
- AT-MIO-64E-3
- AT-MIO-16E-10
- AT-MIO-16DE-10
- AT-MIO-16XE-10
- AT-AI-16XE-10
- AT-MIO-16XE-50

The AT E Series devices are high-performance multifunction analog, digital, and timing I/O devices for the PC AT series computers. Supported functions include analog input (AI), analog output (AO), digital I/O (DIO), and timing I/O (TIO).

Conventions

The following conventions appear in this manual:

<> — Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DIO<3..0>.

♦ — The ♦ symbol indicates that the following text applies only to a specific product, a specific operating system, or a specific software version.

 — This icon denotes a note, which alerts you to important information.

 — This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on the device, see the *Safety Information* section of Chapter 1, *Introduction*, for precautions to take.

bold	Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names.
italic	Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.
NI-DAQ	NI-DAQ refers to the NI-DAQ software for PC compatibles unless otherwise noted.
PC	PC refers to the PC AT series computers.
SCXI	SCXI stands for Signal Conditioning eXtensions for Instrumentation and is a National Instruments product line designed to perform front-end signal conditioning for NI plug-in DAQ devices.

National Instruments Documentation

The *AT-MIO/AI E Series User Manual* is one piece of the documentation set for the DAQ system. You could have any of several types of manuals depending on the hardware and software in the system. Use the manuals you have as follows:

- *Getting Started with SCXI*—If you are using SCXI, this is the first manual you should read. It gives an overview of the SCXI system and contains the most commonly needed information for the modules, chassis, and software.
- The SCXI hardware user manuals—If you are using SCXI, read these manuals next for detailed information about signal connections and module configuration. They also explain in greater detail how the module works and contain application hints.
- *SCXI Chassis Manual*—If you are using SCXI, read this manual for maintenance information on the chassis and installation instructions.
- The DAQ hardware user manuals—These manuals have detailed information about the DAQ hardware that plugs into or is connected to the computer. Use these manuals for hardware installation and configuration instructions, specification information about the DAQ hardware, and application hints.
- Software documentation—Examples of software documentation you may have are the LabVIEW and LabWindows/CVI documentation sets and the NI-DAQ documentation. After you set up the hardware system, use either the application software (LabVIEW or LabWindows/CVI)

or the NI-DAQ documentation to help you write your application. If you have a large and complicated system, it is worthwhile to look through the software documentation before you configure the hardware.

- Accessory installation guides or manuals—If you are using accessory products, read the terminal block and cable assembly installation guides. They explain how to physically connect the relevant pieces of the system. Consult these guides when you are making the connections.

Related Documentation

The following documents contain information that you might find helpful as you read this manual:

- *AT E Series Register-Level Programmer Manual*
- *DAQ-STC Technical Reference Manual*
- NI Developer Zone tutorial, *Field Wiring and Noise Considerations for Analog Signals*, at `ni.com/zone`

1

Introduction

This chapter describes the AT E Series devices, lists what you need to get started, describes the optional software and optional equipment, and explains how to unpack the AT E Series device.

About the AT E Series

Thank you for buying an NI AT E Series device. The AT E Series devices are the first completely Plug and Play-compatible multifunction analog, digital, and timing I/O devices for the PC AT and compatible computers. This family of devices features 12-bit and 16-bit ADCs with 16 and 64 analog inputs, 12-bit and 16-bit DACs with voltage outputs, eight and 32 lines of TTL-compatible DIO, and two 24-bit counter/timers for TIO. Because the AT E Series devices have no DIP switches, jumpers, or potentiometers, they are easily configured and calibrated using software.

The AT E Series devices are the first completely switchless and jumperless data acquisition (DAQ) devices. This feature is made possible by the National Instruments DAQ-PnP bus interface chip that connects the device to the AT I/O bus. The DAQ-PnP implements the Plug and Play ISA Specification so that the DMA, interrupts, and base I/O addresses are all software configurable. This allows you to easily change the AT E Series device configuration without having to remove the device from the computer. The DAQ-STC makes possible such applications as buffered pulse generation, equivalent time sampling, and seamlessly changing the sampling rate.

The AT E Series devices use the National Instruments DAQ-STC system timing controller for time-related functions. The DAQ-STC consists of three timing groups that control AI, AO, and general-purpose counter/timer functions. These groups include a total of seven 24-bit and three 16-bit counters and a maximum timing resolution of 50 ns.

A common problem with DAQ devices is that you cannot easily synchronize several measurement functions to a common trigger or timing event. The AT E Series devices have the Real-Time System Integration (RTSI) bus to solve this problem. The RTSI bus consists of the RTSI bus

interface and a ribbon cable to route timing and trigger signals between several functions on as many as five DAQ devices in the PC.

The AT E Series devices can interface to an SCXI system so that you can acquire over 3,000 analog signals from thermocouples, RTDs, strain gauges, voltage sources, and current sources. You can also acquire or generate digital signals for communication and control. SCXI is the instrumentation front end for plug-in DAQ devices.

Detailed specifications of the AT E Series devices are in Appendix A, *Specifications*.

What You Need to Get Started

To set up and use the AT E Series device, you need the following:

- ❑ One of the following devices:
  - AT-MIO-16E-1 (NI 6070E) for ISA
  - AT-MIO-16E-2 (NI 6060E) for ISA
  - AT-MIO-64E-3 (NI 6061E) for ISA
  - AT-MIO-16E-10 (NI 6020E) for ISA
  - AT-MIO-16DE-10 (NI 6021E) for ISA
  - AT-MIO-16XE-10 (NI 6030E) for ISA
  - AT-AI-16XE-10 (NI 6032E) for ISA
  - AT-MIO-16XE-50 (NI 6011E) for ISA
- ❑ *AT E Series User Manual*
- ❑ One of the following software packages and documentation
  - LabVIEW for Windows
  - Measurement Studio
  - NI-DAQ for PC Compatibles
  - VI Logger
- ❑ A computer

Software Programming Choices

When programming National Instruments DAQ hardware, you can use an NI application development environment (ADE) or other ADEs. In either case, you use NI-DAQ.

NI-DAQ

NI-DAQ, which shipped with the AT E Series device, has an extensive library of functions that you can call from the ADE. These functions allow you to use all the features of the AT E Series device.

NI-DAQ carries out many of the complex interactions, such as programming interrupts, between the computer and the DAQ hardware. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to the code. Whether you are using LabVIEW, Measurement Studio, or other ADEs, your application uses NI-DAQ, as illustrated in Figure 1-1.

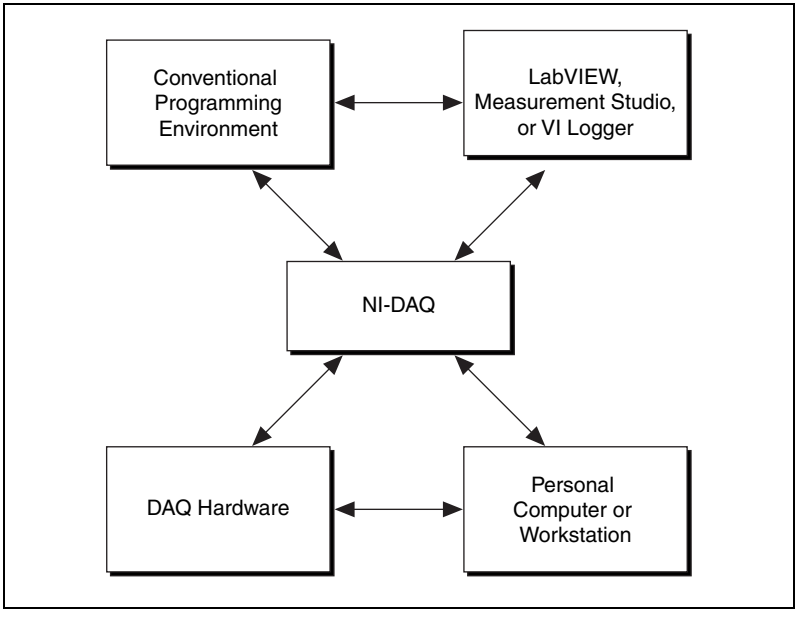


Figure 1-1. The Relationship Between the Programming Environment, NI-DAQ, and the Hardware

To download a free copy of the most recent version of NI-DAQ, click **Download Software** at `ni.com`.

National Instruments ADE Software

LabVIEW features interactive graphics, a state-of-the-art interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

Measurement Studio, which includes LabWindows/CVI, tools for Visual C++, and tools for Visual Basic, is a development suite that allows you to use ANSI C, Visual C++, and Visual Basic to design the test and measurement software. For C developers, Measurement Studio includes LabWindows/CVI, a fully integrated ANSI C application development environment that features interactive graphics and the LabWindows/CVI Data Acquisition and Easy I/O libraries. For Visual Basic developers, Measurement Studio features a set of ActiveX controls for using National Instruments DAQ hardware. These ActiveX controls provide a high-level programming interface for building virtual instruments. For Visual C++ developers, Measurement Studio offers a set of Visual C++ classes and tools to integrate those classes into Visual C++ applications. The libraries, ActiveX controls, and classes are available with Measurement Studio and NI-DAQ.

Using LabVIEW or Measurement Studio greatly reduces the development time for your data acquisition and control application.

Register-Level Programming

The final option for programming any National Instruments DAQ hardware is to write register-level software. Writing register-level programming software can be very time-consuming and inefficient and is not recommended for most users.

Even if you are an experienced register-level programmer, consider using NI-DAQ, LabVIEW, or LabWindows/CVI to program the National Instruments DAQ hardware. Using the NI-DAQ, LabVIEW, or LabWindows/CVI software is as easy and as flexible as register-level programming and can save weeks of development time. For more information, refer to the *AT E Series Register-Level Programmer Manual*.

Optional Equipment

NI offers a variety of products to use with the AT E Series device, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies, shielded and ribbon
- Connector blocks, shielded and unshielded 50-, 68-, and 100-pin screw terminals
- RTSI bus cables
- SCXI modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output. With SCXI you can condition and acquire up to 3,072 channels.
- Low channel count signal conditioning modules, devices, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample and hold, and relays

For more specific information about these products, refer to `ni.com/catalog` or call the office nearest you.

Custom Cabling

National Instruments offers cables and accessories for you to prototype your application or to use if you frequently change device interconnections.

If you want to develop your own cable, however, the following guidelines may be useful:

- For the AI signals, shielded twisted-pair wires for each AI pair yield the best results, assuming that you use differential inputs. Tie the shield for each signal pair to the ground reference at the source.
- You should route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

Mating connectors and a backshell kit for making custom 68-pin cables are available from NI.

Unpacking

The AT E Series device is shipped in an antistatic package to prevent electrostatic damage to the device. Electrostatic discharge can damage several components on the device.

Caution *Never* touch the exposed pins of connectors.

To avoid such damage in handling the device, take the following precautions:

- Ground yourself using a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of the computer chassis before removing the device from the package.

Remove the device from the package and inspect the device for loose components or any sign of damage. Notify NI if the device appears damaged in any way. Do *not* install a damaged device into the computer.

Store the AT E Series device in the antistatic envelope when not in use.

Safety Information

The following section contains important safety information that you *must* follow during installation and use of the product.

Do *not* operate the product in a manner not specified in this document. Misuse of the product can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to NI for repair.

If the product is rated for use with hazardous voltages (>30 V_{rms}, 42.4 V_{pk}, or 60 V_{dc}), you may need to connect a safety earth-ground wire according to the installation instructions. Refer to Appendix A, *Specifications*, for maximum voltage ratings.

Do *not* substitute parts or modify the product. Use the product only with the chassis, modules, accessories, and cables specified in the installation instructions. You *must* have all covers and filler panels installed during operation of the product.

Do *not* operate the product in an explosive atmosphere or where there may be flammable gases or fumes. Operate the product only at or below the

pollution degree stated in Appendix A, *Specifications*. Pollution is foreign matter in a solid, liquid, or gaseous state that can produce a reduction of dielectric strength or surface resistivity. The following is a description of pollution degrees:

- Pollution degree 1 means no pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- Pollution degree 2 means that only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- Pollution degree 3 means that conductive pollution occurs, or dry, nonconductive pollution occurs, which becomes conductive due to condensation.

Clean the product with a soft nonmetallic brush. The product *must* be completely dry and free from contaminants before returning it to service.

You *must* insulate signal connections for the maximum voltage for which the product is rated. Do *not* exceed the maximum ratings for the product. Remove power from signal lines before connection to or disconnection from the product.

Operate this product only at or below the installation category stated in Appendix A, *Specifications*.

The following is a description of installation categories:

- Installation Category I is for measurements performed on circuits not directly connected to MAINS[1]. This category is a signal level such as voltages on a printed wire board (PWB) on the secondary of an isolation transformer.

  Examples of Installation Category I are measurements on circuits not derived from MAINS and specially protected (internal) MAINS-derived circuits.

- Installation Category II is for measurements performed on circuits directly connected to the low-voltage installation. This category refers to local-level distribution such as that provided by a standard wall outlet.

  Examples of Installation Category II are measurements on household appliances, portable tools, and similar equipment.

[1] MAINS is defined as the electricity supply system to which the equipment concerned is designed to be connected either for powering the equipment or for measurement purposes.

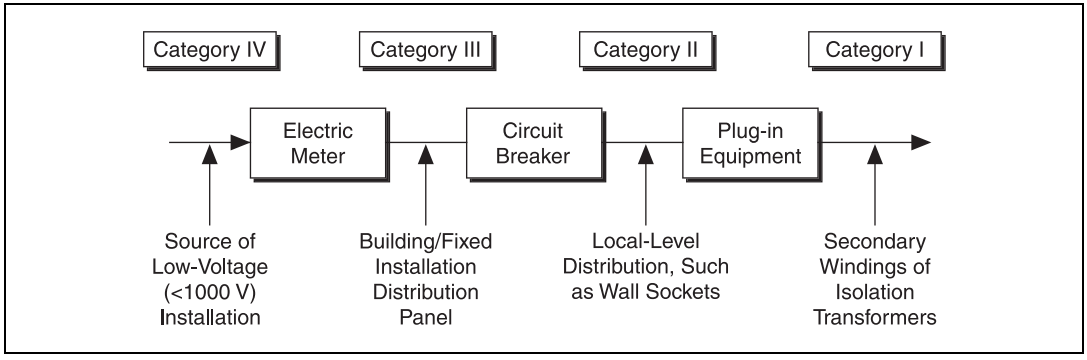
- Installation Category III is for measurements performed in the building installation. This category is a distribution level referring to hardwired equipment that does not rely on standard building insulation.

  Examples of Installation Category III include measurements on distribution circuits and circuit breakers. Other examples of Installation Category III are wiring including cables, bus-bars, junction boxes, switches, socket outlets in the building/fixed installation, and equipment for industrial use, such as stationary motors with a permanent connection to the building/fixed installation.

- Installation Category IV is for measurements performed at the source of the low-voltage (<1,000 V) installation.

  Examples of Installation Category IV are electric meters, and measurements on primary overcurrent protection devices and ripple-control units.

Below is a diagram of a sample installation.



2

Installing and Configuring the Device

This chapter explains how to install and configure the AT E Series device.

Installing the Software

Complete the following steps to install the software before installing the DAQ device.

1. Install the application development environment (ADE), such as LabVIEW or Measurement Studio, according to the instructions on the CD and the release notes.
2. Install NI-DAQ according to the instructions on the CD and the *DAQ Quick Start Guide* included with the device.

Note It is important to install NI-DAQ before installing the DAQ device to ensure that the device is properly detected.

Installing the Hardware

You can install an AT E Series device in any available expansion slot in the PC. However, to achieve best noise performance, you should leave as much room as possible between the AT E Series device and other devices and hardware. The following are general installation instructions, but consult the PC user manual or technical reference manual for specific instructions and warnings.

1. Write down the AT E Series device serial number. You need this serial number when you install and configure the software.
2. Turn off and unplug the computer.
3. Remove the top cover or access port to the I/O channel.
4. Remove the expansion slot cover on the back panel of the computer.
5. Ground yourself using a grounding strap or by holding a grounded object. Follow the ESD protection precautions described in the *Unpacking* section of Chapter 1, *Introduction*.

6. Insert the AT E Series device into an EISA or 16-bit ISA slot. It may be a tight fit, but *do not force* the device into place.
7. Screw the mounting bracket of the AT E Series device to the back panel rail of the computer.
8. Visually verify the installation. Make sure the device is not touching other devices or components and is fully inserted in the slot.
9. Replace the cover.
10. Plug in and turn on the computer.

The AT E Series device is installed. You are now ready to install and configure the software.

Configuring the Device

Due to the DAQ-PnP features, the AT E Series devices are completely software configurable. Two types of configuration must be performed on the AT E Series devices—bus-related configuration and data acquisition-related configuration. Bus-related configuration includes setting the base I/O address, DMA channels, and interrupt channels. Data acquisition-related configuration, explained in Chapter 3, *Hardware Overview*, includes such settings as AI polarity and range, AO reference source, and other settings. For more information about data acquisition-related configuration, refer to the NI-DAQ user manual.

Bus Interface

The AT E Series devices work in either a Plug and Play mode or a switchless mode. These modes dictate how the base I/O address, DMA channels, and interrupt channels are determined and assigned to the device.

Plug and Play

The AT E Series devices are fully compatible with the industry-standard Plug and Play ISA specification. A Plug and Play system arbitrates and assigns resources through software, freeing you from manually setting switches and jumpers. These resources include the device base I/O address, DMA channels, and interrupt channels. Each AT E Series device is configured at the factory to request these resources from the Plug and Play Configuration Manager.

The Configuration Manager receives all of the resource requests at start up, compares the available resources to those requested, and assigns the available resources as efficiently as possible to the Plug and Play devices.

Application software can query the Configuration Manager to determine the resources assigned to each device without your involvement. The Plug and Play software is installed as a device driver or as an integral component of the computer BIOS.

Switchless Data Acquisition

You can use an AT E Series device in a non-Plug and Play system as a switchless DAQ device. A non-Plug and Play system is a system in which the Configuration Manager has not been installed and which does not contain any non-NI Plug and Play products. You use a configuration utility to enter the base address, DMA, and interrupt selections, and the application software assigns them to the device.



Note Avoid resource conflicts with non-NI devices. For example, do not configure two devices for the same base address.

Base I/O Address Selection

The AT E Series devices can be configured to use base addresses in the range of 20 to FFE0 hex. Each AT E Series device occupies 32 bytes of address space and must be located on a 32-byte boundary. Therefore, valid addresses include 100, 120, 140, ..., 3C0, 3E0 hex. This selection is software configured and does not require you to manually change any settings on the device.

DMA Channel Selection

The AT E Series devices can achieve high transfer rates by using up to three 16-bit DMA channels. You can use these DMA channels for data transfers with the AI, AO, and general-purpose counter sections of the device. The AT E Series devices can use only 16-bit DMA channels, which correspond to channels 5, 6, and 7 in an ISA computer and channels 0, 1, 2, 3, 5, 6, and 7 in an EISA computer. These selections are all software configured and do not require you to manually change any settings on the device.

Interrupt Channel Selection

The AT E Series devices can increase bus efficiency by using an interrupt channel. You can use an interrupt channel for event notification without the use of polling techniques. AT E Series devices can use interrupt channels 3, 4, 5, 7, 10, 11, 12, and 15. These selections are all software configured and do not require you to manually change any settings on the device.

The following tables provide information concerning possible conflicts when configuring the AT E Series device.

Table 2-1. PC AT I/O Address Map

I/O Address Range (Hex)	Device
100 to 1EF	—
1F0 to 1F8	IBM PC AT Fixed Disk
200 to 20F	PC and PC AT Game Controller, reserved
210 to 213	PC-DIO-24 (default)
218 to 21F	—
220 to 23F	Previous generation of AT-MIO devices (default)
240 to 25F	AT-DIO-32F (default)
260 to 27F	Lab-PC/PC+ (default)
278 to 28F	AT Parallel Printer Port 2 (LPT2)
279	Reserved for Plug and Play operation
280 to 29F	WD EtherCard+ (default)
2A0 to 2BF	—
2E2 to 2F7	—
2F8 to 2FF	PC, AT Serial Port 2 (COM2)
300 to 30F	3Com EtherLink (default)
310 to 31F	—
320 to 32F	ICM PC/XT Fixed Disk Controller
330 to 35F	—
360 to 363	PC Network (low address)
364 to 367	Reserved
368 to 36B	PC Network (high address)
36C to 36F	Reserved
370 to 366	PC, AT Parallel Printer Port 1 (LPT1)

Table 2-1. PC AT I/O Address Map (Continued)

I/O Address Range (Hex)	Device
380 to 38C	SDLC Communications
380 to 389	Bisynchronous (BSC) Communications (alternate)
390 to 393	Cluster Adapter 0
394 to 39F	—
3A0 to 3A9	BSC Communications (primary)
3AA to 3AF	—
3B0 to 3BF	Monochrome Display/Parallel Printer Adapter 0
3C0 to 3CF	Enhanced Graphics Adapter, VGA
3D0 to 3DF	Color/Graphics Monitor Adapter, VGA
3E0 to 3EF	—
3F0 to 3F7	Diskette Controller
3F8 to 3FF	Serial Port 1 (COM1)
A79	Reserved for Plug and Play operation

Table 2-2. PC AT Interrupt Assignment Map

IRQ	Device
15	Available
14	Fixed Disk Controller
13	Coprocessor
12	AT-DIO-32F (default)
11	AT-DIO-32F (default)
10	AT-MIO-16 (default)
9	PC Network (default) PC Network Alternate (default)
8	Real Time Clock

Table 2-2. PC AT Interrupt Assignment Map (Continued)

IRQ	Device
7	Parallel Port 1 (LPT1)
6	Diskette Drive Controller Fixed Disk and Diskette Drive Controller
5	Parallel Port 2 (LPT2) PC-DIO-24 (default) Lab-PC/PC+ (default)
4	Serial Port 1 (COM1) BSC, BSC Alternate
3	Serial Port 2 (COM2) BSC, BSC Alternate Cluster (primary) PC Network, PC Network Alternate WD EtherCard+ (default) 3Com EtherLink (default)
2	IRQ 8–15 Chain (from interrupt controller 2)
1	Keyboard Controller Output Buffer Full
0	Timer Channel 0 Output

Table 2-3. PC AT 16-bit DMA Channel Assignment Map

Channel	Device
7	AT-MIO-16 series (default)
6	AT-MIO-16 series (default) AT-DIO-32F (default)
5	AT-DIO-32F (default)
4	Cascade for DMA Controller #1 (channels 0 through 3)

Note EISA computers also have channels 0–3 available as 16-bit DMA channels.

3

Hardware Overview

This chapter presents an overview of the hardware functions on the AT E Series device.

Figure 3-1 shows the block diagram for the AT-MIO-16E-1 and AT-MIO-16E-2.

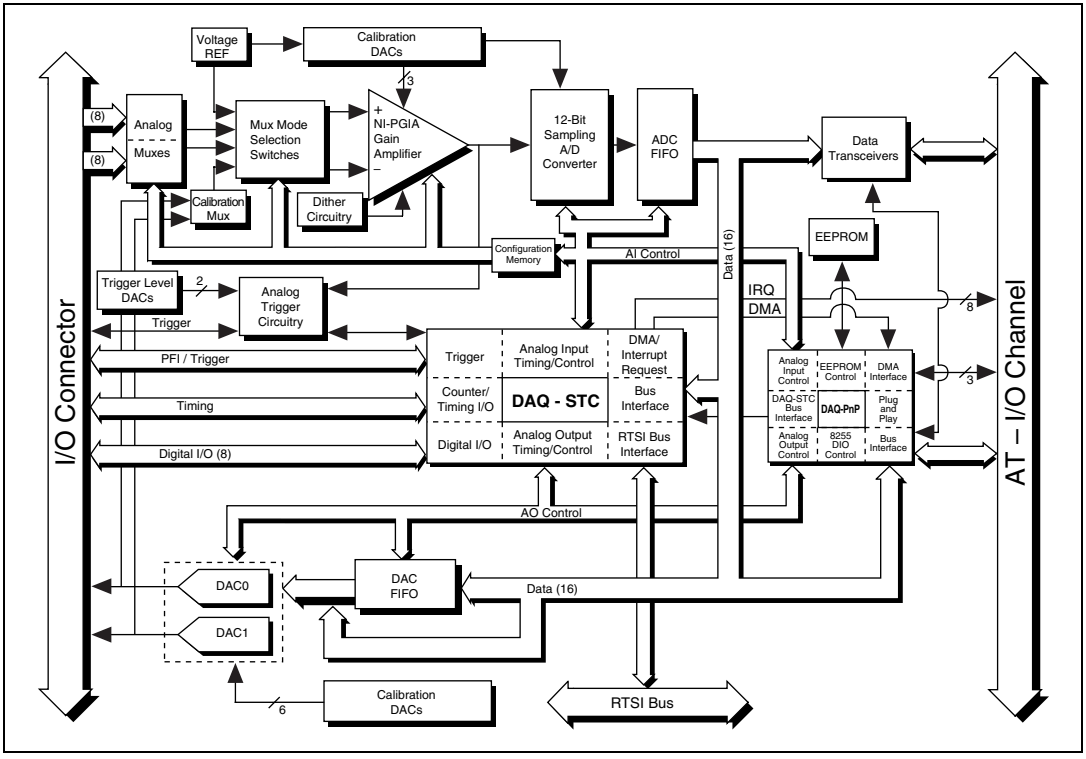


Figure 3-1. AT-MIO-16E-1 and AT-MIO-16E-2 Block Diagram

Figure 3-2 shows the block diagram for the AT-MIO-64E-3.

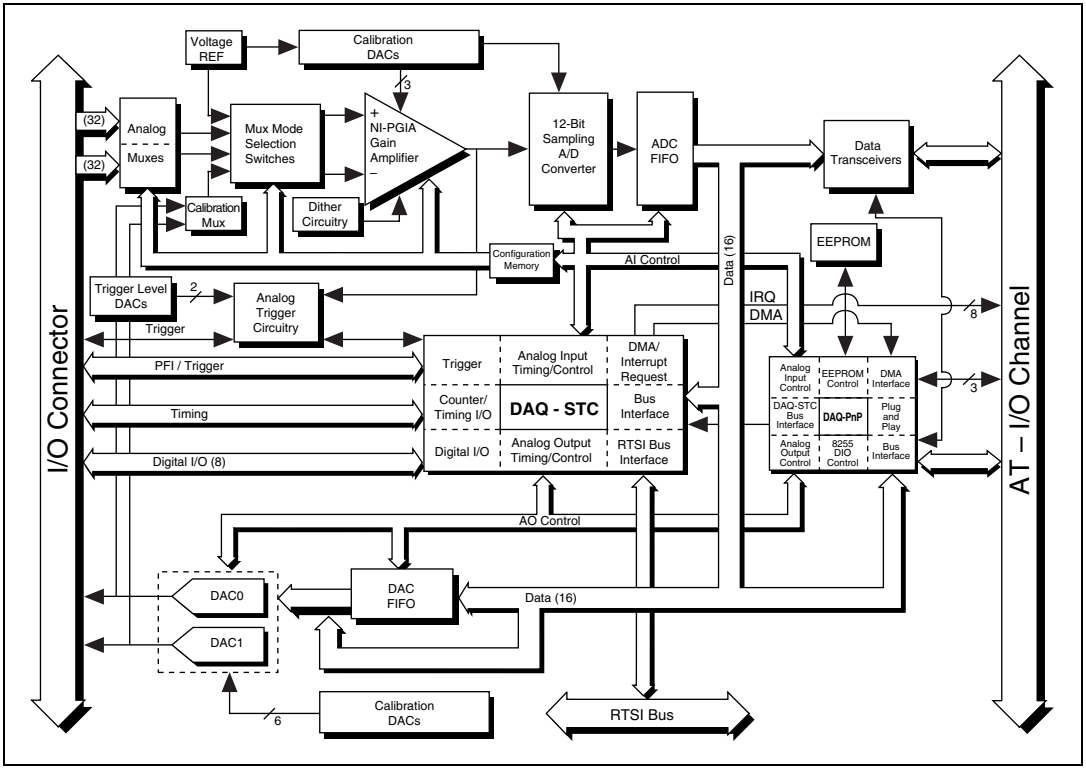


Figure 3-2. AT-MIO-64E-3 Block Diagram

Figure 3-3 shows the block diagram for the AT-MIO-16E-10 and AT-MIO-16DE-10.

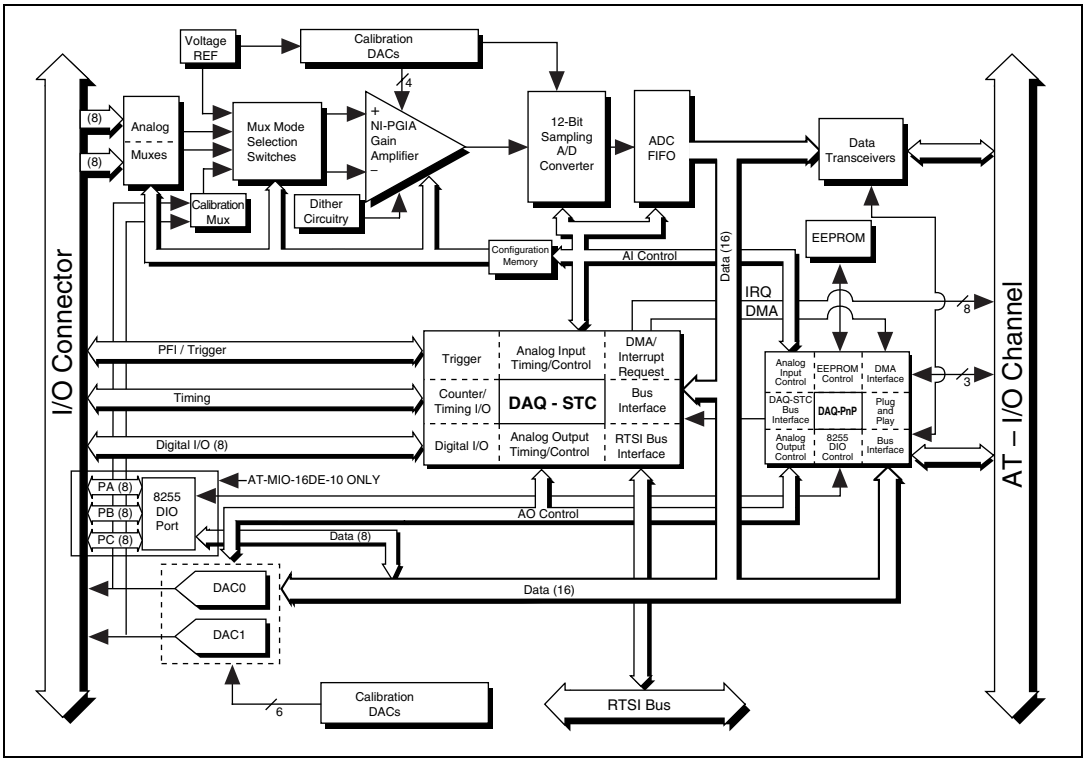


Figure 3-3. AT-MIO-16E-10 and AT-MIO-16DE-10 Block Diagram

The primary differences between the AT-MIO-16E-10 and the AT-MIO-16DE-10 are in the 8255 DIO port, which is not present on the AT-MIO-16E-10, and the I/O connector.

Figure 3-4 shows a block diagram for the AT-MIO-16XE-10.

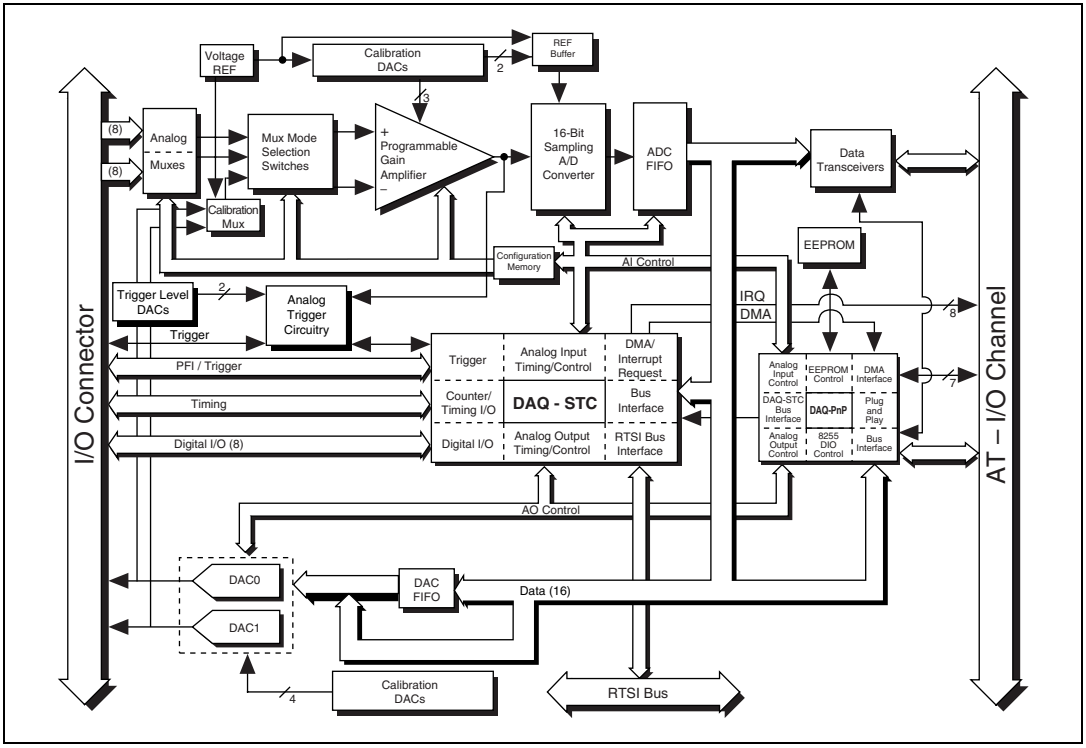


Figure 3-4. AT-MIO-16XE-10 Block Diagram

Figure 3-5 shows a block diagram for the AT-AI-16XE-10.

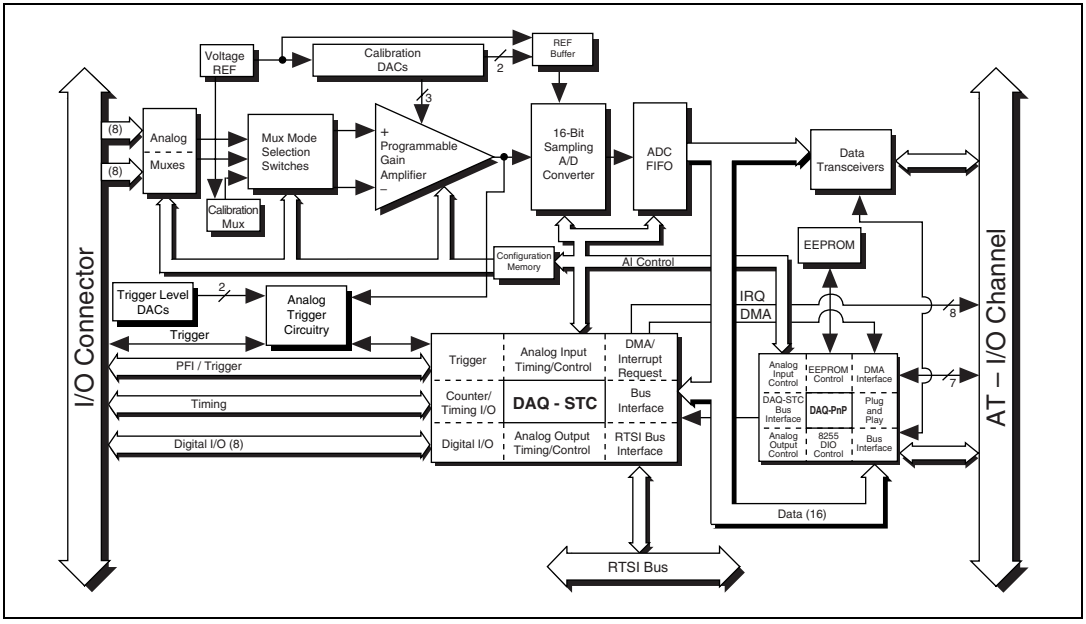


Figure 3-5. AT-AI-16XE-10 Block Diagram

Figure 3-6 shows a block diagram for the AT-MIO-16XE-50.

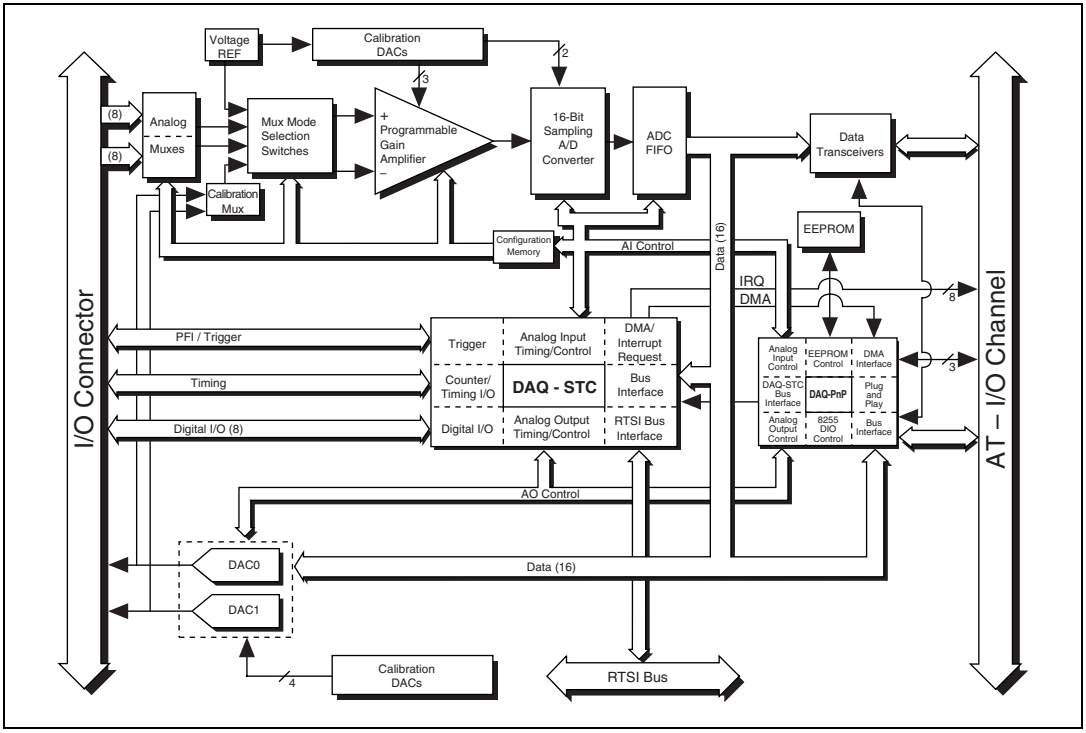


Figure 3-6. AT-MIO-16XE-50 Block Diagram

Analog Input

The AI section of each AT E Series device is software configurable. You can select different AI configurations through application software designed to control the AT E Series devices. The following sections describe in detail each of the AI categories.

Input Mode

The AT E Series devices have three different input modes—nonreferenced single-ended (NRSE) input, referenced single-ended (RSE) input, and differential (DIFF) input. The single-ended input configurations use up to 16 channels (64 channels on the AT-MIO-64E-3). The DIFF input configuration uses up to eight channels (32 channels on the AT-MIO-64E-3). Input modes are programmed on a per channel basis for multimode scanning. For example, you can configure the circuitry to scan

12 channels—four differentially configured channels and eight single-ended channels. Table 3-1 describes the three input configurations.

Table 3-1. Available Input Configurations for the AT E Series

Configuration	Description
DIFF	A channel configured in DIFF mode uses two analog channel input lines. One line connects to the positive input of the device programmable gain instrumentation amplifier (PGIA), and the other connects to the negative input of the PGIA.
RSE	A channel configured in RSE mode uses one analog channel input line, which connects to the positive input of the PGIA. The negative input of the PGIA is internally tied to AI ground (AIGND).
NRSE	A channel configured in NRSE mode uses one analog channel input line, which connects to the positive input of the PGIA. The negative input of the PGIA connects to the AI sense (AISENSE) input.

For more information about the three types of input configuration, refer to the *Analog Input Signal Connections* section of Chapter 4, *Connecting Signals*, which contains diagrams showing the signal paths for the three configurations.

Input Polarity and Input Range

- AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3, AT-MIO-16E-10, and AT-MIO-16DE-10

These devices have two input polarities—unipolar and bipolar. Unipolar input means that the input voltage range is between 0 and V_{ref}, where V_{ref} is a positive reference voltage. Bipolar input means that the input voltage range is between $-V_{ref}/2$ and $+V_{ref}/2$. The AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3, AT-MIO-16E-10, and AT-MIO-16DE-10 have a unipolar input range of 10 V (0 to 10 V) and a bipolar input range of 10 V (±5 V). You can program polarity and range settings on a per channel basis so that you can configure each input channel uniquely.

The software-programmable gain on these devices increases their overall flexibility by matching the input signal ranges to those that the ADC can accommodate. The AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3,

AT-MIO-16E-10, and AT-MIO-16DE-10 have gains of 0.5, 1, 2, 5, 10, 20, 50, and 100 and are suited for a wide variety of signal levels. With the proper gain setting, you can use the full resolution of the ADC to measure the input signal. Table 3-2 shows the overall input range and precision according to the input range configuration and gain used.

Table 3-2. Actual Range and Measurement Precision

Range Configuration	Gain	Actual Input Range	Precision[1]
0 to +10 V	1.0	0 to +10 V	2.44 mV
	2.0	0 to +5 V	1.22 mV
	5.0	0 to +2 V	488.28 µV
	10.0	0 to +1 V	244.14 µV
	20.0	0 to +500 mV	122.07 µV
	50.0	0 to +200 mV	48.83 µV
	100.0	0 to +100 mV	24.41 µV
–5 to +5 V	0.5	–10 to +10 V	4.88 mV
	1.0	–5 to +5 V	2.44 mV
	2.0	–2.5 to +2.5 V	1.22 mV
	5.0	–1 to +1 V	488.28 µV
	10.0	–500 to +500 mV	244.14 µV
	20.0	–250 to +250 mV	122.07 µV
	50.0	–100 to +100 mV	48.83 µV
	100.0	–50 to +50 mV	24.41 µV

[1] The value of 1 LSB of the 12-bit ADC; that is, the voltage increment corresponding to a change of one count in the ADC 12-bit count.

Note: Refer to Appendix A, *Specifications*, for absolute maximum ratings.

- AT-MIO-16XE-10, AT-AI-16XE-10, AT-MIO-16XE-50

These devices have two input polarities—unipolar and bipolar. Unipolar input means that the input voltage range is between 0 and V_{ref}, where V_{ref} is a positive reference voltage. Bipolar input means that the input voltage range is between $-V_{ref}$ and $+V_{ref}$. The AT-MIO-16XE-10, AT-AI-16XE-10, and AT-MIO-16XE-50 have a unipolar input range of 10 V (0 to 10 V) and a bipolar input range of 20 V (±10 V). You can program polarity and range settings on a per channel basis so that you can configure each input channel uniquely.

Note You can calibrate the AT-MIO-16XE-10, AT-AI-16XE-10, and AT-MIO-16XE-50 AI circuitry for either a unipolar or bipolar polarity. If you mix unipolar and bipolar channels in the scan list and you are using NI-DAQ, then NI-DAQ loads the calibration constants appropriate to the polarity for which AI channel 0 is configured.

The software-programmable gain on these devices increases their overall flexibility by matching the input signal ranges to those that the ADC can accommodate. The AT-MIO-16XE-10 and AT-AI-16XE-10 have gains of 1, 2, 5, 10, 20, 50, and 100 and the AT-MIO-16XE-50 has gains of 1, 2, 10, and 100. These gains are suited for a wide variety of signal levels. With the proper gain setting, you can use the full resolution of the ADC to measure the input signal. Table 3-3 shows the overall input range and precision according to the input range configuration and gain used.

Table 3-3. Actual Range and Measurement Precision for the AT-MIO-16XE-10, AT-AI-16XE-10, and AT-MIO-16XE-50

Range Configuration	Gain	Actual Input Range	Precision[1]
0 to +10 V	1.0	0 to +10 V	152.59 µV
	2.0	0 to +5 V	76.29 µV
	5.0[2]	0 to +2 V	30.52 µV
	10.0	0 to +1 V	15.26 µV
	20.0[2]	0 to +500 mV	.63 µV
	50.0[2]	0 to +200 mV	3.05 µV
	100.0	0 to 100 mV	1.53 µV
–10 to +10 V	1.0	–10 to +10 V	305.18 µV
	2.0	–5 to +5 V	152.59 µV
	5.0[2]	–2 to +2 V	61.04 µV
	10.0	–1 to +1 V	30.52 µV
	20.0[2]	–500 to +500 mV	15.26 µV
	50.0[2]	–200 to +200 mV	6.10 µV
	100.0	–100 to +100 mV	3.05 µV

[1] The value of 1 LSB of the 16-bit ADC; that is, the voltage increment corresponding to a change of one count in the ADC 16-bit count.

[2] AT-MIO-16XE-10 and AT-AI-16XE-10 only

Note: Refer to Appendix A, *Specifications*, for absolute maximum ratings.

Considerations for Selecting Input Ranges

Which input polarity and range you select depends on the expected range of the incoming signal. A large input range can accommodate a large signal variation but reduces the voltage resolution. Choosing a smaller input range improves the voltage resolution but may result in the input signal going out of range. For best results, you should match the input range as closely as possible to the expected range of the input signal. For example, if you are certain the input signal is not negative (below 0 V), unipolar input polarity is best. However, if the signal is negative or equal to zero, inaccurate readings occur if you use unipolar input polarity.

Dither

When you enable dither, you add approximately 0.5 LSB_{rms} of white Gaussian noise to the signal to be converted by the ADC. This addition is useful for applications involving averaging to increase the resolution of the AT E Series device, as in calibration or spectral analysis. In such applications, noise modulation is decreased and differential linearity is improved by the addition of the dither. When taking DC measurements, such as when checking the device calibration, you should enable dither and average about 1,000 points to take a single reading. This process removes the effects of quantization and reduces measurement noise, resulting in improved resolution. For high-speed applications not involving averaging or spectral analysis, you may want to disable the dither to reduce noise. You enable and disable the dither circuitry through software.

Figure 3-7 illustrates the effect of dither on signal acquisition. Figure 3-7a shows a small (±4 LSB) sine wave acquired with dither off. The quantization of the ADC is clearly visible. Figure 3-7b shows what happens when 50 such acquisitions are averaged together; quantization is still plainly visible. In Figure 3-7c, the sine wave is acquired with dither on. There is a considerable amount of noise visible. But averaging about 50 such acquisitions, as shown in Figure 3-7d, eliminates both the added noise and the effects of quantization. Dither has the effect of forcing quantization noise to become a zero-mean random variable rather than a deterministic function of the input signal.

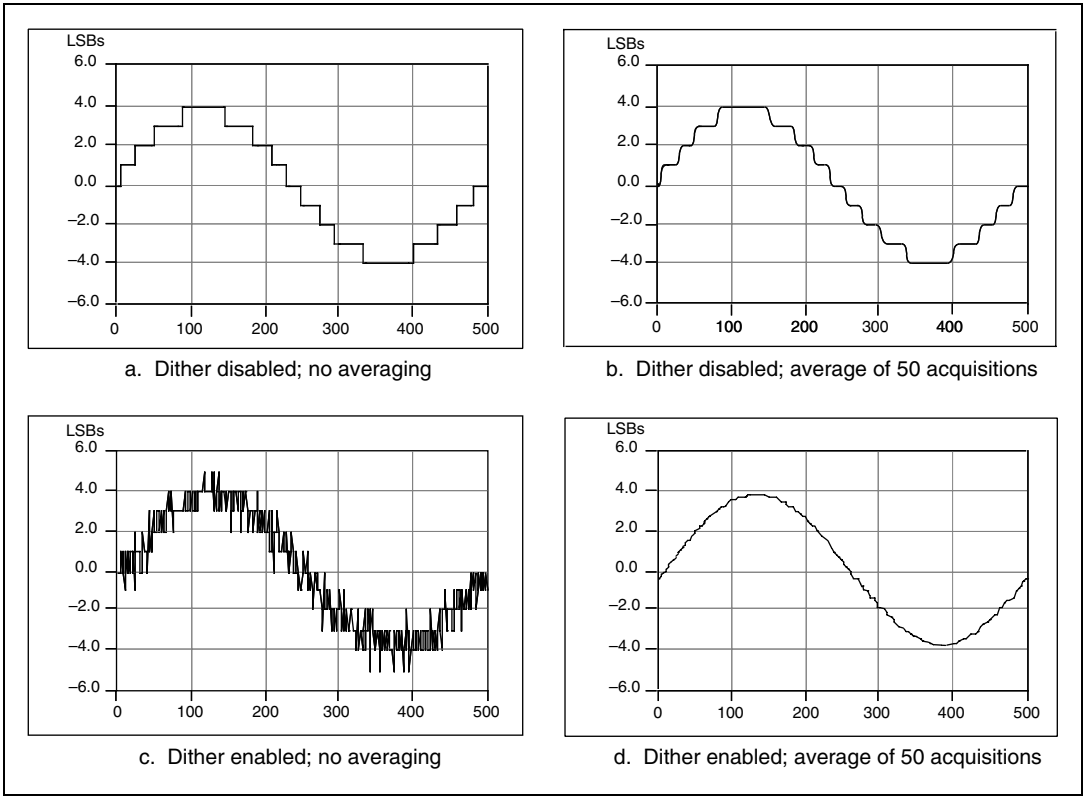


Figure 3-7. Dither

You cannot disable dither on the AT-MIO-16XE-10, AT-AI-16XE-10, or AT-MIO-16XE-50. This is because the resolution of the ADC is so fine that the ADC and the PGIA inherently produce almost 0.5 LSB_{rms} of noise. This is equivalent to having a dither circuit that is always enabled.

Multiple-Channel Scanning Considerations

All of the AT E Series devices can scan multiple channels at the same maximum rate as their single-channel rate; however, you should pay careful attention to the settling times for each of the devices. The settling time for most of the AT E Series devices is independent of the selected gain, even at the maximum sampling rate. The settling time for the high channel count and very high-speed devices is gain dependent, which can affect the useful sampling rate for a given gain. No extra settling time is necessary between channels as long as the gain is constant and source impedances are low. Refer to Appendix A, *Specifications*, for a complete listing of settling times for each of the AT E Series devices.

When scanning among channels at various gains, the settling times may increase. When the PGIA switches to a higher gain, the signal on the previous channel may be well outside the new, smaller range. For instance, suppose a 4 V signal is connected to channel 0 and a 1 mV signal is connected to channel 1, and suppose the PGIA is programmed to apply a gain of one to channel 0 and a gain of 100 to channel 1. When the multiplexer switches to channel 1 and the PGIA switches to a gain of 100, the new full-scale range is 100 mV (if the ADC is in unipolar mode).

The approximately 4 V step from 4 V to 1 mV is 4,000% of the new full-scale range. For a 12-bit device to settle within 0.012% (120 ppm or 1/2 LSB) of the 100 mV full-scale range on channel 1, the input circuitry has to settle to within 0.0003% (3 ppm or 1/80 LSB) of the 4 V step. It may take as long as 100 µs for the circuitry to settle this much. For a 16-bit device to settle within 0.0015% (15 ppm or 1 LSB) of the 100 mV full-scale range on channel 1, the input circuitry has to settle within 0.00004% (0.4 ppm or 1/400 LSB) of the 4 V step. It may take as long as 200 µs for the circuitry to settle this much. In general, this extra settling time is not needed when the PGIA is switching to a lower gain.

Settling times can also increase when scanning high-impedance signals due to a phenomenon called *charge injection*, where the AI multiplexer injects a small amount of charge into each signal source when that source is selected. If the impedance of the source is not low enough, the effect of the charge—a voltage error—does not have decayed by the time the ADC samples the signal. For this reason, you should keep source impedances under 1 kΩ to perform high-speed scanning.

Due to the previously described limitations of settling times resulting from these conditions, multiple-channel scanning is not recommended unless sampling rates are low enough or it is necessary to sample several signals as nearly simultaneously as possible. The data is much more accurate and channel-to-channel independent if you acquire data from each channel independently (for example, 100 points from channel 0, then 100 points from channel 1, then 100 points from channel 2, and so on).

Analog Output

- AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3, AT-MIO-16E-10, and AT-MIO-16DE-10

  The AT E Series devices supply two channels of AO voltage at the I/O connector. You can select the reference and range for the AO circuitry through software. The reference can be either internal or external, whereas the range can be either bipolar or unipolar.

- AT-MIO-16XE-50

  The AT-MIO-16XE-50 supplies two channels of AO voltage at the I/O connector. The range is fixed at bipolar ±10 V.

- AT-MIO-16XE-10

  The AT-MIO-16XE-10 supplies two channels of AO voltage at the I/O connector. The range is software selectable between unipolar (0 to 10 V) and bipolar (±10 V).

Analog Output Reference Selection

- AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3, AT-MIO-16E-10, and AT-MIO-16DE-10 only

  You can connect each D/A converter (DAC) to the AT E Series device internal reference of 10 V or to the external reference signal connected to the external reference (EXTREF) pin on the I/O connector. This signal applied to EXTREF should be between –10 and +10 V. You do not need to configure both channels for the same mode.

Analog Output Polarity Selection

- AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3, AT-MIO-16E-10, and AT-MIO-16DE-10 only

  You can configure each AO channel for either unipolar or bipolar output. A unipolar configuration has a range of 0 to V_{ref} at the AO. A bipolar configuration has a range of $-V_{ref}$ to $+V_{ref}$ at the AO. V_{ref} is the voltage reference used by the DACs in the AO circuitry and can be either the +10 V onboard reference or an externally supplied reference between –10 and +10 V. You do not need to configure both channels for the same range.

Selecting a bipolar range for a particular DAC means that any data written to that DAC is interpreted as two's complement format. In two's complement mode, data values written to the AO channel can be either positive or negative. If you select unipolar range, data is interpreted in straight binary format. In straight binary mode, data values written to the AO channel range must be positive.

- AT-MIO-16XE-10

  You can configure each AO channel for either unipolar or bipolar output. A unipolar configuration has a range of 0 to 10 V at the analog output. A bipolar configuration has a range of –10 to +10 V at the analog output. You do not need to configure both channels for the same range.

Analog Output Reglitch Selection

- AT-MIO-16E-1, AT-MIO-16E-2, and AT-MIO-64E-3 only

  In normal operation, a DAC output glitches whenever it is updated with a new value. The glitch energy differs from code to code and appears as distortion in the frequency spectrum. Each analog output of the AT-MIO-16E-1, AT-MIO-16E-2, and AT-MIO-64E-3 contains a reglitch circuit that generates uniform glitch energy at every code rather than large glitches at the major code transitions. This uniform glitch energy appears as a multiple of the update rate in the frequency spectrum. Notice that this reglitch circuit does *not* eliminate the glitches; it only makes them more uniform in size. Reglitching is normally disabled at startup and can be independently enabled for each channel through software.

Analog Trigger

- AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3, AT-MIO-16XE-10, and AT-AI-16XE-10 only

  In addition to supporting internal software triggering and external digital triggering to initiate a data acquisition sequence, the AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3, AT-MIO-16XE-10, and AT-AI-16XE-10 also support analog triggering. You can configure the analog trigger circuitry to accept either a direct analog input from the PFI0/TRIG1 pin on the I/O connector or a postgain signal from the output of the PGIA, as shown in Figure 3-8. The trigger-level range for the direct analog channel is ±10 V in 78 mV steps for the AT-MIO-16E-1, AT-MIO-16E-2, and AT-MIO-64E-3, and ±10 V in 4.9 mV steps for the AT-MIO-16XE-10 and AT-AI-16XE-10. The range for the post-PGIA trigger selection is simply

the full-scale range of the selected channel, and the resolution is that range divided by 256 for the AT-MIO-16E-1, AT-MIO-16E-2, and AT-MIO-64E-3, and divided by 4,096 for the AT-MIO-16XE-10 and AT-AI-16XE-10.

Note The PFI0/TRIG1 pin is a high-impedance input. Therefore, it is susceptible to crosstalk from adjacent pins, which can result in false triggering when the pin is left unconnected. To avoid false triggering, make sure this pin is connected to a low-impedance signal source (less than 10 kΩ source impedance) if you plan to enable this input using software.

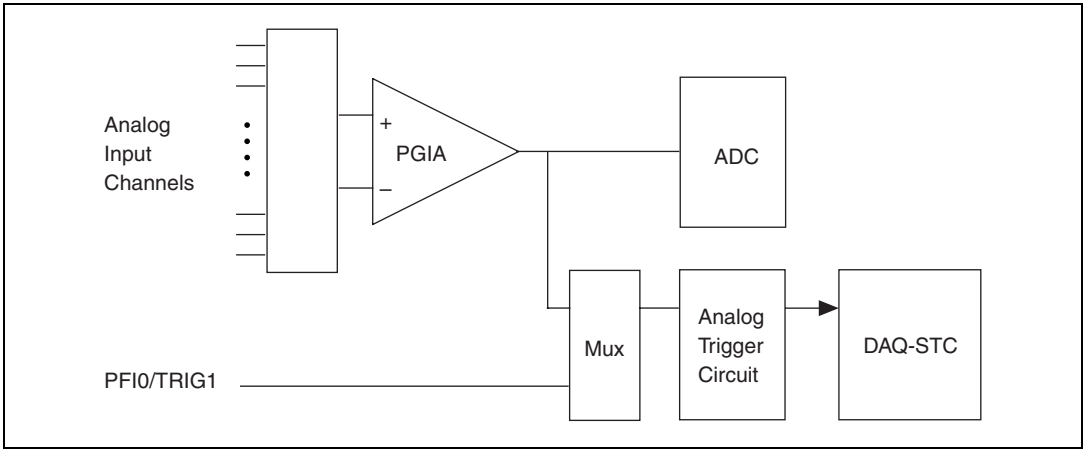


Figure 3-8. Analog Trigger Block Diagram

There are five analog triggering modes available, as shown in Figures 3-9 through 3-13. You can set **lowValue** and **highValue** independently in software.

In below-low-level analog triggering mode, the trigger is generated when the signal value is less than **lowValue**. **HighValue** is unused.

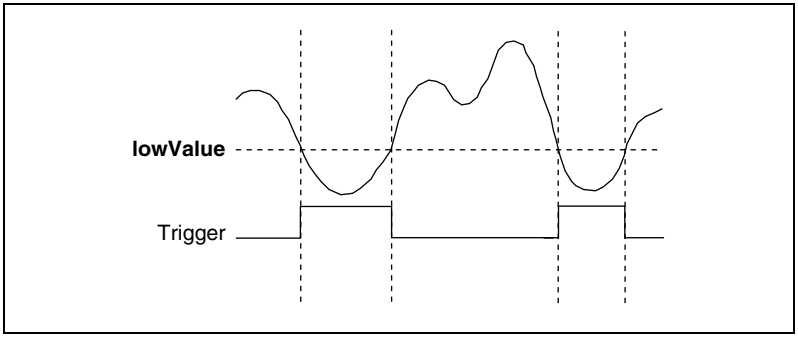


Figure 3-9. Below-Low-Level Analog Triggering Mode

In above-high-level analog triggering mode, the trigger is generated when the signal value is greater than **highValue**. **LowValue** is unused.

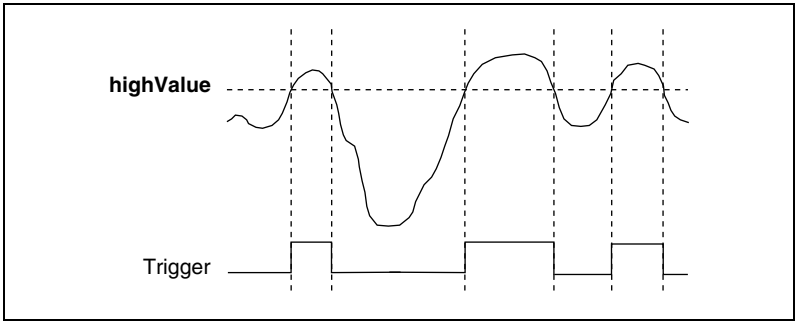


Figure 3-10. Above-High-Level Analog Triggering Mode

In inside-region analog triggering mode, the trigger is generated when the signal value is between the **lowValue** and the **highValue.**

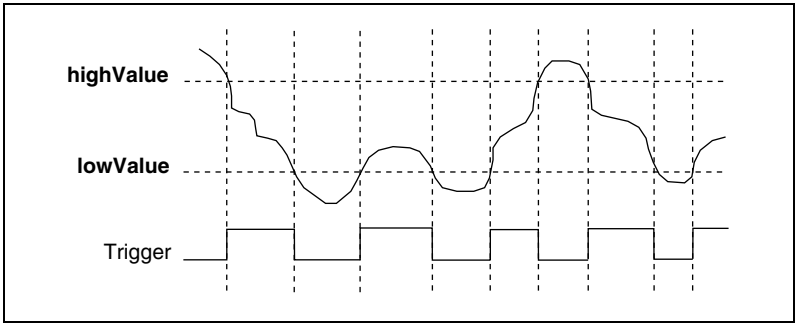


Figure 3-11. Inside-Region Analog Triggering Mode

In high-hysteresis analog triggering mode, the trigger is generated when the signal value is greater than **highValue**, with the hysteresis specified by **lowValue**.

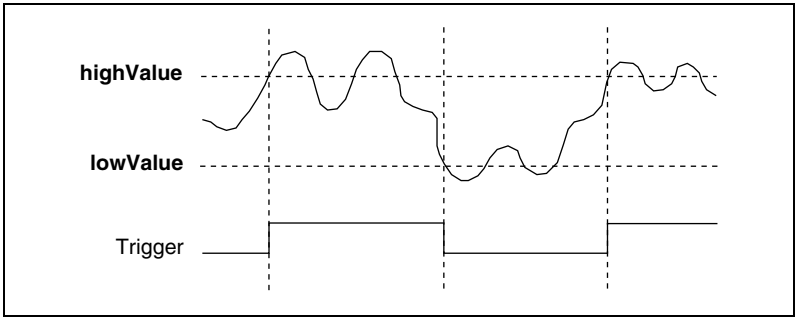


Figure 3-12. High-Hysteresis Analog Triggering Mode

In low-hysteresis analog triggering mode, the trigger is generated when the signal value is less than **lowValue**, with the hysteresis specified by **highValue**.

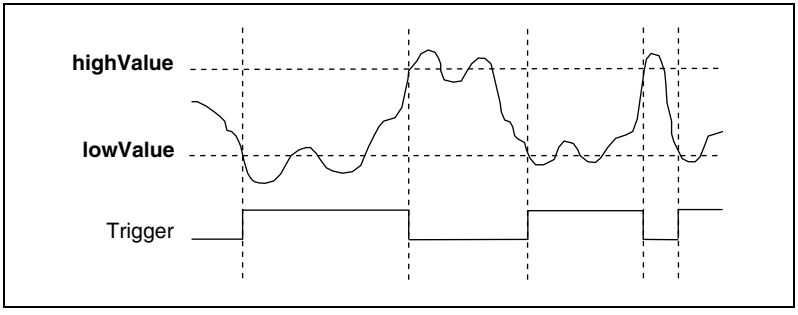


Figure 3-13. Low-Hysteresis Analog Triggering Mode

The analog trigger circuit generates an internal digital trigger based on the AI signal and the user-defined trigger levels. This digital trigger can be used by any of the timing sections of the DAQ-STC, including the AI, AO, and general-purpose counter/timer sections. For example, the AI section can be configured to acquire *n* scans after the AI signal crosses a specific threshold. As another example, the AO section can be configured to update its outputs whenever the AI signal crosses a specific threshold.

Digital I/O

The AT E Series devices contain eight lines of DIO for general-purpose use. You can individually configure each line through software for either input or output. The AT-MIO-16DE-10 has 24 additional DIO lines, configured as three 8-bit ports: PA<0..7>, PB<0..7>, and PC<0..7>. You can configure each port for both input and output in various combinations, with some handshaking capabilities. At system startup and reset, the digital I/O ports are all high impedance.

The hardware up/down control for general-purpose counters 0 and 1 are connected onboard to DIO6 and DIO7, respectively. Thus, you can use DIO6 and DIO7 to control the general-purpose counters. The up/down control signals are input only and do not affect the operation of the DIO lines.

Timing Signal Routing

The DAQ-STC provides a very flexible interface for connecting timing signals to other devices or external circuitry. The AT E Series device uses the RTSI bus for interconnecting timing signals between devices and the Programmable Function Input (PFI) pins on the I/O connector for connecting to external circuitry. These connections are designed to enable the AT E Series device to both control and be controlled by other devices and circuits.

There are a total of 13 timing signals internal to the DAQ-STC that can be controlled by an external source. These timing signals can also be controlled by signals generated internally to the DAQ-STC, and these selections are fully software configurable. For example, the signal routing multiplexer for controlling the CONVERT* signal is shown in Figure 3-14.

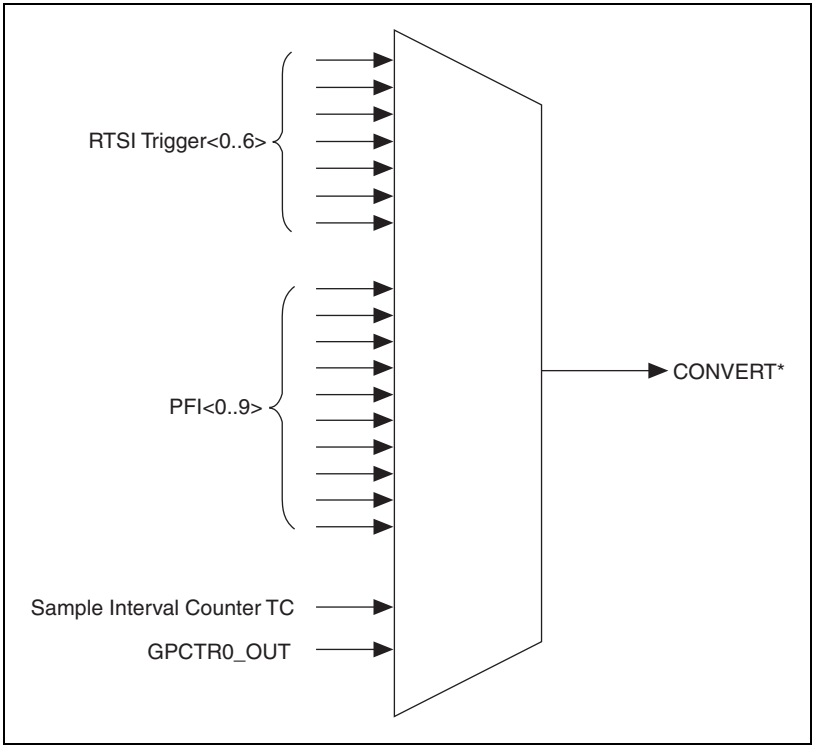


Figure 3-14. CONVERT* Signal Routing

This figure shows that CONVERT* can be generated from a number of sources, including the external signals RTSI<0..6> and PFI<0..9> and the internal signals Sample Interval Counter TC and GPCTR0_OUT.

Many of these timing signals are also available as outputs on the RTSI pins, as indicated in the *RTSI Triggers* section later in this chapter, and on the PFI pins, as indicated in Chapter 4, *Connecting Signals*.

Programmable Function Inputs

The 10 PFIs are connected to the signal routing multiplexer for each timing signal, and software can select one of the PFIs as the external source for a given timing signal. It is important to note that any of the PFIs can be used as an input by any of the timing signals and that multiple timing signals can use the same PFI simultaneously. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications.

You can also individually enable each of the PFI pins to output a specific internal timing signal. For example, if you need the UPDATE* signal as an output on the I/O connector, software can turn on the output driver for the PFI5/UPDATE* pin. To use the PFI pins as outputs, you must use the Route Signal VI to individually enable each of the PFI pins to output a specific timing signal.

Device and RTSI Clocks

Many functions performed by the AT E Series devices require a frequency timebase to generate the necessary timing signals for controlling A/D conversions, DAC updates, or general-purpose signals at the I/O connector.

An AT E Series device can use either its internal 20 MHz timebase or a timebase received over the RTSI bus. In addition, if you configure the device to use the internal timebase, you can also program the device to drive its internal timebase over the RTSI bus to another device that is programmed to receive this timebase signal. This clock source, whether local or from the RTSI bus, is used directly by the device as the primary frequency source. The default configuration at startup is to use the internal timebase without driving the RTSI bus timebase signal. You select this timebase through software.

RTSI Triggers

The seven RTSI trigger lines on the RTSI bus provide a very flexible interconnection scheme for any AT E Series device sharing the RTSI bus. These bidirectional lines can drive any of eight timing signals onto the RTSI bus and can receive any of these timing signals. This signal connection scheme is shown in Figure 3-15.

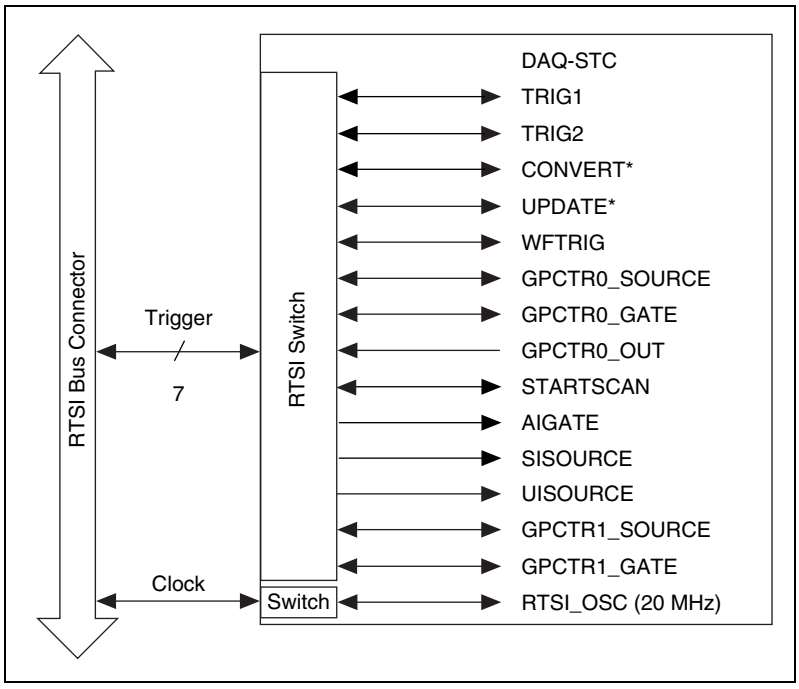


Figure 3-15. RTSI Bus Signal Connection

Refer to the *Timing Connections* section of Chapter 4, *Connecting Signals*, for a description of the signals shown in Figure 3-15.

4

Connecting Signals

This chapter describes how to make input and output signal connections to the AT E Series device using the device I/O connector.

Table 4-1. I/O Connector Details

Device with I/O Connector	Number of Pins	Cable for Connecting to 100-pin Accessories	Cable for Connecting to 68-pin Accessories	Cable for Connecting to 50-pin Signal Accessories
68-Pin AT E Series Device	68	N/A	SH6868-EP Shielded Cable, R6868 Ribbon Cable SH6868R1-EP	SH6850 Shielded Cable, R6850 Ribbon Cable
100-Pin AT E Series Device	100	SH100100 Shielded Cable	SH1006868 Shielded Cable	R1005050 Ribbon Cable

Caution Connections that exceed any of the maximum ratings of input or output signals on the devices can damage the device and the computer. Maximum input ratings for each signal are given in Tables 4-3 through 4-6 in the *Protection* column. National Instruments is *not* liable for any damage resulting from such signal connections.

I/O Connector

Figure 4-1 shows the pin assignments for the 68-pin I/O connector on the AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-16E-10, AT-MIO-16XE-10, AT-AI-16XE-10, and AT-MIO-16XE-50. Figure 4-2 shows the pin assignments for the 100-pin I/O connector on the AT-MIO-64E-3. Figure 4-3 shows the pin assignments for the 100-pin I/O connector on the AT-MIO-16DE-10. Refer to Appendix B, *Optional Cable Connector Descriptions*, for the pin assignments for the 50-pin connectors. A signal description follows the connector pinouts.

Caution Connections that exceed any of the maximum ratings of input or output signals on the AT E Series devices can damage the AT E Series device and the PC. Maximum input ratings for each signal are given in Tables 4-3 through 4-6 in the *Protection* column. NI is *not* liable for any damage resulting from such signal connections.

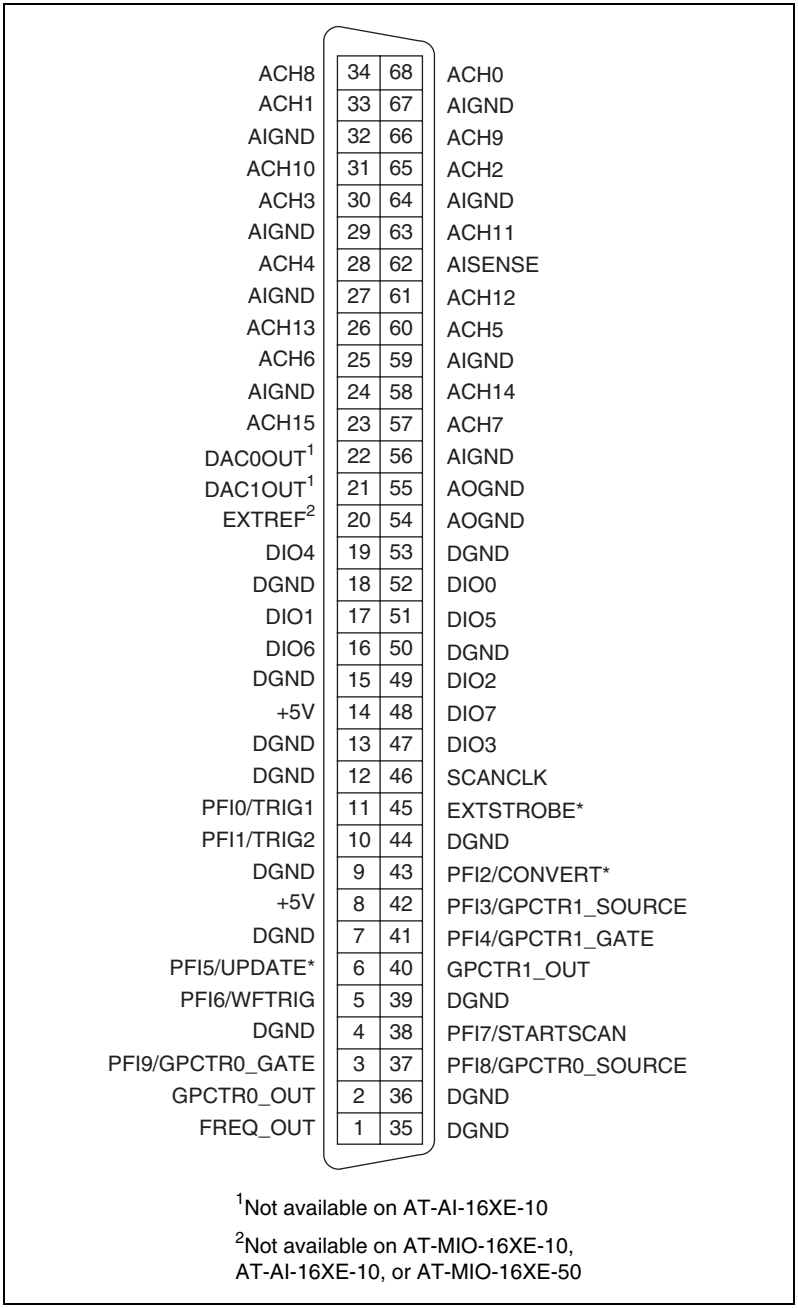


Figure 4-1. I/O Connector Pin Assignment for the AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-16E-10, AT-MIO-16XE-10, AT-AI-16XE-10, and AT-MIO-16XE-50

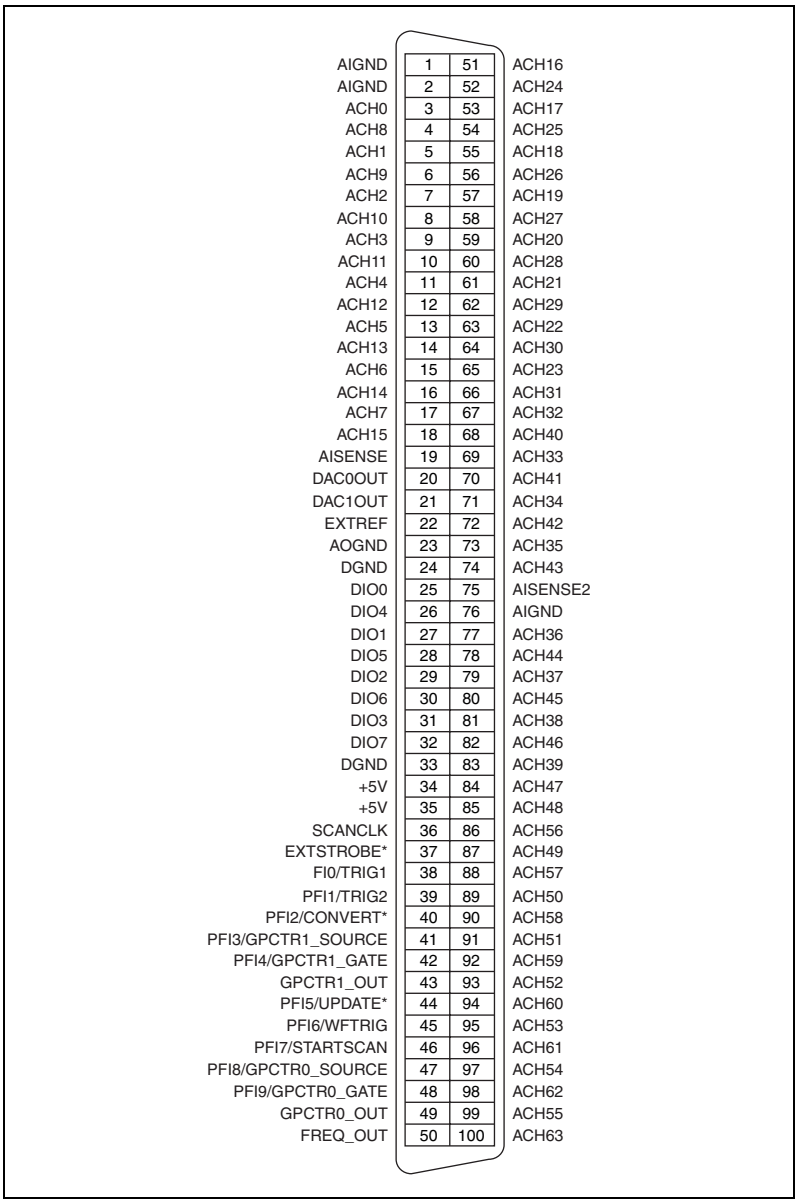


Figure 4-2. I/O Connector Pin Assignment for the AT-MIO-64E-3

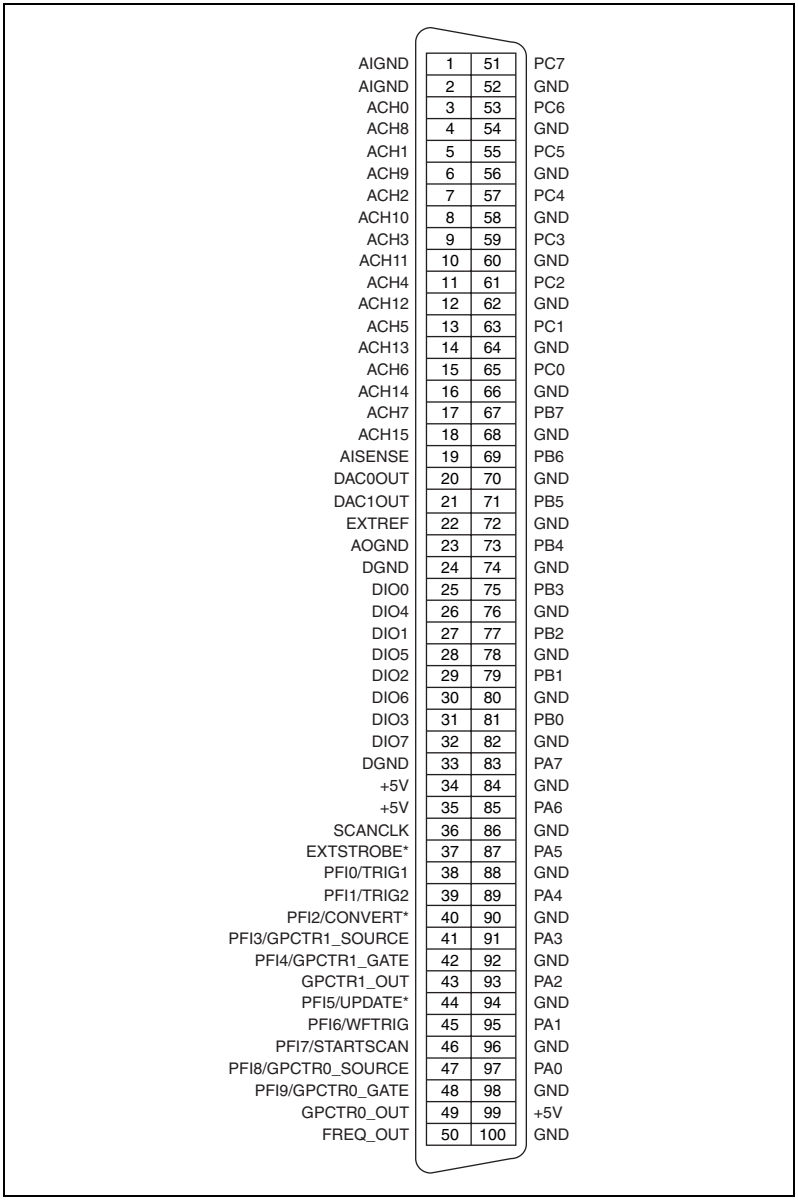


Figure 4-3. I/O Connector Pin Assignment for the AT-MIO-16DE-10

I/O Connector Signal Descriptions

Table 4-2. I/O Signal Summary for the AT E Series

Signal Name	Reference	Direction	Description
AIGND	—	—	Analog Input Ground—These pins are the reference point for single-ended measurements and the bias current return point for differential measurements. All three ground references—AIGND, AOGND, and DGND—are connected together on the AT E Series device.
ACH<0..15>	AIGND	Input	Analog Input Channels 0 through 15—Each channel pair, ACH<*i*, *i*+8> (*i* = 0..7), can be configured as either one differential input or two single-ended inputs.
ACH<16..63>	AIGND	Input	Analog Input Channels 16 through 63 (AT-MIO-64E-3 only)—Each channel pair, ACH<*i*, *i*+8> (*i* = 16..23, 32..39, 48..55), can be configured as either one differential input or two single-ended inputs.
AISENSE	AIGND	Input	Analog Input Sense—This pin serves as the reference node for any of channels ACH <0..15> in NRSE configuration.
AISENSE2	AIGND	Input	Analog Input Sense (AT-MIO-64E-3 only)—This pin serves as the reference node for any of channels ACH <16..63> in NRSE configuration.
DAC0OUT	AOGND	Output	Analog Channel 0 Output—This pin supplies the voltage output of analog output channel 0. This pin is *not* available on the AT-AI-16XE-10.
DAC1OUT	AOGND	Output	Analog Channel 1 Output—This pin supplies the voltage output of analog output channel 1. This pin is *not* available on the AT-AI-16XE-10.
EXTREF	AOGND	Input	External Reference—This is the external reference input for the analog output circuitry. This pin is *not* available on the AT-MIO-16XE-10, AT-AI-16XE-10, or AT-MIO-16XE-50.
AOGND	—	—	Analog Output Ground—The analog output voltages are referenced to this node. All three ground references—AIGND, AOGND, and DGND—are connected together on the AT E Series device.
DGND	—	—	Digital Ground—This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply. All three ground references—AIGND, AOGND, and DGND—are connected together on the AT E Series device.
DIO<0..7>	DGND	Input or Output	Digital I/O signals—DIO6 and 7 can control the up/down signal of general-purpose counters 0 and 1, respectively.

Table 4-2. I/O Signal Summary for the AT E Series (Continued)

Signal Name	Reference	Direction	Description
PA<0..7>	DGND	Input or Output	Port A—These pins are port A of the extra digital I/O signals on the AT-MIO-16DE-10.
PB<0..7>	DGND	Input or Output	Port B—These pins are port B of the extra digital I/O signals on the AT-MIO-16DE-10.
PC<0..7>	DGND	Input or Output	Port C—These pins are port C of the extra digital I/O signals on the AT-MIO-16DE-10.
+5V	DGND	Output	+5 VDC Source—These pins are fused for up to 1 A of +5 V supply. The fuse is self-resetting.
SCANCLK	DGND	Output	Scan Clock—This pin pulses once for each A/D conversion in the scanning modes when enabled. The low-to-high edge indicates when the input signal can be removed from the input or switched to another signal.
EXTSTROBE*	DGND	Output	External Strobe—This output can be toggled under software control to latch signals or trigger events on external devices.
PFI0/TRIG1	DGND	Input	PFI0/Trigger 1—As an input, this is either one of the Programmable Function Inputs (PFIs) or the source for the hardware analog trigger. PFI signals are explained in the *Timing Connections* section later in this chapter. The hardware analog trigger is explained in the *Analog Trigger* section of Chapter 3, *Hardware Overview*. Analog trigger is available only on the AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-16XE-10, AT-AI-16XE-10, and the AT-MIO-64E-3.
		Output	As an output, this is the TRIG1 signal. In posttrigger data acquisition sequences, a low-to-high transition indicates the initiation of the acquisition sequence. In pretrigger applications, a low-to-high transition indicates the initiation of the pretrigger conversions.
PFI1/TRIG2	DGND	Input	PFI1/Trigger 2—As an input, this is one of the PFIs.
		Output	As an output, this is the TRIG2 signal. In pretrigger applications, a low-to-high transition indicates the initiation of the posttrigger conversions. TRIG2 is not used in posttrigger applications.
PFI2/CONVERT*	DGND	Input	PFI2/Convert—As an input, this is one of the PFIs.
		Output	As an output, this is the CONVERT* signal. A high-to-low edge on CONVERT* indicates that an A/D conversion is occurring.

Table 4-2. I/O Signal Summary for the AT E Series (Continued)

Signal Name	Reference	Direction	Description
PFI3/GPCTR1_SOURCE	DGND	Input	PFI3/Counter 1 Source—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR1_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 1.
PFI4/GPCTR1_GATE	DGND	Input	PFI4/Counter 1 Gate—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR1_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 1.
GPCTR1_OUT	DGND	Output	Counter 1 Output—This output is from the general-purpose counter 1 output.
PFI5/UPDATE*	DGND	Input	PFI5/Update—As an input, this is one of the PFIs.
		Output	As an output, this is the UPDATE* signal. A high-to-low edge on UPDATE* indicates that the analog output primary group is being updated.
PFI6/WFTRIG	DGND	Input	PFI6/Waveform Trigger—As an input, this is one of the PFIs.
		Output	As an output, this is the WFTRIG signal. In timed analog output sequences, a low-to-high transition indicates the initiation of the waveform generation.
PFI7/STARTSCAN	DGND	Input	PFI7/Start of Scan—As an input, this is one of the PFIs.
		Output	As an output, this is the STARTSCAN signal. This pin pulses once at the start of each analog input scan in the interval scan. A low-to-high transition indicates the start of the scan.
PFI8/GPCTR0_SOURCE	DGND	Input	PFI8/Counter 0 Source—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR0_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 0.
PFI9/GPCTR0_GATE	DGND	Input	PFI9/Counter 0 Gate—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR0_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 0.

Table 4-2. I/O Signal Summary for the AT E Series (Continued)

Signal Name	Reference	Direction	Description
GPCTR0_OUT	DGND	Output	Counter 0 Output—This output is from the general-purpose counter 0 output.
FREQ_OUT	DGND	Output	Frequency Output—This output is from the frequency generator output.

Table 4-3. I/O Signal Summary for the AT-MIO-16E-1, AT-MIO-16E-2, and AT-MIO-64E-3

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..63>	AI	100 GΩ in parallel with 100 pF	25/15	—	—	—	±200 pA
AISENSE, AISENSE2	AI	100 GΩ in parallel with 100 pF	25/15	—	—	—	±200 pA
AIGND	AO	—	—	—	—	—	—
DAC0OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	20 V/µs	—
DAC1OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	20 V/µs	—
EXTREF	AI	10 kΩ	25/15	—	—	—	—
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
VCC	DO	0.1 Ω	Short-circuit to ground	1 A	—	—	—
DIO<0..7>	DIO	—	V_{cc} +0.5	13 at (V_{cc} –0.4)	24 at 0.4	1.1	50 kΩ pu[1]
SCANCLK	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	ADIO	10 kΩ	V_{cc} +0.5/±35	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu[2]

Table 4-3. I/O Signal Summary for the AT-MIO-16E-1, AT-MIO-16E-2, and AT-MIO-64E-3 (Continued)

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
PFI1/TRIG2	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{cc}–0.4)	5 at 0.4	1.5	50 kΩ pu

[1] DIO<6..7> are also pulled down with a 50 kΩ resistor.

AI = Analog Input DIO = Digital Input/Output pu = pull up

AO = Analog Output DO = Digital Output ADIO = Analog/Digital Input/Output

[2] Also pulled down with a 10 kΩ resistor.

The tolerance on the 50 kΩ pull-up and pull-down resistors is very large. Actual value may range between 17 kΩ and 100 kΩ.

Table 4-4. I/O Signal Summary for the AT-MIO-16E-10 and AT-MIO-16DE-10

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..15>	AI	100 GΩ in parallel with 50 pF	35/25	—	—	—	±200 pA
AISENSE	AI	100 GΩ in parallel with 50 pF	35/25	—	—	—	±200 pA
AIGND	AO	—	—	—	—	—	—
DAC0OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	15 V/µs	—
DAC1OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	15 V/µs	—
EXTREF	AI	10 kΩ	35/25	—	—	—	—
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
VCC	DO	0.1 Ω	Short-circuit to ground	1A	—	—	—
DIO<0..7>	DIO	—	V_{cc} +0.5	13 at (V_{cc} –0.4)	24 at 0.4	1.1	50 kΩ pu[1]
PA<0..7>	DIO	—	V_{cc} +0.5	2.5 at 3.9	2.5 at 0.4	5	100 kΩ pu
PB<0..7>	DIO	—	V_{cc} +0.5	2.5 at 3.9	2.5 at 0.4	5	100 kΩ pu
PC<0..7>	DIO	—	V_{cc} +0.5	2.5 at 3.9	2.5 at 0.4	5	100 kΩ pu
SCANCLK	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI1/TRIG2	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu

Table 4-4. I/O Signal Summary for the AT-MIO-16E-10 and AT-MIO-16DE-10 (Continued)

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
PFI4/GPCTR1_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc}–0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu

[1] DIO<6..7> are also pulled down with a 50 kΩ resistor.
AI = Analog Input DIO = Digital Input/Output pu = pull up
AO = Analog Output DO = Digital Output

The tolerance on the 50 kΩ pull-up and pull-down resistors is very large. Actual value may range between 17 kΩ and 100 kΩ.

Table 4-5. I/O Signal Summary for the AT-MIO-16XE-10 and AT-AI-16XE-10

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..15>	AI	100 GΩ in parallel with 100 pF	25/15	—	—	—	±1 nA
AISENSE	AI	100 GΩ in parallel with 100 pF	25/15	—	—	—	±1 nA
AIGND	AO	—	—	—	—	—	—
DAC0OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	5 V/µs	—
DAC1OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	5 V/µs	—
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
VCC	DO	0.1 Ω	Short-circuit to ground	1A	—	—	—
DIO<0..7>	DIO	—	V_{cc} +0.5	13 at (V_{cc} –0.4)	24 at 0.4	1.1	50 kΩ pu
SCANCLK	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	4.75 kΩ pu
PFI1/TRIG2	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu

Table 4-5. I/O Signal Summary for the AT-MIO-16XE-10 and AT-AI-16XE-10 (Continued)

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
PFI6/WFTRIG	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{cc}–0.4)	5 at 0.4	1.5	50 kΩ pu

AI = Analog Input DIO = Digital Input/Output pu = pull up
AO = Analog Output DO = Digital Output

The tolerance on the 50 kΩ pull-up and pull-down resistors is very large. Actual value may range between 17 kΩ and 100 kΩ.

Table 4-6. I/O Signal Summary for the AT-MIO-16XE-50

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..15>	AI	20 GΩ in parallel with 100 pF	25/15	—	—	—	±3 nA
AISENSE	AI	20 GΩ in parallel with 100 pF	25/15	—	—	—	±3 nA
AIGND	AO	—	—	—	—	—	—
DAC0OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	2 V/µs	—
DAC1OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	2 V/µs	—
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—

Table 4-6. I/O Signal Summary for the AT-MIO-16XE-50 (Continued)

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
VCC	DO	0.1 Ω	Short-circuit to ground	1A	—	—	—
DIO<0..7>	DIO	—	V_{cc} +0.5	13 at (V_{cc} –0.4)	24 at 0.4	1.1	50 kΩ pu[1]
SCANCLK	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI1/TRIG2	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu

Table 4-6. I/O Signal Summary for the AT-MIO-16XE-50 (Continued)

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
FREQ_OUT	DO	—	—	3.5 at (V_{cc}–0.4)	5 at 0.4	1.5	50 kΩ pu

[1] DIO<6..7> are also pulled down with a 50 kΩ resistor.
AI = Analog Input DIO = Digital Input/Output pu = pull up
AO = Analog Output DO = Digital Output

The tolerance on the 50 kΩ pull-up and pull-down resistors is very large. Actual value may range between 17 kΩ and 100 kΩ.

Analog Input Signal Connections

- AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-16E-10, AT-MIO-16DE-10, AT-MIO-16XE-10, AT-AI-16XE-10, and AT-MIO-16XE-50

  The AI signals are ACH<0..15>, AISENSE, and AIGND. The ACH<0..15> signals are tied to the 16 analog input channels of the AT E Series device. In single-ended mode, signals connected to ACH<0..15> are routed to the positive input of the device PGIA. In differential mode, signals connected to ACH<0..7> are routed to the positive input of the PGIA, and signals connected to ACH<8..15> are routed to the negative input of the PGIA.

- AT-MIO-64E-3

  The AI signals are ACH<0..63>, AISENSE, AISENSE2, and AIGND. The ACH<0..63> signals are tied to the 64 AI channels of the AT-MIO-64E-3. In single-ended mode, signals connected to ACH<0..63> are routed to the positive input of the AT-MIO-64E-3 PGIA. In differential mode, signals connected to ACH<0..7, 16..23, 32..39, 48..55> are routed to the positive input of the PGIA, and signals connected to ACH<8..15, 24..31, 40..47, 56..63> are routed to the negative input of the PGIA.

Caution Exceeding the differential and common-mode input ranges distorts the input signals. Exceeding the maximum input voltage rating can damage the AT E Series device and the PC. NI is *not* liable for any damage resulting from such signal connections. The maximum input voltage ratings are listed in Tables 4-3 through 4-6 in the *Protection* column.

In NRSE mode, the AISENSE and AISENSE2 signals are connected internally to the negative input of the AT E Series device PGIA when their corresponding channels are selected. In DIFF and RSE modes, these signals are left unconnected.

AIGND is an AI common signal that is routed directly to the ground tie point on the AT E Series devices. You can use this signal for a general analog ground tie point to the AT E Series device if necessary.

Connection of AI signals to the AT E Series device depends on the configuration of the AI channels you are using and the type of input signal source. With the different configurations, you can use the PGIA in different ways. Figure 4-4 shows a diagram of the AT E Series device PGIA.

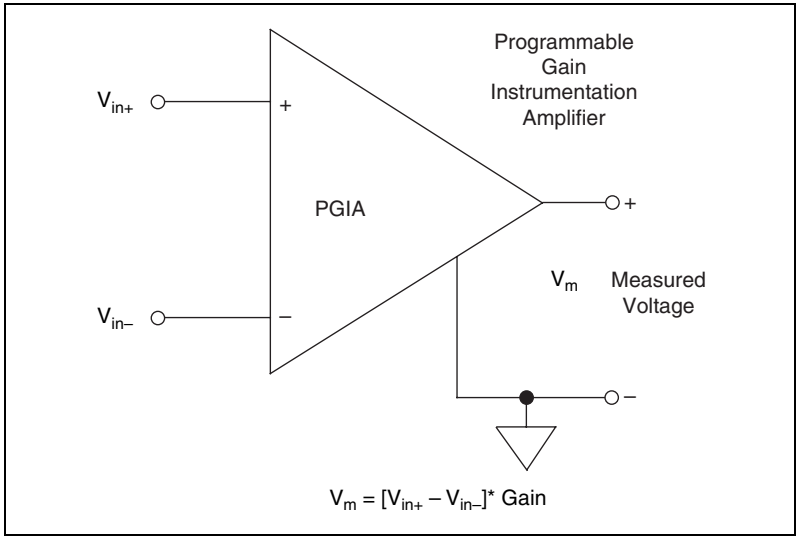


Figure 4-4. AT E Series PGIA

The PGIA applies gain and common-mode voltage rejection and presents high input impedance to the analog input signals connected to the AT E Series device. Signals are routed to the positive and negative inputs of the PGIA through input multiplexers on the device. The PGIA converts two input signals to a signal that is the difference between the two input signals multiplied by the gain setting of the amplifier. The amplifier output voltage is referenced to the ground for the device. The AT E Series device A/D converter (ADC) measures this output voltage when it performs A/D conversions.

You must reference all signals to ground either at the source device or at the device. If you have a floating source, you should reference the signal to ground by using the RSE input mode or the DIFF input configuration with bias resistors. See the *Differential Connections for Nonreferenced or Floating Signal Sources* section later in this chapter. If you have a grounded source, you should not reference the signal to AIGND. You can avoid this reference by using DIFF or NRSE input configurations.

Types of Signal Sources

When configuring the input channels and making signal connections, you must first determine whether the signal sources are floating or ground-referenced. The following sections describe these two types of signals.

Floating Signal Sources

A floating signal source is one that is not connected in any way to the building ground system but, rather, has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source. You must tie the ground reference of a floating signal to the AT E Series device AIGND to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats out of the common-mode input range.

Ground-Referenced Signal Sources

A ground-referenced signal source is one that is connected in some way to the building system ground and is, therefore, already connected to a common ground point with respect to the AT E Series device, assuming that the PC is plugged into the same power system. Nonisolated outputs of instruments and devices that plug into the building power system fall into this category.

The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV but can be much higher if power distribution circuits are not properly connected. If a grounded signal source is improperly measured, this difference may appear as an error in the measurement. The connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

Input Configurations

You can configure the AT E Series device for one of three input modes—NRSE, RSE, or DIFF. The following sections discuss the use of single-ended and differential measurements and considerations for measuring both floating and ground-referenced signal sources.

Figure 4-5 summarizes the recommended input configuration for both types of signal sources.

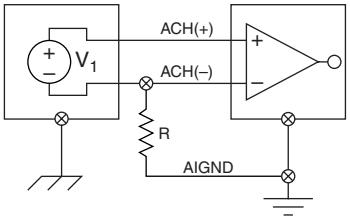
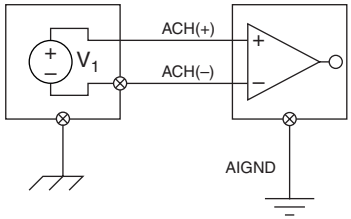
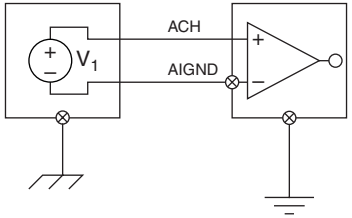
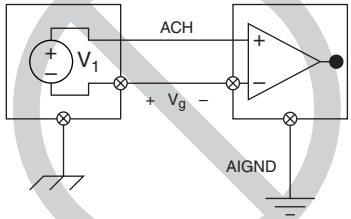
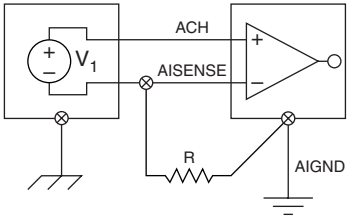
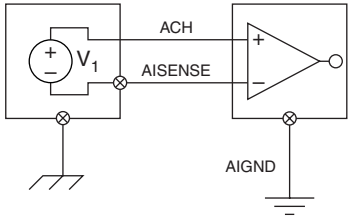
Input	Signal Source Type	
	Floating Signal Source (Not Connected to Building Ground)	**Grounded Signal Source**
	Examples • Ungrounded Thermocouples • Signal Conditioning with Isolated Outputs • Battery Devices	Examples • Plug-in Instruments with Nonisolated Outputs
Differential (DIFF)	 See text for information on bias resistors.	
Single-Ended — Ground Referenced (RSE)		NOT RECOMMENDED  Ground-loop losses, V_g, are added to measured signal.
Single-Ended — Nonreferenced (NRSE)	 See text for information on bias resistors.	

Figure 4-5. Summary of Analog Input Connections

Differential Connection Considerations (DIFF Input Configuration)

A differential connection is one in which the AT E Series device AI signal has its own reference signal or signal return path. These connections are available when the selected channel is configured in DIFF input mode. The input signal is tied to the positive input of the PGIA, and its reference signal, or return, is tied to the negative input of the PGIA.

When you configure a channel for differential input, each signal uses two multiplexer inputs—one for the signal and one for its reference signal. Therefore, with a differential configuration for every channel, up to eight AI channels are available (up to 32 channels on the AT-MIO-64E-3).

In DIFF input mode, the AI channels are paired, with ACH<*i*> as the signal input and ACH<*i*+*8*> as the signal reference. For example, ACH0 is paired with ACH8, ACH1 is paired with ACH9, and so on.

You should use differential input connections for any channel that meets any of the following conditions:

- The input signal is low level (less than 1 V).
- The leads connecting the signal to the AT E Series device are greater than 10 ft (3 m).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce picked-up noise and increase common-mode noise rejection. Differential signal connections also allow input signals to float within the common-mode limits of the PGIA.

Differential Connections for Ground-Referenced Signal Sources

Figure 4-6 shows how to connect a ground-referenced signal source to an AT E Series device channel configured in DIFF input mode.

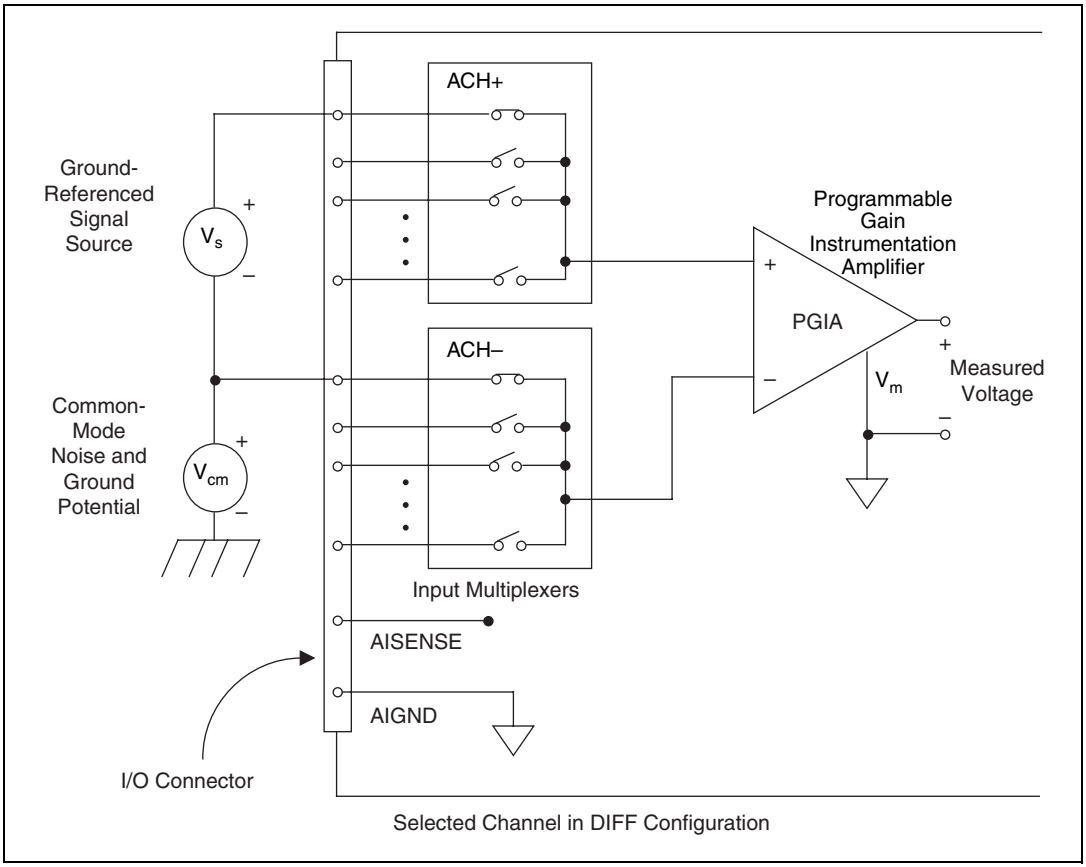


Figure 4-6. Differential Input Connections for Ground-Referenced Signals

With this type of connection, the PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the AT E Series device ground, shown as V_{cm} in Figure 4-6.

Differential Connections for Nonreferenced or Floating Signal Sources

Figure 4-7 shows how to connect a floating signal source to an AT E Series device channel configured in DIFF input mode.

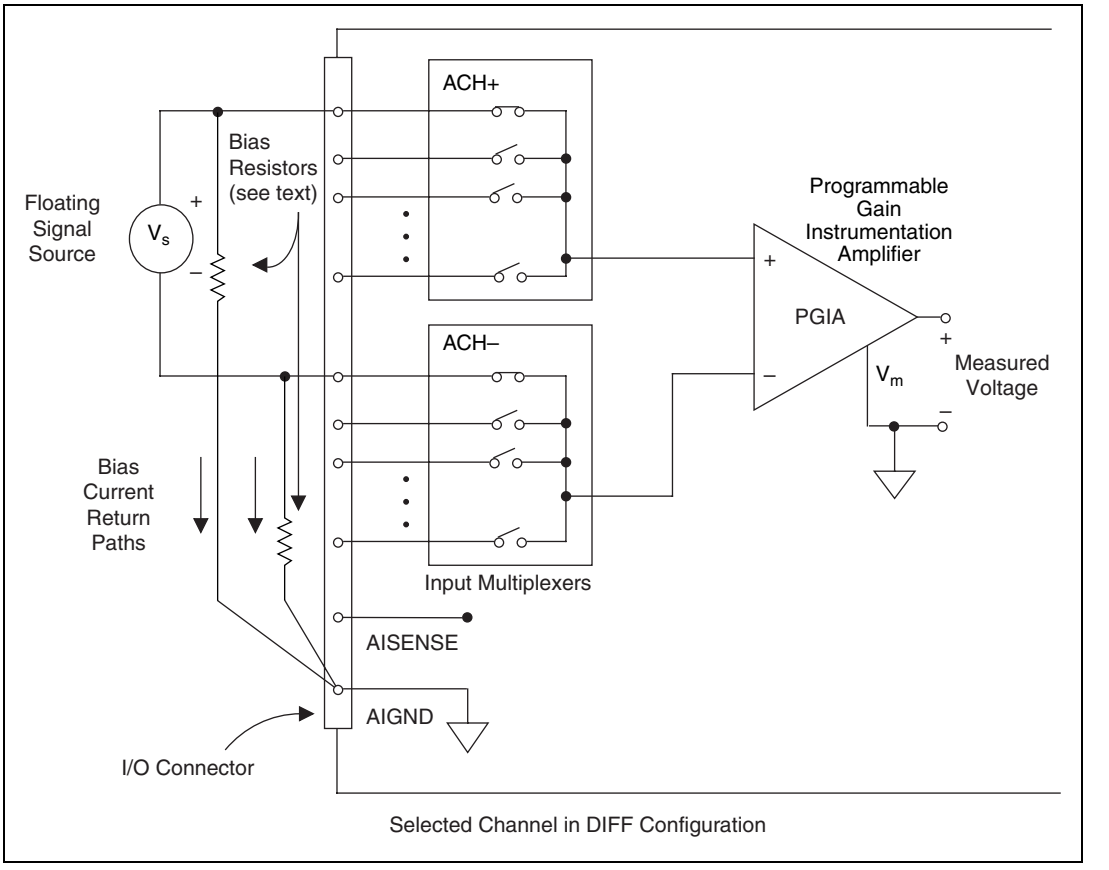


Figure 4-7. Differential Input Connections for Nonreferenced Signals

Figure 4-7 shows two bias resistors connected in parallel with the signal leads of a floating signal source. If you do not use the resistors and the source is truly floating, the source is not likely to remain within the common-mode signal range of the PGIA, and the PGIA saturates, causing erroneous readings. You must reference the source to AIGND. The easiest way is simply to connect the positive side of the signal to the positive input of the PGIA and connect the negative side of the signal to AIGND as well

as to the negative input of the PGIA, without any resistors at all. This connection works well for DC-coupled sources with low source impedance (less than 100 Ω).

However, for larger source impedances, this connection leaves the differential signal path significantly out of balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line because it is connected to ground. Hence, this noise appears as a differential-mode signal instead of a common-mode signal, and so the PGIA does not reject it. In this case, instead of directly connecting the negative line to AIGND, connect it to AIGND through a resistor that is about 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance, so that about the same amount of noise couples onto both connections, yielding better rejection of electrostatically coupled noise. Also, this configuration does not load down the source (other than the very high input impedance of the PGIA).

You can fully balance the signal path by connecting another resistor of the same value between the positive input and AIGND, as shown in Figure 4-7. This fully balanced configuration offers slightly better noise rejection but has the disadvantage of loading the source down with the series combination (sum) of the two resistors. If, for example, the source impedance is 2 kΩ and each of the two resistors is 100 kΩ, the resistors load down the source with 200 kΩ and produce a –1% gain error.

Both inputs of the PGIA require a DC path to ground in order for the PGIA to work. If the source is AC coupled (capacitively coupled), the PGIA needs a resistor between the positive input and AIGND. If the source has low impedance, choose a resistor that is large enough not to significantly load the source but small enough not to produce significant input offset voltage as a result of input bias current (typically 100 kΩ to 1 MΩ). In this case, you can tie the negative input directly to AIGND. If the source has high output impedance, you should balance the signal path as previously described using the same value resistor on both the positive and negative inputs; you should be aware that there is some gain error from loading down the source.

Single-Ended Connection Considerations

A single-ended connection is one in which the AT E Series device AI signal is referenced to a ground that can be shared with other input signals. The input signal is tied to the positive input of the PGIA, and the ground is tied to the negative input of the PGIA.

When every channel is configured for single-ended input, up to 16 analog input channels are available (up to 64 channels on the AT-MIO-64E-3).

You can use single-ended input connections for any input signal that meets the following conditions:

- The input signal is high level (greater than 1 V).
- The leads connecting the signal to the AT E Series device are less than 10 ft (3 m).
- The input signal can share a common reference point with other signals.

DIFF input connections are recommended for greater signal integrity for any input signal that does not meet the preceding conditions.

You can software configure the AT E Series device channels for two different types of single-ended connections—RSE configuration and NRSE configuration. The RSE configuration is used for floating signal sources; in this case, the AT E Series device provides the reference ground point for the external signal. The NRSE input configuration is used for ground-referenced signal sources; in this case, the external signal supplies its own reference ground point and the AT E Series device should not supply one.

In single-ended configurations, more electrostatic and magnetic noise couples into the signal connections than in differential configurations. The coupling is the result of differences in the signal path. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two conductors.

Single-Ended Connections for Floating Signal Sources (RSE Configuration)

Figure 4-8 shows how to connect a floating signal source to an AT E Series device channel configured for RSE mode.

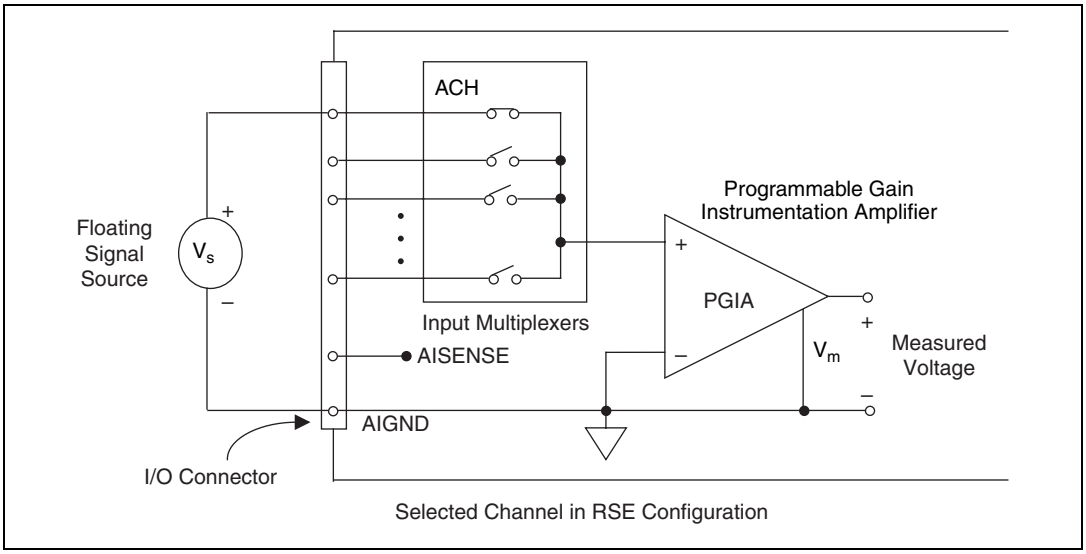


Figure 4-8. Single-Ended Input Connections for Nonreferenced or Floating Signals

Single-Ended Connections for Grounded Signal Sources (NRSE Configuration)

To measure a grounded signal source with a single-ended configuration, you must configure the AT E Series device in the NRSE input configuration. The signal is then connected to the positive input of the AT E Series PGIA, and the signal local ground reference is connected to the negative input of the PGIA. The ground point of the signal should, therefore, be connected to the AISENSE pin. Any potential difference between the AT E Series ground and the signal ground appears as a common-mode signal at both the positive and negative inputs of the PGIA, and this difference is rejected by the amplifier. If the input circuitry of an AT E Series device were referenced to ground, in this situation as in the RSE input configuration, this difference in ground potentials would appear as an error in the measured voltage.

Figure 4-9 shows how to connect a grounded signal source to an AT E Series device channel configured for NRSE mode.

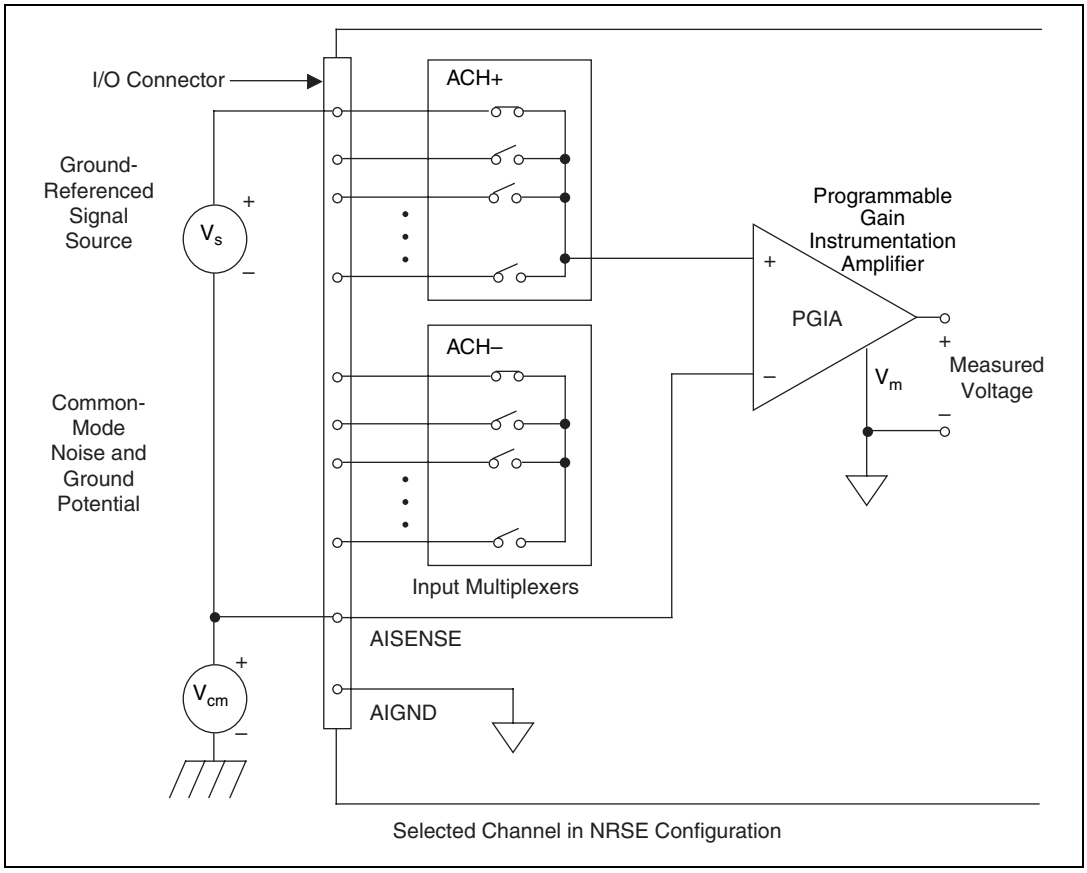


Figure 4-9. Single-Ended Input Connections for Ground-Referenced Signal

Common-Mode Signal Rejection Considerations

Figures 4-6 and 4-9 show connections for signal sources that are already referenced to some ground point with respect to the AT E Series device. In these cases, the PGIA can reject any voltage caused by ground potential differences between the signal source and the device. In addition, with differential input connections, the PGIA can reject common-mode noise pickup in the leads connecting the signal sources to the device. The PGIA can reject common-mode signals as long as V_{in}+ and V_{in}– are both within ±11 V of AIGND. The AT-MIO-16XE-50 has the additional restriction

that (V_{in}+) + (V_{in}–) added to the gain times (V_{in}+) – (V_{in}–) must be within ±26 V of AIGND. At gains of 10 and 100, this is roughly equivalent to restricting the two input voltages to within ±8 V of AIGND.

Analog Output Signal Connections

The AO signals are DAC0OUT, DAC1OUT, EXTREF, and AOGND.

Note DAC0OUT and DAC1OUT are *not* available on the AT-AI-16XE-10. EXTREF is *not* available on the AT-MIO-16XE-10, AT-AI-16XE-10, or AT-MIO-16XE-50.

DAC0OUT is the voltage output signal for AO channel 0. DAC1OUT is the voltage output signal for AO channel 1.

EXTREF is the external reference input for both AO channels. You must configure each AO channel individually for external reference selection in order for the signal applied at the external reference input to be used by that channel. If you do not specify an external reference, the channel uses the internal reference.

Note You cannot use an external AO reference with the AT-MIO-16XE-10, AT-AI-16XE-10, or AT-MIO-16XE-50.

AO configuration options are explained in the *Analog Output* section of Chapter 3, *Hardware Overview*.

AOGND is the ground reference signal for both AO channels and the external reference signal.

Figure 4-10 shows how to make AO connections and the external reference input connection to the AT E Series device.

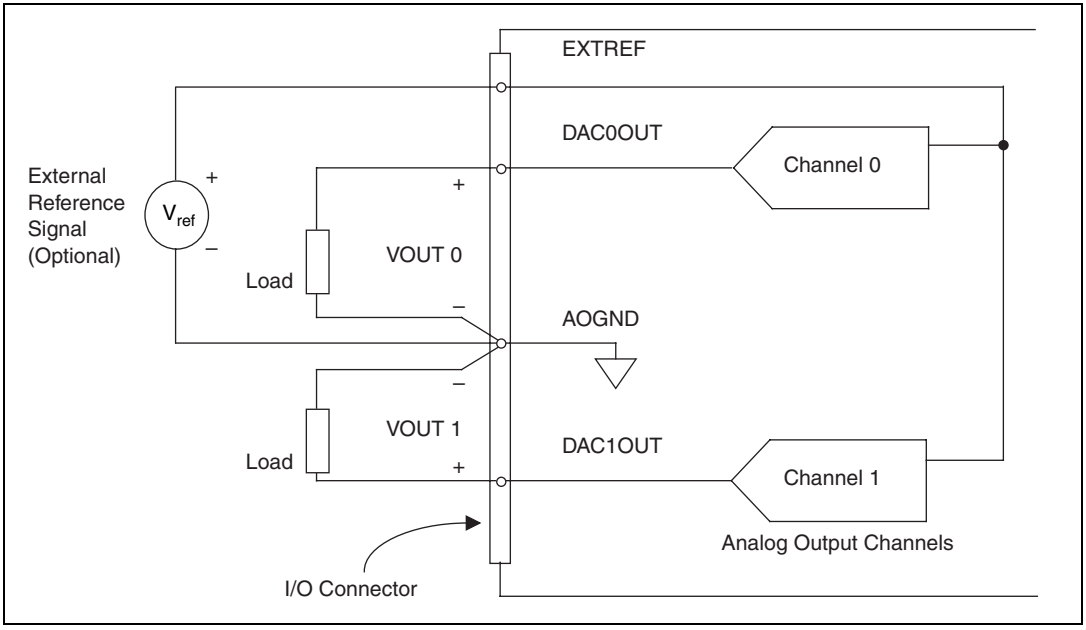


Figure 4-10. AO Connections

The external reference signal can be either a DC or an AC signal. The device multiplies this reference signal by the DAC code (divided by the full-scale DAC code) to generate the output voltage.

Digital I/O Signal Connections

The digital I/O signals are DIO<0..7> and DGND. DIO<0..7> are the signals making up the DIO port, and DGND is the ground reference signal for the DIO port. You can program all lines individually to be inputs or outputs. The AT-MIO-16DE-10 has 24 additional DIO lines, configured as three 8-bit ports: PA<0..7>, PB<0..7>, and PC<0..7>. You can configure each port for both input and output in various combinations, with some handshaking capabilities.

Caution Exceeding the maximum input voltage ratings, which are listed in Tables 4-3 through 4-6, can damage the AT E Series device and the PC. NI is *not* liable for any damage resulting from such signal connections.

Figure 4-11 shows signal connections for three typical DIO applications.

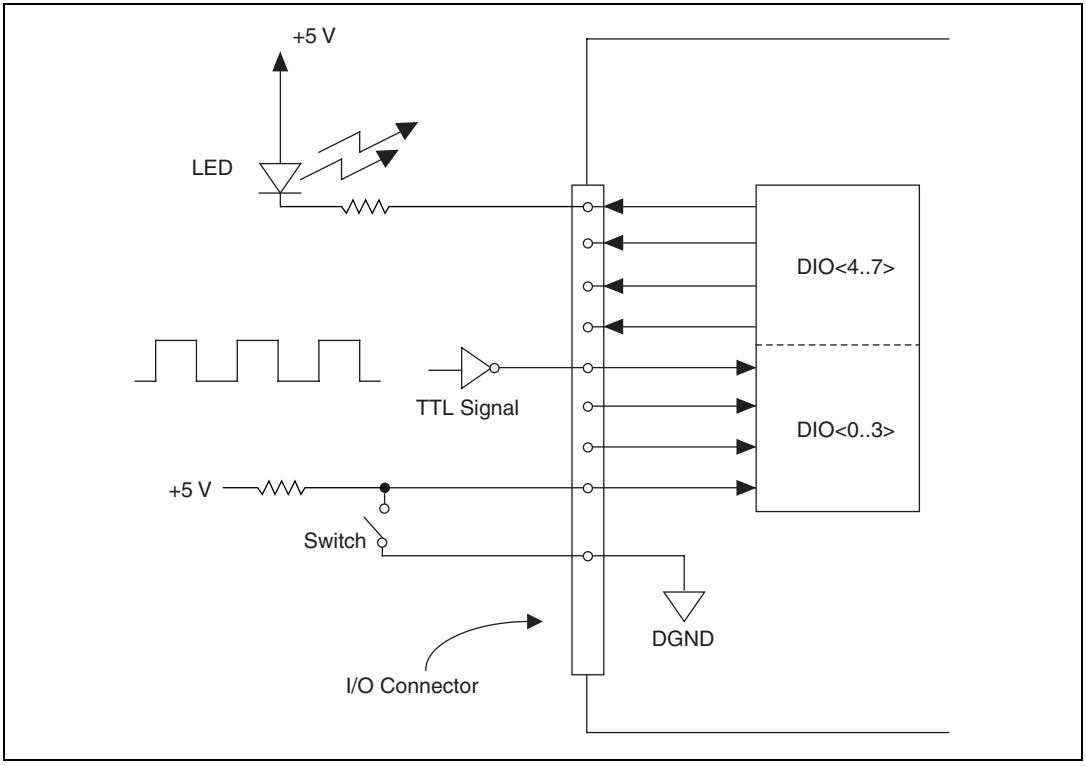


Figure 4-11. DIO Connections

Figure 4-11 shows DIO<0..3> configured for digital input and DIO<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states such as the state of the switch shown in the figure. Digital output applications include sending TTL signals and driving external devices such as the LED shown in the figure.

Power Connections

Two pins on the I/O connector supply +5 V from the PC power supply using a self-resetting fuse. The fuse resets automatically within a few seconds after the overcurrent condition is removed. These pins are referenced to DGND and can be used to power external digital circuitry. The combined total power rating for both pins should be between +4.65 VDC to +5.25 VDC at 1 A.

Caution Under no circumstances should you connect these +5 V power pins directly to analog or digital ground or to any other voltage source on the AT E Series device or any other device. Doing so can damage the AT E Series device and the PC. NI is *not* liable for damage resulting from such a connection.

Timing Connections

Caution Exceeding the maximum input voltage ratings, which are listed in Tables 4-3 through 4-6, can damage the AT E Series device and the PC. NI is *not* liable for any damage resulting from such signal connections.

All external control over the timing of the AT E Series device is routed through the 10 programmable function inputs labeled PFI0 through PFI9. These signals are explained in detail in the next section, *Programmable Function Input Connections*. These PFIs are bidirectional; as outputs they are not programmable and reflect the state of many data acquisition, waveform generation, and general-purpose timing signals. There are five other dedicated outputs for the remainder of the timing signals. As inputs, the PFI signals are programmable and can control any data acquisition, waveform generation, and general-purpose timing signals.

The data acquisition signals are explained in the *DAQ Timing Connections* section later in this chapter. The waveform generation signals are explained in the *Waveform Generation Timing Connections* section later in this chapter. The general-purpose timing signals are explained in the *General-Purpose Timing Signal Connections* section later in this chapter.

All digital timing connections are referenced to DGND. This reference is demonstrated in Figure 4-12, which shows how to connect an external TRIG1 source and an external CONVERT* source to two of the AT E Series device PFI pins.

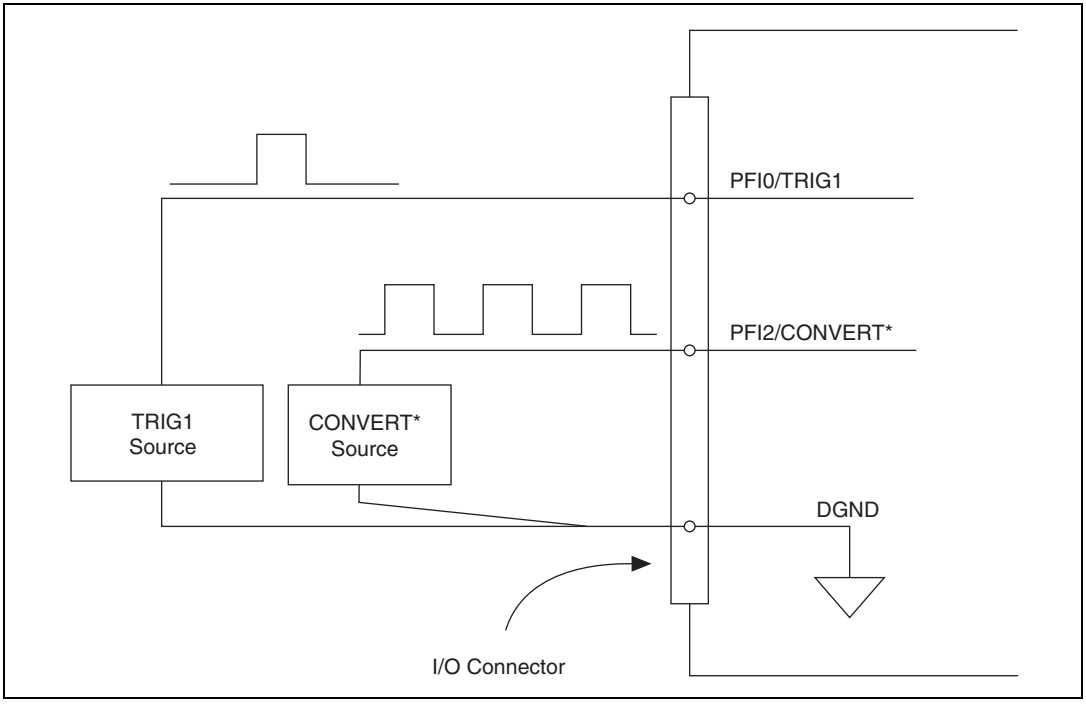


Figure 4-12. TIO Connections

Programmable Function Input Connections

There are a total of 13 internal timing signals that you can externally control from the PFI pins. The source for each of these signals is software selectable from any of the PFIs when you want external control. This flexible routing scheme reduces the need to change the physical wiring to the device I/O connector for different applications requiring alternative wiring.

You can individually enable each of the PFI pins to output a specific internal timing signal. For example, if you need the CONVERT* signal as an output on the I/O connector, software can turn on the output driver for the PFI2/CONVERT* pin. You must be careful not to drive a PFI signal externally when it is configured as an output.

As an input, you can individually configure each PFI for edge or level detection and for polarity selection, as well. You can use the polarity selection for any of the 13 timing signals, but the edge or level detection

depends upon the particular timing signal being controlled. The detection requirements for each timing signal are listed within the section that discusses that individual signal.

In edge-detection mode, the minimum pulse width required is 10 ns. This applies for both rising-edge and falling-edge polarity settings. There is no maximum pulse-width requirement in edge-detect mode.

In level-detection mode, there are no minimum or maximum pulse-width requirements imposed by the PFIs themselves, but there may be limits imposed by the particular timing signal being controlled. These requirements are listed later in this chapter.

DAQ Timing Connections

The DAQ timing signals are TRIG1, TRIG2, STARTSCAN, CONVERT*, AIGATE, SISOURCE, SCANCLK, and EXTSTROBE*.

Posttriggered DAQ allows you to view only data that is acquired after a trigger event is received. A typical posttriggered DAQ sequence is shown in Figure 4-13. Pretriggered DAQ allows you to view data that is acquired before the trigger of interest in addition to data acquired after the trigger. Figure 4-14 shows a typical pretriggered DAQ sequence. The description for each signal shown in these figures is included later in this chapter.

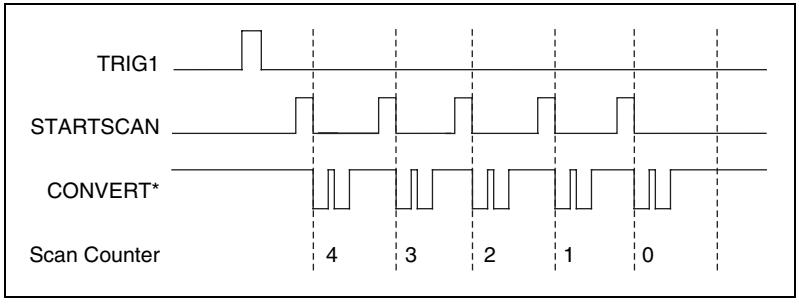


Figure 4-13. Typical Posttriggered Acquisition

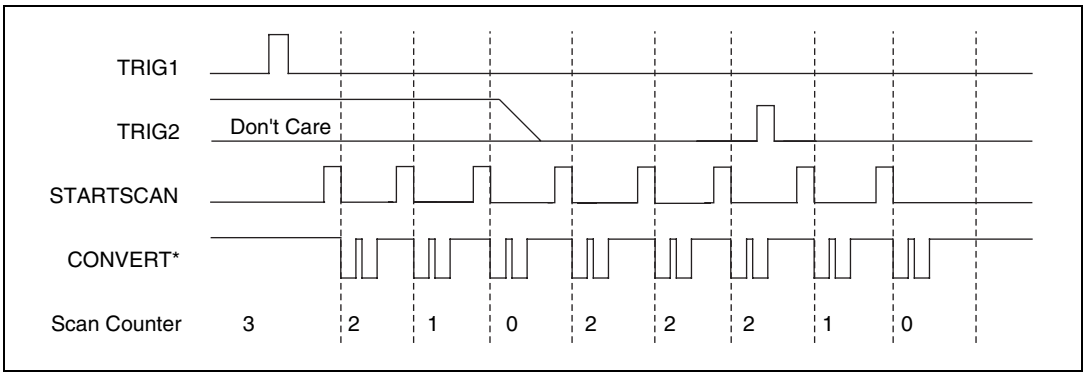


Figure 4-14. Typical Pretriggered Acquisition

TRIG1 Signal

Any PFI pin can externally input the TRIG1 signal, which is available as an output on the PFI0/TRIG1 pin.

Refer to Figures 4-13 and 4-14 for the relationship of TRIG1 to the DAQ sequence.

As an input, the TRIG1 signal is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG1 and configure the polarity selection for either rising or falling edge. The selected edge of the TRIG1 signal starts the DAQ sequence for both posttriggered and pretriggered acquisitions. The AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-16XE-10, AT-AI-16XE-10, and AT-MIO-64E-3 support analog triggering on the PFI0/TRIG1 pin. Refer to Chapter 3, *Hardware Overview*, for more information on analog triggering.

As an output, the TRIG1 signal reflects the action that initiates a DAQ sequence, even if the acquisition is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-15 and 4-16 show the input and output timing requirements for the TRIG1 signal.

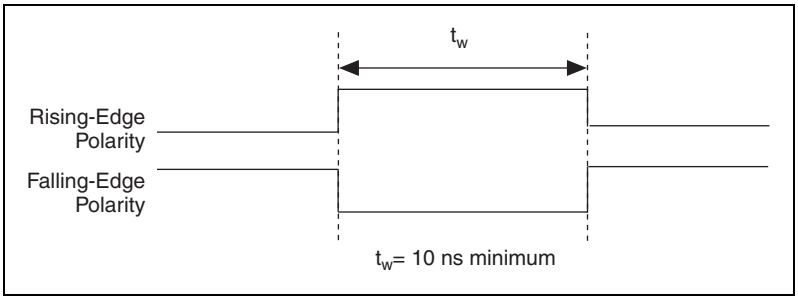


Figure 4-15. TRIG1 Input Signal Timing

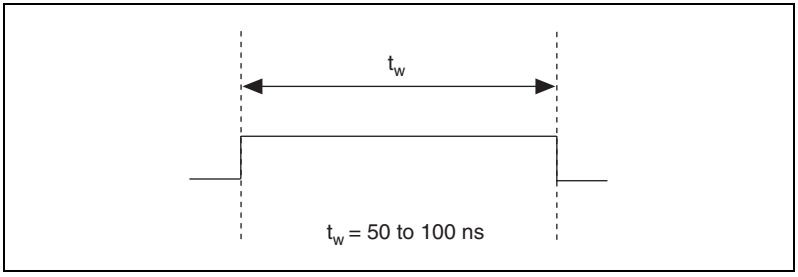


Figure 4-16. TRIG1 Output Signal Timing

The device also uses the TRIG1 signal to initiate pretriggered DAQ operations. In most pretriggered applications, the TRIG1 signal is generated by a software trigger. Refer to the TRIG2 signal description for a complete description of the use of TRIG1 and TRIG2 in a pretriggered DAQ operation.

TRIG2 Signal

Any PFI pin can externally input the TRIG2 signal, which is available as an output on the PFI1/TRIG2 pin.

Refer to Figure 4-13 for the relationship of TRIG2 to the DAQ sequence.

As an input, the TRIG2 signal is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG2 and configure the polarity selection for either rising or falling edge. The selected edge of the TRIG2 signal initiates the posttriggered phase of a pretriggered acquisition sequence. In pretriggered mode, the TRIG1 signal initiates the data acquisition. The scan counter indicates the minimum number of scans

before TRIG2 can be recognized. After the scan counter decrements to zero, it is loaded with the number of posttrigger scans to acquire while the acquisition continues. The device ignores the TRIG2 signal if it is asserted prior to the scan counter decrementing to zero. After the selected edge of TRIG2 is received, the device acquires a fixed number of scans and the acquisition stops. This mode acquires data both before and after receiving TRIG2.

As an output, the TRIG2 signal reflects the posttrigger in a pretriggered acquisition sequence, even if the acquisition is being externally triggered by another PFI. The TRIG2 signal is not used in posttriggered data acquisition. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-17 and 4-18 show the input and output timing requirements for the TRIG2 signal.

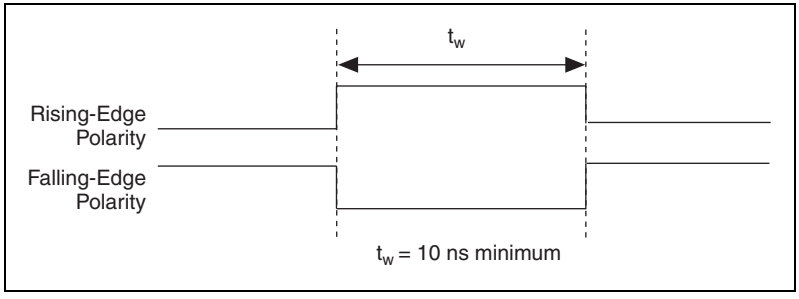


Figure 4-17. TRIG2 Input Signal Timing

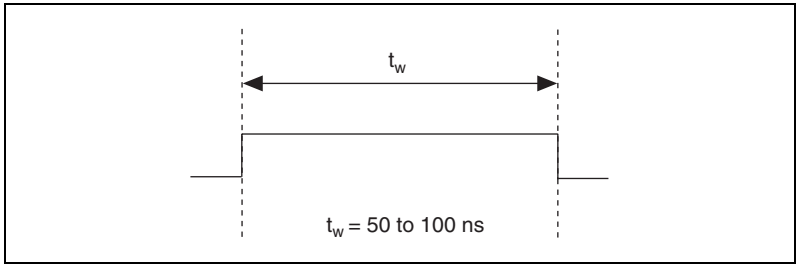


Figure 4-18. TRIG2 Output Signal Timing

STARTSCAN Signal

Any PFI pin can externally input the STARTSCAN signal, which is available as an output on the PFI7/STARTSCAN pin.

Refer to Figures 4-13 and 4-14 for the relationship of STARTSCAN to the DAQ sequence.

As an input, the STARTSCAN signal is configured in the edge-detection mode. You can select any PFI pin as the source for STARTSCAN and configure the polarity selection for either rising or falling edge. The selected edge of the STARTSCAN signal initiates a scan. The sample interval counter is started if you select internally triggered CONVERT*.

As an output, the STARTSCAN signal reflects the actual start pulse that initiates a scan, even if the starts are being externally triggered by another PFI. You have two output options. The first is an active high pulse with a pulse width of 50 to 100 ns, which indicates the start of the scan. The second action is an active high pulse that terminates at the start of the last conversion in the scan, which indicates a scan in progress. STARTSCAN is deserted t_{off} after the last conversion in the scan is initiated. This output is set to high-impedance at startup.

Figures 4-19 and 4-20 show the input and output timing requirements for the STARTSCAN signal.

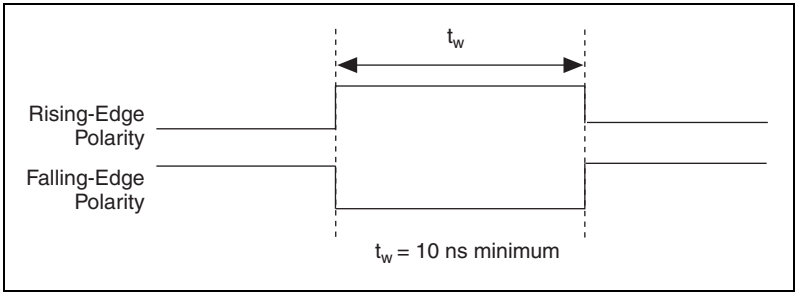


Figure 4-19. STARTSCAN Input Signal Timing

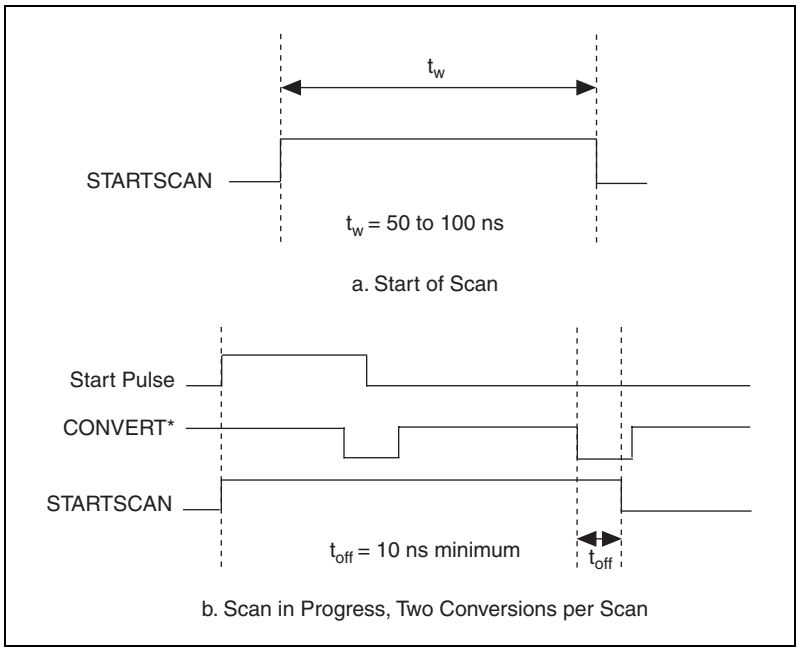


Figure 4-20. STARTSCAN Output Signal Timing

The CONVERT* pulses are masked off until the device generates the STARTSCAN signal. If you are using internally generated conversions, the first CONVERT* appears when the onboard sample interval counter reaches zero. If you select an external CONVERT*, the first external pulse after STARTSCAN generates a conversion. The STARTSCAN pulses should be separated by at least one scan period.

A counter on the AT E Series device internally generates the STARTSCAN signal unless you select some external source. This counter is started by the TRIG1 signal and is stopped either by software or by the sample counter.

Scans generated by either an internal or external STARTSCAN signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

CONVERT* Signal

Any PFI pin can externally input the CONVERT* signal, which is available as an output on the PFI2/CONVERT* pin.

Refer to Figures 4-13 and 4-14 for the relationship of CONVERT* to the DAQ sequence.

As an input, the CONVERT* signal is configured in the edge-detection mode. You can select any PFI pin as the source for CONVERT* and configure the polarity selection for either rising or falling edge. The selected edge of the CONVERT* signal initiates an A/D conversion.

As an output, the CONVERT* signal reflects the actual convert pulse that is connected to the ADC, even if the conversions are being externally generated by another PFI. The output is an active low pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-21 and 4-22 show the input and output timing requirements for the CONVERT* signal.

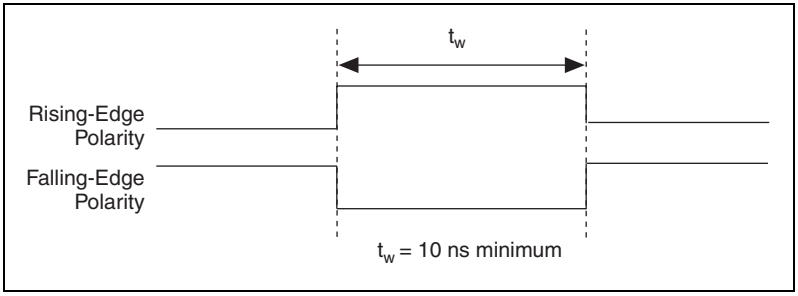


Figure 4-21. CONVERT* Input Signal Timing

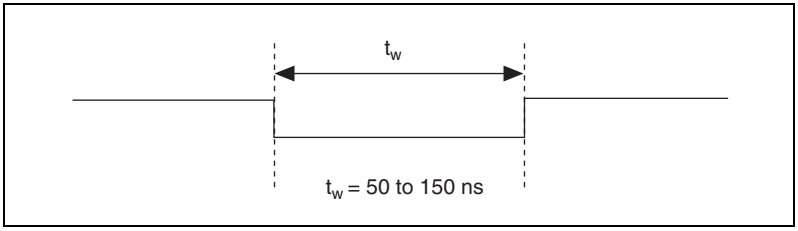


Figure 4-22. CONVERT* Output Signal Timing

The ADC switches to hold mode within 60 ns of the selected edge. This hold-mode delay time is a function of temperature and does not vary from one conversion to the next. Separate the CONVERT* pulses by at least one conversion period.

The sample interval counter on the AT E Series device normally generates the CONVERT* signal unless you select some external source. The counter is started by the STARTSCAN signal and continues to count down and reload itself until the scan is finished. It then reloads itself in readiness for the next STARTSCAN pulse.

A/D conversions generated by either an internal or external CONVERT* signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

AIGATE Signal

Any PFI pin can externally input the AIGATE signal, which is not available as an output on the I/O connector. The AIGATE signal can mask off scans in a DAQ sequence. You can configure the PFI pin you select as the source for the AIGATE signal in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low. In the level-detection mode if AIGATE is active, the STARTSCAN signal is masked off and no scans can occur.

The AIGATE signal can neither stop a scan in progress nor continue a previously gated-off scan; in other words, once a scan has started, AIGATE does not gate off conversions until the beginning of the next scan and, conversely, if conversions are being gated off, AIGATE does not gate them back on until the beginning of the next scan.

SISOURCE Signal

Any PFI pin can externally input the SISOURCE signal, which is not available as an output on the I/O connector. The onboard scan interval counter uses the SISOURCE signal as a clock to time the generation of the STARTSCAN signal. You must configure the PFI pin you select as the source for the SISOURCE signal in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase generates the SISOURCE signal unless you select some external source. Figure 4-23 shows the timing requirements for the SISOURCE signal.

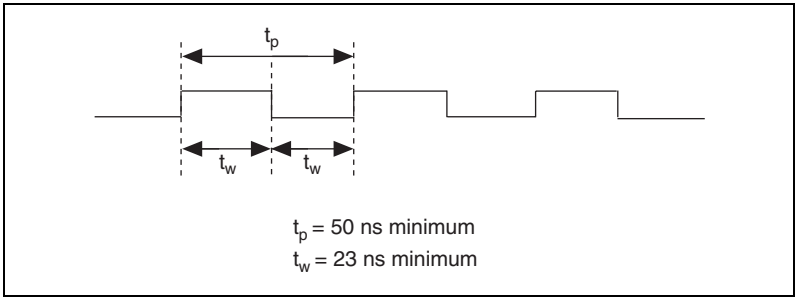


Figure 4-23. SISOURCE Signal Timing

SCANCLK Signal

SCANCLK is an output-only signal that generates a pulse with the leading edge occurring approximately 50 to 100 ns after an A/D conversion begins. The polarity of this output is software selectable but is typically configured so that a low-to-high leading edge can clock external AI multiplexers indicating when the input signal has been sampled and can be removed. This signal has a 400 to 500 ns pulse width and is software enabled. Figure 4-24 shows the timing for the SCANCLK signal.

Note When using NI-DAQ, SCANCLK polarity is low-to-high and cannot be changed programmatically.

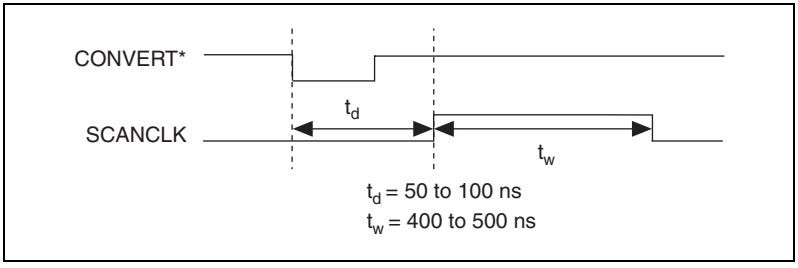


Figure 4-24. SCANCLK Signal Timing

EXTSTROBE* Signal

EXTSTROBE* is an output-only signal that generates either a single pulse or a sequence of eight pulses in the hardware-strobe mode. An external device can use this signal to latch signals or to trigger events. In the single-pulse mode, software controls the level of the EXTSTROBE* signal. A 10 µs and a 1.2 µs clock are available for generating a sequence of eight pulses in the hardware-strobe mode. Figure 4-25 shows the timing for the hardware-strobe mode EXTSTROBE* signal.

Note EXSTROBE* cannot be enabled through NI-DAQ.

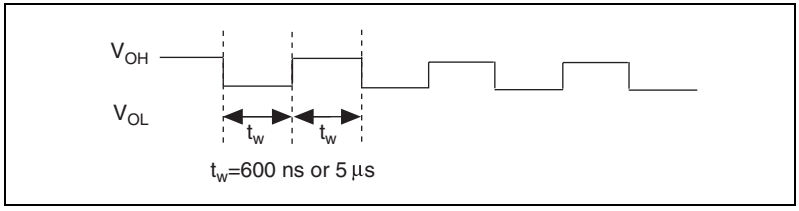


Figure 4-25. EXTSTROBE* Signal Timing

Waveform Generation Timing Connections

The analog group defined for the AT E Series device is controlled by WFTRIG, UPDATE*, and UISOURCE.

WFTRIG Signal

Any PFI pin can externally input the WFTRIG signal, which is available as an output on the PFI6/WFTRIG pin.

As an input, the WFTRIG signal is configured in the edge-detection mode. You can select any PFI pin as the source for WFTRIG and configure the polarity selection for either rising or falling edge. The selected edge of the WFTRIG signal starts the waveform generation for the DACs. The update interval (UI) counter is started if you select internally generated UPDATE*.

As an output, the WFTRIG signal reflects the trigger that initiates waveform generation, even if the waveform generation is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-26 and 4-27 show the input and output timing requirements for the WFTRIG signal.

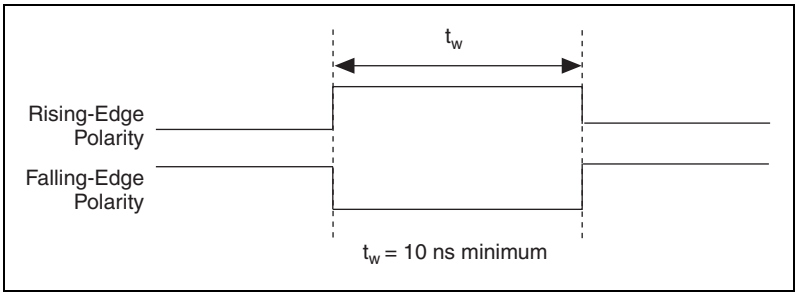


Figure 4-26. WFTRIG Input Signal Timing

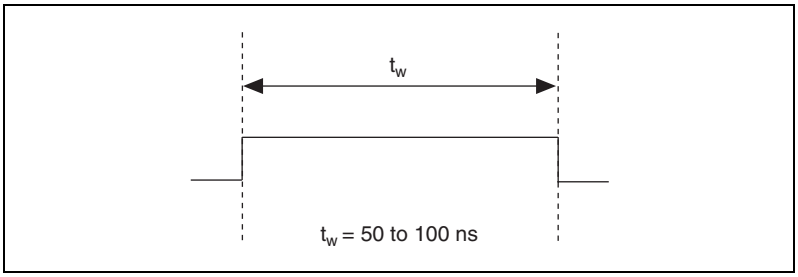


Figure 4-27. WFTRIG Output Signal Timing

UPDATE* Signal

Any PFI pin can externally input the UPDATE* signal, which is available as an output on the PFI5/UPDATE* pin.

As an input, the UPDATE* signal is configured in the edge-detection mode. You can select any PFI pin as the source for UPDATE* and configure the polarity selection for either rising or falling edge. The selected edge of the UPDATE* signal updates the outputs of the DACs. In order to use UPDATE*, you must set the DACs to posted-update mode.

As an output, the UPDATE* signal reflects the actual update pulse that is connected to the DACs, even if the updates are being externally generated by another PFI. The output is an active low pulse with a pulse width of 300 to 350 ns. This output is set to high-impedance at startup.

When using an external UPDATE signal, you must apply at least one more external update pulse than the number of points that you want to generate. This is necessary for proper hardware operation, otherwise the device does not indicate that the waveform generation is complete.

Figures 4-28 and 4-29 show the input and output timing requirements for the UPDATE* signal.

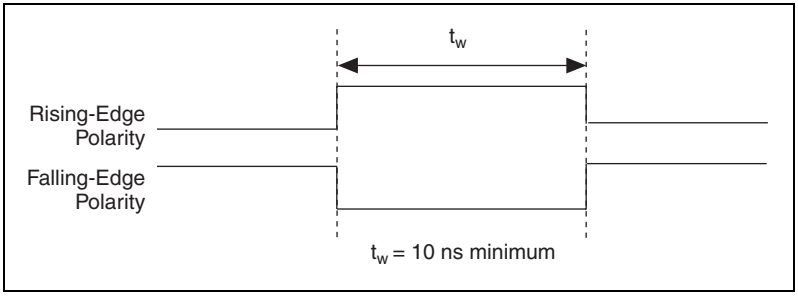


Figure 4-28. UPDATE* Input Signal Timing

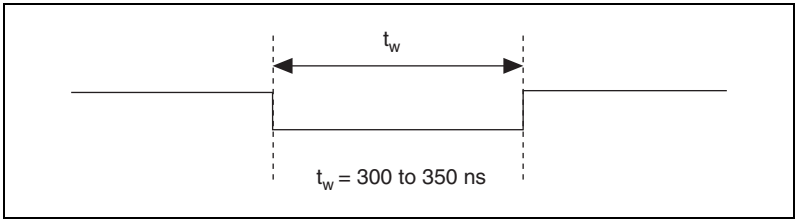


Figure 4-29. UPDATE* Output Signal Timing

The DACs are updated within 100 ns of the leading edge. Separate the UPDATE* pulses with enough time that new data can be written to the DAC latches.

The AT E Series device UI counter normally generates the UPDATE* signal unless you select some external source. The UI counter is started by the WFTRIG signal and can be stopped by software or the internal Buffer Counter.

D/A conversions generated by either an internal or external UPDATE* signal do not occur when gated by the software command register gate.

UISOURCE Signal

Any PFI pin can externally input the UISOURCE signal, which is not available as an output on the I/O connector. The UI counter uses the UISOURCE signal as a clock to time the generation of the UPDATE* signal. You must configure the PFI pin you select as the source for the UISOURCE signal in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low. Figure 4-30 shows the timing requirements for the UISOURCE signal.

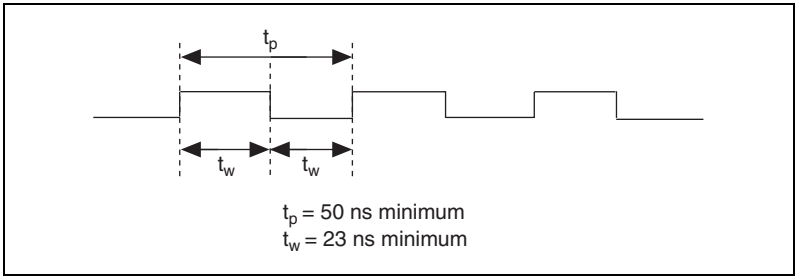


Figure 4-30. UISOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase normally generates the UISOURCE signal unless you select some external source.

General-Purpose Timing Signal Connections

The general-purpose timing signals are GPCTR0_SOURCE, GPCTR0_GATE, GPCTR0_OUT, GPCTR0_UP_DOWN, GPCTR1_SOURCE, GPCTR1_GATE, GPCTR1_OUT, GPCTR1_UP_DOWN, and FREQ_OUT.

GPCTR0_SOURCE Signal

Any PFI pin can externally input the GPCTR0_SOURCE signal, which is available as an output on the PFI8/GPCTR0_SOURCE pin.

As an input, the GPCTR0_SOURCE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, the GPCTR0_SOURCE signal reflects the actual clock connected to general-purpose counter 0, even if another PFI is externally inputting the source clock. This output is set to high-impedance at startup.

Figure 4-31 shows the timing requirements for the GPCTR0_SOURCE signal.

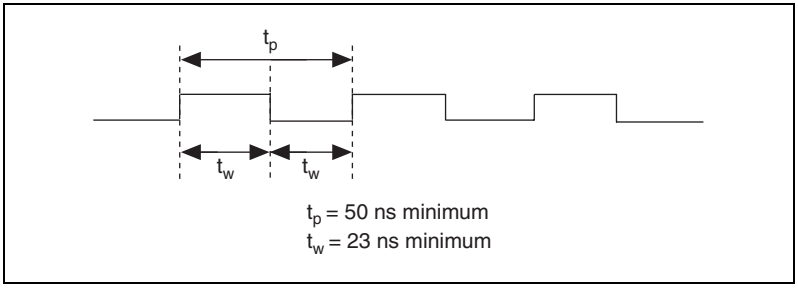


Figure 4-31. GPCTR0_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR0_SOURCE signal unless you select some external source.

GPCTR0_GATE Signal

Any PFI pin can externally input the GPCTR0_GATE signal, which is available as an output on the PFI9/GPCTR0_GATE pin.

As an input, the GPCTR0_GATE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform actions such as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, the GPCTR0_GATE signal reflects the actual gate signal connected to general-purpose counter 0, even if the gate is being externally generated by another PFI. This output is set to high-impedance at startup.

Figure 4-32 shows the timing requirements for the GPCTR0_GATE signal.

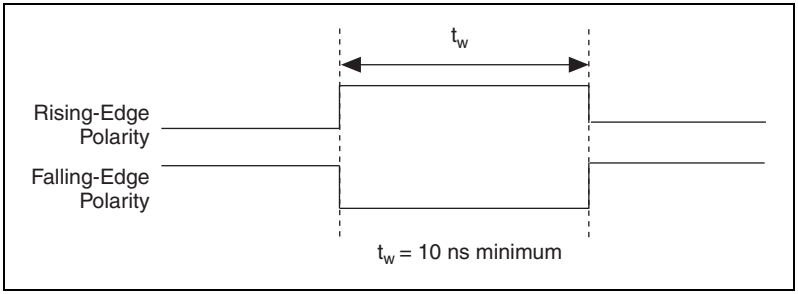


Figure 4-32. GPCTR0_GATE Signal Timing in Edge-Detection Mode

GPCTR0_OUT Signal

This signal is available only as an output on the GPCTR0_OUT pin. The GPCTR0_OUT signal reflects the terminal count (TC) of general-purpose counter 0. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software selectable for both options. This output is set to high-impedance at startup.
Figure 4-33 shows the timing of the GPCTR0_OUT signal.

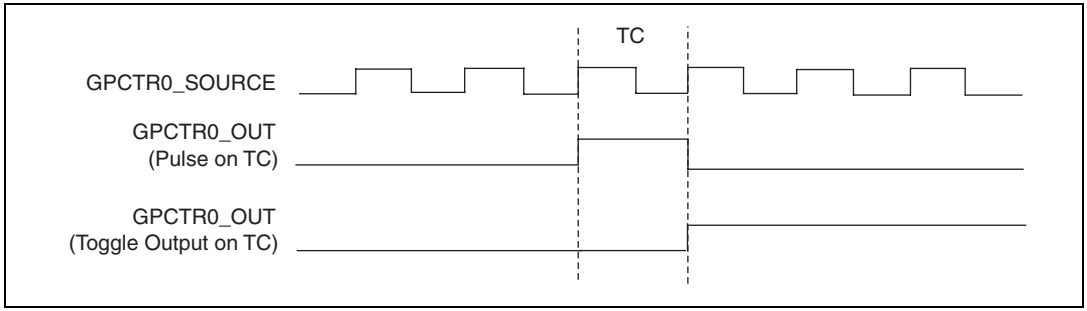


Figure 4-33. GPCTR0_OUT Signal Timing

GPCTR0_UP_DOWN Signal

This signal can be externally input on the DIO6 pin and is not available as an output on the I/O connector. The general-purpose counter 0 counts down when this pin is at a logic low and counts up when it is at a logic high. You can disable this input so that software can control the up-down functionality and leave the DIO6 pin free for general use.

GPCTR1_SOURCE Signal

Any PFI pin can externally input the GPCTR1_SOURCE signal, which is available as an output on the PFI3/GPCTR1_SOURCE pin.

As an input, the GPCTR1_SOURCE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR1_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, the GPCTR1_SOURCE monitors the actual clock connected to general-purpose counter 1, even if the source clock is being externally generated by another PFI. This output is set to high-impedance at startup.

Figure 4-34 shows the timing requirements for the GPCTR1_SOURCE signal.

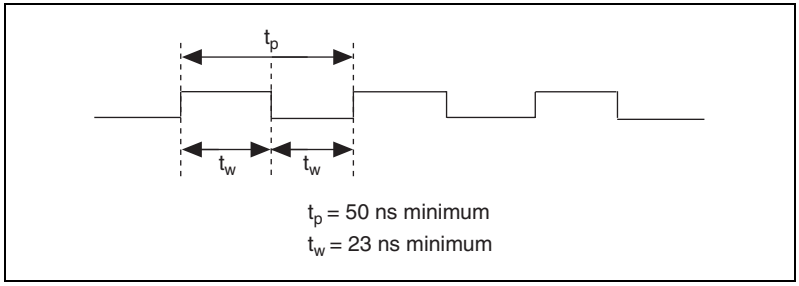


Figure 4-34. GPCTR1_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR1_SOURCE unless you select some external source.

GPCTR1_GATE Signal

Any PFI pin can externally input the GPCTR1_GATE signal, which is available as an output on the PFI4/GPCTR1_GATE pin.

As an input, the GPCTR1_GATE signal is configured in edge-detection mode. You can select any PFI pin as the source for GPCTR1_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform such actions as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, the GPCTR1_GATE signal monitors the actual gate signal connected to general-purpose counter 1, even if the gate is being externally generated by another PFI. This output is set to high-impedance at startup.

Figure 4-35 shows the timing requirements for the GPCTR1_GATE signal.

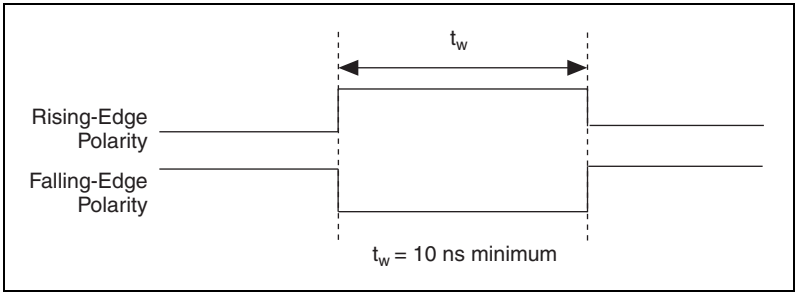


Figure 4-35. GPCTR1_GATE Signal Timing in Edge-Detection Mode

GPCTR1_OUT Signal

This signal is available only as an output on the GPCTR1_OUT pin. The GPCTR1_OUT signal monitors the TC device general-purpose counter 1. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software selectable for both options. This output is set to high-impedance at startup. Figure 4-36 shows the timing requirements for the GPCTR1_OUT signal.

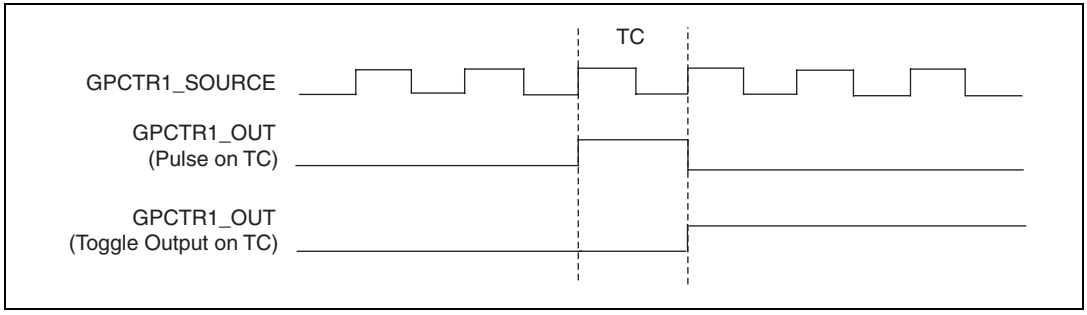


Figure 4-36. GPCTR1_OUT Signal Timing

GPCTR1_UP_DOWN Signal

This signal can be externally input on the DIO7 pin and is not available as an output on the I/O connector. General-purpose counter 1 counts down when this pin is at a logic low and counts up at a logic high. This input can be disabled so that software can control the up-down functionality and

leave the DIO7 pin free for general use. Figure 4-37 shows the timing requirements for the GATE and SOURCE input signals and the timing specifications for the OUT output signals of the AT E Series device.

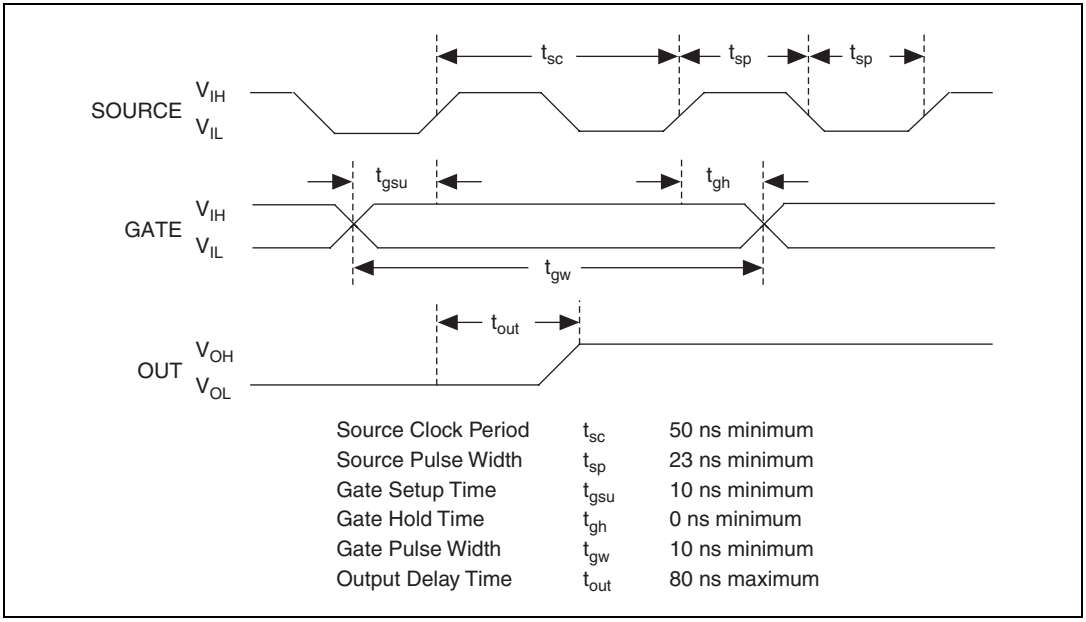


Figure 4-37. GPCTR Timing Summary

The GATE and OUT signal transitions shown in Figure 4-37 are referenced to the rising edge of the SOURCE signal. This timing diagram assumes that the counters are programmed to count rising edges. The same timing diagram, but with the source signal inverted and referenced to the falling edge of the source signal, would apply when the counter is programmed to count falling edges.

The GATE input timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated signals on the AT E Series device. Figure 4-37 shows the GATE signal referenced to the rising edge of a source signal. The gate must be valid (either high or low) for at least 10 ns before the rising or falling edge of a source signal for the gate to take effect at that source edge, as shown by t_{gsu} and t_{gh} in Figure 4-37. The gate signal is not required to be held after the active edge of the source signal.

If an internal timebase clock is used, the gate signal cannot be synchronized with the clock. In this case, gates applied close to a source edge take effect either on that source edge or on the next one. This arrangement results in an uncertainty of one source clock period with respect to unsynchronized gating sources.

The OUT output timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated clock signals on the AT E Series devices. Figure 4-37 shows the OUT signal referenced to the rising edge of a source signal. Any OUT signal state changes occur within 80 ns after the rising or falling edge of the source signal.

FREQ_OUT Signal

This signal is available only as an output on the FREQ_OUT pin. The FREQ_OUT signal is the output of the AT E Series device frequency generator. The frequency generator is a 4-bit counter that can divide its input clock by the numbers 1 through 16. The input clock of the frequency generator is software selectable from the internal 10 MHz and 100 kHz timebases. The output polarity is software selectable. This output is set to high-impedance at startup.

Timing Specifications for Digital I/O Ports A, B, and C

- AT-MIO-16DE-10 only

In addition to its function as a digital I/O port, digital port C, PC<0..7>, can also be used for handshaking when performing data transfers with ports A and B. The signals assigned to port C depend on the mode in which it is programmed. In mode 0, port C is considered two 4-bit I/O ports. In modes 1 and 2, port C is used for status and handshaking signals with two or three additional I/O bits. Table 4-7 summarizes the signal assignments of port C for each programmable mode. Refer to Table 4-7 for descriptions of the signals for port C.

Table 4-7. Port C Signal Assignments

Programming Mode	Group A					Group B		
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Mode 0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
Mode 1 Input	I/O	I/O	IBF_A	STB_A*	$INTR_A$	STB_B*	$IBFB_B$	$INTR_B$
Mode 1 Output	OBF_A*	ACK_A*	I/O	I/O	$INTR_A$	ACK_B*	OBF_B*	$INTR_B$

Table 4-7. Port C Signal Assignments (Continued)

Programming Mode	Group A					Group B		
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Mode 2	OBF_A*	ACK_A*	IBF_A	STB_A*	$INTR_A$	I/O	I/O	I/O
* Indicates that the signal is active low.								

This section lists the timing specifications for handshaking with the AT-MIO-16DE-10 port C circuitry. The handshaking lines STB* and IBF synchronize input transfers. The handshaking lines OBF* and ACK* synchronize output transfers.

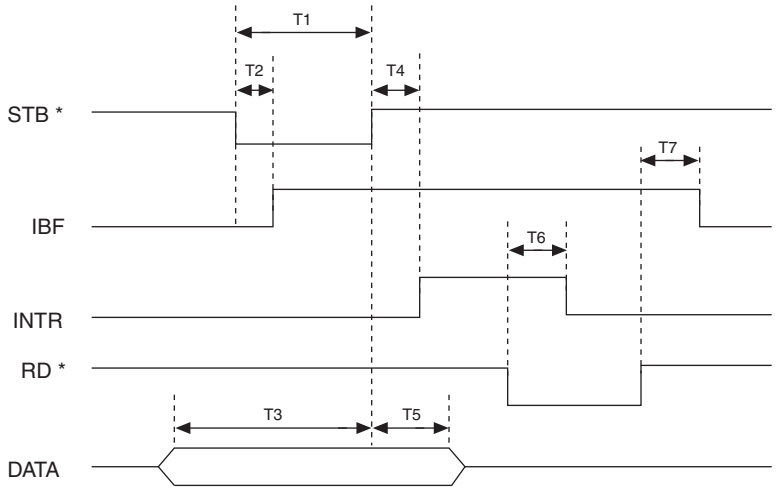
Table 4-8 summarizes the port C signals used in the timing diagrams that follow.

Table 4-8. Port C Signal Descriptions

Name	Type	Description
STB*	Input	Strobe Input—A low signal on this handshaking line loads data into the input latch.
IBF	Output	Input Buffer Full—A high signal on this handshaking line indicates that data has been loaded into the input latch. This is an input acknowledge signal.
ACK*	Input	Acknowledge Input—A low signal on this handshaking line indicates that the data written from the selected port has been accepted. This signal is a response from the external device that it has received the data from the AT-MIO-16DE-10.
OBF*	Output	Output Buffer Full—A low signal on this handshaking line indicates that data has been written from the selected port.
INTR	Output	Interrupt Request—This signal becomes high to request service during a data transfer. The appropriate interrupt enable bits must be set to generate this signal and to allow it to interrupt the computer.
RD*	Internal	Read Signal—This signal is the read signal generated by the host computer.
WR*	Internal	Write Signal—This signal is the write signal generated by the host computer.
DATA	Input or Output	Data Lines at the Selected Port (PA or PB)—This signal indicates when the data on the data lines at a selected port is or should be available.

Mode 1 Input Timing

Figure 4-38 details the timing specifications for an input transfer in Mode 1.



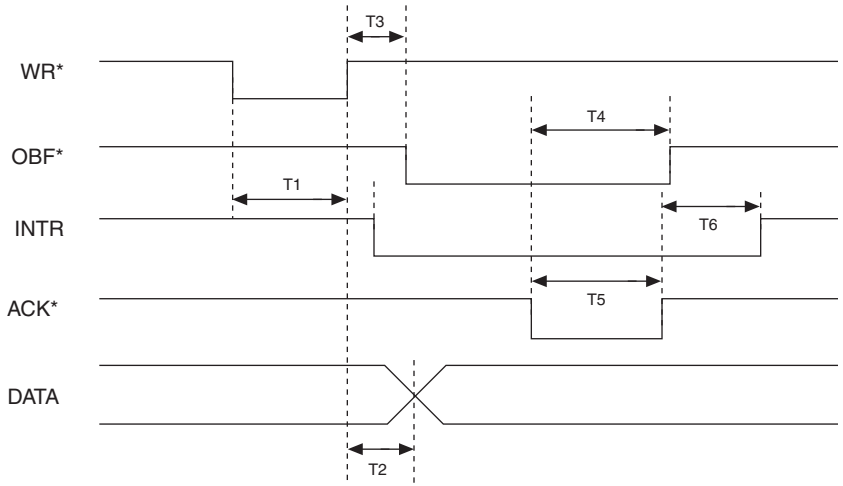
Name	Description	Minimum	Maximum
T1	STB* Pulse Width	100	—
T2	STB* = 0 to IBF = 1	—	150
T3	Data before STB* = 1	20	—
T4	STB* = 1 to INTR = 1	—	150
T5	Data after STB* = 1	50	—
T6	RD* = 0 to INTR = 0	—	200
T7	RD* = 1 to IBF = 0	—	150

All timing values are in nanoseconds.

Figure 4-38. Mode 1 Input Timing

Mode 1 Output Timing

Figure 4-39 details the timing specifications for an output transfer in Mode 1.



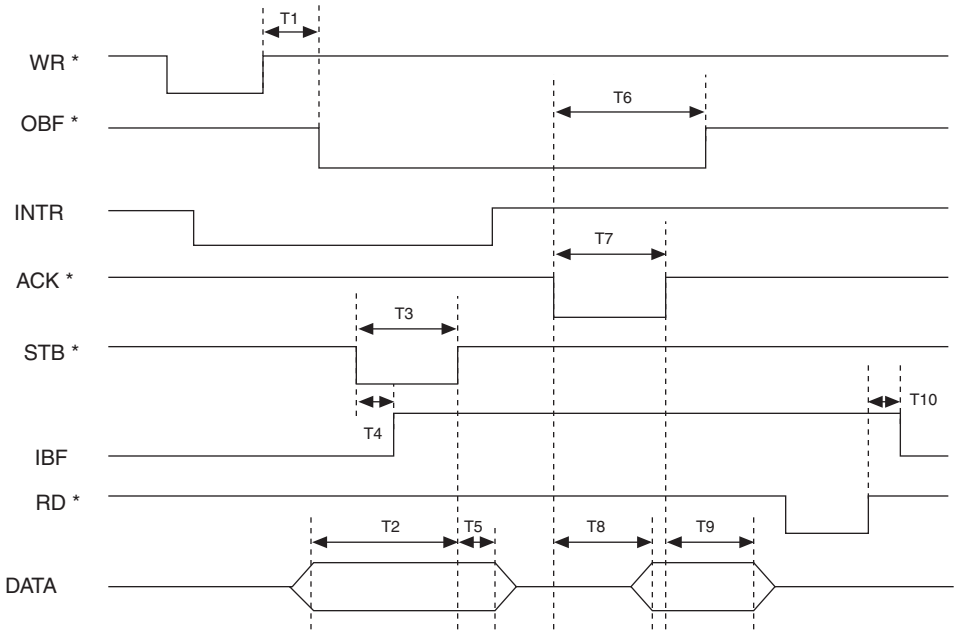
Name	Description	Minimum	Maximum
T1	WR* = 0 to INTR = 0	—	250
T2	WR* = 1 to Output	—	200
T3	WR* = 1 to OBF* = 0	—	150
T4	ACK* = 0 to OBF* = 1	—	150
T5	ACK* Pulse Width	100	—
T6	ACK* = 1 to INTR = 1	—	150

All timing values are in nanoseconds.

Figure 4-39. Mode 1 Output Timing

Mode 2 Bidirectional Timing

Figure 4-40 details the timing specifications for bidirectional transfers in Mode 2.



Name	Description	Minimum	Maximum
T1	WR* = 1 to OBF* = 0	—	150
T2	Data before STB* = 1	20	—
T3	STB* Pulse Width	100	—
T4	STB* = 0 to IBF = 1	—	150
T5	Data after STB* = 1	50	—
T6	ACK* = 0 to OBF = 1	—	150
T7	ACK* Pulse Width	100	—
T8	ACK* = 0 to Output	—	150
T9	ACK* = 1 to Output Float	20	250
T10	RD* = 1 to IBF = 0	—	150

All timing values are in nanoseconds.

Figure 4-40. Mode 2 Bidirectional Timing

Field Wiring Considerations

Environmental noise can seriously affect the accuracy of measurements made with the AT E Series device if you do not take proper care when running signal wires between signal sources and the device. The following recommendations apply mainly to AI signal routing to the device, although they also apply to signal routing in general.

You can minimize noise pickup and maximize measurement accuracy by taking the following precautions:

- Use differential analog input connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect AI signals to the device. With this type of wire, the signals attached to the CH+ and CH– inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.
- Route signals to the device carefully. Keep cabling away from noise sources. The most common noise source in a PC DAQ system is the video monitor. Separate the monitor from the analog signals as much as possible.

The following recommendations apply for all signal connections to the AT E Series device:

- Separate AT E Series device signal lines from high-current or high-voltage lines. These lines are capable of inducing currents in or voltages on the AT E Series device signal lines if they run in parallel paths at a close distance. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel, or run the lines at right angles to each other.
- Do not run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

For more information, refer to the NI Developer Zone tutorial, *Field Wiring and Noise Consideration for Analog Signals*, at `ni.com/zone`.

5

Calibrating the Device

This chapter discusses the calibration procedures for the AT E Series device. NI-DAQ includes calibration functions for performing all of the steps in the calibration process.

Calibration refers to the process of minimizing measurement and output voltage errors by making small circuit adjustments. On the AT E Series devices, these adjustments take the form of writing values to onboard calibration DACs (CalDACs).

Some form of device calibration is required for all but the most forgiving applications. If no device calibration were performed, the signals and measurements could have very large offset, gain, and linearity errors.

Three levels of calibration are available to you, and these are described in this chapter. The first level is the fastest, easiest, and least accurate, whereas the last level is the slowest, most difficult, and most accurate.

Loading Calibration Constants

The AT E Series device is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the values that were written to the CalDACs to achieve calibration in the factory—are stored in the onboard nonvolatile memory (EEPROM). Because the CalDACs have no memory capability, they do not retain calibration information when the device is unpowered. Loading calibration constants refers to the process of loading the CalDACs with the values stored in the EEPROM. NI-DAQ determines when this is necessary and does it automatically. If you are not using NI-DAQ, you must load these values yourself.

In the EEPROM there is a user-modifiable calibration area in addition to the permanent factory calibration area. This means that you can load the CalDACs with values either from the original factory calibration or from a calibration that you performed subsequently.

This method of calibration is not very accurate because it does not take into account the fact that the device measurement and output voltage errors can

vary with time and temperature. It is better to self-calibrate when the device is installed in the environment in which it is used.

Self-Calibration

The AT E Series device can measure and correct for almost all of its calibration-related errors without any external signal connections. The NI software provides a self-calibration method you can use. This self-calibration process, which generally takes less than a minute, is the preferred method of assuring accuracy in your application. You should initiate self-calibration to ensure that the effects of any offset, gain, and linearity drifts, particularly those due to warmup, are minimized.

Immediately after self-calibration, the only significant residual calibration error could be gain error due to time or temperature drift of the onboard voltage reference. This error is addressed by external calibration, which is discussed in the *External Calibration* section. If you are interested primarily in relative measurements, you can ignore a small amount of gain error, and self-calibration should be sufficient.

External Calibration

The AT E Series device has an onboard calibration reference to ensure the accuracy of self-calibration. Its specifications are listed in Appendix A, *Specifications*. The reference voltage is measured at the factory and stored in the EEPROM for subsequent self-calibrations. This voltage is stable enough for most applications, but if you are using the device at an extreme temperature or if the onboard reference has not been measured for a year or more, you may wish to externally calibrate the device.

An external calibration refers to calibrating the device with a known external reference rather than relying on the onboard reference. Redetermining the value of the onboard reference is part of this process and the results can be saved in the EEPROM, so you should not have to perform an external calibration very often. You can externally calibrate the device by calling the NI-DAQ calibration function.

To externally calibrate the device, be sure to use a very accurate external reference. The reference should be several times more accurate than the device itself. For example, to calibrate a 12-bit device, the external reference should be at least ±0.005% (±50 ppm) accurate. To calibrate

a 16-bit device, the external reference should be at least ±0.001% (±10 ppm) accurate.

For a detailed calibration procedure for the AT E Series device, refer to the *E Series Calibration Procedure* by clicking **Manual Calibration Procedures** at `ni.com/calibration`.

Other Considerations

The CalDACs adjust the gain error of each AO channel by adjusting the value of the reference voltage supplied to that channel. This calibration mechanism is designed to work only with the internal 10 V reference. Thus, in general, it is not possible to calibrate the AO gain error when using an external reference. In this case, it is advisable to account for the nominal gain error of the AO channel either in software or with external hardware. Refer to Appendix A, *Specifications*, for AO gain error information.

A

Specifications

This appendix lists the specifications of each device in the AT E Series. These specifications are typical at 25 °C unless otherwise noted.

AT-MIO-16E-1, AT-MIO-16E-2, and AT-MIO-64E-3

Analog Input

Input Characteristics

Number of channels

- AT-MIO-16E-1, AT-MIO-16E-2 ..... 16 single-ended or 8 differential (software selectable)
- AT-MIO-64E-3 ..... 64 single-ended or 32 differential (software selectable)

Type of ADC ..... Successive approximation

Resolution ..... 12 bits, 1 in 4,096

Max sampling rate

- AT-MIO-16E-1 ..... 1.25 MS/s guaranteed
- AT-MIO-16E-2, AT-MIO-64E-3 ..... 500 kS/s guaranteed

Throughput to system memory

- EISA machines ..... 1.0–1.25 MS/s
- ISA machines ..... 600–900 kS/s

Input signal ranges

Range (Software Selectable)	Input Range	
	Bipolar	Unipolar
20 V	±10 V	—
10 V	±5 V	0 to 10 V
5 V	±2.5 V	0 to 5 V
2 V	±1 V	0 to 2 V
1 V	±500 mV	0 to 1 V
500 mV	±250 mV	0 to 500 mV
200 mV	±100 mV	0 to 200 mV
100 mV	±50 mV	0 to 100 mV

Input coupling.....DC

Max working voltage
(signal + common mode).....Each input should remain within ±11 V of ground

Overvoltage protection .....±25 V powered on, ± 15 V powered off

Inputs protected

100-pin devices.....ACH<0..63>, AISENSE, AISENSE2

68-pin devices.....ACH<0..15>, AISENSE

FIFO buffer size

AT-MIO-16E-1.....8,192 samples

AT-MIO-16E-2, AT-MIO-64E-3.....2,048 samples

Data transfers.....DMA, interrupts, programmed I/O

DMA modes .....Single transfer, demand transfer

Configuration memory size .....512 words

Transfer Characteristics

Relative accuracy ..... ±0.5 LSB typ dithered,
±1.5 LSB max undithered

DNL ..... ±0.5 LSB typ, ±1.0 LSB max

No missing codes ..... 12 bits, guaranteed

Offset error

- Pregain error after calibration ..... ±12 µV max
- Pregain error before calibration ..... ±2.5 mV max
- Postgain error after calibration ..... ±0.5 mV max
- Postgain error before calibration..... ±100 mV max

Gain error (relative to calibration reference)

- After calibration (gain = 1) ..... ±0.02% of reading max
- Before calibration ..... ±2.5% of reading max
  - Gain ≠ 1 with gain error adjusted to 0 at gain = 1..... ±0.02% of reading max

Amplifier Characteristics

Input impedance

- Normal powered on ..... 100 GΩ in parallel with 100 pF
- Powered off..... 820 Ω min
- Overload..... 820 Ω min

Input bias current ..... ±200 pA

Input offset current..... ±100 pA

CMRR, DC to 60 Hz

Range	CMRR
20 V	95 dB
10 V	100 dB
100 mV to 5 V	106 dB

Dynamic Characteristics

Bandwidth

	Small Signal (–3dB)	Large Signal (1% THD)
AT-MIO-16E-1	1.6 MHz	1 MHz
AT-MIO-16E-2, AT-MIO-64E-3	1 MHz	300 kHz

Settling time for full-scale step

	Gain	Accuracy*		
		±0.012% (±0.5 LSB)	±0.024% (±1 LSB)	±0.098% (±4 LSB)
AT-MIO-16E-1	0.5	2 µs typ 3 µs max	1.5 µs typ 2 µs max	1.5 µs typ 2 µs max
	1	2 µs typ 3 µs max	1.5 µs typ 2 µs max	1.3 µs typ 1.5 µs max
	2 to 50	2 µs typ 3 µs max	1.5 µs typ 2 µs max	0.9 µs typ 1 µs max
	100	2 µs typ 3 µs max	1.5 µs typ 2 µs max	1 µs typ 1.5 µs max
AT-MIO-16E-2	All	2 µs typ 4 µs max	1.9 µs typ 2 µs max	1.8 µs typ 2 µs max
AT-MIO-64E-3	All	3 µs typ 5 µs max	2 µs typ 3 µs max	1.8 µs typ 2 µs max

* Accuracy values valid for source impedances < 1 kΩ. Refer to the *Multiple-Channel Scanning Considerations* section of Chapter 3, *Hardware Overview*, for more information.

System noise (LSB_{rms} not including quantization)

	Gain	Noise, Dither Off	Noise, Dither On
AT-MIO-16E-1	0.5 to 10	0.25	0.5
	20	0.4	0.6
	50	0.5	0.7
	100	0.8	0.9
AT-MIO-16E-2, AT-MIO-64E-3	0.5 to 20	0.15	0.5
	50	0.3	0.6
	100	0.5	0.7

Crosstalk, DC to 100 kHz

Adjacent channels ..... –75 dB

All other channels ..... –90 dB

Stability

Offset temperature coefficient

Pregain ..... ±5 µV/°C

Postgain..... ±240 µV/°C

Gain temperature coefficient..... ±20 ppm/°C

Analog Output

Output Characteristics

Number of channels ..... 2 voltage

Resolution ..... 12 bits, 1 in 4,096

Max update rate

FIFO mode waveform generation

Internally timed..... 1 MS/s per channel

Externally timed ..... 950 kS/s per channel

Non-FIFO mode waveform generation

1 channel .....800 kS/s (system dependent)

2 channel .....400 kS/s (system dependent)

Type of DAC .....Double buffered, multiplying

FIFO buffer size .....2,048 samples

Data transfers .....DMA, interrupts, programmed I/O

DMA modes .....Single transfer, demand transfer

Transfer Characteristics

Relative accuracy (INL)

After calibration.....±0.3 LSB typ, ±0.5 LSB max

Before calibration .....±4 LSB max

DNL

After calibration.....±0.3 LSB typ, ±1.0 LSB max

Before calibration .....±3 LSB max

Monotonicity .....12 bits, guaranteed after calibration

Offset error

After calibration.....±1.0 mV max

Before calibration .....±200 mV max

Gain error (relative to internal reference)

After calibration.....±0.01% of output max

Before calibration .....±0.5% of output max

Gain error (relative to external reference).....+0% to +0.67% of output max, not adjustable

Voltage Output

Ranges ..... ±10 V, 0 to 10 V, ±EXTREF, 0 to EXTREF (software selectable)

Output coupling ..... DC

Output impedance ..... 0.1 Ω max

Current drive ..... ±5 mA max

Protection ..... Short-circuit to ground

Power-on state ..... 0 V (±200 mV)

External reference input

- Range ..... ±11 V
- Overvoltage protection ..... ±25 V powered on, ±15 V powered off
- Input impedance ..... 10 kΩ
- Bandwidth (–3 dB) ..... 1 MHz

Dynamic Characteristics

Settling time for full-scale step ..... 3 µs to ±0.5 LSB accuracy

Slew rate ..... 20 V/µs

Noise ..... 200 μV_{rms}, DC to 1 MHz

Glitch energy (at midscale transition)

- Magnitude
  - Reglitching disabled ..... ±200 mV
  - Reglitching enabled ..... ±30 mV
- Duration ..... 1.5 µs

Stability

Offset temperature coefficient ..... ±50 µV/°C

Gain temperature coefficient

- Internal reference ..... ±25 ppm/°C
- External reference ..... ±25 ppm/°C

Digital I/O

Number of channels.....8 input/output

Compatibility.....TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V
Input low current (V_{in} = 0 V)	—	–320 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Power-on state.....Input (High-Z)

Data transfers.....Programmed I/O

Max transfer rate (1 word = 8 bits).....50 kwords/s, system dependent

Constant sustainable rate.....1 to 10 kwords/s, typical

Timing I/O

Number of channels.....2 up/down counter/timers,
1 frequency scaler

Resolution

Counter/timers.....24 bits

Frequency scalers.....4 bits

Compatibility.....TTL/CMOS

Base clocks available

Counter/timers.....20 MHz, 100 kHz

Frequency scalers.....10 MHz, 100 kHz

Base clock accuracy.....±0.01%

Max source frequency.....20 MHz

Min source pulse duration..... 10 ns in edge-detect mode

Min gate pulse duration..... 10 ns in edge-detect mode

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes..... Single transfer, demand transfer

Triggers

Analog Trigger

Source..... ACH<0..63>, PFI0/TRIG1

Level..... ± full-scale, internal; ±10 V, external

Slope..... Positive or negative (software selectable)

Resolution ..... 8 bits, 1 in 256

Hysteresis ..... Programmable

Bandwidth (–3 dB)..... 1.5 MHz internal, 7 MHz external

External input (PFI0/TRIG1)

- Impedance ..... 10 kΩ
- Coupling ..... DC
- Protection ..... –0.5 to V_{cc} + 0.5 V when configured as a digital signal

  ±35 V when configured as an analog trigger signal or disabled

  ±35 V powered off

Digital Trigger

Compatibility ..... TTL

Response ..... Rising or falling edge

Pulse width..... 10 ns min

RTSI

Trigger lines.....7

Calibration

Recommended warm-up time.....15 min

Calibration interval.....1 year

External calibration reference.....>6 and <10 V

Onboard calibration reference

Level.....5.000 V (±3.5 mV) (over full operating temperature, actual value stored in EEPROM)

Temperature coefficient.....±5 ppm/°C max

Long-term stability.....±15 ppm/$\sqrt{1{,}000\ \text{h}}$

Bus Interface

Type.....Slave

Power Requirement

+5 VDC (±5%).....1.0 A

Power available at I/O connector.....+4.65 VDC to +5.25 VDC at 1 A

Physical

Dimensions
(not including connectors).....33.8 by 9.9 cm (13.3 by 3.9 in.)

I/O connector

AT-MIO-16E-1,
AT-MIO-16E-2.....68-pin male SCSI-II type

AT-MIO-64E-3.....100-pin female 0.050 D-type

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth..... 42 V, Installation Category II

Channel-to-channel ..... 42 V, Installation Category II

Environmental

Operating temperature..... 0 to 55 °C

Storage temperature ..... –20 to 70 °C

Humidity ..... 10 to 90% RH, noncondensing

Maximum altitude ..... 2,000 meters

Pollution degree (indoor use only)..... 2

Safety

The DAQ device meets the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:

- EN 61010-1:1993/A2:1995, IEC 61010-1:1990/A2:1995
- UL 3101-1:1993, UL 3111-1:1994, UL 3121:1998
- CAN/CSA c22.2 no. 1010.1:1992/A2:1997

Electromagnetic Compatibility

CE, C-Tick, and FCC Part 15 (Class A) Compliant

Electrical emissions..... EN 55011 Class A at 10 m
FCC Part 15A above 1 GHz

Electrical immunity..... Evaluated to EN 61326:1998, Table 1

Note For full EMC compliance, you must operate this device with shielded cabling. In addition, all covers and filler panels must be installed. Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the

appropriate product family, followed by the product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

AT-MIO-16E-10 and AT-MIO-16DE-10

Analog Input

Input Characteristics

Number of channels.....16 single-ended or 8 differential, software selectable

Type of ADC .....Successive approximation

Resolution.....12 bits, 1 in 4,096

Max sampling rate .....100 kS/s guaranteed

Input signal ranges

Range (Software Selectable)	Input Range	
	Bipolar	Unipolar
20 V	±10 V	—
10 V	±5 V	0 to 10 V
5 V	±2.5 V	0 to 5 V
2 V	±1 V	0 to 2 V
1 V	±500 mV	0 to 1 V
500 mV	±250 mV	0 to 500 mV
200 mV	±100 mV	0 to 200 mV
100 mV	±50 mV	0 to 100 mV

Input coupling.....DC

Max working voltage
(signal + common mode).....Each input should remain within ±11 V of ground

Overvoltage protection .....±35 V powered on, ±25 V powered off

Inputs protected ..... ACH<0..15>, AISENSE

FIFO buffer size ..... 512 samples

Data transfers ..... DMA, interrupts, programmed I/O

Transfer rate (1 word = 8 bits) ..... 50 kwords/s

DMA modes ..... Single transfer, demand transfer

Configuration memory size ..... 512 words

Transfer Characteristics

Relative accuracy ..... ±0.2 LSB typ dithered, ±1.5 LSB max undithered

DNL ..... ±0.2 LSB typ, ±1.0 LSB max

No missing codes ..... 12 bits, guaranteed

Offset error

- Pregain error after calibration ..... ±2 µV max
- Pregain error before calibration ..... ±24 mV max
- Postgain error after calibration ..... ±0.5 mV max
- Postgain error before calibration..... ±100 mV max

Gain error (relative to calibration reference)

- After calibration (Gain = 1) ..... ±0.01% of reading max
- Before calibration ..... ±2.0% of reading max
- Gain ≠ 1 with gain error adjusted to 0 at gain = 1 ..... ±0.05% of reading max

Amplifier Characteristics

Input impedance

- Normal powered on ..... 100 GΩ in parallel with 50 pF
- Powered off ..... 3 kΩ min
- Overload ..... 3 kΩ min

Input bias current ..... ±200 pA

Input offset current .....±100 pA

CMRR (all input ranges) .....90 dB, DC to 60 Hz

Dynamic Characteristics

Bandwidth

Small signal (–3 dB).....150 kHz

Large signal (1% THD).....120 kHz

Settling time for full-scale step[1] .....10 µs max to ±0.5 LSB accuracy

System noise (not including quantization)

Gain	Noise, Dither Off	Noise, Dither On
0.5 to 10	0.07 LSB_{rms}	0.5
20	0.12 LSB_{rms}	0.5
50	0.25 LSB_{rms}	0.6
100	0.5 LSB_{rms}	0.7

Crosstalk, DC to 100 kHz

Adjacent channels.....–60 dB

All other channels.....–80 dB

Stability

Offset temperature coefficient

Pregain.....±15 µV/°C

Postgain .....±240 µV/°C

Gain temperature coefficient .....±20 ppm/°C

Analog Output

Output Characteristics

Number of channels.....2 voltage

Resolution.....12 bits, 1 in 4,096

[1] Source impedance < 1 kΩ

Max update rate ..... 100 kS/s, system dependent

Type of DAC ..... Double buffered, multiplying

FIFO buffer size ..... None

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes ..... Single transfer, demand transfer

Transfer Characteristics

Relative accuracy (INL)

- After calibration ..... ±0.3 LSB typ, ±0.5 LSB max
- Before calibration ..... ±4 LSB max

DNL

- After calibration ..... ±0.3 LSB typ, ±1.0 LSB max
- Before calibration ..... ±3 LSB max

Monotonicity ..... 12 bits, guaranteed after calibration

Offset error

- After calibration ..... ±1.0 mV max
- Before calibration ..... ±200 mV max

Gain error (relative to internal reference)

- After calibration ..... ±0.01% of output max
- Before calibration ..... ±0.5% of output max

Gain error (relative to external reference) ..... 0 to +0.67% of output max, not adjustable

Voltage Output

Ranges ..... ±10 V, 0 to 10 V, ±EXTREF, 0 to EXTREF (software selectable)

Output coupling ..... DC

Output impedance.....0.1 Ω max

Current drive.....±5 mA max

Protection.....Short-circuit to ground

Power-on state .....0 V (±200 mV)

External reference input

- Range.....±11 V
- Overvoltage protection .....±35 V powered on, ±25 V powered off
- Input impedance .....10 kΩ
- Bandwidth (–3 dB) .....300 kHz

Dynamic Characteristics

Settling time for full-scale step.....10 µs to ±0.5 LSB accuracy

Slew rate .....10 V/µs

Noise.....200 μV_{rms}, DC to 1 MHz

Glitch energy (at midscale transition)

- Magnitude.....±100 mV
- Duration.....3 µs

Stability

Offset temperature coefficient .....±50 µV/°C

Gain temperature coefficient

- Internal reference.....±25 ppm/°C
- External reference.....±25 ppm/°C

Digital I/O

Number of channels

- AT-MIO-16E-10.....8 input/output
- AT-MIO-16DE-10.....32 input/output

Compatibility .....TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V
Input low current (V_{in} = 0 V)	—	–320 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

PA<0..7>, PB<0..7>, PC<0..7>

- (AT-MIO-16DE-10 only)

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V
Input low current (V_{in} = 0 V)	—	–60 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 2.5 mA)	—	0.4 V
Output high voltage (I_{OH} = 2.5 mA)	3.9 V	—

Handshaking Modes
(AT-MIO-16DE-10 only) 2-wire

Direction..... Input or output

Power-on state..... Input (High-Z)

Data transfers

AT-MIO-16E-10..... Programmed I/O

AT-MIO-16DE-10..... Interrupts, programmed I/O

Max transfer rate (1 word = 8 bits) ..... 50 kwords/s, system dependent

Constant sustainable rate..... 1 to 10 kwords/s, typical

Timing I/O

Number of channels.....2 up/down counter/timers, 1 frequency scaler

Resolution

- Counter/timers.....24 bits
- Frequency scalers.....4 bits

Compatibility.....TTL/CMOS

Base clocks available

- Counter/timers.....20 MHz, 100 kHz
- Frequency scaler.....10 MHz, 100 kHz

Base clock accuracy.....±0.01%

Max source frequency.....20 MHz

Min source pulse duration.....10 ns in edge-detect mode

Min gate pulse duration.....10 ns in edge-detect mode

Data transfers.....DMA, interrupts, programmed I/O

DMA modes.....Single transfer, demand transfer

Triggers

Digital Trigger

Compatibility.....TTL

Response.....Rising or falling edge

Pulse width.....10 ns min

RTSI

Trigger lines.....7

Calibration

Recommended warm-up time ..... 15 min

Calibration interval ..... 1 year

External calibration reference ..... >6 and <10V

Onboard calibration reference

- Level ..... 5.000 V (±3.5 mV) (over full operating temperature, actual value stored in EEPROM)
- Temperature coefficient ..... ±5 ppm/°C max
- Long-term stability ..... ±15 ppm/$\sqrt{1{,}000\ \text{h}}$

Bus Interface

Type ..... Slave

Power Requirement

+5 VDC (±5%)..... 0.7 A

Power available at I/O connector ..... +4.65 VDC to +5.25 VDC at 1 A

Physical

Dimensions
(not including connectors) ..... 17.45 by 10.56 cm (6.87 by 4.16 in.)

I/O connector

- AT-MIO-16E-10 ..... 68-pin male SCSI-II type
- AT-MIO-16DE-10 ..... 100-pin female 0.050 D-type

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth..... 42 V, Installation Category II

Channel-to-channel ..... 42 V, Installation Category II

Environmental

Operating temperature .....0 to 55 °C

Storage temperature .....–20 to 70 °C

Humidity .....10 to 90% RH, noncondensing

Maximum altitude.....2,000 meters

Pollution degree (indoor use only) 2

Safety

The DAQ device meets the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:

- EN 61010-1:1993/A2:1995, IEC 61010-1:1990/A2:1995
- UL 3101-1:1993, UL 3111-1:1994, UL 3121:1998
- CAN/CSA c22.2 no. 1010.1:1992/A2:1997

Electromagnetic Compatibility

CE, C-Tick, and FCC Part 15 (Class A) Compliant

Electrical emissions .....EN 55011 Class A at 10 m
FCC Part 15A above 1 GHz

Electrical immunity .....Evaluated to EN 61326:1998, Table 1

Note For full EMC compliance, you must operate this device with shielded cabling. In addition, all covers and filler panels must be installed. Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by the product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

AT-MIO-16XE-10 and AT-AI-16XE-10

Analog Input

Input Characteristics

Number of channels ..... 16 single-ended or 8 differential (software-selectable)

Type of ADC..... Successive approximation

Resolution ..... 16 bits, 1 in 65,536

Maximum sampling rate ..... 100 kS/s guaranteed

Input signal ranges

Range (Software Selectable)	Input Range	
	Bipolar	Unipolar
20 V	±10 V	—
10 V	±5 V	0 to 10 V
5 V	—	0 to 5 V
4 V	±2 V	—
2 V	±1 V	0 to 2 V
1 V	±500 mV	0 to 1 V
500 mV	—	0 to 500 mV
400 mV	±200 mV	—
200 mV	±100 mV	0 to 200 mV
100 mV	—	0 to 100 mV

Input coupling ..... DC

Maximum working voltage..... Each input should remain within ±11 V of ground

Overvoltage protection..... ±25 V powered on, ±15 V powered off

Inputs protected..... ACH<0..15>, AISENSE

FIFO buffer size.....512 samples

Data transfers.....DMA, interrupts, programmed I/O

DMA modes.....Single transfer, demand transfer

Configuration memory size.....512 words

Transfer Characteristics

Relative accuracy.....±0.75 LSB typ, ±1 LSB max

DNL.....±0.5 LSB typ, ±1 LSB max

No missing codes.....16 bits, guaranteed

Offset error

- Pregain error after calibration.....±3 μV max
- Pregain error before calibration.....±2.2 mV max
- Postgain error after calibration.....±76 μV max
- Postgain error before calibration.....±102 mV max

Gain error (relative to calibration reference)

- After calibration (gain = 1).....±30.5 ppm of reading max
- Before calibration.....±2,150 ppm of reading max

With gain error adjusted to 0 at gain = 1

- Gain ≠ 1.....±200 ppm of reading

Amplifier Characteristics

Input impedance

- Normal, powered on.....100 GΩ in parallel with 100 pF
- Powered off.....820 Ω min
- Overload.....820 Ω min

Input bias current.....±1 nA

Input offset current.....±2 nA

CMRR, DC to 60 Hz

Range	CMRR (Bipolar)	CMRR (Unipolar)
20 V	92 dB	—
10 V	97 dB	92 dB
5 V	—	97 dB
4 V	101 dB	—
2 V	104 dB	101 dB
1 V	105 dB	104 dB
100 mV to 500 mV	105 dB	105 dB

Dynamic Characteristics

Bandwidth

All gains ..... 255 kHz

Settling time for full-scale step

Accuracy*		
±0.00076% (±0.5 LSB)	**±0.0015% (±1 LSB)**	**±0.0016% (±4 LSB)**
40 µs max	20 µs max	10 µs max

* Accuracy values valid for source impedances < 1 kΩ. Refer to the *Multiple-Channel Scanning Considerations* section of Chapter 3, *Hardware Overview*, for more information.

System noise (LSB_{rms} including quantization noise)

Range	Bipolar	Unipolar
2 to 20 V	0.6	0.8
1 V	0.7	0.8
400 to 500 mV	1.1	1.1
200 mV	2.0	2.0
100 mV	—	3.8

Crosstalk, DC to 100 kHz

Adjacent channels.....–75 dB max

All other channels.....–90 dB max

Stability

Offset temperature coefficient

Pregain.....±5 µV/°C

Postgain .....±120 µV/°C

Gain temperature coefficient .....±7 ppm/°C

Analog Output (AT-MIO-16XE-10 only)

Output Characteristics

Number of channels.....2 voltage

Resolution.....16 bits, 1 in 65,536

Max update rate .....100 kS/s

Type of DAC .....Double-buffered

FIFO buffer size.....2,048 samples

Data transfers.....DMA, interrupts, programmed I/O

DMA modes .....Single transfer, demand transfer

Transfer Characteristics

Relative accuracy (INL) .....±0.5 LSB typ, ±1 LSB max

DNL.....±1 LSB max

Monotonicity .....16 bits, guaranteed

Offset error

After calibration.....305 µV max

Before calibration .....20 mV max

Gain error (relative to internal reference)

After calibration ..... ±30.5 ppm max

Before calibration ..... ±2,000 ppm max

Voltage Output

Range ..... ±10 V, 0 to 10 V (software selectable)

Output coupling..... DC

Output impedance ..... 0.1 Ω

Current drive ..... ±5 mA

Protection ..... Short-circuit to ground

Power-on state..... 0 V (±20 mV)

Dynamic Characteristics

Settling time for full-scale step ..... 10 µs to ±1 LSB accuracy

Slew rate..... 5 V/µs

Noise ..... 60 μV_{rms}, DC to 1 MHz

Stability

Offset temperature coefficient ..... ±50 µV/°C

Gain temperature coefficient..... ±7.5 ppm/°C

Digital I/O

Number of channels ..... 8 input/output

Compatibility ..... TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V

Level	Min	Max
Input low current	—	–320 µA
Input high current	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Power-on state .....Input (high-impedance)

Data transfers.....Programmed I/O

Max transfer rate (1 word = 8 bits).....50 kwords/s, system dependent

Constant sustainable rate .....1 to 10 kwords/s, typical

Timing I/O

Number of channels.....2 up/down counter/timers,
1 frequency scaler

Resolution

Counter/timers .....24 bits

Frequency scaler.....4 bits

Compatibility .....TTL/CMOS

Base clocks available

Counter/timers .....20 MHz, 100 kHz

Frequency scaler.....10 MHz, 100 kHz

Base clock accuracy.....±0.01%

Max source frequency.....20 MHz

Min source pulse duration .....10 ns, edge-detect mode

Min gate pulse duration .....10 ns, edge-detect mode

Data transfers.....DMA, interrupts,
programmed I/O

DMA modes .....Single transfer, demand transfer

Triggers

Analog Trigger

Source ..... ACH<0..15>, PFI0/TRIG1

Level ..... ± Full-scale, internal;
±10 V, external

Slope ..... Positive or negative
(software selectable)

Resolution ..... 12 bits, 1 in 4,096

Hysteresis ..... Programmable

Bandwidth (–3 dB) ..... 255 kHz internal,
4 MHz external

External input (PFI0/TRIG1)

- Impedance ..... 10 kΩ
- Coupling ..... DC
- Protection ..... –0.5 to Vcc +0.5 V when configured as a digital signal

  ±35 V when configured as an analog trigger signal or disabled

  ±35 V powered off

Accuracy ..... ±1% of full-scale range

Digital Trigger

Compatibility ..... TTL

Response ..... Rising or falling edge

Pulse width ..... 10 ns min

RTSI

Trigger Lines 7

Calibration

Recommended warm-up time.....15 min

Calibration interval.....1 year

External calibration reference.....>6 and <9.999V

Onboard calibration reference

Level.....5.000 V (±1.0 mV) (over full operating temperature, actual value stored in EEPROM)

Temperature coefficient.....±0.6 ppm/°C max

Long-term stability.....±6 ppm/$\sqrt{1{,}000\ \text{h}}$

Bus Interface

Type.....Slave

Power Requirement

+5 VDC (±5%).....1.2 A

Power available at I/O connector.....+4.65 VDC to +5.25 VDC at 1 A

Physical

Dimensions
(not including connectors).....33.8 by 9.9 cm (13.3 by 3.9 in)

I/O connector.....68-pin male SCSI-II type

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth.....42 V, Installation Category II

Channel-to-channel.....42 V, Installation Category II

Environmental

Operating temperature..... 0 to 55 °C

Storage temperature ..... –20 to 70 °C

Humidity ..... 10 to 90% RH, noncondensing

Maximum altitude ..... 2,000 meters

Pollution degree (indoor use only)..... 2

Safety

The DAQ device meets the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:

- EN 61010-1:1993/A2:1995, IEC 61010-1:1990/A2:1995
- UL 3101-1:1993, UL 3111-1:1994, UL 3121:1998
- CAN/CSA c22.2 no. 1010.1:1992/A2:1997

Electromagnetic Compatibility

CE, C-Tick, and FCC Part 15 (Class A) Compliant

Electrical emissions..... EN 55011 Class A at 10 m
FCC Part 15A above 1 GHz

Electrical immunity..... Evaluated to EN 61326:1998, Table 1

Note For full EMC compliance, you must operate this device with shielded cabling. In addition, all covers and filler panels must be installed. Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by the product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

AT-MIO-16XE-50

Analog Input

Input Characteristics

Number of channels.....16 single-ended or 8 differential (software-selectable)

Type of ADC.....Successive approximation

Resolution.....16 bits, 1 in 65,536

Maximum sampling rate.....20 kS/s guaranteed

Input signal ranges

Range (Software Selectable)	Input Range	
	Bipolar	Unipolar
20 V	±10 V	—
10 V	±5 V	0 to 10 V
5 V	—	0 to 5 V
2 V	±1 V	—
1 V	—	0 to 1 V
200 mV	±100 mV	—
100 mV	—	0 to 100 mV

Input coupling.....DC

Maximum working voltage (signal + common mode).....The average voltage of each differential pair should remain within ±8 V of ground

Overvoltage protection.....±25 V powered on, ±15 V powered off

Inputs protected.....ACH<0..15>, AISENSE

FIFO buffer size.....512 samples

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes ..... Single transfer, demand transfer

Configuration memory size ..... 512 words

Transfer Characteristics

Relative accuracy ..... ±0.5 LSB typ, ±1 LSB max

DNL ..... ±0.5 LSB typ, ±1 LSB max

No missing codes ..... 16 bits, guaranteed

Offset error

- Pregain error after calibration ..... ±3 µV max
- Pregain error before calibration ..... ±1 mV max
- Postgain error after calibration ..... ±76 µV max
- Postgain error before calibration ..... ±4 mV max

Gain error (relative to calibration reference)

- After calibration (gain = 1) ..... ±30.5 ppm of reading max
- Before calibration ..... ±2,250 ppm of reading max

With gain error adjusted to 0 at gain = 1

- Gain = 2, 10 ..... ±100 ppm of reading
- Gain = 100 ..... ±250 ppm of reading

Amplifier Characteristics

Input impedance

- Normal, powered on ..... 7 GΩ in parallel with 100 pF
- Powered off ..... 820 Ω min
- Overload ..... 820 Ω min

Input bias current ..... ±10 nA

Input offset current ..... ±20 nA

CMRR, DC to 60 Hz

Range	CMRR (Bipolar)	CMRR (Unipolar)
20 V	80 dB	—
10 V	86 dB	80 dB
5 V	—	86 dB
2 V	100 dB	—
1 V	—	100 dB
200 mV	120 dB	—
100 mV	—	120 dB

Dynamic Characteristics

Bandwidth

Range	Small Signal (–3dB)
5 to 20 V	63 kHz
1 to 2 V	57 kHz
100 to 200 mV	33 kHz

Settling time for full-scale step

Range	Accuracy*	
	±0.0015% (±1 LSB)	±0.0061% (±4 LSB)
1 to 20 V	50 µs max	50 µs max
200 mV (bipolar)	75 µs max	50 µs max
100 mV (unipolar)	75 µs max	50 µs max

* Accuracy values valid for source impedances < 1 kΩ. Refer to the *Multiple-Channel Scanning Considerations* section of Chapter 3, *Hardware Overview*, for more information.

System noise (LSB_{rms} including quantization noise)

Range	Bipolar	Unipolar
1 to 20 V	1.0	1.0
100 to 200 mV	1.2	1.6

Crosstalk, DC to 20 kHz

Adjacent channels ..... –85 dB max

All other channels ..... –100 dB max

Stability

Offset temperature coefficient

Pregain ..... ±1 µV/°C

Postgain..... ±12 µV/°C

Gain temperature coefficient..... ±5 ppm/°C

Analog Output

Output Characteristics

Number of channels ..... 2 voltage

Resolution ..... 12 bits, 1 in 4,096

Max update rate..... 20 kS/s, system dependent

Type of DAC ..... Double-buffered

FIFO buffer size ..... None

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes..... Single transfer, demand transfer

Transfer Characteristics

Relative accuracy (INL)..... ±0.5 LSB max

DNL ..... ±1 LSB max

Monotonicity..... 12 bits, guaranteed

Offset error

After calibration.....±0.5 mV max

Before calibration .....±85 mV max

Gain error (relative to calibration reference)

After calibration.....±0.01% of output max

Before calibration .....±1% of output max

Voltage Output

Range .....±10 V

Output coupling .....DC

Output impedance.....0.1 Ω max

Current drive.....±5 mA

Protection.....Short-circuit to ground

Power-on state .....0 V (±85 mV)

Dynamic Characteristics

Settling time for full-scale step.....50 µs to ±0.5 LSB accuracy

Slew rate .....2 V/µs

Noise.....40 μV_{rms}, DC to 1 MHz

Glitch energy (at midscale transition)

Magnitude.....±30 mV

Duration.....10 µs

Stability

Offset temperature coefficient .....±25 µV/°C

Gain temperature coefficient .....±15 ppm/°C

Digital I/O

Number of channels.....8 input/output

Compatibility .....TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V
Input low current (V_{in} = 0 V)	—	–320 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Power-on state ..... Input (high-impedance)

Data transfers ..... Programmed I/O

Max transfer rate (1 word = 8 bits) ..... 50 kwords/s, system dependent

Constant sustainable rate ..... 1 to 10 kwords/s, typical

Timing I/O

Number of channels ..... 2 up/down counter/timers,
1 frequency scaler

Resolution

- Counter/timers ..... 24 bits
- Frequency scaler ..... 4 bits

Compatibility ..... TTL/CMOS

Base clocks available

- Counter/timers ..... 20 MHz, 100 kHz
- Frequency scaler ..... 10 MHz, 100 kHz

Base clock accuracy ..... ±0.01%

Max source frequency ..... 20 MHz

Min source pulse duration ..... 10 ns, edge-detect mode

Min gate pulse duration ..... 10 ns, edge-detect mode

Data transfers .....DMA, interrupts, programmed I/O

DMA modes .....Single transfer

Triggers

Digital Trigger

Compatibility .....TTL

Response .....Rising or falling edge

Pulse width .....10 ns min

RTSI

Trigger Lines 7

Calibration

Recommended warm-up time.....15 min

Calibration interval .....1 year

External calibration reference.....>6 and <9.999V

Onboard calibration reference

Level.....5.000 V (±3 mV) (over full operating temperature, actual value stored in EEPROM)

Temperature coefficient.....±2 ppm/°C max

Long-term stability .....±15 ppm/$\sqrt{1{,}000\ \text{h}}$

Bus Interface

Type .....Slave

Power Requirement

+5 VDC (±5%) .....0.75 A

Power available at I/O connector.....+4.65 VDC to +5.25 VDC at 1 A

Physical

Dimensions
(not including connectors) ..... 33.8 by 9.9 cm
(13.3 by 3.9 in)

I/O connector..... 68-pin male SCSI-II type

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth..... 42 V, Installation Category II

Channel-to-channel ..... 42 V, Installation Category II

Environmental

Operating temperature..... 0 to 55 °C

Storage temperature ..... –20 to 70 °C

Humidity ..... 10 to 90% RH, noncondensing

Maximum altitude ..... 2,000 meters

Pollution degree (indoor use only)..... 2

Safety

The DAQ device meets the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:

- EN 61010-1:1993/A2:1995, IEC 61010-1:1990/A2:1995
- UL 3101-1:1993, UL 3111-1:1994, UL 3121:1998
- CAN/CSA c22.2 no. 1010.1:1992/A2:1997

Electromagnetic Compatibility

CE, C-Tick, and FCC Part 15 (Class A) Compliant

Electrical emissions .....EN 55011 Class A at 10 m
FCC Part 15A above 1 GHz

Electrical immunity .....Evaluated to EN 61326:1998, Table 1

Note For full EMC compliance, you must operate this device with shielded cabling. In addition, all covers and filler panels must be installed. Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by the product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

Maximum Signal Ratings for AT Series Devices

Note NI is *not* liable for any damage resulting from signal connections that exceed these ratings. Refer to the warranty for specific information on warranty coverage.

Connections that exceed any of the maximum ratings of input signals on the data acquisition (DAQ) devices listed in the table below can damage the computer and the device.

Note These are the absolute maximum ratings of the input signals, not the working ratings. Refer to the user manual for the recommended operating conditions of the device.

Use the following specifications as definitive values. Signal ratings change depending on whether the DAQ device is powered on or off.

	AT-MIO-16E-1 AT-MIO-16E-2 AT-MIO-64E-3 AT-MIO-16XE-10 AT-AI-16XE-10		**AT-MIO-16E-10 AT-MIO-16DE-10**		**AT-MIO-16XE-50**	
Signal Name	**On**	**Off**	**On**	**Off**	**On**	**Off**
ACH<*x*>	±25 V	±15 V	±35 V	±25 V	±25 V	±15 V
AISENSE	±25 V	±15 V	±35 V	±25 V	±25 V	±15 V

Signal Name	AT-MIO-16E-1 AT-MIO-16E-2 AT-MIO-64E-3 AT-MIO-16XE-10 AT-AI-16XE-10		AT-MIO-16E-10 AT-MIO-16DE-10		AT-MIO-16XE-50	
	On	**Off**	**On**	**Off**	**On**	**Off**
EXTREF	±25 V[1]	±15 V[1]	±35 V	±25 V	±25 V[2]	±15 V[2]
PFI0	5.5 to –0.5 V[3]	±35 V[4]	5.5 to –0.5 V[3]	±0.5 V[5]	5.5 to –0.5 V[3]	±0.5 V[5]
PFI<1..9>	5.5 to –0.5 V[3]	±0.5 V[5]	5.5 to –0.5 V[3]	±0.5 V[5]	5.5 to –0.5 V[3]	±0.5 V[5]
DIO<*x*>	5.5 to –0.5 V[3]	±0.5 V[5]	5.5 to –0.5 V[3]	±0.5 V[5]	5.5 to –0.5 V[3]	±0.5 V[5]
PA, PB, PC<*x*>	N/A	N/A	5.5 to –0.5 V[3, 6]	±0.5 V[5, 6]	N/A	N/A
DAC*x*OUT	Output only					
EXTSTROBE*	Output only					
SCANCLK	Output only					
GPCTR0_OUT	Output only					
FREQ_OUT	Output only					
VCC	Output only					

[1] N/A for AT-MIO-16XE-10 and AT-AI-16XE-10.

[2] N/A for AT-MIO-16XE-50, PCI-MIO-16XE-50, and DAQPad-MIO-16XE-50.

[3] When configured as a digital input.

[4] When PFI0 is configured as an analog trigger or the DAQ device is powered off, the input protection level is ±35 V.

[5] The E Series devices guarantee a powered off input protection level of ±0.5 V. This level can be exceeded if the source of the input signal has a current limited output, such as any member of the LS, HC, or HCT logic families.

[6] N/A for AT-MIO-16E-10.

Test the Connections

The easiest way to check the proper limits of the I/O signals is to measure them with a voltmeter. Be sure to check the signal levels *before* connecting them to the I/O connector of the DAQ device. Connect the negative lead (usually black) of the voltmeter to a ground terminal on the computer chassis. This can be a grounding lug at the back of the computer, or any part of the base metal computer chassis. Then measure each signal input using the voltmeter's positive terminal (usually red). In the case of a differential signal, measure each signal in the differential pair individually. Measure both the DC and AC voltage of each signal.

If any signal should fall outside of the specified limits for *any* of the input signals, do *not* connect it to the DAQ device. Before proceeding, add signal-conditioning circuitry to the signal in question to either attenuate or clip the voltage signal.

If dynamic (for example, AC) signals are connected to the inputs, you must anticipate or calculate the maximum voltage that the signal may attain. Again, if you suspect it will exceed the maximum signal rating allowed for the selected signal, you should add protection or signal-conditioning circuitry to prevent damage to the DAQ device and computer.

B

Optional Cable Connector Descriptions

This appendix describes the connectors on the optional cables for the AT E Series devices.

Figure B-1 shows the pin assignments for the 68-pin MIO connector. This connector is available when you use the SH6868-EP or R6868 cable assemblies with the AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-16E-10, AT-MIO-16XE-10, AT-AI-16XE-10, or AT-MIO-16XE-50. It is also one of the two 68-pin connectors available when you use the SH1006868 cable assembly with the AT-MIO-16DE-10 or AT-MIO-64E-3.

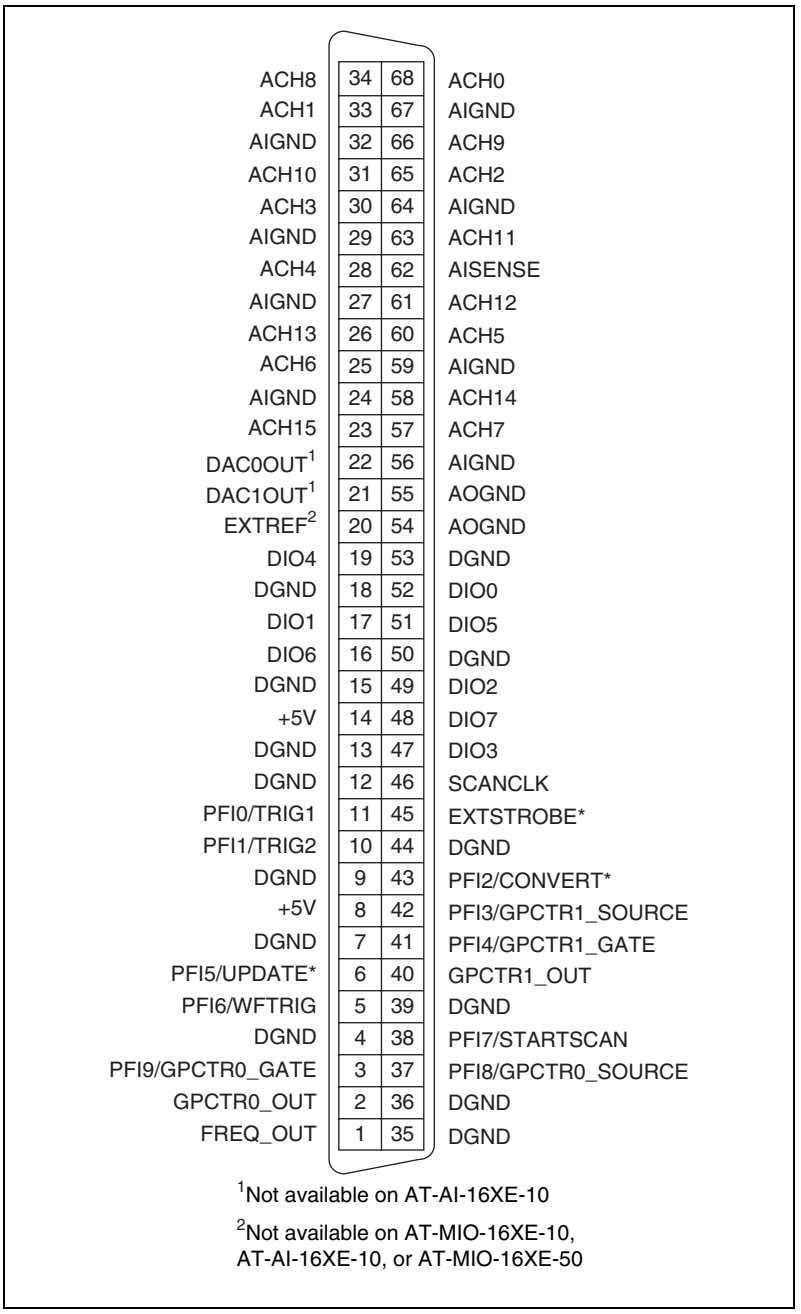


Figure B-1. 68-Pin MIO Connector Pin Assignments

Figure B-2 shows the pin assignments for the 68-pin DIO connector. This is the other 68-pin connector available when you use the SH1006868 cable assembly with the AT-MIO-16DE-10.

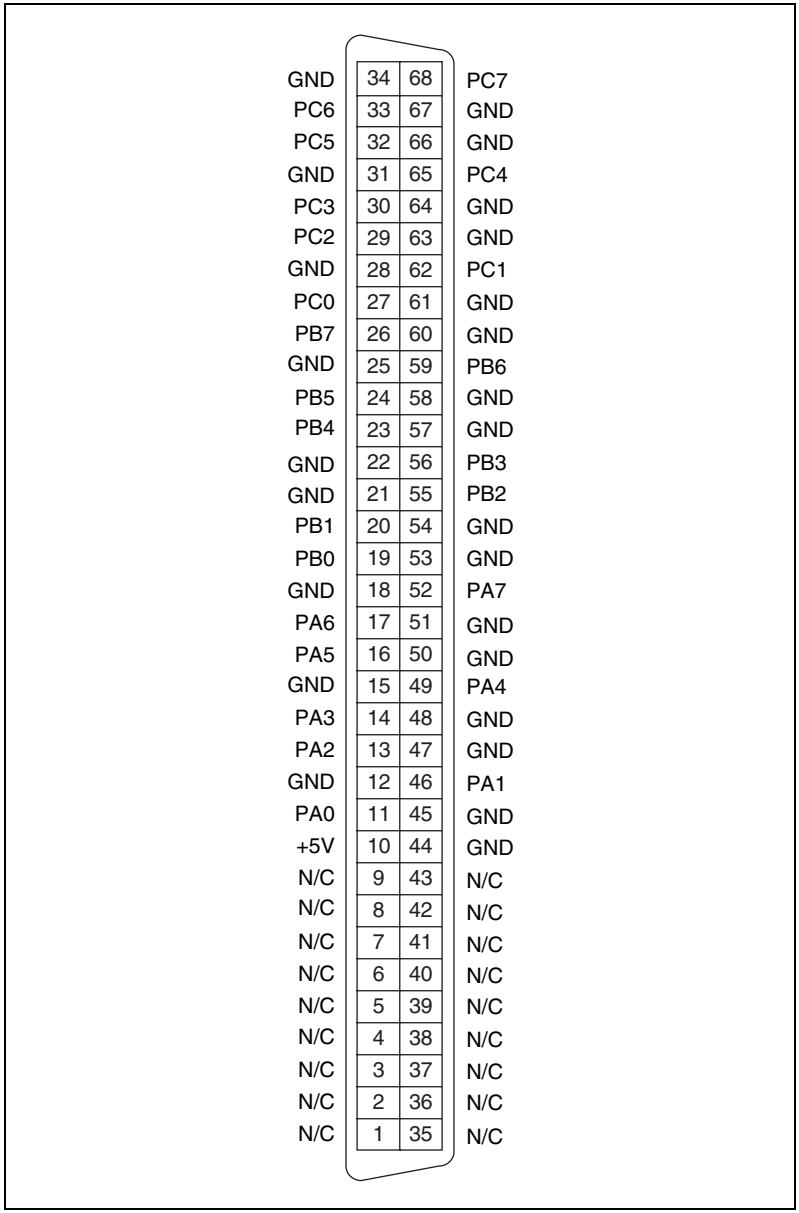


Figure B-2. 68-Pin DIO Connector Pin Assignments

Figure B-3 shows the pin assignments for the 68-pin extended AI connector. This is the other 68-pin connector available when you use the SH1006868 cable assembly with the AT-MIO-64E-3.

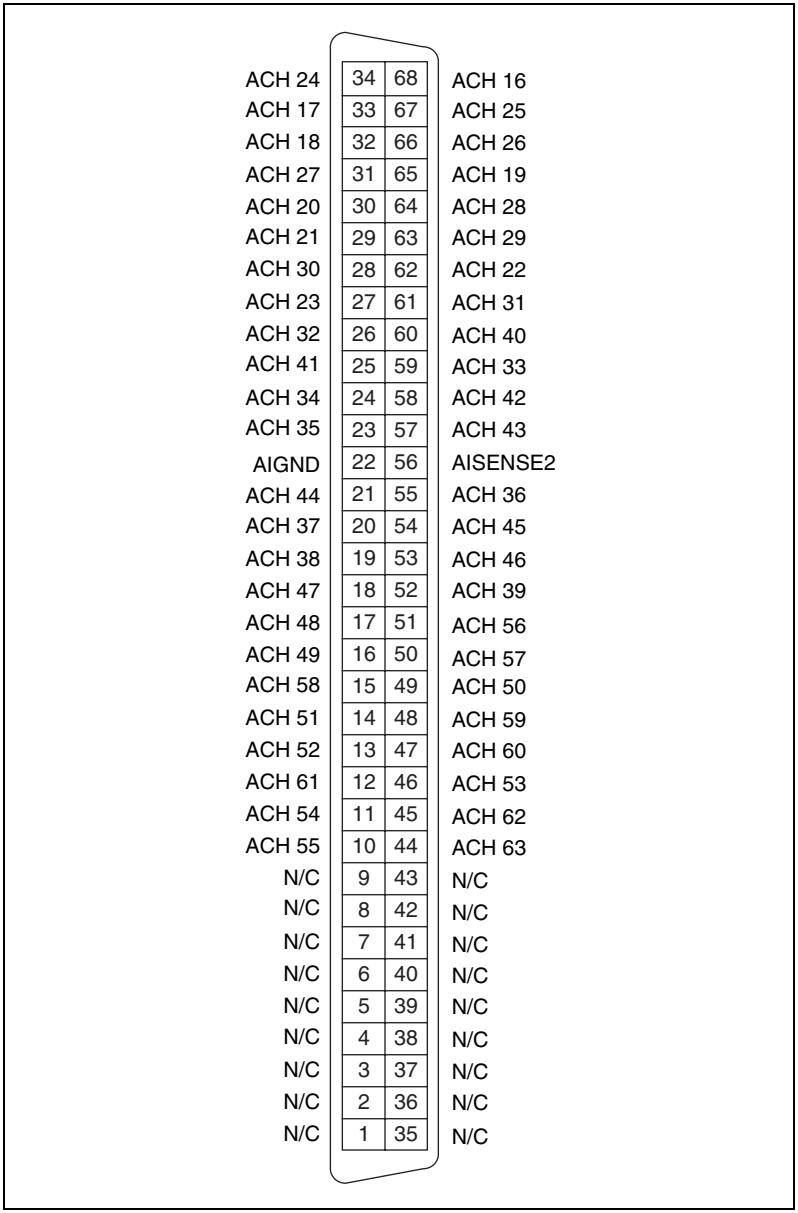


Figure B-3. 68-Pin Extended AI Connector Pin Assignments

Figure B-4 shows the pin assignments for the 50-pin MIO connector. This connector is available when you use the SH6850 or R6850 cable assemblies with the AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-16E-10, AT-MIO-16XE-10, AT-AI-16XE-10, or AT-MIO-16XE-50. It is also one of the two 50-pin connectors available when you use the R1005050 cable assembly with the AT-MIO-16DE-10 or AT-MIO-64E-3.

AIGND	1	2	AIGND
ACH0	3	4	ACH8
ACH1	5	6	ACH9
ACH2	7	8	ACH10
ACH3	9	10	ACH11
ACH4	11	12	ACH12
ACH5	13	14	ACH13
ACH6	15	16	ACH14
ACH7	17	18	ACH15
AISENSE	19	20	DAC0OUT
DAC1OUT	21	22	EXTREF
AOGND	23	24	DGND
DIO0	25	26	DIO4
DIO1	27	28	DIO5
DIO2	29	30	DIO6
DIO3	31	32	DIO7
DGND	33	34	+5V
+5V	35	36	SCANCLK
EXTSTROBE*	37	38	PFI0/TRIG1
PFI1/TRIG2	39	40	PFI2/CONVERT*
PFI3/GPCTR1_SOURCE	41	42	PFI4/GPCTR1_GATE
GPCTR1_OUT	43	44	PFI5/UPDATE*
PFI6/WFTRIG	45	46	PFI7/STARTSCAN
PFI8/GPCTR0_SOURCE	47	48	PFI9/GPCTR0_GATE
GPCTR0_OUT	49	50	FREQ_OUT

Figure B-4. 50-Pin MIO Connector Pin Assignments

Figure B-5 shows the pin assignments for the 50-pin DIO connector. This is the other 50-pin connector available when you use the R1005050 cable assembly with the AT-MIO-16DE-10.

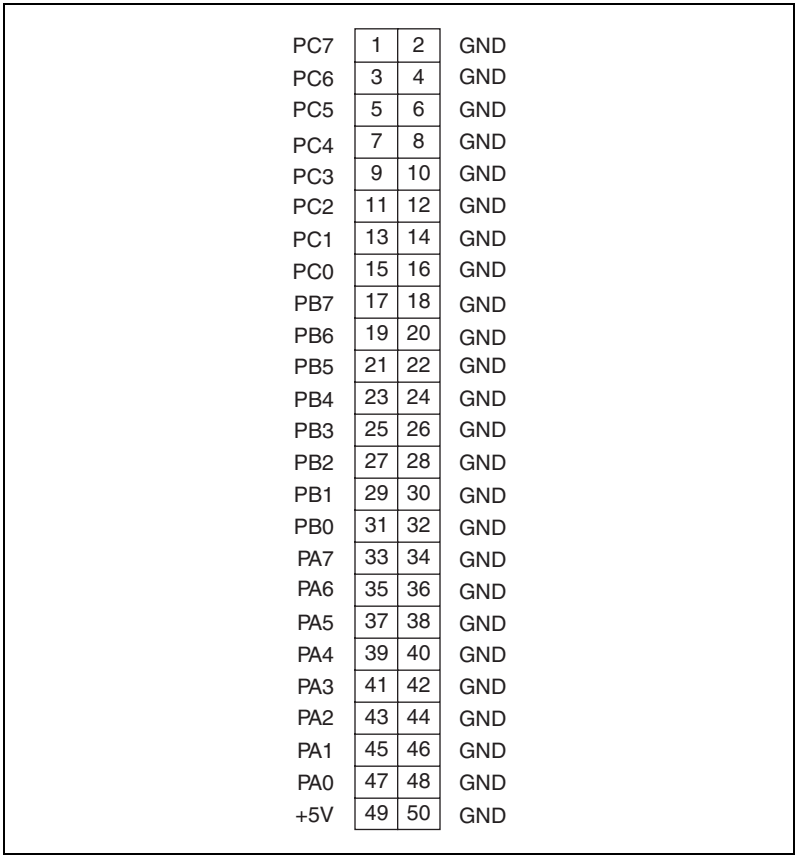
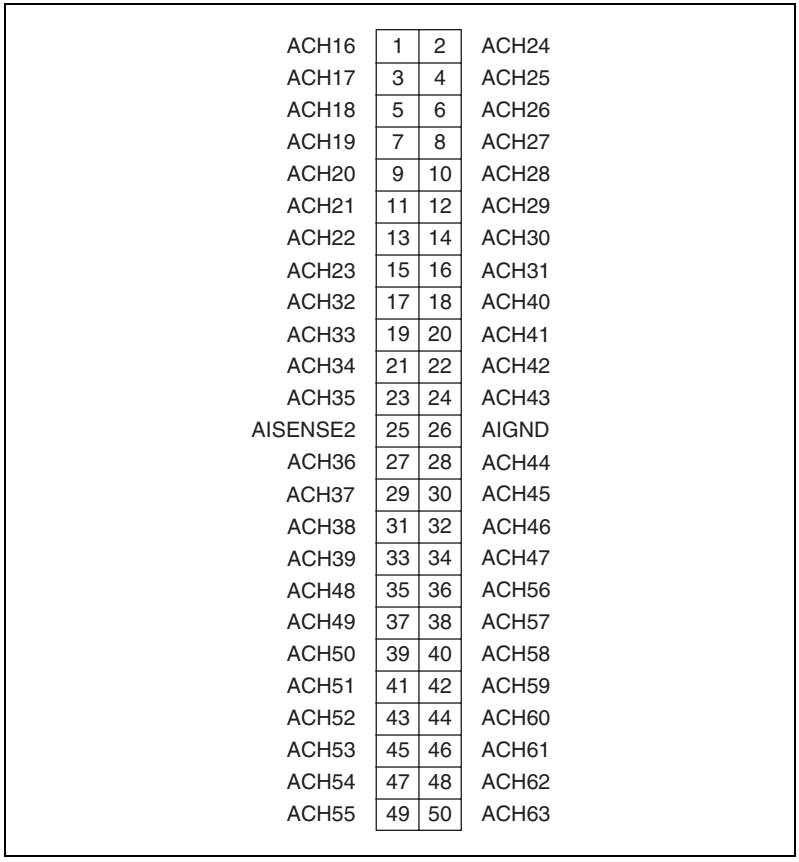


Figure B-5. 50-Pin DIO Connector Pin Assignments

Figure B-6 shows the pin assignments for the 50-pin extended AI connector. This is the other 50-pin connector available when you use the R1005050 cable assembly with the AT-MIO-64E-3.



ACH16	1	2	ACH24
ACH17	3	4	ACH25
ACH18	5	6	ACH26
ACH19	7	8	ACH27
ACH20	9	10	ACH28
ACH21	11	12	ACH29
ACH22	13	14	ACH30
ACH23	15	16	ACH31
ACH32	17	18	ACH40
ACH33	19	20	ACH41
ACH34	21	22	ACH42
ACH35	23	24	ACH43
AISENSE2	25	26	AIGND
ACH36	27	28	ACH44
ACH37	29	30	ACH45
ACH38	31	32	ACH46
ACH39	33	34	ACH47
ACH48	35	36	ACH56
ACH49	37	38	ACH57
ACH50	39	40	ACH58
ACH51	41	42	ACH59
ACH52	43	44	ACH60
ACH53	45	46	ACH61
ACH54	47	48	ACH62
ACH55	49	50	ACH63

Figure B-6. 50-Pin Extended AI Connector Pin Assignments

C

Common Questions

This appendix contains a list of commonly asked questions and their answers relating to usage and special features of the AT E Series device.

General Information

What are the AT E Series devices?

The AT E Series devices are switchless and jumperless, enhanced MIO devices that use the DAQ-STC for timing.

What is the DAQ-STC?

The DAQ-STC is the new system timing control ASIC (application-specific integrated circuit) designed by NI and is the backbone of the AT E Series devices. The DAQ-STC contains seven 24-bit counters and three 16-bit counters. The counters are divided into three groups:

- Analog input—two 24-bit, two 16-bit counters
- Analog output—three 24-bit, one 16-bit counters
- General-purpose counter/timer functions—two 24-bit counters

The groups can be configured independently with timing resolutions of 50 ns or 10 µs. With the DAQ-STC, you can interconnect a wide variety of internal timing signals to other internal blocks. The interconnection scheme is quite flexible and completely software configurable. New capabilities such as buffered pulse generation, equivalent time sampling, and seamlessly changing the sampling rate are possible.

How fast is each AT E Series device?

The last numeral in the name of an AT E Series device specifies the settling time in microseconds for that particular device. For example, the AT-MIO-16E-2 has a 2 µs settling time, which corresponds to a sampling rate of 500 kS/s. These sampling rates are aggregate: one channel at 500 kS/s or two channels at 250 kS/s per channel illustrates the

relationship. Notice, however, that some AT E Series devices have settling times that vary with gain and accuracy. Refer to Appendix A, *Specifications*, for exact specifications

What type of 5 V protection do the AT E Series devices have?

The AT E Series devices have 5 V lines equipped with a self-resetting 1 A fuse.

How do I use the AT E Series device with the NI-DAQ C API?

The *NI-DAQ User Manual for PC Compatibles* describes the general programming flow when using the NI-DAQ C API as well as contains example code. For a list of functions that support the AT E Series device, you can refer to the *NI-DAQ Help* (NI-DAQ version 6.7 or later) or the *NI-DAQ Function Reference Manual* (NI-DAQ version 6.6 or earlier).

Installing and Configuring the Device

How do you set the base address for an AT E Series device?

Windows NT will automatically detect an AT E Series device. However, you must use the Measurement & Automation Explorer (MAX) to assign the base address. For Windows 95, the base address can be changed in the Device Manager. For Windows 2000/XP/Me/9*x*, the operating system detects the device and preassigns a base address. 0x180, 200, 220, 240, 280, and 300 are typical base addresses. For operating system-specific installation and troubleshooting instructions, refer to `ni.com/support/daq`.

What jumpers should I be aware of when configuring my AT E Series device?

The AT E Series devices do not contain any jumpers; they are also switchless.

Which NI document should I read first to get started using DAQ software?

The *DAQ Quick Start Guide* and NI-DAQ or application software release notes documentation are good places to start.

What version of NI-DAQ must I have to program my AT E Series device?

You must have version 4.9.0 or later for the AT-MIO-16XE-10 and AT-AI-16XE-10, version 4.8.0 or later for the AT-MIO-16E-1, and version 4.6.1 or later for all other AT E Series devices.

For AT-MIO-16E-10 and AT-MIO-16DE-10 users, you must have version 5.04 for Windows 3.1*x*, or 5.1 or later for Windows 95 and Windows NT.

What is the best way to test my device without having to program the device?

If you are using Windows, Measurement & Automation Explorer (MAX) has a Test Panel option that is available by selecting **Devices and Interfaces** and then selecting the device. The Test Panels are excellent tools for performing simple functional tests of the device, such as analog input, digital I/O, and counter/timer tests.

I have several DAQ devices that use more total interrupt and DMA channels than I have available in my PC. What should I do?

Visit `ni.com/support/daq` for operating system-specific troubleshooting instructions.

Analog Input and Output

I'm using my device in differential AI mode and I have connected a differential input signal, but my readings are random and drift rapidly. What's wrong?

Check the ground reference connections. The signal may be referenced to a level that is considered *floating* with reference to the device ground reference. Even if you are in differential mode, the signal *must* still be referenced to the same ground level as the device reference. There are various methods of achieving this while maintaining a high common-mode rejection ratio (CMRR). These methods are outlined in Chapter 4, *Signal Connections*.

I'm using the DACs to generate a waveform, but I discovered with a digital oscilloscope that there are glitches on the output signal. Is this normal?

When it switches from one voltage to another, any DAC produces glitches due to released charges. The largest glitches occur when the most significant bit (MSB) of the D/A code switches. You can build a lowpass deglitching filter to remove some of these glitches, depending on the frequency and nature of the output signal. The AT-MIO-16E-1, AT-MIO-16E-2 and the AT-MIO-64E-3 devices have built-in reglitchers, which can be enabled through software, on their AO channels. Refer to the *Analog Output Reglitch Selection* section of Chapter 3, *Hardware Overview*, for more information about reglitching.

Can I synchronize a one-channel AI data acquisition with a one-channel AO waveform generation on my AT E Series device?

Yes. One way to accomplish this synchronization is to use the waveform generation timing pulses to control the AI data acquisition. To do this, follow steps 1 through 4, in addition to the usual steps for data acquisition and waveform generation configuration.

1. Enable the PFI5 line for output, as follows:

   If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_PFI_5, ND_OUT_UPDATE, ND_HIGH_TO_LOW).`

   If you are using LabVIEW, invoke Route Signal VI with signal name set to PFI5 and signal source set to AO Update.

2. Set up DAQ timing so that the timing signal for A/D conversion comes from PFI5, as follows:

   If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_IN_CONVERT, ND_PFI_5, ND_HIGH_TO_LOW).`

   If you are using LabVIEW, invoke AI Clock Config VI with clock source code set to PFI pin, high to low, and clock source string set to 5.

3. Initiate AI data acquisition, which starts only when the AO waveform generation starts.

   For example, if you are using NI-DAQ, you can call `DAQ_Start` with appropriate parameters.

   Similarly, if you are using LabVIEW, you can invoke AI Control VI with control code set to 0 (start).

4. Initiate AO waveform generation.

   If you are using NI-DAQ, call `WFM_Group_Control` with operation set to 1 (start).

   If you are using LabVIEW, you can invoke AO Control VI with control code set to 0 (start).

Can I programmatically enable different channels on an E Series board to acquire in different modes? For example, Channel 0 is differential and Channel 1 is RSE.

Different channels on an E Series device can be enabled to acquire in different modes. However, different pairs of channels are used in different modes. In the example configuration given above, ACH0 and ACH8 would be configured in differential mode and ACH1 and AIGND would be configured in RSE mode. In this configuration, ACH8 could not be used in a single-ended configuration. To enable multi-mode scanning in LabVIEW, you would use the **coupling & input config** cluster input of the AI Config VI. This input has a 1-to-1 correspondence with the channels array input of the AI Config VI. Therefore, you must list all channels either individually or in groups of channels with the same input configuration. For example, if you want Channel 0 to be differential and Channels 1 and 2 to be RSE. Figure C-1 demonstrates how to program this configuration in LabVIEW.

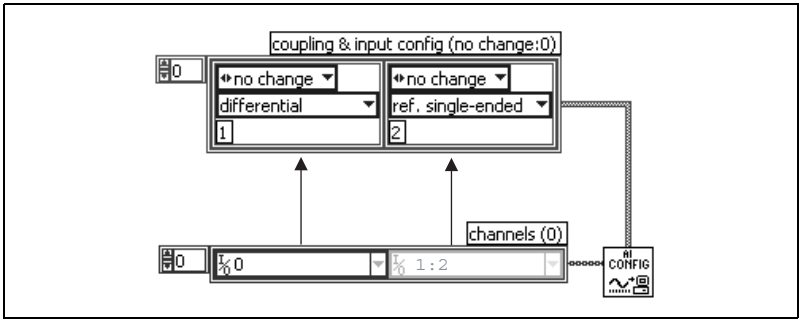


Figure C-1. Configuring Channels for Different Acquisition Modes in LabVIEW

I am seeing crosstalk or ghost voltages when sampling multiple channels. What does this mean?

You maybe experiencing a phenomenon called charge injection, which occurs when you are sampling a series of high output impedance sources with a multiplexer. Multiplexers contain switches, usually made of switched capacitors. When one of the channels, for example channel 0, is selected in a multiplexer, those capacitors accumulate charge. When the

next channel, for example channel 1, is selected, the accumulated charge (current) leaks backward through that channel. If the output impedance of the source connected to channel 1 is high enough, the resulting reading can somewhat reflect the voltage trends in channel 0. To circumvent this problem, you must use a voltage follower (op-amp with unity gain) for each high impedance source before connecting up to the DAQ device or decrease the rate at which each channel is sampled. Another common cause of channel crosstalk is due to sampling among multiple channels at various gains. In this situation, the settling times may increase. For more information on charge injection and sampling channels at different gains, refer to Chapter 3, *Hardware Overview*.

How are the AI channels of the AT-MIO-64E-3 addressed when they are used in differential mode?

The 32 differential channel pairs are addressed as shown in the following table.

Differential Channel Name	I/O Terminals
<0..7>	ACH<0,8...7,15>
<16..23>	ACH<16,24...23,31>
<32..39>	ACH<32,40...39,47>
<44..58>	ACH<48,56...55,63>

How can I use STARTSCAN and CONVERT* on my device to sample my AI channel(s)?

An E series device employs both the STARTSCAN and CONVERT* signals to perform interval sampling. The STARTSCAN signal of the DAQ-STC controls the scan interval (1/scan interval = scan rate) shown in Figure C-2. The CONVERT* signal controls the interchannel delay (1/interchannel delay = sampling rate). This method allows multiple channels to be sampled relatively quickly in relationship to the overall scan rate providing a pseudo simultaneous effect with a fixed delay between channels.

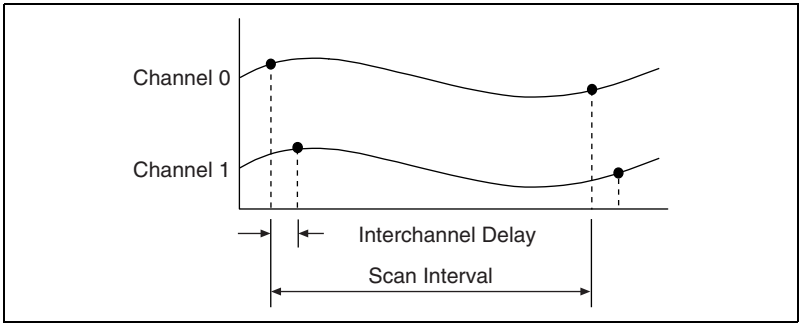


Figure C-2. Comparing Interchannel Delay and Scan Interval

Timing and Digital I/O

What types of triggering can be implemented in hardware on my AT E Series device?

Digital triggering is supported by hardware on every AT E Series MIO device. In addition, the AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3, AT-MIO-16XE-10, and AT-AI-16XE-10 support analog triggering in hardware.

What added functionality does the DAQ-STC make possible in contrast to the Am9513?

The DAQ-STC incorporates much more than just 10 Am9513-style counters within one chip. In fact, the DAQ-STC has the complexity of more than 24 chips. The DAQ-STC makes possible PFI lines, analog triggering, selectable logic level, and frequency shift keying. The DAQ-STC also makes buffered operations possible, such as direct up/down control, single or pulse train generation, equivalent time sampling, buffered period, and buffered semiperiod measurement.

What is the difference in timebases between the Am9513 counter/timer and the DAQ-STC?

The DAQ-STC-based MIO devices have a 20 MHz timebase. The Am9513-based MIO devices have a 1 MHz or 5 MHz timebase.

The counter/timer examples supplied with NI-DAQ are not compatible with an AT E Series device. Where can I find examples to illustrate the use of the DAQ-STC as a general-purpose counter/timer?

If you are using the NI-DAQ language interface and a C compiler under DOS, a new subdirectory called `GPCTR`, which lies beneath the `examples` directory, contains 16 examples of the most common uses of the DAQ-STC.

Do the counter/timer applications that I wrote previously work with the DAQ-STC?

If you are using NI-DAQ with LabVIEW, some of your applications drawn using the CTR VIs do still run. However, there are many differences in the counters between the AT E Series and other devices; the counter numbers are different, timebase selections are different, the DAQ-STC counters are 24-bit counters (unlike the 16-bit counters on devices without the DAQ-STC).

If you are using NI-DAQ or Measurement Studio, the answer is no. The counter/time applications that you wrote previously do not work with the DAQ-STC. You must use the GPCTR functions; ICTR and CTR functions do not work with the DAQ-STC. The GPCTR functions have the same capabilities as the ICTR and CTR functions, plus more, but you must rewrite the application with the GPCTR function calls.

I'm using one of the general-purpose counter/timers on my AT E Series device, but I do not see the counter/timer output on the I/O connector. What am I doing wrong?

If you are using NI-DAQ or Measurement Studio, you must configure the output line to output the signal to the I/O connector. Use the `Select_Signal` call in NI-DAQ to configure the output line. By default, all timing I/O lines except EXTSTROBE* are high-impedance.

How does NI-DAQ treat bogus missed data transfer errors that can arise during DMA-driven GPCTR buffered-input operations?

When doing buffered transfers using GPCTR function calls with DMA, you can call `GPCTR_Watch` to indicate **dataTransfer** errors. NI-DAQ takes a snapshot of transfers and counts how many points have been transferred. If all the points have been transferred and the first instance of this error occurs, NI-DAQ returns a **gpctrDataTransferWarning** indicating that the error could be bogus. If all the points have not been transferred, NI-DAQ returns the genuine error. The error continues to be returned until the

acquisition completes. The above error occurs because NI-DAQ disarms the counter from generating any more requests in the interrupt service routine. Due to interrupt latencies, it is possible that the counter may have generated some spurious requests which the DMA controller may not satisfy because it has already transferred the required number of points.

What are the PFIs and how do I configure these lines?

PFIs are Programmable Function Inputs. These lines serve as connections to virtually all internal timing signals.

If you are using NI-DAQ or LabWindows/CVI, use the `Select_Signal` function to route internal signals to the I/O connector, route external signals to internal timing sources, or tie internal timing signals together.

If you are using NI-DAQ with LabVIEW and you want to connect external signal sources to the PFI lines, you can use AI Clock Config, AI Trigger Config, AO Clock Config, AO Trigger and Gate Config, and Counter Set Attribute advanced-level VIs to indicate which function the connected signal serves. Use the Route Signal VI to enable the PFI lines to output internal signals.

Table C-1. Signal Name Equivalencies

Hardware Signal Name	LabVIEW	Route Signal NI-DAQ Select_Signal
TRIG1	AI Start	Trigger ND_IN_START_TRIGGER
TRIG2	AI Stop	Trigger ND_IN_STOP_TRIGGER
STARTSCAN	AI Scan	Start ND_IN_SCAN_START
SISOURCE	—	ND_IN_SCAN_CLOCK_TIMEBASE
CONVERT*	AI Convert	ND_IN_CONVERT
AIGATE	—	ND_IN_EXTERNAL_GATE
WFTRIG	AO Start Trigger	ND_OUT_START_TRIGGER
UPDATE*	AO Update	ND_OUT_UPDATE
UISOURCE	—	ND_OUT_UPDATE_CLOCK_TIMEBASE
AOGATE	—	ND_OUT_EXTERNAL_GATE

Caution If you enable a PFI line for output, do *not* connect any external signal source to it; if you do, you can damage the device, the computer, and the connected equipment.

What are the power-on states of the PFI and DIO lines on the I/O connector?

At system power-on and reset, both the PFI and DIO lines are set to high impedance by the hardware. This means that the device circuitry is not actively driving the output either high or low. However, these lines may have pull-up or pull-down resistors connected to them as shown in Tables 4-2 to 4-5. These resistors weakly pull the output to either a logic high or logic low state. For example, DIO(0) is in the high impedance state after power on, and Table 4-2, *I/O Signal Summary for the AT E Series*, shows that there is a 50 kΩ pull-up resistor. This pull-up resistor sets the DIO(0) pin to a logic high when the output is in a high-impedance state.

D

Technical Support and Professional Services

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Glossary

Prefix	Meaning	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

Numbers/Symbols

%	percent
±	plus or minus
°	degrees
/	per
+	positive of, or plus
–	negative of, or minus
Ω	ohms
$\sqrt{}$	square root of
+5V	+5 VDC source signal

A

A	amperes
A/D	analog-to-digital

AC	alternating current
ACH	analog input channel signal
ADC	A/D converter
AIGATE	analog input gate signal
AIGND	analog input ground signal
AISENSE	analog input sense signal
AISENSE2	analog input sense 2 signal
ANSI	American National Standards Institute
AOGND	analog output ground signal
ASIC	application-specific integrated circuit

B

BIOS	basic input/output system or built-in operating system

C

C	Celsius
CalDAC	calibration DAC
channel rate	reciprocal of the interchannel delay
CMOS	complementary metal-oxide semiconductor
CMRR	common-mode rejection ratio
CONVERT*	convert signal

D

D/A	digital-to-analog
DAC	D/A converter

DAC0OUT	analog channel 0 output signal
DAC1OUT	analog channel 1 output signal
DAQ	data acquisition
DC	direct current
DGND	digital ground signal
DIFF	differential mode
DIO	digital input/output
DMA	direct memory access
DNL	differential nonlinearity

E

EEPROM	electrically erasable programmable read-only memory
EISA	Extended Industry Standard Architecture
EXTREF	external reference signal
EXTSTROBE	external strobe signal

F

FIFO	first-in-first-out
FREQ_OUT	frequency output signal
ft	feet

G

GPCTR0_GATE	general purpose counter 0 gate signal
GPCTR1_GATE	general purpose counter 1 gate signal
GPCTR0_OUT	general purpose counter 0 output signal

GPCTR1_OUT	general purpose counter 1 output signal
GPCTR0_SOURCE	general purpose counter 0 clock source signal
GPCTR1_SOURCE	general purpose counter 1 clock source signal

H

h	hour
hex	hexadecimal
Hz	hertz

I

interchannel delay	amount of time that passes between sampling consecutive channels. The interchannel delay must be short enough to allow sampling of all the channels in the channel list, within the scan interval. The greater the interchannel delay, the more time the PGIA is allowed to settle before the next channel is sampled. The interchannel delay is regulated by CONVERT*.
I/O	input/output
I_{OH}	current, output high
I_{OL}	current, output low
ISA	Industry Standard Architecture

L

LASTCHAN	last channel (bit)
LSB	least significant bit

M

MB	megabytes of memory
min	minimum
min.	minutes
MIO	multifunction I/O
MSB	most significant bit

N

NRSE	nonreferenced single-ended mode

O

OUT	output

P

PC	personal computer
PFI	Programmable Function Input
PGIA	Programmable Gain Instrumentation Amplifier
ppm	parts per million

R

reglitch	to modify the glitches in a signal in order to make them less disruptive
rms	root mean square
RSE	referenced single-ended mode
RTD	resistive temperature device
RTSI	Real-Time System Integration

S

s	seconds
S	samples
SCANCLK	scan clock signal
scan interval	controls how often a scan is initialized. The scan interval is regulated by STARTSCAN.
scan rate	reciprocal of the scan interval
SCXI	Signal Conditioning eXtensions for Instrumentation
SE	single-ended inputs
SISOURCE	SI counter clock signal
STARTSCAN	start scan signal

T

TC	terminal count
THD	total harmonic distortion
TRIG	trigger signal
TTL	transistor-transistor logic

U

UI	update interval
UISOURCE	update interval counter clock signal
UPDATE	update signal

V

V	volts
VDC	volts direct current
V_{IH}	volts, input high
V_{IL}	volts, input low
V_{in}	volts in
V_{OH}	volts, output high
V_{OL}	volts, output low
V_{ref}	reference voltage

W

WFTRIG	waveform generation trigger signal

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