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# DAQ E Series

## E Series User Manual

February 2007
370503K-01

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## Compliance with FCC/Canada Radio Frequency Interference Regulations

### Determining FCC Class

The Federal Communications Commission (FCC) has rules to protect wireless communications from interference. The FCC places digital electronics into two classes. These classes are known as Class A (for use in industrial commercial locations only) or Class B (for use in residential or commercial locations). All National Instruments (NI) products are FCC Class A products.

Depending on where it is operated, this Class A product could be subject to restrictions in the FCC rules. (In Canada, the Department of Communications (DOC), of Industry Canada, regulates wireless interference in much the same way.) Digital electronics emit weak signals during normal operation that can affect radio, television, or other wireless products.

All Class A products display a simple warning statement of one paragraph in length regarding interference and undesired operation. The FCC rules have restrictions regarding the locations where FCC Class A products can be operated.

Consult the FCC Web site at `www.fcc.gov` for more information.

### FCC/DOC Warnings

This equipment generates and uses radio frequency energy and, if not installed and used in strict accordance with the instructions in this manual and the CE marking Declaration of Conformity*, may cause interference to radio and television reception. Classification requirements are the same for the Federal Communications Commission (FCC) and the Canadian Department of Communications (DOC).

Changes or modifications not expressly approved by NI could void the user's authority to operate the equipment under the FCC Rules.

### Class A

#### Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user is required to correct the interference at their own expense.

#### Canadian Department of Communications

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Cet appareil numérique de la classe A respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

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* The CE marking Declaration of Conformity contains important supplementary information and instructions for the user or installer.

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# About This Manual

The *E Series User Manual* contains information about using the National Instruments E Series and several B Series data acquisition (DAQ) devices with NI-DAQ 8.0 or later. E Series devices feature up to 64 analog input (AI) channels, two counters, eight or 32 lines of digital input/output (DIO), and up to two analog output (AO) channels. The B Series devices discussed in this document are similar to E Series devices, but do not support SCXI, RTSI, or referenced single-ended AI mode.

## Conventions

The following conventions are used in this manual:

<> Angle brackets indicate function keys. Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, P0.<3..0>.

» The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.



This icon denotes a note, which alerts you to important information.



This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on the product, refer to the *Read Me First: Safety and Radio-Frequency Interference* document shipped with the product for precautions to take.

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| | |
|---|---|
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| **Platform** | Text in this font denotes a specific platform and indicates that the text following it applies only to that platform. |

# Related Documentation

Each application software package and driver includes information about writing applications for taking measurements and controlling measurement devices. The following references to documents assume you have NI-DAQ 8.0 or later, and where applicable, version 7.0 or later of the NI application software.

## NI-DAQ for Windows

The *DAQ Getting Started Guide* describes how to install your NI-DAQmx for Windows software, how to install your NI-DAQmx-supported DAQ device, and how to confirm that your device is operating properly. Select **Start»All Programs»National Instruments»NI-DAQ»DAQ Getting Started Guide**.

The *NI-DAQ Readme* lists which devices are supported by this version of NI-DAQ. Select **Start»All Programs»National Instruments»NI-DAQ» NI-DAQ Readme**.

The *NI-DAQmx Help* contains general information about measurement concepts, key NI-DAQmx concepts, and common applications that are applicable to all programming environments. Select **Start»All Programs» National Instruments»NI-DAQ»NI-DAQmx Help**.

The *Traditional NI-DAQ (Legacy) User Manual* contains an API overview and general information about measurement concepts. Select **Start»All Programs»National Instruments»NI-DAQ»Traditional NI-DAQ (Legacy) User Manual.**

## NI-DAQmx for Linux

The *DAQ Getting Started Guide* describes how to install your NI-DAQmx-supported DAQ device and confirm that your device is operating properly.

The *NI-DAQ Readme for Linux* lists supported devices and includes software installation instructions, frequently asked questions, and known issues.

The *C Function Reference Help* describes functions and attributes.

The *NI-DAQmx for Linux Configuration Guide* provides configuration instructions, templates, and instructions for using test panels.

**Note** All NI-DAQmx documentation for Linux is installed at `/usr/local/natinst/NI-DAQmx/docs`.

## NI-DAQmx Base

The *NI-DAQmx Base Getting Started Guide* describes how to install your NI-DAQmx Base software, your NI-DAQmx Base-supported DAQ device, and how to confirm that your device is operating properly. Select **Start»All Programs»National Instruments»NI-DAQmx Base»Documentation» Getting Started Guide**.

The *NI-DAQmx Base Readme* lists which devices are supported by this version of NI-DAQmx Base. Select **Start»All Programs»National Instruments»NI-DAQmx Base»DAQmx Base Readme**.

The *NI-DAQmx Base VI Reference Help* contains VI reference and general information about measurement concepts. In LabVIEW, select **Help» NI-DAQmx Base VI Reference Help**.

The *NI-DAQmx Base C Reference Help* contains C reference and general information about measurement concepts. Select **Start»All Programs» National Instruments»NI-DAQmx Base»Documentation»C Function Reference Help**.

## LabVIEW

If you are a new user, use the *Getting Started with LabVIEW* manual to familiarize yourself with the LabVIEW graphical programming environment and the basic LabVIEW features you use to build data acquisition and instrument control applications. Open the *Getting Started with LabVIEW* manual by selecting **Start»All Programs»National Instruments»LabVIEW»LabVIEW Manuals** or by navigating to the `labview\manuals` directory and opening `LV_Getting_Started.pdf`.

Use the *LabVIEW Help*, available by selecting **Help»Search the LabVIEW Help** in LabVIEW, to access information about LabVIEW

programming concepts, step-by-step instructions for using LabVIEW, and reference information about LabVIEW VIs, functions, palettes, menus, and tools. Refer to the following locations on the **Contents** tab of the *LabVIEW Help* for information about NI-DAQmx:

- **Getting Started»Getting Started with DAQ**—Includes overview information and a tutorial to learn how to take an NI-DAQmx measurement in LabVIEW using the DAQ Assistant.
- **VI and Function Reference»Measurement I/O VIs and Functions**—Describes the LabVIEW NI-DAQmx VIs and properties.
- **Taking Measurements**—Contains the conceptual and how-to information you need to acquire and analyze measurement data in LabVIEW, including common measurements, measurement fundamentals, NI-DAQmx key concepts, and device considerations.

## LabWindows/CVI

The **Data Acquisition** book of the *LabWindows/CVI Help* contains measurement concepts for NI-DAQmx. This book also contains *Taking an NI-DAQmx Measurement in LabWindows/CVI*, which includes step-by-step instructions about creating a measurement task using the DAQ Assistant. In LabWindows™/CVI™, select **Help»Contents**, then select **Using LabWindows/CVI»Data Acquisition**.

The **NI-DAQmx Library** book of the *LabWindows/CVI Help* contains API overviews and function reference for NI-DAQmx. Select **Library Reference»NI-DAQmx Library** in the *LabWindows/CVI Help*.

## Measurement Studio

If you program your NI-DAQmx-supported device in Measurement Studio using Visual C++, Visual C#, or Visual Basic .NET, you can interactively create channels and tasks by launching the DAQ Assistant from MAX or from within Visual Studio .NET. You can generate the configuration code based on your task or channel in Measurement Studio. Refer to the *DAQ Assistant Help* for additional information about generating code. You also can create channels and tasks, and write your own applications in your ADE using the NI-DAQmx API.

For help with NI-DAQmx methods and properties, refer to the NI-DAQmx .NET Class Library or the NI-DAQmx Visual C++ Class Library included in the *NI Measurement Studio Help*. For general help with programming in Measurement Studio, refer to the *NI Measurement Studio Help*, which is fully integrated with the Microsoft Visual Studio .NET help. To view

this help file in Visual Studio. NET, select **Measurement Studio» NI Measurement Studio Help**.

To create an application in Visual C++, Visual C#, or Visual Basic .NET, follow these general steps:

1. In Visual Studio .NET, select **File»New»Project** to launch the New Project dialog box.
2. Find the Measurement Studio folder for the language you want to create a program in.
3. Choose a project type. You add DAQ tasks as a part of this step.

The *Measurement Studio Reference* contains the Traditional NI-DAQ (Legacy) API overview, measurement concepts, and function reference. In Visual Studio .NET, select **Measurement Studio»Measurement Studio Reference**.

## ANSI C without NI Application Software

*The Traditional NI-DAQ (Legacy) User Manual* and the *NI-DAQmx Help* contain API overviews. The NI-DAQmx Help also contains general information about measurement concepts. Traditional NI-DAQ (Legacy) Function Reference Help and NI-DAQmx C Reference Help describe the C functions and attributes. Select **Start»All Programs»National Instruments»NI-DAQ** and the document title for the NI-DAQ API you are using.

## .NET Languages without NI Application Software

With the Microsoft .NET Framework version 1.1 or later, you can use NI-DAQmx to create applications using Visual C# and Visual Basic .NET without Measurement Studio. You need Microsoft Visual Studio .NET 2003 or Microsoft Visual Studio 2005 for the API documentation to be installed.

The installed documentation contains the NI-DAQmx API overview, measurement tasks and concepts, and function reference. This help is fully integrated into the Visual Studio .NET documentation. To view the NI-DAQmx .NET documentation, go to **Start»Programs»National Instruments»NI-DAQ»NI-DAQmx .NET Reference Help**. Expand **NI Measurement Studio Help»NI Measurement Studio .NET Class Library»Reference** to view the function reference. Expand **NI Measurement Studio Help»NI Measurement Studio .NET Class Library»Using the Measurement Studio .NET Class Libraries** to view

conceptual topics for using NI-DAQmx with Visual C# and Visual Basic .NET.

To get to the same help topics from within Visual Studio, go to **Help» Contents**. Select **Measurement Studio** from the **Filtered By** drop-down list and follow the previous instructions.

## Device Documentation and Specifications

NI-DAQmx includes the Device Document Browser, which contains online documentation for supported DAQ and SCXI devices, such as documents describing device pinouts, features, and operation. You can find, view, and/or print the documents for each device using the Device Document Browser at any time by inserting the CD. After installing the Device Document Browser, device documents are accessible from **Start» All Programs»National Instruments»NI-DAQ»Browse Device Documentation**.

## Training Courses

If you need more help getting started developing an application with NI products, NI offers training courses. To enroll in a course or obtain a detailed course outline, refer to `ni.com/training`.

## Technical Support on the Web

For additional support, refer to `ni.com/support` or `zone.ni.com`.

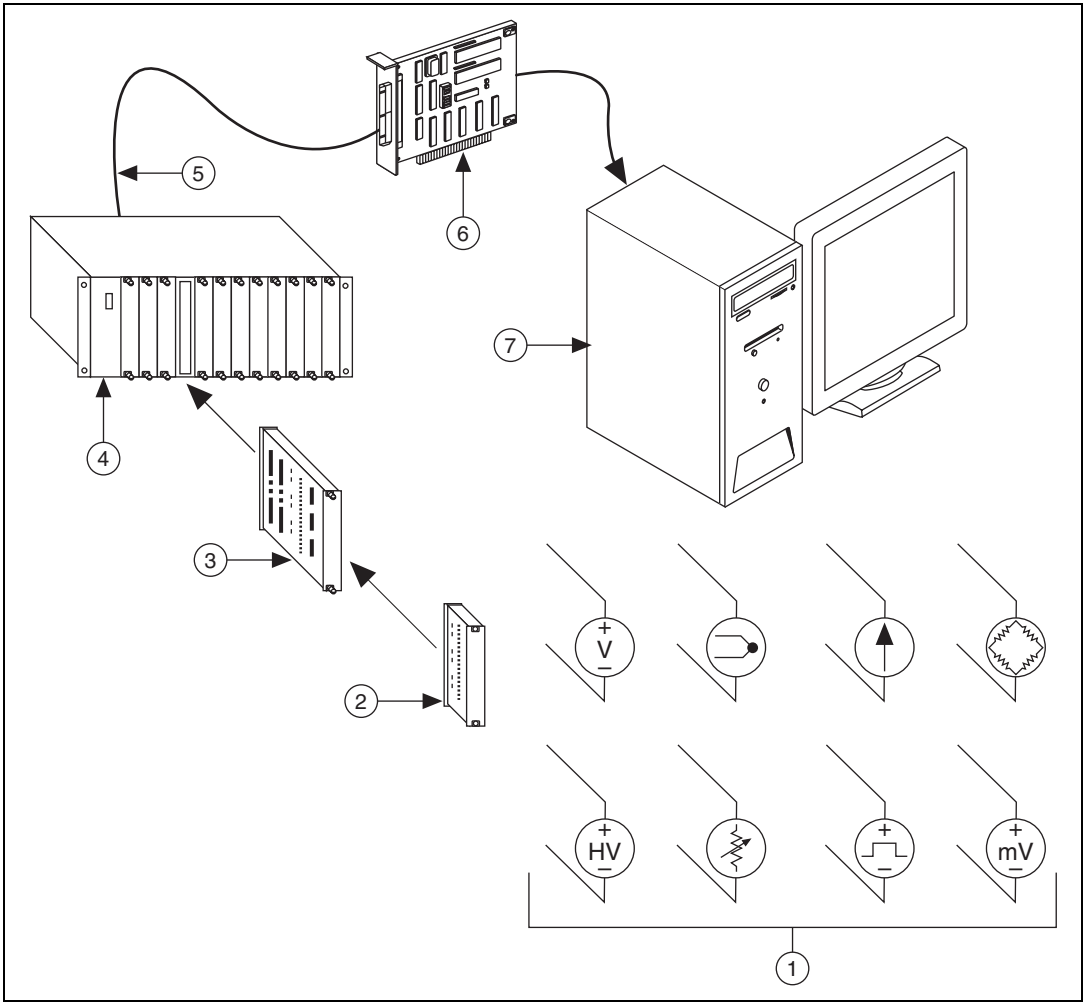
**Note** You can download these documents at `ni.com/manuals`.

DAQ specifications and some DAQ manuals are available as PDFs. You must have Adobe Acrobat Reader with Search and Accessibility 5.0.5 or later installed to view the PDFs. Refer to the Adobe Systems Incorporated Web site at `www.adobe.com` to download Acrobat Reader. Refer to the National Instruments Product Manuals Library at `ni.com/manuals` for updated documentation resources.

# 1

# DAQ System Overview

Figure 1-1 shows a typical DAQ system setup, which includes transducers, signal conditioning, cables that connect the various devices to the accessories, the E Series device, and the programming software. Refer to the *Using Accessories with Devices* section for a list of devices and their compatible accessories.




| | | | |
|---|---|---|---|
| 1 | Sensors and Transducers | 5 | Cable Assembly |
| 2 | Terminal Block Accessory | 6 | DAQ Device |
| 3 | SCXI Module | 7 | Personal Computer |
| 4 | SCXI Chassis | | |

**Figure 1-1.** DAQ System Overview

# DAQ Hardware

DAQ hardware digitizes signals, performs D/A conversions to generate analog output signals, and measures and controls digital I/O signals.

## DAQ-STC

E Series devices use the National Instruments DAQ system timing controller (DAQ-STC) for time-related functions. The DAQ-STC consists of the following timing groups.

- **AI**—Two 24-bit, two 16-bit counters
- **AO**—Three 24-bit, one 16-bit counter
- **General-purpose counter/timer functions**—Two 24-bit counters

You can independently configure the groups for timing resolutions of 50 ns or 10 µs. With the DAQ-STC, you can interconnect a wide variety of internal timing signals to other internal blocks. The interconnection scheme is flexible and completely software-configurable.

The DAQ-STC offers PFI lines to import external timing and trigger signals or to export internally generated clocks and triggers. The DAQ-STC also supports buffered operations, such as buffered waveform acquisition, buffered waveform generation, and buffered period measurement. It also supports numerous non-buffered operations, such as single pulse or pulse train generation, digital input, and digital output.

## Calibration Circuitry

Calibration is the process of making adjustments to a measurement device to reduce errors associated with measurements. Without calibration, the measurement results of your device will drift over time and temperature. Calibration adjusts for these changes to improve measurement accuracy and ensure that your product meets its required specifications.

DAQ devices have high precision analog circuits that must be adjusted to obtain optimum accuracy in your measurements. Calibration determines what adjustments these analog circuits should make to the device measurements. During calibration, the value of a known, high precision measurement source is compared to the value your device acquires or generates. The adjustment values needed to minimize the difference between the known and measured values are stored in the EEPROM of the device as calibration constants. Before performing a measurement, these constants are read out of the EEPROM and are used to adjust the calibration hardware on the device. NI-DAQ determines when this is necessary and does it automatically. If you are not using NI-DAQ, you must load these values yourself.

You can calibrate E Series devices using either internal calibration or external calibration.

### Internal or Self-Calibration

Self-calibration is a process to adjust the device relative to a highly accurate and stable internal reference on the device. Self-calibration is similar to the auto-calibration or auto-zero found on some instruments. You should perform a self-calibration whenever environmental conditions, such as ambient temperature, change significantly. To perform self-calibration, use the self-calibrate function or VI that is included with your driver software. Self-calibration requires no external connections.

### External Calibration

External calibration is a process to adjust the device relative to a traceable, high precision calibration standard. The accuracy specifications of your device change depending on how long it has been since your last external calibration. National Instruments recommends that you calibrate your device at least as often as the intervals listed in the accuracy specifications.

For a detailed calibration procedure for E Series devices (and B Series devices such as the NI 6013, NI 6014, NI 6015, and NI 6016) using NI-DAQmx, refer to the *E/S/M/B Series Calibration Procedure for NI-DAQmx*. For a detailed calibration procedure for B/E Series devices using Traditional NI-DAQ (Legacy), refer to the *E Series Calibration Procedure*. These documents can be found by selecting **Manual Calibration Procedures** at `ni.com/calibration`.

## Signal Conditioning

Many sensors and transducers require signal conditioning before a computer-based measurement system can effectively and accurately acquire the signal. The front-end signal conditioning system can include functions such as signal amplification, attenuation, filtering, electrical isolation, simultaneous sampling, and multiplexing. In addition, many transducers require excitation currents or voltages, bridge completion, linearization, or high amplification for proper and accurate operation. Therefore, most computer-based measurement systems include some form of signal conditioning in addition to plug-in data acquisition DAQ devices.

### Sensors and Transducers

Sensors can generate electrical signals to measure physical phenomena, such as temperature, force, sound, or light. Some commonly used sensors are strain gauges, thermocouples, thermistors, angular encoders, linear encoders, and resistance temperature detectors (RTDs).

To measure signals from these various transducers, you must convert them into a form that a DAQ device can accept. For example, the output voltage of most thermocouples is very small and susceptible to noise. Therefore, you may need to amplify or filter the thermocouple output before digitizing it. The manipulation of signals to prepare them for digitizing is called signal conditioning.

For more information about sensors, refer to the following documents.

- For general information about sensors, visit `ni.com/sensors`.
- If you are using LabVIEW, refer to the *LabVIEW Help* by selecting **Help»Search the LabVIEW Help** in LabVIEW, and then navigate to the **Taking Measurements** book on the **Contents** tab.
- If you are using other application software, refer to **Common Sensors** in the *NI-DAQmx Help*, which you can access from **Start»All Programs»National Instruments»NI-DAQ»NI-DAQmx Help**, or the *LabVIEW 8.x Help*.

## Signal Conditioning Options

### SCXI

SCXI is a front-end signal conditioning and switching system for various measurement devices, including E Series devices. An SCXI system consists of a rugged chassis that houses shielded signal conditioning modules that amplify, filter, isolate, and multiplex analog signals from thermocouples or other transducers. SCXI is designed for large measurement systems or systems requiring high-speed acquisition.

System features include:

- **Modular architecture**—Choose your measurement technology
- **Expandability**—Expand your system to 3,072 channels
- **Integration**—Combine analog input, analog output, digital I/O, and switching into a single, unified platform
- **High bandwidth**—Acquire signals at an aggregate rate of up to 333 kHz
- **Connectivity**—Select from SCXI modules with thermocouple connectors or terminal blocks

### SCC

SCC is a front-end signal conditioning system for E Series plug-in data acquisition devices. A SCC system consists of a shielded carrier that holds up to 20 single or dual-channel SCC modules for conditioning thermocouples and other transducers. SCC is designed for small measurement systems where you need only a few channels of each signal type, or for portable applications. SCC systems also offer the most comprehensive and flexible signal connectivity options.

System features include:

- **Modular architecture**—Select your measurement technology on a per-channel basis
- **Small-channel systems**—Condition up to 16 analog input and eight digital I/O lines
- **Low-profile/portable**—Integrates well with other laptop computer measurement technologies
- **High bandwidth**—Acquire signals at rates up to 1.25 MHz
- **Connectivity**—Incorporates panelette technology to offer custom connectivity to thermocouple, BNC, LEMO™ (B Series), and MIL Spec connectors

### 5B Series

5B is a front-end signal conditioning system for plug-in data acquisition devices. A 5B system consists of eight or 16 single-channel modules that plug into a backplane for conditioning thermocouples and other analog signals. National Instruments offers a complete line of 5B modules, carriers, backplanes, and accessories.

**Note** For more information about SCXI, SCC, and 5B series products, refer to `ni.com/signalconditioning`.

## Cables and Accessories

NI offers a variety of products to use with E Series devices, such as:

- Cables and cable assemblies, shielded and ribbon
- Connector blocks, shielded and unshielded 50- and 68-pin screw terminals
- RTSI bus cables

- SCXI modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output; with SCXI you can condition and acquire up to 3,072 channels
- Low-channel-count signal conditioning modules, devices, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample-and-hold circuitry, and relays

For more specific information about these products, refer to `ni.com`.

## Using Accessories with Devices

Complete the following steps to choose a cable to connect an E Series device and an accessory:

1. Select an E Series device.
2. Using Table 1-1 or Table 1-2 as a guide, determine which accessories are appropriate for that device. Select an accessory. Table 1-3 provides descriptions for E Series device accessories.
3. Using Table 1-1 or Table 1-2 as a guide, determine which cable is required to connect your selected device and accessory.

**Table 1-1.** 68-Pin and DAQCard E Series Accessories and Recommended Cables

| Device | Acessories and Recommended Cables | |
|---|---|---|
| | **TBX-68, CB-68LP, CB-68LPR, DAQ Signal Accessory, CA-1000, BNC-2110, BNC-2111, BNC-2120, BNC-2090, SCB-68** | **TB-2705** |
| 68-pin E Series (except DAQCard) | SH6868EP (shielded) R6868 (unshielded) | Connects directly to the device (PXI only) |
| E Series DAQCards: NI 6024E, NI 6036E, NI 6062E | SHC6868EP/M (shielded) RC6868 (unshielded) | — |

**Table 1-2.** 100-Pin E Series Accessories and Recommended Cables

| Device | Acessories and Recommended Cables | | | |
|---|---|---|---|---|
| | **TBX-68, CB-68LP, CB-68LPR, DAQ Signal Accessory, CA-1000, BNC-2110, BNC-2111, BNC-2120, BNC-2090, SCB-68** | **BNC-2115** | **TBX-68, CB-68LP, CB-68LPR, CA-1000, SCB-68** | **SCB-100** |
| 100-pin E Series with 64 AI channels: NI 6071E, NI 6031E, NI 6033E | SH1006868 (shielded); splits into two 68-pin connectors; these accessories are used with the first 68-pin connector | SH1006868 (shielded); splits into two 68-pin connectors; these accessories are used with the second 68-pin connector | SH1006868 (shielded); splits into two 68-pin connectors; these accessories are used with the second 68-pin connector | SH100100 (shielded) |
| 100-pin E Series with 16 AI channels and 32 DIO lines: NI PCI-6025E | SH1006868 (shielded); splits into two 68-pin connectors; these accessories are used with the first 68-pin connector | SH1006868 (shielded); splits into two 68-pin connectors; these accessories are used with the second 68-pin connector | SH1006868 (shielded); splits into two 68-pin connectors; these accessories are used with the second 68-pin connector | SH100100 (shielded) |

**Table 1-3.** E Series DAQ Accessories Overview

| Accessory | Description |
|---|---|
| SCXI Signal Conditioning | High-channel-count signal conditioning platform |
| SCC Modular Signal Conditioning | Single or dual-channel signal conditioning modules |
| AMUX-64T, 5B, SSR, ER, and SC-204*x* Signal Conditioning | External signal conditioning accessories |
| BNC-2110 | BNC accessory for 68-pin E Series devices |

**Table 1-3.** E Series DAQ Accessories Overview (Continued)

| Accessory | Description |
|---|---|
| BNC-2111 | BNC accessory for 68- or 100-pin E Series devices |
| BNC-2115 | BNC accessory for extended I/O on 100-pin E Series devices |
| BNC-2120 | BNC accessory with function generator (for 68-pin E Series devices) |
| BNC-2090 | Rack-mountable BNC accessory (for 68-pin E Series devices) |
| CA-1000 enclosure | Configurable connectivity enclosure |
| TB-2705 | Latching screw terminal block for PXI E Series modules |
| SCB-100 | 100-pin, shielded screw terminal block with breadboard areas |
| SCB-68 | 68-pin, shielded screw terminal block with breadboard areas |
| TBX-68 | 68-pin, DIN rail-mountable screw terminal block |
| CB-68LP, CB-68LPR | 68-pin, low-cost screw terminal block |
| Signal Source and Demo Accessory | DAQ signal accessory to demo and test analog, digital, and counter/timer functions |

## Custom Cabling

NI offers a variety of cables and accessories to help you prototype your application or to use if you frequently change device interconnections.

However, if you want to develop your own cable, adhere to the following guidelines for best results.

- Use shielded twisted-pair wires for each differential AI pair. Connect the shield for each signal pair to the ground reference at the source.
- Route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

Mating connectors and a back-shell kit for making custom 68-pin cables are available from NI. For more information about the 68- and 100-pin

connectors used for DAQ devices, refer to the KnowledgeBase document, *Specifications and Manufacturers for Board Mating Connectors*.

# Programming Devices in Software

National Instruments measurement devices are packaged with NI-DAQ driver software, an extensive library of functions and VIs you can call from your application software, such as LabVIEW or LabWindows/CVI, to program all the features of your NI measurement devices. Driver software has an application programming interface (API), which is a library of VIs, functions, classes, attributes, and properties for creating applications for your device.

NI-DAQ includes two NI-DAQ drivers, Traditional NI-DAQ (Legacy) and NI-DAQmx. Each driver has its own API, hardware configuration, and software configuration. Refer to the *DAQ Getting Started Guide* for more information about the two drivers.

Traditional NI-DAQ (Legacy) and NI-DAQmx each include a collection of programming examples to help you get started developing an application. You can modify example code and save it in an application. You can use examples to develop a new application or add example code to an existing application.

To locate LabVIEW and LabWindows/CVI examples, open the National Instruments Example Finder:

- In LabVIEW, select **Help»Find Examples**.
- In LabWindows/CVI, select **Help»NI Example Finder**.

Measurement Studio, Visual Basic, and ANSI C examples are in the following directories:

- NI-DAQmx examples for Measurement Studio-supported languages are in the following directories:
  - `MeasurementStudio\VCNET\Examples\NI-DAQ`
  - `MeasurementStudio\DotNET\Examples\NI-DAQ`
- Traditional NI-DAQ (Legacy) examples for Visual Basic are in the following two directories:
  - `NI-DAQ\Examples\Visual Basic with Measurement Studio` directory contains a link to the ActiveX control examples for use with Measurement Studio

  - NI-DAQ\Examples\VBasic directory contains the examples not associated with Measurement Studio
- NI-DAQmx examples for ANSI C are in the NI-DAQ\Examples\DAQmx ANSI C Dev directory
- Traditional NI-DAQ (Legacy) examples for ANSI C are in the NI-DAQ\Examples\VisualC directory

For additional examples, refer to zone.ni.com.

# I/O Connector Signal Descriptions

Table 1-4 describes the signals found on the I/O connectors. For a summary of the I/O signals by device family, refer to the specifications document for your device. Refer to Appendix A, *Device-Specific Information*, for the I/O pinout for your device.

**Table 1-4.** I/O Connector Signal Descriptions

| Signal Name | Reference | Direction | Description |
|---|---|---|---|
| AI GND | — | — | **AI Ground**—These pins are the reference point for single-ended AI measurements in RSE mode and the bias current return point for DIFF measurements. All three ground references—AI GND, AO GND, and D GND—are connected on the device. |
| AI <0..15> | AI GND | Input | **AI Channels 0 through 15**—You can configure each channel pair, AI <*i*, *i*+8> (*i* = 0..7), as either one differential input or two single-ended inputs. |
| AI <16..63> | AI GND | Input | **AI Channels 16 through 63 (NI PCI-6031E/6033E/6071E only)**—Each channel pair, AI <*i*, *i* +8> (*i* = 16..23, 32..39, 48..55), can be configured as either one differential input or two single-ended inputs. |
| AI SENSE | — | Input | **AI Sense**—This pin is the reference node for AI <0..15> in NRSE mode. |
| AI SENSE 2 | — | Input | **AI Sense 2**—This pin is the reference node for AI <16..63> in NRSE mode. |
| AO 0 | AO GND | Output | **Analog Channel 0 Output**—This pin supplies the voltage output of AO channel 0. |
| AO 1 | AO GND | Output | **Analog Channel 1 Output**—This pin supplies the voltage output of AO channel 1. |
| AO GND | — | — | **AO Ground**—The AO voltages are referenced to these pins. All three ground references—AI GND, AO GND, and D GND—are connected on the device. |

**Table 1-4.** I/O Connector Signal Descriptions (Continued)

| Signal Name | Reference | Direction | Description |
|---|---|---|---|
| D GND | — | — | **Digital Ground**—These pins supply the reference for the digital signals at the I/O connector as well as the +5 VDC supply. All three ground references—AI GND, AO GND, and D GND—are connected on the device. |
| P0.<0..7> | D GND | Input or Output | **Digital I/O Signals**—You can individually configure each signal as an input or output. P0.6 and P0.7 can also control the up/down signal of Counters 0 and 1, respectively. |
| AO EXT REF | AO GND | Input | **External Reference**—This is the external reference input for the AO circuitry. |
| P1.<0..7> | D GND | Input or Output | **NI 6025E only**—Port 1 bidirectional digital data lines for the 82C55A programmable peripheral interface. P1.7 is the most significant bit (MSB). P1.0 is the least significant bit (LSB). |
| P2.<0..7> | D GND | Input or Output | **NI 6025E only**—Port 2 bidirectional digital data lines for the 82C55A programmable peripheral interface. P2.7 is the MSB. P2.0 is the LSB. |
| P3.<0..7> | D GND | Input or Output | **NI 6025E only**—Port 3 bidirectional digital data lines for the 82C55A programmable peripheral interface. P3.7 is the MSB. P3.0 is the LSB. |
| +5 V | D GND | Output | **+5 V Power Source**—These pins provide +5 V power. |
| AI HOLD COMP | D GND | Output | **AI Hold Complete Event Signal**—When enabled, this signal pulses once for each A/D conversion in sampling mode. The low-to-high edge indicates when the input signal can be removed from the input or switched to another signal. |
| EXT STROBE | D GND | Output | **External Strobe Signal**—You can toggle this output with software controls to latch signals or trigger events on external devices. This functionality is not available in LabVIEW or NI-DAQ. EXT STROBE is used for controlling SCXI chassis, and it is not a general-purpose signal. If you want to use or control this signal, you must perform register-level programming. |
| PFI 0/AI START TRIG | D GND | Input | **PFI 0**—As an input, this pin is a programmable function interface (PFI). |
| | | Output | **AI Start Trigger Signal**—As an output, this pin is the ai/StartTrigger signal. In post-trigger DAQ sequences, a low-to-high transition indicates the initiation of the acquisition sequence. In applications with pre-trigger samples, a low-to-high transition indicates the initiation of the pre-trigger samples. |

**Table 1-4.** I/O Connector Signal Descriptions (Continued)

| Signal Name | Reference | Direction | Description |
|---|---|---|---|
| PFI 1/AI REF TRIG, PFI 1 | D GND | Input | **PFI 1**—As an input, this pin is a PFI. |
| | | Output | **AI Reference Trigger Signal**—As an output, this pin is the ai/ReferenceTrigger signal. In applications with pre-trigger samples, a low-to-high transition indicates the initiation of the post-trigger samples. AI Reference Trigger is not used in applications with post-trigger samples. |
| PFI 2/AI CONV CLK | D GND | Input | **PFI 2**—As an input, this pin is a PFI. |
| | | Output | **AI Convert Clock Signal**—As an output, this pin is the ai/ConvertClock signal. A high-to-low edge on AI CONV indicates that an A/D conversion is occurring. |
| PFI 3/CTR 1 SRC | D GND | Input | **PFI 3**—As an input, this pin is a PFI. |
| | | Output | **Counter 1 Source Signal**—As an output, this pin is the Ctr1Source signal. This signal reflects the actual source connected to the general-purpose Counter 1. |
| PFI 4/CTR 1 GATE | D GND | Input | **PFI 4**—As an input, this pin is a PFI. |
| | | Output | **Counter 1 Gate Signal**—As an output, this pin is the Ctr1Gate signal. This signal reflects the actual gate signal connected to the general-purpose Counter 1. |
| CTR 1 OUT | D GND | Input | **CTR 1 OUT**—As an input, this pin can be used to route signals directly to the RTSI bus. |
| | | Output | **Counter 1 Output Signal**—As an output, this pin emits the Ctr1InternalOutput signal. |
| PFI 5/AO SAMP CLK | D GND | Input | **PFI 5**—As an input, this pin is a PFI. |
| | | Output | **AO Sample Clock Signal**—As an output, this pin is the ao/SampleClock signal. A high-to-low edge on AO SAMP indicates that the AO primary group is being updated. |
| PFI 6/AO START TRIG | D GND | Input | **PFI 6**—As an input, this pin is a PFI. |
| | | Output | **AO Start Trigger Signal**—As an output, this pin is the ao/StartTrigger signal. In timed AO sequences, a low-to-high transition indicates the initiation of the waveform generation. |
| PFI 7/AI SAMP CLK | D GND | Input | **PFI 7**—As an input, this pin is a PFI. |
| | | Output | **AI Sample Clock Signal**—As an output, this pin is the ai/SampleClock signal. This pin pulses once at the start of each AI sample in the interval sample. A low-to-high transition indicates the start of the sample. |

**Table 1-4.** I/O Connector Signal Descriptions (Continued)

| Signal Name | Reference | Direction | Description |
|---|---|---|---|
| PFI 8/CTR 0 SRC | D GND | Input | **PFI 8**—As an input, this pin is a PFI. |
| | | Output | **Counter 0 Source Signal**—As an output, this pin is the Ctr0Source signal. This signal reflects the actual source connected to the general-purpose Counter 0. |
| PFI 9/CTR 0 GATE | D GND | Input | **PFI 9**—As an input, this pin is a PFI. |
| | | Output | **Counter 0 Gate Signal**—As an output, this pin is the Ctr0Gate signal. This signal reflects the actual gate signal connected to the general-purpose Counter 0. |
| CTR 1 OUT | D GND | Input | **Counter 1 Output Signal**—As an input, this pin can be used to route signals directly to the RTSI bus. |
| | | Output | As an output, this pin emits the Ctr0InternalOutput signal. |
| FREQ OUT/USER <1..2> | D GND | Output | **Frequency Output Signal**—This output is from the frequency generator. |
| | | I/O | **User <1..2>**—On BNC devices, these signals connect directly from a screw terminal to a BNC. For example, if you connect CTR 0 OUT to the USER 1 screw terminal with a wire, the Ctr0Out signal also is driven to the User 1 BNC. |

# Terminal Name Equivalents

With NI-DAQmx, National Instruments has revised its terminal names so they are easier to understand and more consistent among National Instruments hardware and software products. The revised terminal names used in this document are usually similar to the names they replace. Refer to Table 1-5 for a list of Traditional NI-DAQ (Legacy) terminal names and their NI-DAQmx equivalents.

**Table 1-5.** Terminal Name Equivalents

| Traditional NI-DAQ (Legacy) | NI-DAQmx |
|---|---|
| ACH# | AI # |
| ACH# + | AI # + |
| ACH# – | AI # – |
| ACHGND | AI GND |
| ACK# | PFI # |

**Table 1-5.** Terminal Name Equivalents (Continued)

| Traditional NI-DAQ (Legacy) | NI-DAQmx |
|---|---|
| AIGND | AI GND |
| AISENSE | AI SENSE |
| AISENSE2 | AI SENSE 2 |
| AOGND | AO GND |
| CONVERT* | AI CONV CLK or AI CONV |
| DAC0OUT | AO 0 |
| DAC1OUT | AO 1 |
| DGND | D GND |
| DIO_# | P0.# |
| DIO# | P0.# |
| DIOA#, DIOB#, DIOC#... | P0.#, P1.#, P2.#... |
| EXTREF | AO EXT REF or EXT REF |
| EXT_STROBE | EXT STROBE |
| EXT_TRIG | EXT TRIG |
| EXT_CONV | EXT CONV |
| FREQ_OUT | FREQ OUT or F OUT |
| GPCTR0_GATE | CTR 0 GATE |
| GPCTR0_OUT | CTR 0 OUT |
| GPCTR0_SOURCE | CTR 0 SOURCE or CTR 0 SRC |
| GPCTR1_GATE | CTR 1 GATE |
| GPCTR1_OUT | CTR 1 OUT |
| GPCTR1_SOURCE | CTR 1 SOURCE or CTR 1 SRC |
| PA#, PB#, PC#... | P0.#, P1.#, P2.#... |
| PFI# | PFI # |
| PFI_# | PFI # |
| PCLK# | PFI # |

**Table 1-5.** Terminal Name Equivalents (Continued)

| Traditional NI-DAQ (Legacy) | NI-DAQmx |
|---|---|
| REQ# | PFI # |
| SCANCLK | AI HOLD COMP or AI HOLD |
| SISOURCE | AI Sample Clock Timebase |
| STARTSCAN | AI SAMP CLK or AI SAMP |
| STOPTRIG# | PFI # |
| TRIG1 | AI START TRIG or AI START |
| TRIG2 | AI REF TRIG or REF TRIG |
| UISOURCE | AO Sample Clock Timebase |
| UPDATE | AO SAMP CLK or AO SAMP |
| WFTRIG | AO START TRIG or AO START |

# +5 V Power Source

The +5 V pins on the I/O connector supply +5 V power on the plug-in cards or from an internal step-down voltage regulator on DAQPads. You can use these pins, referenced to D GND, to power external circuitry. A self-resetting fuse protects the supply from overcurrent conditions. The fuse resets automatically within a few seconds after the overcurrent condition is removed.

Power rating (most devices): +4.65 to +5.25 VDC at 1 A.

To find your device power rating, refer to the specifications document for your device.



**Caution** Never connect these +5 V power pins to analog or digital ground or to any other voltage source on the E Series device or any other device. Doing so can damage the device and the computer. NI is not liable for damage resulting from such a connection.

# 2

# Analog Input

Figure 2-1 shows the analog input circuitry of E Series devices.

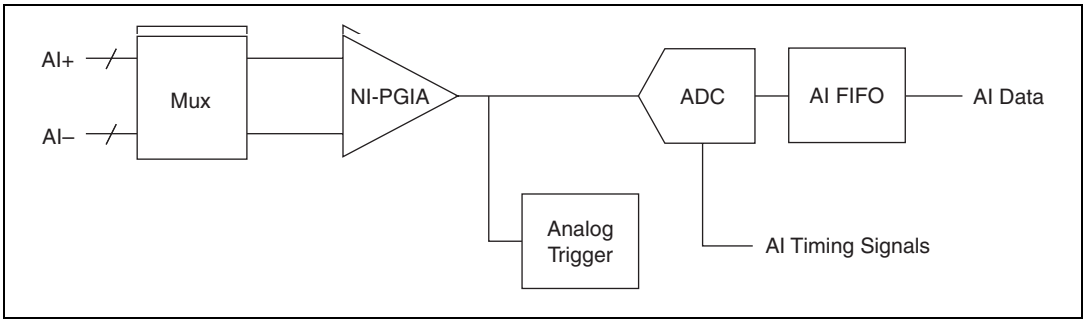



**Figure 2-1.** Analog Input Circuitry Block Diagram

E Series AI signals include the following signals: AI <0..15>, AI SENSE, and AI GND. The NI 6031E/6033E/6071E devices include AI <16..63> and AI SENSE 2 in addition to the previous list of signals. The type of input signal source and the configuration of the AI channels being used determine how you connect these AI signals to the E Series devices. This chapter provides an overview of the different types of signal sources and AI configuration modes.

## Analog Input Circuitry

### Mux

Each E Series device has one analog-to-digital converter (ADC). The multiplexer (mux) routes one AI channel at a time to the ADC through the NI-PGIA. The mux also gives you the ability to use three different analog input terminal configuration. For more information, refer to the *Analog Input Terminal Configuration* section.

## Instrumentation Amplifier (NI-PGIA)

The NI programmable gain instrumentation amplifier (NI-PGIA) is a measurement and instrument class amplifier that guarantees minimum settling times at all gains. The NI-PGIA can amplify or attenuate an AI signal to ensure that you use the maximum resolution of the ADC.

E Series devices use the NI-PGIA to deliver full 16- and 12-bit accuracy when sampling multiple channels at high gains and fast rates. E Series devices can sample channels in any order at the maximum conversion rate, and you can individually program each channel with a different input polarity and range, as discussed in the *Input Polarity and Range* section.

## A/D Converter

The analog-to-digital converter (ADC) digitizes the AI signal by converting the analog voltage into a digital number.

## AI FIFO

A large first-in-first-out (FIFO) buffer holds data during A/D conversions to ensure that no data is lost. E Series devices can handle multiple A/D conversion operations with DMA, interrupts, or programmed I/O.

## Analog Trigger

Refer to the *Analog Input Triggering* section for information about the trigger circuitry of E Series devices.

## AI Timing Signals

Refer to the *Analog Input Timing Signals* section for information about the analog input timing signals available on E Series devices.

# Input Polarity and Range

You can individually program the input range of each AI channel on your E Series device. Input range refers to the set of input voltages that an analog input channel can digitize with the specified accuracy.

The input range affects the resolution of the E Series device for an AI channel. Resolution refers to the voltage of one ADC code. For example, a 16-bit ADC converts analog inputs into one of 65,536 (= $2^{16}$) codes that is one of 65,536 possible digital values. These values are spread fairly evenly

across the input range. So, for an input range of 0 to 10 V, the voltage of each code of a 16-bit ADC is

$$\frac{10\ V - 0\ V}{2^{16}} = 153\ \mu V$$

Some E Series devices support both unipolar and bipolar input ranges. A unipolar input range means that the input voltage range is between 0 and $V_{ref}$, where $V_{ref}$ is a positive reference voltage. A bipolar input range means that the input voltage range is between $-V_{ref}$ and $V_{ref}$.

The NI-PGIA applies a different gain setting to the AI signal depending on the input range. Gain refers to the factor by which the NI-PGIA multiplies (amplifies) the input signal before sending it to the ADC. For example, for the input range 0 to 100 mV, the NI-PGIA applies a gain of 100 to the signal; for an input range of 0 to 5 V, the NI-PGIA applies a gain of 2.

Choose an input range that matches the expected input range of your signal. A large input range can accommodate a large signal variation, but reduces the voltage resolution. Choosing a smaller input range improves the voltage resolution, but may result in the input signal going out of range.

For more information about programming these settings, refer to the *NI-DAQmx Help* or the *LabVIEW 8.x Help*.

Tables 2-1, 2-2, and 2-3 show the input ranges and resolutions supported by each E Series device.

**Table 2-1.** Input Ranges for NI 6020E, NI 6040E, NI 6052E, NI 6062E, and NI 6070E/6071E

| Input Range | Gain | Polarity | Precision | | | | |
|---|---|---|---|---|---|---|---|
| | | | NI 6020E | NI 6040E | NI 6052E | NI 6062E | NI 6070E/ 6071E |
| 0 to +10 V | 1 | Unipolar | 2.44 mV | 2.44 mV | 153 µV | 2.44 mV | 2.44 mV |
| 0 to +5 V | 2 | | 1.22 mV | 1.22 mV | 76.3 µV | 1.22 mV | 1.22 mV |
| 0 to +2V | 5 | | 488 µV | 488 µV | 30.5 µV | 488 µV | 488 µV |
| 0 to +1 V | 10 | | 244 µV | 244 µV | 15.3 µV | 244 µV | 244 µV |
| 0 to +500 mV | 20 | | 122 µV | 122 µV | 7.63 µV | 122 µV | 122 µV |
| 0 to +200 mV | 50 | | 48.8 µV | 48.8 µV | 3.05 µV | 48.8 µV | 48.8 µV |
| 0 to +100 mV | 100 | | 24.4 µV | 24.4 µV | 1.53 µV | 24.4 µV | 24.4 µV |

**Table 2-1.** Input Ranges for NI 6020E, NI 6040E, NI 6052E, NI 6062E, and NI 6070E/6071E (Continued)

| Input Range | Gain | Polarity | Precision | | | | |
|---|---|---|---|---|---|---|---|
| | | | NI 6020E | NI 6040E | NI 6052E | NI 6062E | NI 6070E/ 6071E |
| –10 to +10 V | 0.5 | Bipolar | 4.88 mV | 4.88 mV | 305 µV | 4.88 mV | 4.88 mV |
| –5 to +5 V | 1 | | 2.44 mV | 2.44 mV | 153 µV | 2.44 mV | 2.44 mV |
| –2.5 to +2.5 V | 2 | | 1.22 mV | 1.22 mV | 76.3 µV | 1.22 mV | 1.22 mV |
| –1 to +1 V | 5 | | 488 µV | 488 µV | 30.5 µV | 488 µV | 488 µV |
| –500 to +500 mV | 10 | | 244 µV | 244 µV | 15.3 µV | 244 µV | 244 µV |
| –250 to +250 mV | 20 | | 122 µV | 122 µV | 7.63 µV | 122 µV | 122 µV |
| –100 to +100 mV | 50 | | 48.8 µV | 48.8 µV | 3.05 µV | 48.8 µV | 48.8 µV |
| –50 to +50 mV | 100 | | 24.4 µV | 24.4 µV | 1.53 µV | 24.4 µV | 24.4 µV |

**Table 2-2.** Input Ranges for NI 6011E and NI 6030E/6031E/6032E/6033E

| Input Range | Gain | Polarity | Precision | |
|---|---|---|---|---|
| | | | NI 6011E | NI 6030E/6030E/ 6032E/6033E |
| 0 to +10 V | 1 | Unipolar | 153 µV | 153 µV |
| 0 to +5 V | 2 | | 76.3 µV | 76.3 µV |
| 0 to +2 V | 5 | | — | 30.5 µV |
| 0 to +1 V | 10 | | 15.3 µV | 15.3 µV |
| 0 to +500 mV | 20 | | — | 7.63 µV |
| 0 to +200 mV | 50 | | — | 3.05 µV |
| 0 to +100 mV | 100 | | 1.53 µV | 1.53 mV |
| –10 to +10 V | 1 | Bipolar | 305 µV | 305 µV |
| –5 to +5 V | 2 | | 153 µV | 153 µV |
| –2 to +2 V | 5 | | — | 61.0 µV |
| –1 to +1 V | 10 | | 30.5 µV | 30.5 µV |
| –500 to +500 mV | 20 | | — | 15.3 µV |
| –200 to +200 mV | 50 | | — | 6.10 µV |
| –100 to +100 mV | 100 | | 3.05 µV | 3.05 µV |

**Note** You can calibrate NI 6011E and NI 6030E/6031E/6032E/6033E circuitry for either unipolar or bipolar polarity. If you mix unipolar and bipolar channels in the scan list and you are using NI-DAQ, NI-DAQ loads the calibration constants appropriate to the polarity for which AI channel 0 is configured.

**Table 2-3.** Input Ranges for NI 6023E/6024E/6025E and NI 6034E/6035E/6036E

| Input Range | Gain | Resolution | |
|---|---|---|---|
| | | NI 6023E/6024E/6025E | NI 6034E/6035E/6036E |
| –10 to +10 V | 0.5 | 4.88 mV | 305 µV |
| –5 to +5 V | 1 | 2.44 mV | 153 µV |
| –500 to +500 mV | 10 | 244 µV | 15.3 µV |
| –50 to +50 mV | 100 | 24.4 µV | 1.53 µV |

# Analog Input Terminal Configuration

To be flexible enough to interface with various signal sources, E Series devices have three different terminal configurations, also referred to as input modes: Non-Referenced Single-Ended (NRSE) input, Referenced Single-Ended (RSE) input, and differential (DIFF) input. Table 2-4 describes the three input configurations.

**Table 2-4.** Analog Input Terminal Configuration

| AI Terminal Configuration | Description |
|---|---|
| DIFF | A channel configured in DIFF mode uses two AI lines. One line connects to the positive input of the device programmable gain instrumentation amplifier (PGIA), and the other connects to the negative input of the PGIA. |
| RSE | A channel configured in RSE mode uses one AI line, which connects to the positive input of the PGIA. The negative input of the PGIA is internally tied to AI ground (AI GND). |
| NRSE | A channel configured in NRSE mode uses one AI line, which connects to the positive input of the PGIA. The negative input of the PGIA connects to the AI sense (AI SENSE) input. |

Refer to the *Connecting Analog Input Signals* section for more information about using these input configurations.

The single-ended input configurations provide up to 16 channels (64 channels on the NI 6031E, NI 6033E, and NI 6071E). The DIFF input configuration provides up to eight channels (32 channels on the NI 6031E, NI 6033E, and NI 6071E). Input modes are programmed on a per channel basis for multi-mode scanning. For example, you can configure the circuitry to scan 12 channels—four differentially-configured channels and eight single-ended channels.

With each input mode configuration, you use the PGIA in a different way. The PGIA applies gain and common-mode voltage rejection and presents high-input impedance to the AI signals connected to the device. Signals are routed to the positive and negative inputs of the PGIA through input multiplexers on the device. The PGIA converts two input signals to a new signal by taking the difference between the two input signals and multiplying the difference by the gain setting of the amplifier. The amplifier output voltage is referenced to the ground for the device. The device A/D converter (ADC) measures this output voltage when it performs A/D conversions. Figure 2-2 shows a diagram of the PGIA.

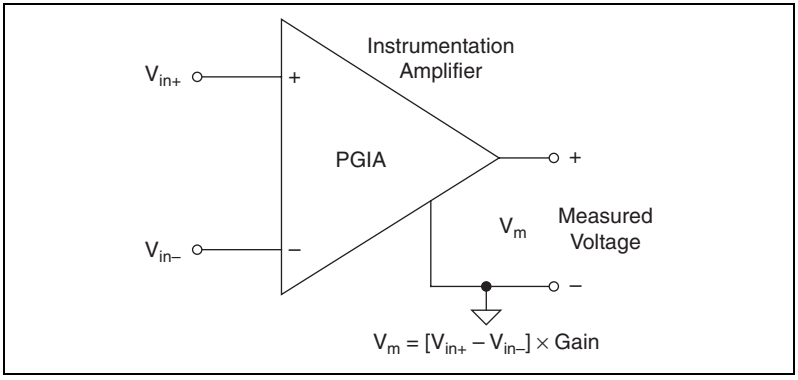



**Figure 2-2.** E Series PGIA

Table 2-5 shows how signals are routed to the NI-PGIA.

**Table 2-5.** NI-PGIA Signal

| AI Terminal Configuration | Signals Routed to the Positive Input of the NI-PGIA | Signals Routed to the Negative Input of the NI-PGIA |
|---|---|---|
| RSE | AI <0..15> | AI GND |
| NRSE | AI <0..15> | AI SENSE |
| DIFF | AI <0..7> | AI <8..15> |

Reference all signals to ground either at the source or at the DAQ device. If you have a floating source, reference the signal to ground by using RSE mode or DIFF mode with bias resistors. Refer to the *Differential Connections for Non-Referenced or Floating Signal Sources* section for more information. If you have a grounded source, do not reference the signal to AI GND. You can avoid this reference by using DIFF or NRSE input modes.

**Caution** Exceeding the DIFF and common-mode input ranges distorts the input signals. Exceeding the maximum input voltage rating can damage the device and the computer. NI is *not* liable for any damage resulting from such signal connections. The maximum input voltage ratings are listed in the specifications document for each E Series family.

**(NI 6031E, NI 6033E, and NI 6071E Only)** For these extended AI devices, the AI signals are AI <0..63>, AI SENSE, AI SENSE 2, and AI GND. In single-ended mode, signals connected to AI <0..63> are routed to the positive input of the PGIA. In differential mode, signals connected to AI <0..7, 16..23, 32..39, 48..55> are routed to the positive input of the PGIA, and signals connected to AI <8..15, 24..31, 40..47, 56..63> are routed to the negative input of the PGIA.

**(NI 6013/6014 Only)** These devices do not support RSE mode. To measure single-ended signals relative to AI GND, connect AI SENSE to AI GND on your accessory and use NRSE mode.

# Dither

With 12-bit E Series devices, you can improve resolution by enabling the Gaussian dither generator and averaging acquired samples. Dithering is a feature on all 12-bit E Series devices. When you enable dithering, you add approximately 0.5 $LSB_{rms}$ of white Gaussian noise to the signal to be converted by the ADC. This addition is useful for applications involving averaging to increase device resolution, as in calibration or spectral analysis. In such applications, noise modulation decreases and differential linearity improves with the addition of dithering. When taking DC measurements, such as when checking device calibration, enable dithering and average about 1,000 points for a single reading. This process removes the effects of quantization and reduces measurement noise, resulting in improved resolution. For high-speed applications not involving averaging or spectral analysis, you may want to disable dithering to reduce noise. The software enables and disables the dithering circuitry.

Figure 2-3 illustrates the effect of dithering on signal acquisition. Graph A shows a small (±4 LSB) sine wave acquired with dithering off. The ADC quantization is clearly visible. Graph B shows 50 such acquisitions averaged together; quantization is still plainly visible. Graph C shows the sine wave acquired with dithering on. There is a considerable amount of visible noise, but averaging about 50 such acquisitions, as shown in graph D, eliminates both the added noise and the effects of quantization. Dithering has the effect of forcing quantization noise to become a zero-mean random variable rather than a deterministic function of the input signal.

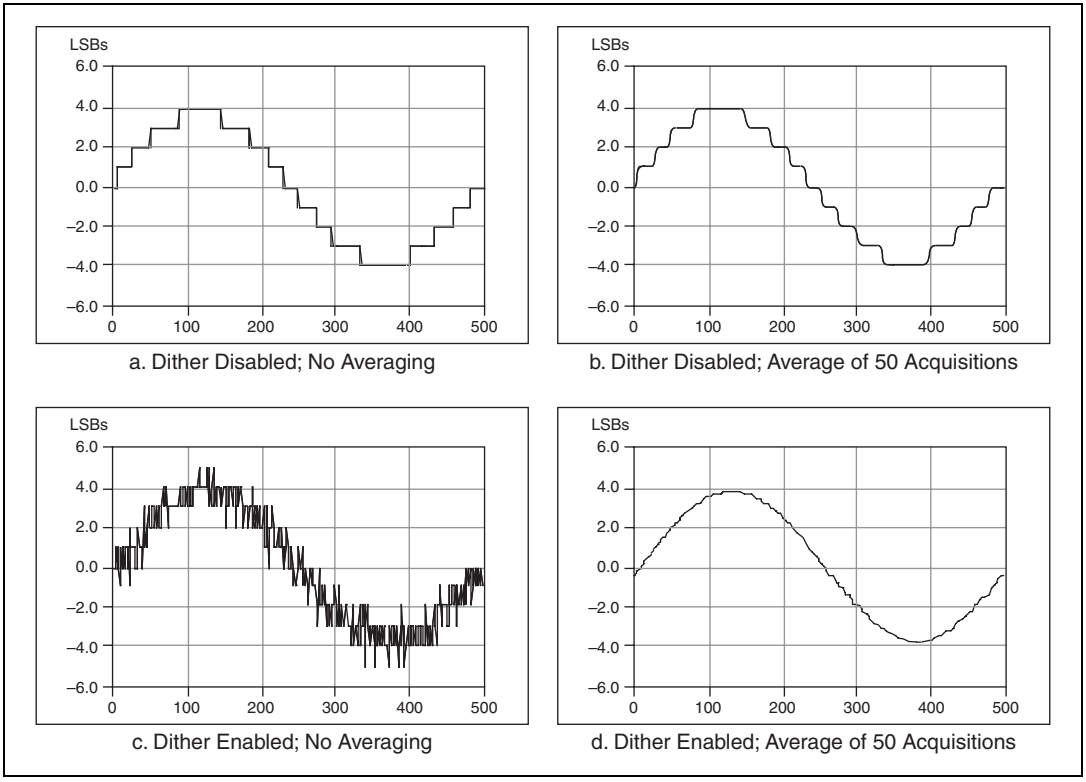



**Figure 2-3.** Dither

Dither cannot be disabled on devices with 16-bit ADCs.

# Multichannel Scanning Considerations

E Series devices can scan multiple channels at high rates and digitize the signals accurately. However, you should consider several issues when designing your measurement system to ensure the high accuracy of your measurements.

In multichannel scanning applications, accuracy is affected by settling time. When your E Series device switches from one AI channel to another AI channel, the device configures the NI-PGIA with the input range of the new channel. The NI-PGIA then amplifies the input signal with the gain and polarity for the new input range. Settling time refers to the time it takes the NI-PGIA to amplify the input signal to the desired accuracy before it is sampled by the ADC. The specification document for your DAQ device shows its settling time.

E Series devices are designed to have fast settling times. Several factors can increase the settling time, which decreases the accuracy of your measurements. To ensure fast settling times, you should (in order of importance):

- Use Low Impedance Sources
- Use Short High-Quality Cabling
- Carefully Choose the Channel Scanning Order
- Avoid Scanning Faster than Necessary

All E Series devices can acquire data in the interval-scanning mode, which fully accommodates multichannel acquisition in both round-robin and pseudo-simultaneous fashions. In multichannel scanning mode, the maximum conversion rate of the device is distributed among the number of channels scanned. With the addition of external signal conditioners, such as the SCXI-1140 or the SC-2040, you can perform true simultaneous sample-and-hold acquisition of eight channels.

## Use Low Impedance Sources

To ensure fast settling times, your signal sources should have an impedances of <1 kΩ. The settling time specifications for your device assume a 1 kΩ source. Large source impedances increase the settling time of the PGIA, and so decrease the accuracy at fast scanning rates.

Settling times increase when scanning high-impedance signals due to a phenomenon called charge injection. Multiplexers contain switches, usually made of switched capacitors. When one of the channels, for example channel 0, is selected in a multiplexer, those capacitors accumulate charge. When the next channel, for example channel 1, is selected, the accumulated charge leaks backward through that channel. If the output impedance of the source connected to channel 1 is high enough, the resulting reading of channel 1 can partially reflect the voltage on channel 0. This is referred to as ghosting, or crosstalk.

If your source impedance is high, you can decrease the scan rate to allow the PGIA more time to settle. Another option is to use a voltage follower circuit external to your DAQ device to decrease the impedance seen by the DAQ device. Refer to the KnowledgeBase document, *How Do I Create a Buffer to Decrease the Source Impedance of My Analog Input Signal?*, for more information.

## Use Short High-Quality Cabling

Using short high-quality cables can decrease several effects that decrease accuracy including crosstalk, transmission line effects, and noise. The capacitance of the cable can also effectively increase the settling time.

National Instruments recommends using individually shielded, twisted-pair wires that are 2 m or less to connect AI signals to the device. Refer to the *Connecting Analog Input Signals* section for more information.

## Carefully Choose the Channel Scanning Order

### Avoid Switching from a Large to a Small Input Range

Switching from a channel with a large input range to a channel with a small input range can greatly increase the settling time.

Suppose a 4 V signal is connected to channel 0 and a 1 mV signal is connected to channel 1. The input range for channel 0 is 0–10 V and the input range of channel 1 is 0–100 mV.

When the multiplexer switches from channel 0 to channel 1, the input to the PGIA switches from 4 V to 1 mV. The approximately 4 V step from 4 V to 1 mV is 4,000% of the new full-scale range. For a 12-bit device to settle within 0.012% (120 ppm or 1/2 LSB) of the 100 mV full-scale range on channel 1, the input circuitry must settle to within 0.0003% (3 ppm or 1/80 LSB) of the 4 V step. Some devices can take as long as 100 µs for the circuitry to settle this much.

To avoid this effect, you should arrange your channel scanning order so that transitions from large to small input ranges are infrequent. Another useful technique is to insert a grounded channel between signal channels.

In general, you do not need this extra settling time when the PGIA is switching from a small input range to a larger input range.

### Insert Grounded Channel between Signal Channels

Another technique to improve settling time is to connect an input channel to ground. Then insert this channel in the scan list between two of your signal channels. The input range of the grounded channel should match the input range of the signal after the grounded channel in the scan list.

Consider again the example above where a 4 V signal is connected to channel 0 and a 1 mV signal is connected to channel 1. The input range for channel 0 is 0–10 V and the input range of channel 1 is 0–100 mV.

Connect channel 2 to AI GND (or you can use the internal ground signal; refer to *Internal Channels for E Series Devices* in the *NI-DAQmx Help* or the *LabVIEW 8.x Help*. Set the input range of channel 2 to 0–100 mV to match channel 1. Then scan channels in the order: 0, 2, 1.

Inserting a grounded channel between signal channels improves settling time because the NI-PGIA adjusts to the new input range setting faster when the input is grounded.

### Minimize Voltage Step between Adjacent Channels

When scanning between channels, the settling time increases when the voltage step is larger between channels. This is true even if all channels being scanned have the same input range. If you know the expected input range of your signals, you can group signals with similar expected ranges together in your scan list.

For example, suppose all channels in a system use a –5 to 5 V input range. The signals on channels 0, 2, and 4 vary between 4.3 V and 5 V. The signals on channels 1, 3, and 5 vary between –4 V and 0 V. Scanning channels in the order 0, 2, 4, 1, 3, 5 will produce more accurate results than scanning channels in the order 0, 1, 2, 3, 4, 5.

## Avoid Scanning Faster than Necessary

Designing your system to scan at slower speeds gives the PGIA more time to settle to a more accurate level. Consider the following examples.

### Example 1

Averaging many AI samples can increase the accuracy of the reading by decreasing noise effects. In general, the more points you average, the more accurate the final result will be. However, you may choose to decrease the number of points you average and slow down the scanning rate.

Suppose you want to sample 10 channels over a period of 20 ms and average the results. You could acquire 500 points from each channel at a scan rate of 250 kS/s. Another method would be to acquire 1,000 points from each channel at a scan rate of 500 kS/s. Both methods take the same amount of time. Doubling the number of samples averaged (from 500 to 1,000) decreases the effect of noise by a factor of 1.4 (the square root of 2). However, doubling the number of samples (in this example) decreases the time the PGIA has to settle from 4 µs to 2 µs. In some cases, the slower scan rate system returns more accurate results.

### Example 2

If the time relationship between channels is not critical, you can sample from the same channel multiple times and scan less frequently. For example, suppose an application requires averaging 100 points from channel 0 and averaging 100 points from channel 1. You could alternate reading between channels

that is, read one point from channel 0, then one point from channel 1, and so on. You also could read all 100 points from channel 0 and then read 100 points from channel 1. The second method switches between channels much less often and is affected much less by settling time.

## AI Data Acquisition Methods

When performing analog input measurements, there are several different data acquisition methods available. You can either perform software-timed or hardware-timed acquisitions. hardware-timed acquisitions can be buffered or non-buffered.

### Software-Timed Acquisitions

With a software-timed acquisition, software controls the rate of the acquisition. Software sends a separate command to the hardware to initiate each ADC conversion. In NI-DAQmx, software-timed acquisitions are referred to as having On Demand timing. software-timed acquisitions are also referred to as immediate or static acquisitions and are typically used for reading a single point of data.

### Hardware-Timed Acquisitions

With hardware-timed acquisitions, a digital hardware signal controls the rate of the acquisition. This signal can be generated internally on your device or provided externally.

Hardware-timed acquisitions have several advantages over software-timed acquisitions:

- The time between samples can be much shorter.
- The timing between samples can be deterministic.

Hardware-timed acquisitions can use hardware triggering.

Hardware-timed operations can be buffered or non-buffered. A buffer is a temporary storage in the computer memory where acquired samples are stored.

### Buffered

In a buffered acquisition, data is moved from the DAQ device onboard FIFO memory to a PC buffer using DMA or interrupts before it is transferred to ADE memory. Buffered acquisitions typically allow for much faster transfer rates than non-buffered acquisitions because data is moved in large blocks, rather than one point at a time. For more information, refer to the *Data Transfer Methods* section of Chapter 9, *Bus Interface*.

One property of buffered I/O operations is the sample mode. The sample mode can be either finite or continuous.

Finite sample mode acquisition refers to the acquisitions of a specific, predetermined number of data samples. Once the specified number of samples has been collected into the buffer, the acquisition stops. If you use a reference trigger, you must use finite sample mode.

Continuous acquisition refers to the acquisition of an unspecified number of samples. Instead of acquiring a set number of data samples and stopping, a continuous acquisition continues until you stop the operation. A continuous acquisition is also referred to as double-buffered or circular-buffered acquisition.

If data cannot be transferred across the bus fast enough, the data in the FIFO will be overwritten and an error will be generated. With continuous operations, if the user program does not read data out of the PC buffer fast enough to keep up with the data transfer, the buffer could reach an overflow condition, causing an error to be generated.

### Non-Buffered

In non-buffered acquisitions, data is read directly from the FIFO on the device. Typically, hardware-timed non-buffered operations are used to read single samples with good latency and known time increments between them.

## Analog Input Triggering

Analog input supports three different triggering actions: start, reference, and pause. An analog or digital hardware trigger can initiate these actions. All E Series devices support digital triggering, and some also support analog triggering. Refer to Chapter 10, *Triggering*, for more information on analog and digital triggering. Refer to Appendix A, *Device-Specific Information*, to find your device triggering options.

# AI Start Trigger Signal

You can use the AI Start Trigger (ai/StartTrigger) signal to begin a measurement acquisition. A measurement acquisition consists of one or more samples. If you do not use triggers, you begin a measurement with a software command. Once the acquisition begins, you can configure the acquisition to stop when one of the following conditions apply:

- When a certain number of points are sampled (in finite mode)
- After a hardware reference trigger (in finite mode)
- With a software command (in continuous mode)

## Using a Digital Source

To use ai/StartTrigger with a digital source, specify a source and an edge. The source can be an external signal connected to any PFI or RTSI <0..6> pin. The source can also be one of several internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW 8.x Help* for more information.

Also, specify whether the measurement acquisition begins on the rising edge or falling edge of the ai/StartTrigger signal.

Figure 2-4 shows the timing requirements of the ai/StartTrigger source.

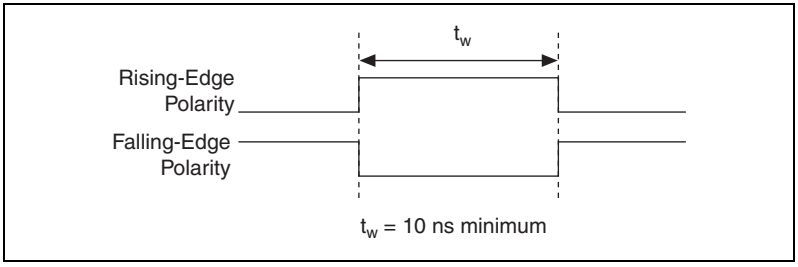



**Figure 2-4.** ai/StartTrigger Source Timing Requirements

## Using an Analog Source

When you use an analog trigger source, the acquisition begins on the first rising edge of the Analog Comparison Event signal. Refer to the *Triggering with an Analog Source* section of Chapter 10, *Triggering*, for more information on analog trigger sources.

## Outputting the AI Start Trigger Signal

You can configure the PFI 0/AI START TRIG pin to output the ai/StartTrigger signal. The output pin reflects the ai/StartTrigger signal regardless of what signal you specify as its source.

The output is an active high pulse. Figure 2-5 shows the timing behavior of the PFI 0/AI START TRIG pin configured as an output.

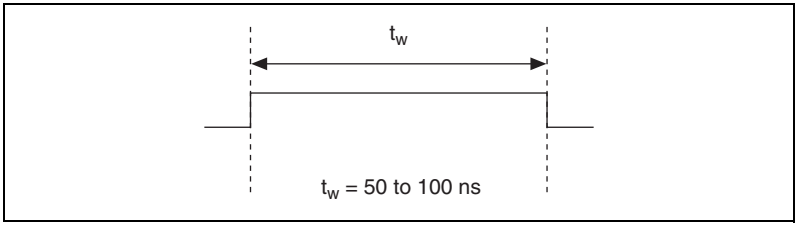



**Figure 2-5.** PFI 0/AI START TRIG Timing Behavior

The PFI 0/AI START TRIG pin is configured as an input by default.

When acquisitions use a start trigger without a reference trigger, they are posttrigger acquisitions because data is acquired only after the trigger. The device also uses ai/StartTrigger to initiate pretrigger DAQ operations. In most pretrigger applications, a software trigger generates ai/StartTrigger. Refer to the *AI Reference Trigger Signal* section for a complete description of the use of ai/StartTrigger and ai/ReferenceTrigger in a pretrigger DAQ operation.

## AI Reference Trigger Signal

You can use the AI Reference Trigger (ai/ReferenceTrigger) signal to stop a measurement acquisition. In Traditional NI-DAQ (Legacy), a reference trigger is referred to as a stop trigger. To use a reference trigger, specify a buffer of finite size and a number of pretrigger samples (samples that occur before the reference trigger). The desired number of posttrigger samples (samples that occur after the reference trigger) is the buffer size minus the number of pretrigger samples.

Once the acquisition begins, the DAQ device writes samples to the buffer. After the DAQ device captures the specified number of pretrigger samples, the DAQ device begins to look for the reference trigger condition. If the reference trigger condition occurs before the DAQ device captures the specified number of pretrigger samples, the DAQ device ignores the condition.

If the buffer becomes full, the DAQ device continuously discards the oldest samples in the buffer to make space for the next sample. You can access this data (with some limitations) before the DAQ device discards it. Refer to the KnowledgeBase document, *Can a Pretriggered Acquisition be Continuous?*, for more information.

When the reference trigger occurs, the DAQ device continues to write samples to the buffer until the buffer contains the desired number of posttrigger samples. Figure 2-6 shows the final buffer.

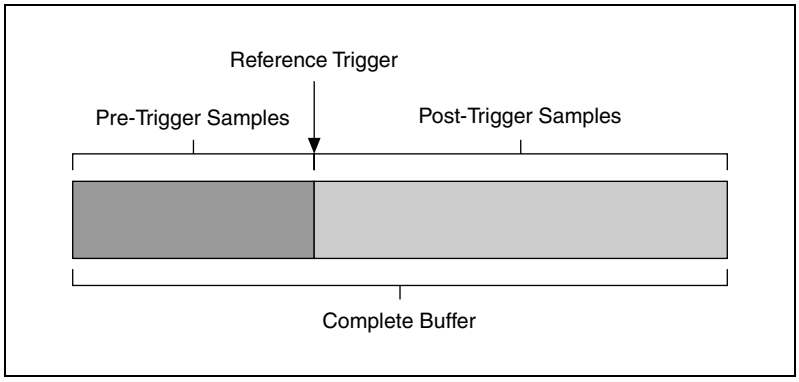



**Figure 2-6.** Reference Trigger Final Buffer

## Using a Digital Source

To use ai/ReferenceTrigger with a digital source, specify a source and an edge. The source can be an external signal connected to any PFI or RTSI <0..6> pin. The source can also be one of several internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW 8.x Help* for more information.

Also, specify whether the measurement acquisition stops on the rising edge or falling edge of the ai/ReferenceTrigger signal.

Figure 2-7 shows the timing requirements of the ai/ReferenceTrigger source.

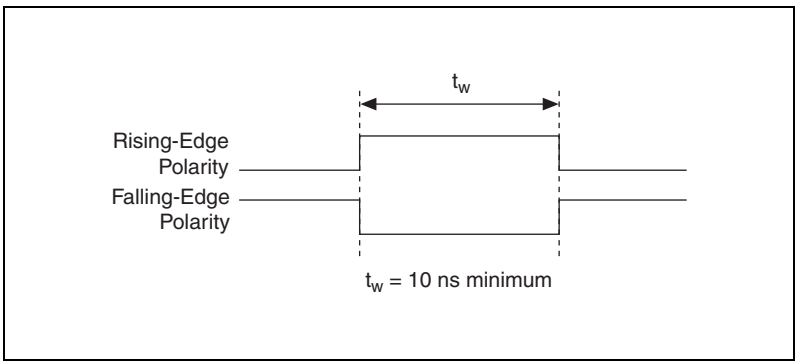



**Figure 2-7.** ai/ReferenceTrigger Source Timing Requirements

## Using an Analog Source

When you use an analog trigger source, the acquisition stops on the first rising edge of the Analog Comparison Event signal. Refer to the *Triggering with an Analog Source* section of Chapter 10, *Triggering*, for more information on analog trigger sources.

## Outputting the AI Reference Trigger Signal

You can configure the PFI 1/AI REF TRIG pin to output the ai/ReferenceTrigger signal. The output pin reflects the ai/ReferenceTrigger signal regardless of what signal you specify as its source.

The output is an active high pulse. Figure 2-8 shows the timing behavior of the PFI 1/AI REF TRIG pin configured as an output.

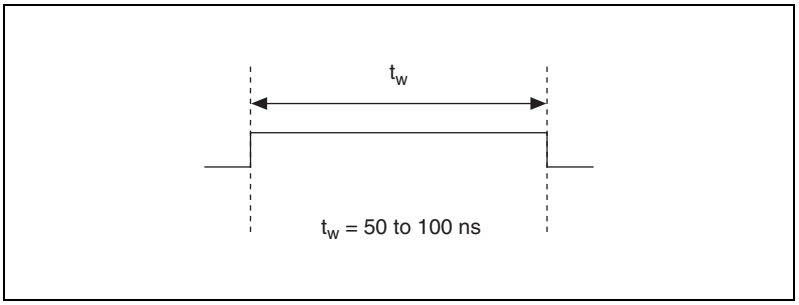



**Figure 2-8.** PFI 1/AI REF TRIG Timing Behavior

The PFI 1/AI REF TRIG pin is configured as an input by default.

## AI Pause Trigger Signal

You can use the AI Pause Trigger (ai/PauseTrigger) signal to pause and resume a measurement acquisition. This signal is not available as an output.

### Using a Digital Source

To use ai/PauseTrigger, specify a source and a polarity. The source can be an external signal connected to any PFI or RTSI <0..6> pin. The source can also be one of several other internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW 8.x Help* for more information.

Also, specify whether the measurement sample is paused when ai/PauseTrigger is at a logic high or low level.

### Using an Analog Source

When you use an analog trigger source, the internal sample clock pauses when the Analog Comparison Event signal is low and resumes when the signal goes high (or vice versa). Refer to the *Triggering with an Analog Source* section of Chapter 10, *Triggering*, for more information on analog trigger sources.

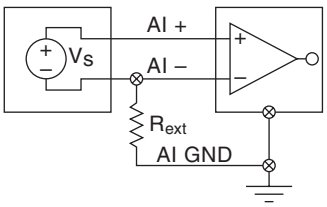
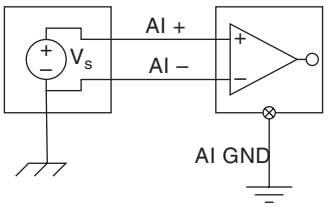
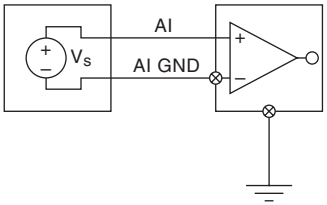
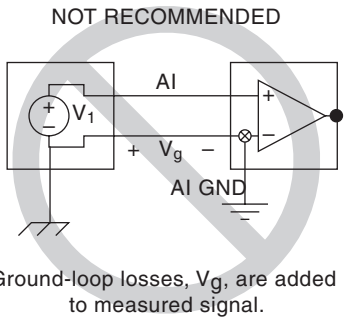
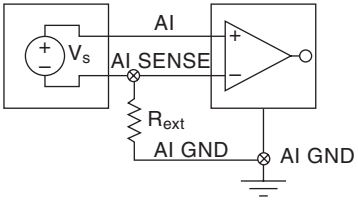
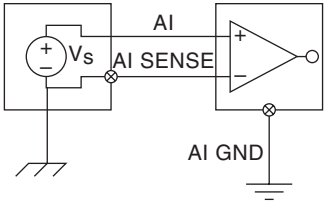
**Note** Pause triggers are only sensitive to the level of the source, not the edge.

# Connecting Analog Input Signals

The following sections discuss the types of signal sources, specify the use of single-ended and DIFF measurements, and provide recommendations for measuring both floating and ground-referenced signal sources.

Table 2-6 summarizes the recommended input configuration for both types of signal sources.

**Table 2-6.** Recommended Input Configurations

| Input | Signal Source Type | |
|---|---|---|
| | **Floating Signal Sources (Not Connect To Building Ground)** | **Ground-Referenced Signal Sources** |
| | Examples<br>• Ungrounded thermocouples<br>• Signal conditioning with isolated outputs<br>• Battery devices | Examples<br>• Plug-in instruments with non-isolated outputs |
| Differential (DIFF) |  |  |
| Single-Ended—Ground Referenced (RSE) |  |  |
| Single-Ended—Non-Referenced (NRSE) |  |  |

Refer to the *Analog Input Terminal Configuration* section for descriptions of the input modes.

## Types of Signal Sources

When configuring the input channels and making signal connections, first determine whether the signal sources are floating or ground-referenced.

### Floating Signal Sources

A floating signal source is not connected to the building ground system, but has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolators, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source. You must connect the ground reference of a floating signal to the AI ground of the device to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats outside the common-mode input range.

### Ground-Referenced Signal Sources

A ground-referenced signal source is connected to the building system ground, so it is already connected to a common ground point with respect to the device, assuming that the computer is plugged into the same power system as the source. Non-isolated outputs of instruments and devices that plug into the building power system fall into this category.

The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV, but the difference can be much higher if power distribution circuits are improperly connected. If a grounded signal source is incorrectly measured, this difference can appear as measurement error. Follow the connection instructions for grounded signal sources to eliminate this ground potential difference from the measured signal.

# Differential Connection Considerations

A DIFF connection is one in which the AI signal has its own reference signal or signal return path. These connections are available when the selected channel is configured in DIFF input mode. The input signal is connected to the positive input of the PGIA, and its reference signal, or return, is connected to the negative input of the PGIA.

When you configure a channel for DIFF input, each signal uses two multiplexer inputs one for the signal and one for its reference signal.

Therefore, half as many DIFF channel pairs are available compared to individual channels.

Use DIFF input connections for any channel that meets any of the following conditions:

- The input signal is low-level (less than 1 V).
- The leads connecting the signal to the device are greater than 3 m (10 ft.).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.

DIFF signal connections reduce noise pickup and increase common-mode noise rejection. DIFF signal connections also allow input signals to float within the common-mode limits of the PGIA.

## Differential Connections for Ground-Referenced Signal Sources

Figure 2-9 shows how to connect a ground-referenced signal source to a channel on the device configured in DIFF mode.

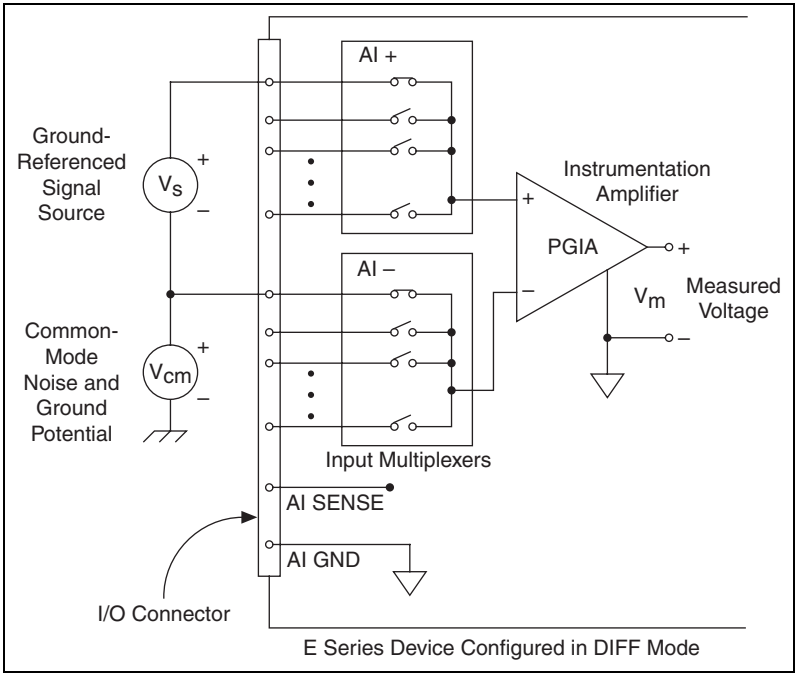



**Figure 2-9.** Differential Connections for Ground-Referenced Signal Sources

With this type of connection, the PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the device ground, shown as $V_{cm}$ in this figure.

## Common-Mode Signal Rejection Considerations

Ground-referenced signal sources with differential connections to the device are referenced to some ground point with respect to the device. In this case, the PGIA can reject any voltage caused by ground potential differences between the signal source and the device. In addition, with DIFF input connections, the PGIA can reject common-mode noise pickup in the leads connecting the signal sources to the device. The PGIA can reject common-mode signals as long as AI + and AI – (input signals) are both within ±11 V of AI GND.

# Differential Connections for Non-Referenced or Floating Signal Sources

Figure 2-10 shows how to connect a floating signal source to a channel configured in DIFF mode.

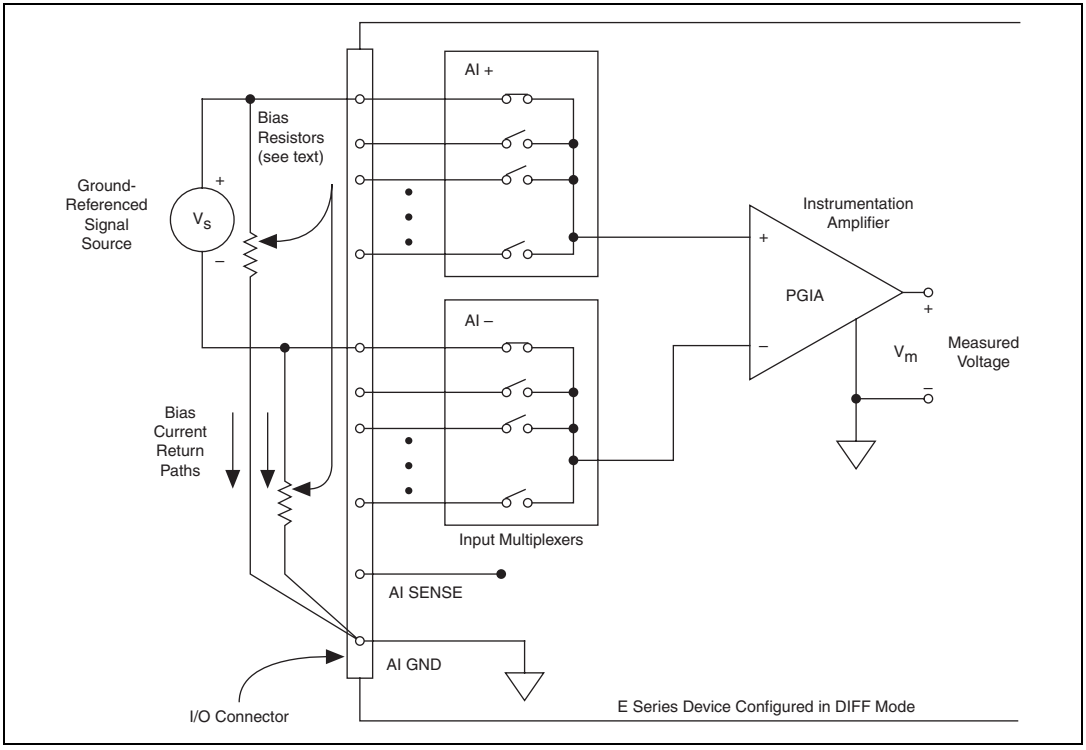



**Figure 2-10.** Connecting a Floating Signal Source to a DIFF Mode Channel

The previous figure shows two bias resistors connected in parallel with the signal leads of a floating signal source. If you do not use the resistors and the source is truly floating, the source is not likely to remain within the common-mode signal range of the PGIA. The PGIA then saturates, causing erroneous readings.

You must reference the source to AI GND. The easiest way to make this reference is to connect the positive side of the signal to the positive input of the PGIA and connect the negative side of the signal to AI GND as well as to the negative input of the PGIA, without using resistors. This connection works well for DC-coupled sources with low source impedance (less than 100 Ω).

However, for larger source impedances, this connection leaves the DIFF signal path significantly off balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line because it is connected to ground. Hence, this noise appears as a DIFF-mode signal instead of a common-mode signal, and the PGIA does not reject it. In this case, instead of directly connecting the negative line to AI GND, connect the negative line to AI GND through a resistor that is about 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance, so that about the same amount of noise couples onto both connections, yielding better rejection of electrostatically coupled noise. This configuration does not load down the source (other than the very high input impedance of the PGIA).

You can fully balance the signal path by connecting another resistor of the same value between the positive input and AI GND, as shown in this figure. This fully balanced configuration offers slightly better noise rejection but has the disadvantage of loading the source down with the series combination (sum) of the two resistors. If, for example, the source impedance is 2 kΩ and each of the two resistors is 100 kΩ, the resistors load down the source with 200 kΩ and produce a –1% gain error.

Both inputs of the PGIA require a DC path to ground in order for the PGIA to work. If the source is AC coupled (capacitively coupled), the PGIA needs a resistor between the positive input and AI GND. If the source has low-impedance, choose a resistor that is large enough not to significantly load the source but small enough not to produce significant input offset voltage as a result of input bias current (typically 100 kΩ to 1 MΩ). In this case, connect the negative input directly to AI GND. If the source has high output impedance, balance the signal path as previously described using the same value resistor on both the positive and negative inputs; be aware that there is some gain error from loading down the source.

# Single-Ended Connection Considerations

A single-ended connection is one in which the device AI signal is referenced to a ground that it can share with other input signals. The input signal connects to the positive input of the PGIA, and the ground connects to the negative input of the PGIA.

When every channel is configured for single-ended input, up to 64 AI channels are available.

You can use single-ended input connections for any input signal that meets the following conditions:

- The input signal is high-level (greater than 1 V).
- The leads connecting the signal to the device are less than 10 ft. (3 m).
- The input signal can share a common reference point with other signals.

DIFF input connections are recommended for greater signal integrity for any input signal that does not meet the preceding conditions.

Using the DAQ Assistant, you can configure the channels for RSE or NRSE input modes. RSE mode is used for floating signal sources; in this case, the device provides the reference ground point for the external signal. NRSE input mode is used for ground-referenced signal sources; in this case, the external signal supplies its own reference ground point and the device should not supply one. Refer to the *DAQ Assistant Help* for more information about the DAQ Assistant.

In the single-ended modes, more electrostatic and magnetic noise couples into the signal connections than in DIFF configurations. The coupling is the result of differences in the signal path. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two conductors.

With this type of connection, the PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the device ground, shown as $V_{cm}$ in Figure 2-11.

## Common-Mode Signal Rejection Considerations

Ground-referenced signal sources with single-ended connections to a device are referenced to some ground point with respect to the device. In this case, the PGIA can reject any voltage caused by ground potential differences between the signal source and the device.

## Single-Ended Connections for Floating Signal Sources (RSE Configuration)

Figure 2-11 shows how to connect a floating signal source to a channel configured for RSE mode.

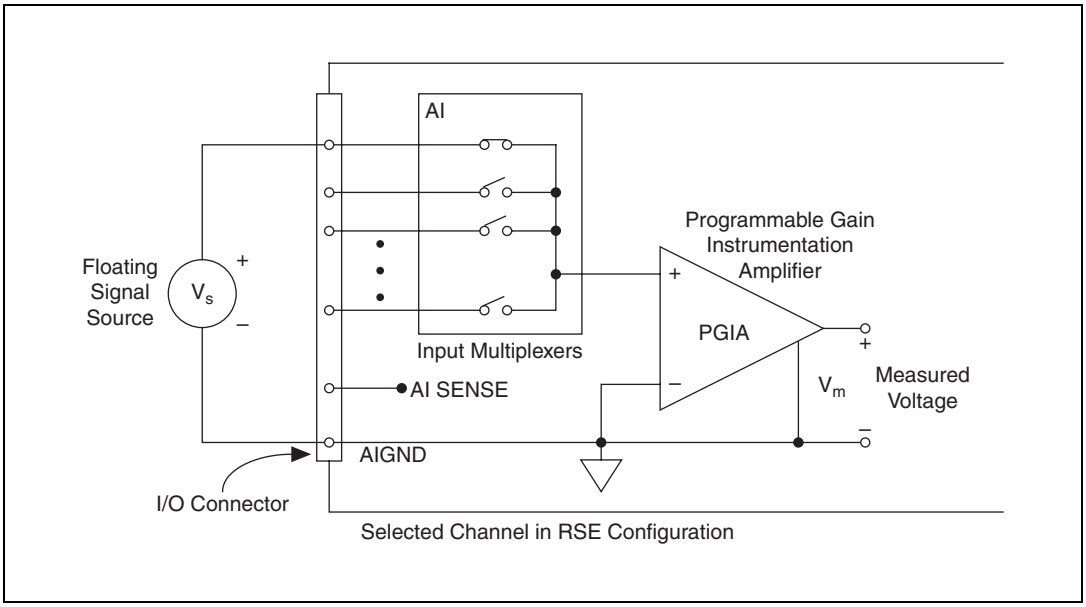



**Figure 2-11.** Single-Ended Connections for Floating Signal Sources (RSE Configuration)

## Single-Ended Connections for Grounded Signal Sources (NRSE Configuration)

To measure a grounded signal source with a single-ended configuration, you must configure your device in the NRSE input configuration. Connect the signal to the positive input of the PGIA, and connect the signal local ground reference to the negative input of the PGIA. The ground point of the signal, therefore, connects to the AI SENSE pin, as shown in Figure 2-12. Any potential difference between the device ground and the signal ground appears as a common-mode signal at both the positive and negative inputs of the PGIA, and this difference is rejected by the amplifier. If the input circuitry of a device were referenced to ground, as it is in the RSE input configuration, this difference in ground potentials would appear as an error in the measured voltage.

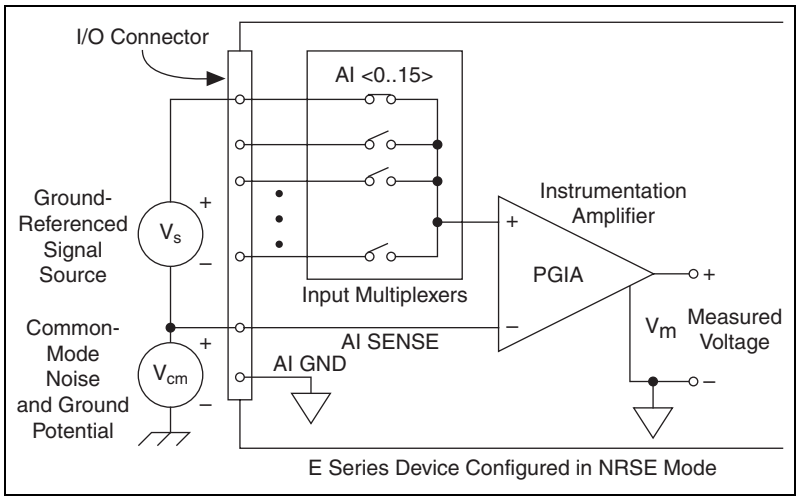



**Figure 2-12.** Single-Ended Connections for Grounded Signal Sources (NRSE Configuration)

# Field Wiring Considerations

Environmental noise can seriously affect the measurement accuracy of the device if you do not take proper care when running signal wires between signal sources and the device. The following recommendations apply mainly to AI signal routing to the device, although they also apply to signal routing in general.

Minimize noise pickup and maximize measurement accuracy by taking the following precautions:

- Use DIFF AI connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect AI signals to the device. With this type of wire, the signals attached to the positive and negative input channels are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.

Refer to the NI Developer Zone document, *Field Wiring and Noise Considerations for Analog Signals*, for more information.

# Configuring AI Modes in Software

You can program channels on an E Series device to acquire in different modes, but once a channel mode is specified, it cannot be reused for another mode. For example, to configure AI 0 for DIFF mode and AI 1 for RSE mode, configure AI 0 and AI 8 in DIFF mode and AI 1 and AI GND in RSE mode. In this configuration, AI 8 is not used in a single-ended configuration.

## Traditional NI-DAQ (Legacy)

To enable multi-mode scanning in LabVIEW using Traditional NI-DAQ (Legacy), use the **coupling & input config** control of the AI Config VI. This input has a one-to-one correspondence with the **channels** control of the VI. You must list all channels either individually or in groups of channels with the same input configuration. For example, if you want AI 0 to be differential, and AI 1 and AI 2 to be RSE, Figure 2-13 demonstrates how to program this configuration in LabVIEW.

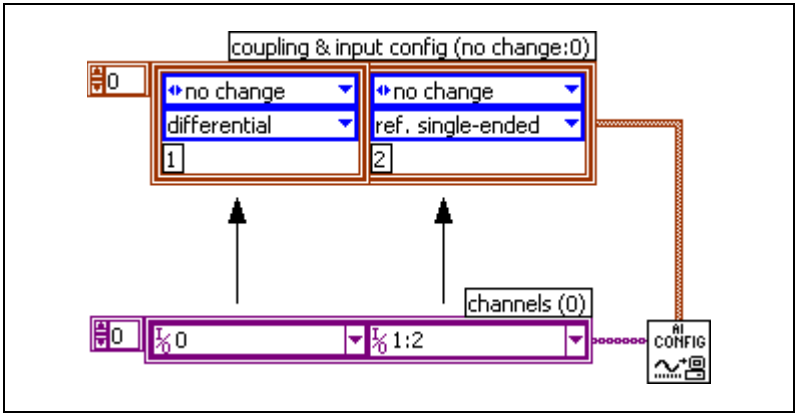



**Figure 2-13.** AI Config VI

To enable multi-mode scanning using NI-DAQ functions, call the `AI_Configure` function for each channel.

## NI-DAQmx

To enable multi-mode scanning in LabVIEW using NI-DAQmx, use the `NI-DAQmx Create Virtual Channel.vi` of the NI-DAQmx API. You must use a new VI for each channel or group of channels configured in a different input mode. In Figure 2-14, channel 0 is configured in differential mode, and channel 1 is configured in RSE mode.

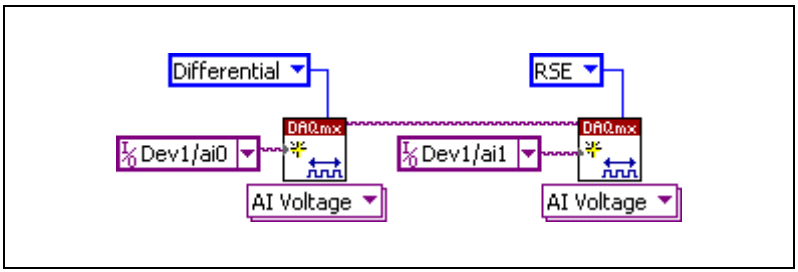



**Figure 2-14.** NI-DAQmx Create Virtual Channel.vi

# Analog Input Timing Signals

In order to provide all of the timing functionality described throughout this section, the DAQ-STC provides an extremely powerful and flexible timing engine. Figure 2-15 summarizes all of the clock routing and timing options provided by the analog input timing engine.

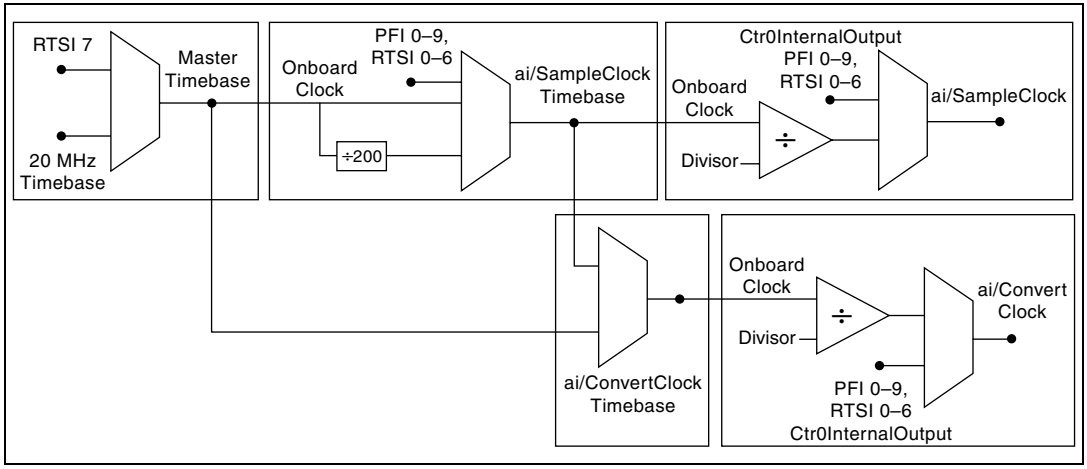



**Figure 2-15.** Analog Input Timing Engine Clock Routing and Timing Options.

E Series devices use the ai/SampleClock and ai/ConvertClock signals to perform interval sampling. As Figure 2-16 shows, ai/SampleClock controls the sample period, which is determined by the following equation:

$$1/\text{sample period} = \text{sample rate}$$

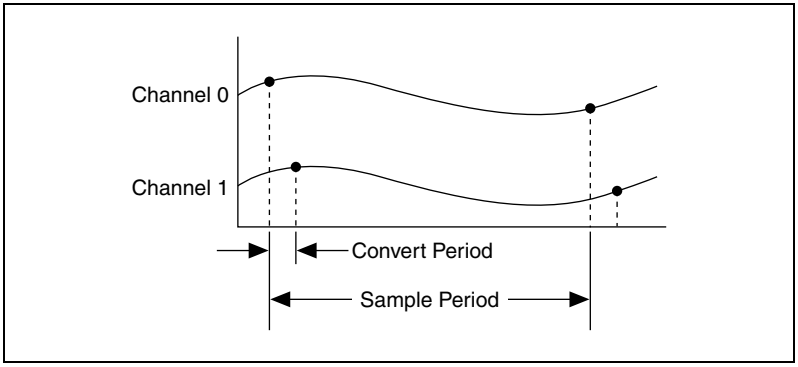



**Figure 2-16.** Interval Sample

The ai/ConvertClock signal controls the convert period, which is determined by the following equation:

1/convert period = convert rate

NI-DAQmx chooses the default convert rate to allow for the maximum settling time between conversions. Typically, this rate is the sampling rate for the task multiplied by the number of channels in the task.

The sampling rate is the fastest you can acquire data on the device and still achieve accurate results. For example, if an E Series device has a sampling rate of 200 kS/s, this sampling rate is aggregate one channel at 200 kS/s or two channels at 100 kS/s per channel illustrates the relationship.

An acquisition with posttrigger data allows you to view data that is acquired after a trigger event is received. A typical posttrigger DAQ sequence is shown in Figure 2-17. The sample counter is loaded with the specified number of posttrigger samples, in this example, five. The value decrements with each pulse on ai/SampleClock, until the value reaches zero and all desired samples have been acquired.

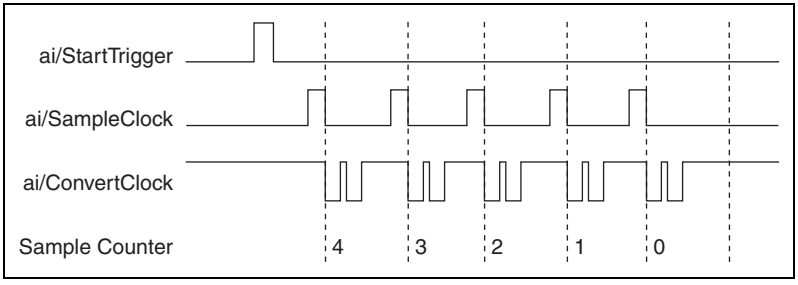



**Figure 2-17.** Typical Posttrigger Acquisition

An acquisition with pretrigger data allows you to view data that is acquired before the trigger of interest, in addition to data acquired after the trigger. Figure 2-18 shows a typical pretrigger DAQ sequence. The ai/StartTrigger signal can be either a hardware or software signal. If ai/StartTrigger is set up to be a software start trigger, an output pulse appears on the AI START TRIG line when the acquisition begins. When the ai/StartTrigger pulse occurs, the sample counter is loaded with the number of pretrigger samples, in this example, four. The value decrements with each pulse on ai/SampleClock, until the value reaches zero. The sample counter is then loaded with the number of posttrigger samples, in this example, three.

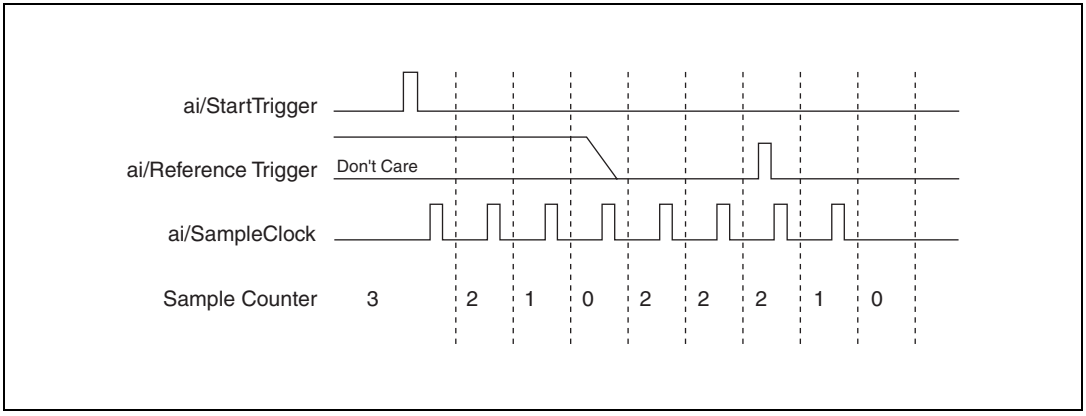



**Figure 2-18.** Typical Pretrigger Acquisition

If an ai/ReferenceTrigger pulse occurs before the specified number of pretrigger samples are acquired, the trigger pulse is ignored. Otherwise, when the ai/ReferenceTrigger pulse occurs, the sample counter value decrements until the specified number of posttrigger samples have been acquired. Refer to the *Analog Input Triggering* section for more information about start and reference triggers.

## AI Start Trigger Signal

You can use the AI Start Trigger (ai/StartTrigger) signal to begin a measurement acquisition. A measurement acquisition consists of one or more samples. If you do not use triggers, you begin a measurement with a software command. Once the acquisition begins, you can configure the acquisition to stop when one of the following conditions apply:

- When a certain number of points are sampled (in finite mode)
- After a hardware reference trigger (in finite mode)
- With a software command (in continuous mode)

## Using a Digital Source

To use ai/StartTrigger with a digital source, specify a source and an edge. The source can be an external signal connected to any PFI or RTSI <0..6> pin. The source can also be one of several internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW 8.x Help* for more information.

Also, specify whether the measurement acquisition begins on the rising edge or falling edge of the ai/StartTrigger signal.

Figure 2-19 shows the timing requirements of the ai/StartTrigger source.

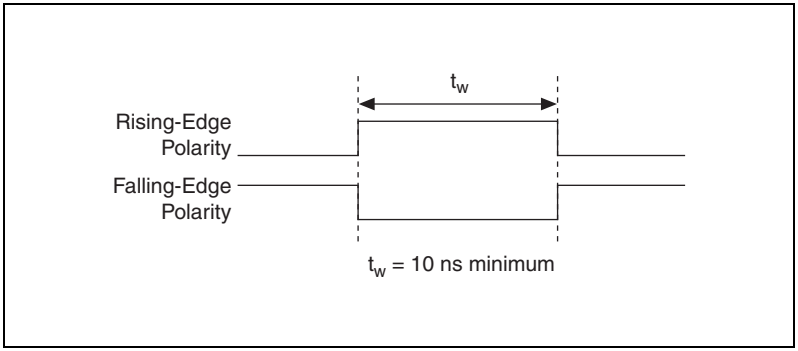



**Figure 2-19.** ai/StartTrigger Timing Requirements

## Using an Analog Source

When you use an analog trigger source, the acquisition begins on the first rising edge of the Analog Comparison Event signal. Refer to Chapter 10, *Triggering*, for more information on analog triggering.

## Outputting the AI Start Trigger Signal

You can configure the PFI 0/AI START TRIG pin to output the ai/StartTrigger signal. The output pin reflects the ai/StartTrigger signal regardless of what signal you specify as its source.

The output is an active high pulse. Figure 2-20 shows the timing behavior of the PFI 0/AI START TRIG pin configured as an output.

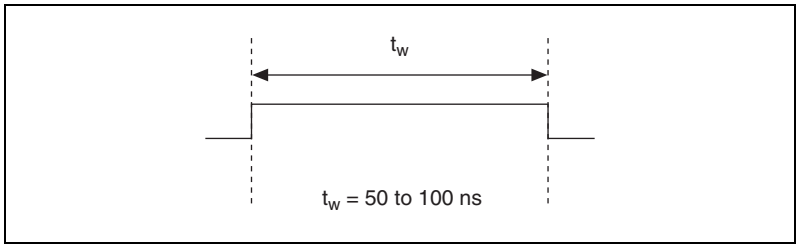



**Figure 2-20.** PFI 0/AI START TRIG Timing Behavior

The PFI 0/AI START TRIG pin is configured as an input by default.

When acquisitions use a start trigger without a reference trigger, they are posttrigger acquisitions because data is acquired only after the trigger. The device also uses ai/StartTrigger to initiate pretrigger DAQ operations. In most pretrigger applications, a software trigger generates ai/StartTrigger. Refer to the *AI Reference Trigger Signal* section for a complete description of the use of ai/StartTrigger and ai/ReferenceTrigger in a pretrigger DAQ operation.

## AI Reference Trigger Signal

You can use the AI Reference Trigger (ai/ReferenceTrigger) signal to stop a measurement acquisition. In Traditional NI-DAQ (Legacy), a reference trigger is referred to as a stop trigger. To use a reference trigger, specify a buffer of finite size and a number of pretrigger samples (samples that occur before the reference trigger). The desired number of posttrigger samples (samples that occur after the reference trigger) is the buffer size minus the number of pretrigger samples.

Once the acquisition begins, the DAQ device writes samples to the buffer. After the DAQ device captures the specified number of pretrigger samples, the DAQ device begins to look for the reference trigger condition. If the reference trigger condition occurs before the DAQ device captures the specified number of pretrigger samples, the DAQ device ignores the condition.

If the buffer becomes full, the DAQ device continuously discards the oldest samples in the buffer to make space for the next sample. You can access this data (with some limitations) before the DAQ device discards it. Refer to the KnowledgeBase document, *Can a Pretriggered Acquisition be Continuous?*, for more information.

When the reference trigger occurs, the DAQ device continues to write samples to the buffer until the buffer contains the desired number of posttrigger samples. Figure 2-21 shows the final buffer.

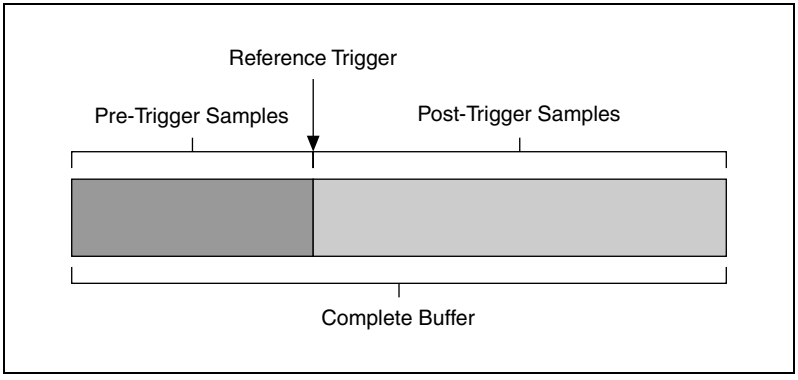



**Figure 2-21.** Reference Trigger Final Buffer

## Using a Digital Source

To use ai/ReferenceTrigger with a digital source, specify a source and an edge. The source can be an external signal connected to any PFI or RTSI <0..6> pin. The source can also be one of several internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW 8.x Help* for more information.

Also, specify whether the measurement acquisition stops on the rising edge or falling edge of the ai/ReferenceTrigger signal.

Figure 2-22 shows the timing requirements of the ai/ReferenceTrigger source.

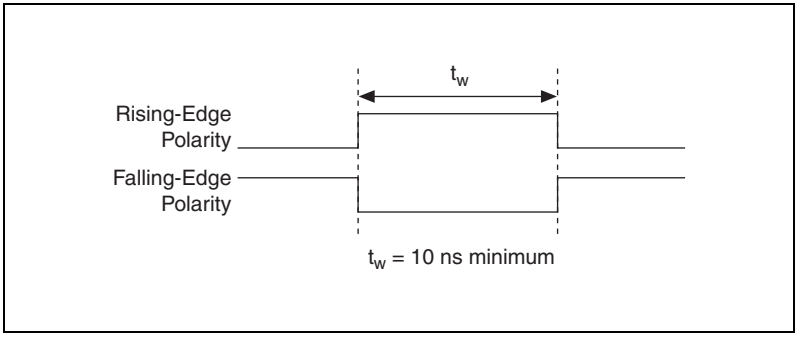



**Figure 2-22.** ai/ReferenceTrigger Source Timing Requirements

## Using an Analog Source

When you use an analog trigger source, the acquisition stops on the first rising edge of the Analog Comparison Event signal. Refer to Chapter 10, *Triggering*, for more information on analog triggering.

## Outputting the AI Reference Trigger Signal

You can configure the PFI 1/AI REF TRIG pin to output the ai/ReferenceTrigger signal. The output pin reflects the ai/ReferenceTrigger signal regardless of what signal you specify as its source.

The output is an active high pulse. Figure 2-23 shows the timing behavior of the PFI 1/AI REF TRIG pin configured as an output.

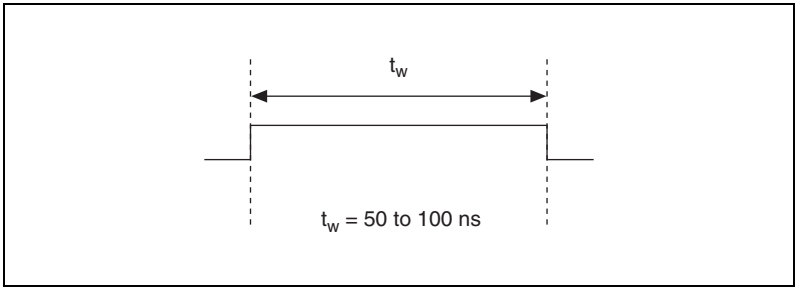



**Figure 2-23.** PFI 1/AI REF TRIG Timing Behavior

The PFI 1/AI REF TRIG pin is configured as an input by default.

# AI Pause Trigger Signal

You can use the AI Pause Trigger (ai/PauseTrigger) signal to pause and resume a measurement acquisition. This signal is not available as an output.

## Using a Digital Source

To use ai/PauseTrigger, specify a source and a polarity. The source can be an external signal connected to any PFI or RTSI <0..6> pin. The source can also be one of several other internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW 8.x Help* for more information.

Also, specify whether the measurement sample is paused when ai/PauseTrigger is at a logic high or low level.

### Using an Analog Source

When you use an analog trigger source, the internal sample clock pauses when the Analog Comparison Event signal is low and resumes when the signal goes high (or vice versa). Refer to Chapter 10, *Triggering*, for more information on analog triggering.

**Note** Pause triggers are only sensitive to the level of the source, not the edge.

## AI Sample Clock Signal

You can use the AI Sample Clock (ai/SampleClock) signal to initiate a set of measurements. Your E Series device samples the AI signals of every channel in the scan list once for every ai/SampleClock. A measurement acquisition consists of one or more samples.

The source of the ai/SampleClock signal can be internal or external. You specify whether the measurement sample begins on the rising edge or falling edge of the ai/SampleClock signal.

### Using an Internal Source

By default, ai/SampleClock is created internally by dividing down the ai/SampleClockTimebase. Refer to the *AI Sample Clock Timebase Signal* section for more information.

Several other internal signals can be routed to the sample clock. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW 8.x Help* for more information.

### Using an External Source

You can use a signal connected to any PFI or RTSI <0..6> pin as the source of ai/SampleClock. Figure 2-24 shows the timing requirements of the ai/SampleClock source.

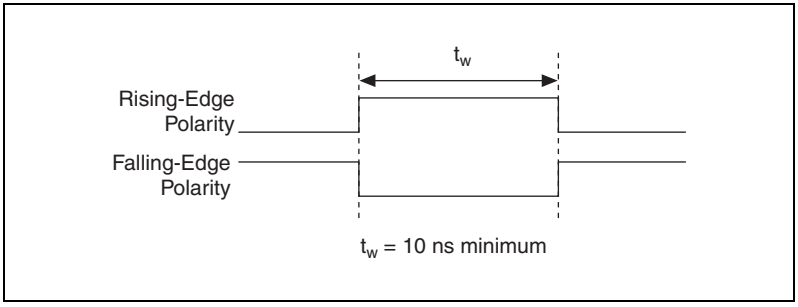



**Figure 2-24.** ai/SampleClock Timing Requirements

## Outputting the AI Sample Clock Signal

You can configure the PFI 7/AI SAMP CLK pin to output the ai/SampleClock signal. The output pin reflects the ai/SampleClock signal regardless of what signal you specify as its source.

You specify the output to have one of two behaviors. With the pulse behavior, your DAQ device briefly pulses the PFI 7/AI SAMP CLK pin once for every occurrence of ai/SampleClock.

With level behavior, your DAQ device drives PFI 7/AI SAMP CLK high during the entire sample. The device drives the pin high in response to the ai/StartTrigger signal. The device drives the pin low in response to the last ai/ConvertClock of the sample.

Figures 2-25 and 2-26 show the timing of pulse and level behavior of the PFI 7/AI SAMP CLK pin.

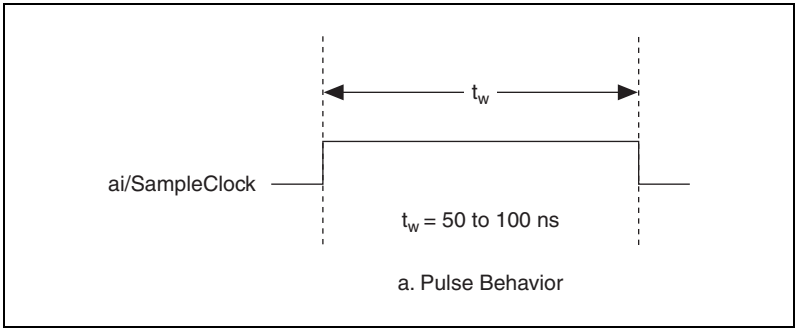



**Figure 2-25.** ai/SampleClock Input

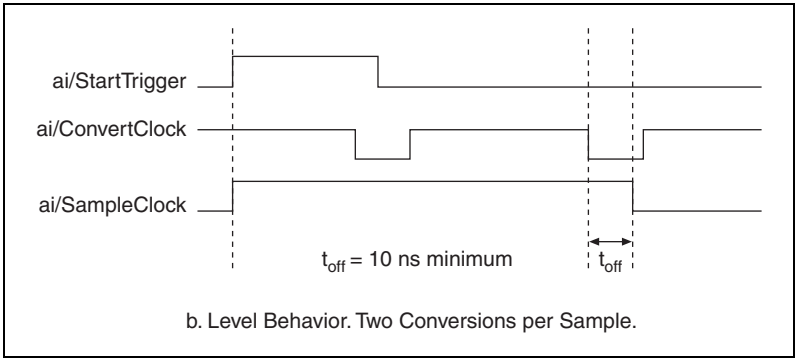



**Figure 2-26.** ai/SampleClock Output

The PFI 7/AI SAMP CLK pin is configured as an input by default.

## Other Timing Requirements

A counter on your device internally generates ai/SampleClock unless you select some external source. The ai/StartTrigger signal starts this counter. It is stopped automatically by hardware once a finite acquisition completes or manually through software. When using an internally generated ai/SampleClock, you can also specify a configurable delay from the ai/StartTrigger to the first ai/SampleClock pulse. By default, this delay is two ticks of the ai/SampleClockTimebase signal. When using an externally generated ai/SampleClock in NI-DAQmx, you must ensure the clock signal is matched with respect to the timing requirements of the ai/ConvertClock signal. Failure to do so may result in ai/SampleClock pulses that are masked off and acquisitions with erratic sampling intervals. Refer to the *AI Convert Clock Signal* section for more information about the timing requirements between ai/ConvertClock and ai/SampleClock.

Figure 2-27 shows the relationship of the ai/SampleClock signal to the ai/StartTrigger signal.

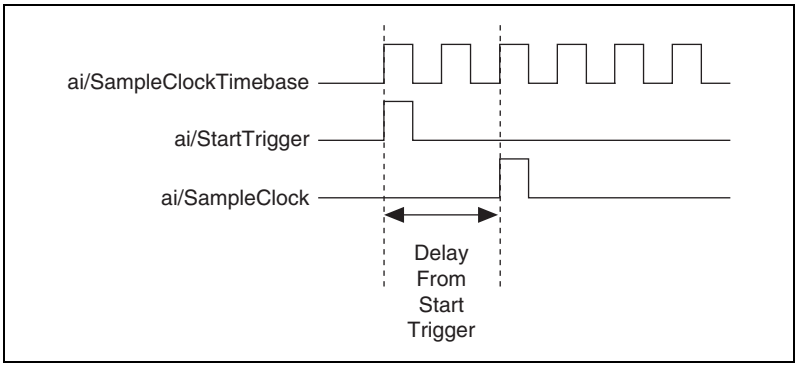



**Figure 2-27.** ai/SampleClock and ai/StartTrigger

## AI Sample Clock Timebase Signal

Any PFI can externally input the AI Sample Clock Timebase (ai/SampleClockTimebase) signal, which is not available as an output on the I/O connector. The ai/SampleClockTimebase is divided down to provide the Onboard Clock source for the ai/SampleClock. You can configure the polarity selection for ai/SampleClockTimebase as either rising or falling edge.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20MHzTimebase or the 100kHzTimebase generates ai/SampleClockTimebase unless you select some external source. Figure 2-28 shows the timing requirements for ai/SampleClockTimebase.

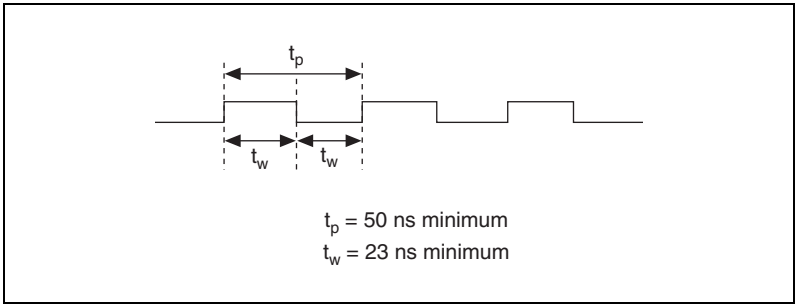



**Figure 2-28.** ai/SampleClockTimebase Timing Requirements

## AI Convert Clock Signal

You can use the AI Convert Clock (ai/ConvertClock) signal to initiate a single A/D conversion on a single channel. A sample (controlled by the AI Sample Clock) consists of one or more conversions.

You specify either an internal or external signal as the source of ai/ConvertClock. You also specify whether the measurement sample begins on the rising edge or falling edge of the ai/ConvertClock signal.

By default, NI-DAQmx will choose a conversion rate so the pulses are evenly spaced throughout the sample. This allows for the maximum settling time between conversions. To approximate simultaneous sampling, you can manually increase the conversion rate. By default, Traditional NI-DAQ (Legacy) chooses the fastest conversion rate possible for the device with 10 µs of delay added between each conversion to allow the channel to some time settle.

**Caution** Setting the conversion rate higher than the maximum rate specified for your device will result in errors.

### Using an Internal Source

One of the following internal signals can drive ai/ConvertClock:

- CTR 0 OUT (the output of Counter 0)
- AI Convert Clock Timebase (divided down)

The AI Convert Clock Timebase is driven by either the AI Sample Clock Timebase or the Master Timebase. A programmable internal counter then divides down the AI Convert Clock Timebase to generate ai/ConvertClock. The counter is started by the ai/SampleClock signal and continues to count down and reload itself until the sample is finished. It then reloads itself in preparation for the next ai/SampleClock pulse.

Several other internal signals can be routed to convert clock timebase through RTSI. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW 8.x Help* for more information.

## Using an External Source

You can use a signal connected to any PFI or RTSI <0..6> pin as the source of ai/ConvertClock. Figure 2-29 shows the timing requirements of the ai/ConvertClock source.

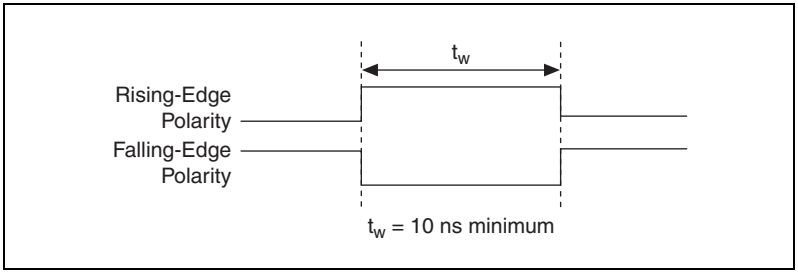



**Figure 2-29.** ai/ConvertClock Source Timing Requirements

## Outputting the AI Convert Clock Signal

You can configure the PFI 2/AI CONV CLK pin to output the ai/ConvertClock signal. The output pin reflects the ai/ConvertClock signal regardless of what signal you specify as its source.

Figure 2-30 shows the timing of behavior of the PFI 2/AI CONV CLK pin configured as an output.

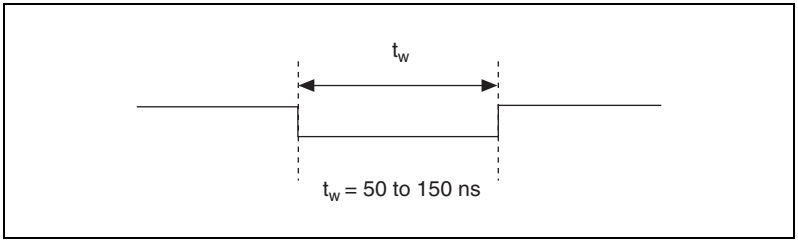



**Figure 2-30.** PFI 2/AI CONV CLK Timing Behavior

The PFI 2/AI CONV CLK pin is configured as an input by default.

## Using a Delay from Sample Clock to Convert Clock

When using an internally generated ai/ConvertClock, you can also specify a configurable delay from the ai/SampleClock to the first ai/ConvertClock pulse within the sample. By default, this delay is two ticks of the ai/ConvertClockTimebase signal.

Figure 2-31 shows the relationship of the ai/SampleClock signal to the ai/ConvertClock signal.

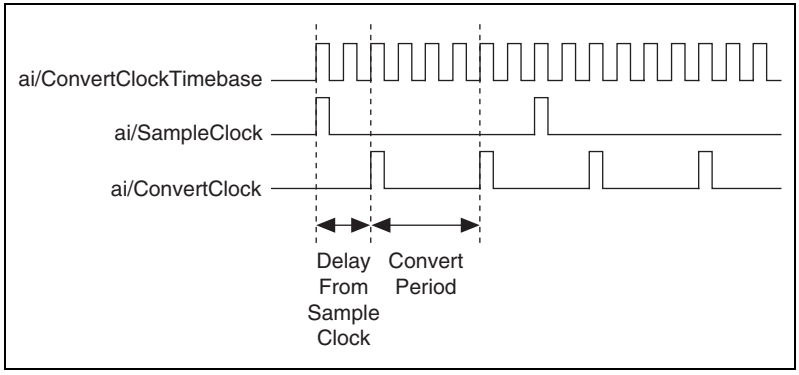



**Figure 2-31.** ai/SampleClock and ai/ConvertClock

## Other Timing Requirements

The sample and conversion level timing of the DAQ-STC work such that clock signals are gated off unless the proper timing requirements are met. For example, the device ignores both the ai/SampleClock and ai/ConvertClock until it receives a valid ai/StartTrigger signal. Once the device recognizes an ai/SampleClock pulse, it ignores subsequent ai/SampleClock pulses until it receives the correct number of ai/ConvertClock pulses.

Similarly, the device ignores all ai/ConvertClock pulses until it recognizes an ai/SampleClock pulse. Once the device receives the correct number of ai/ConvertClock pulses, it ignores subsequent ai/ConvertClock pulses until it receives another ai/SampleClock. Figure 2-32 shows timing sequences for a four-channel acquisition and demonstrate proper and improper sequencing of the ai/SampleClock and ai/ConvertClock signals.

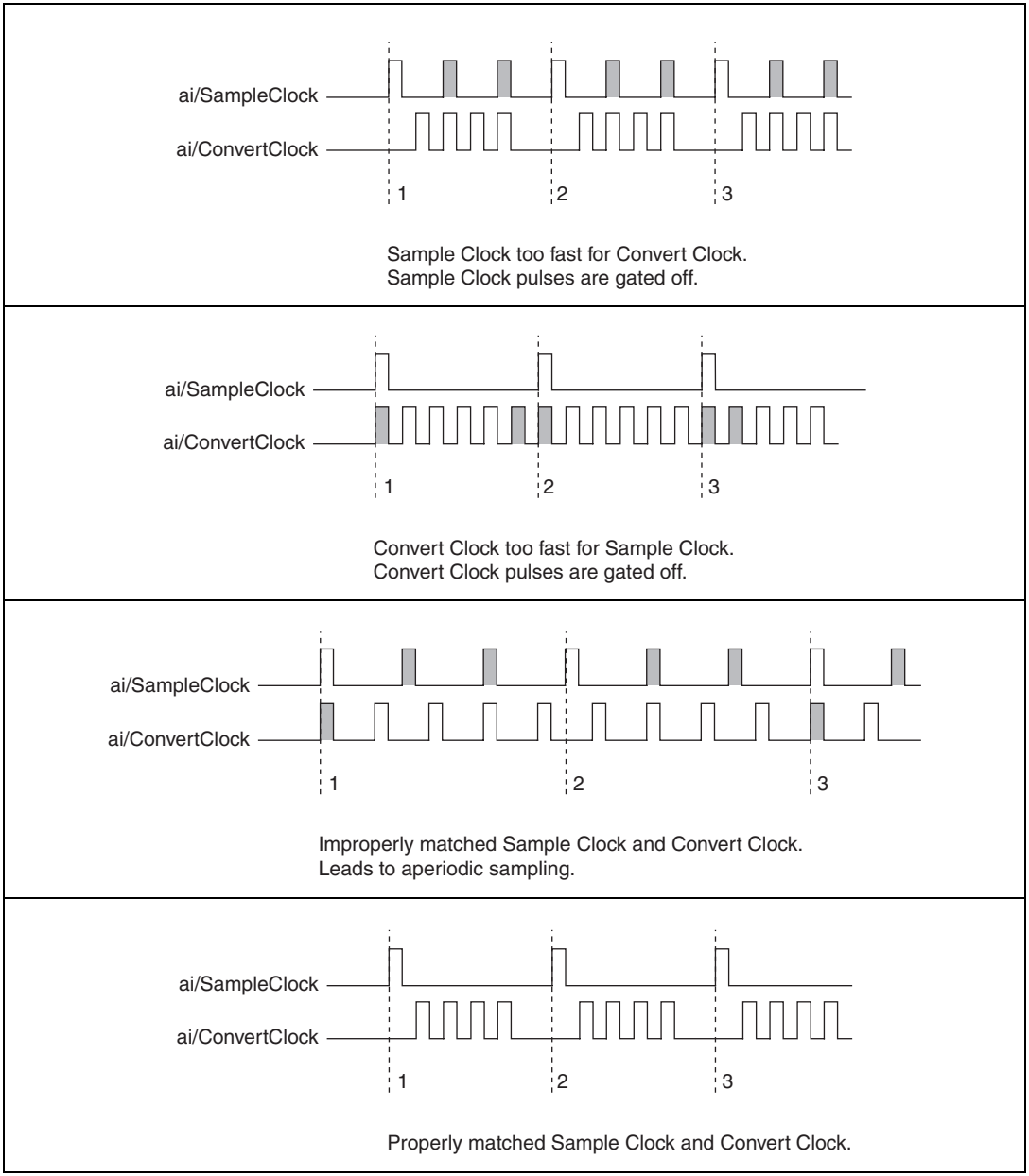



**Figure 2-32.** ai/SampleClock and ai/ConvertClock Signals

## AI Convert Clock Timebase Signal

Either the ai/SampleClockTimebase or the MasterTimebase signal can serve as the source of the AI Convert Clock Timebase signal (ai/ConvertClockTimebase), which is not available as an output on the I/O connector. The ai/ConvertClockTimebase is divided down to provide the Onboard Clock source for the ai/ConvertClock.

## Master Timebase Signal

The Master Timebase (MasterTimebase) signal, or Onboard Clock, is the timebase from which all other internally generated clocks and timebases on the board are derived. It controls the timing for the analog input, analog output, and counter subsystems. It is available as an output on the I/O connector, but you must use one or more counters to do so.

The maximum allowed frequency for the MasterTimebase is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The two possible sources for the MasterTimebase signal are the internal 20MHzTimebase signal or an external signal through RTSI 7. Typically the 20MHzTimebase signal is used as the MasterTimebase unless you wish to synchronize multiple devices, in which case, you should use RTSI 7. Refer to Chapter 8, *Real-Time System Integration Bus (RTSI)*, for more information about which signals are available through RTSI.

Figure 2-33 shows the timing requirements for MasterTimebase.

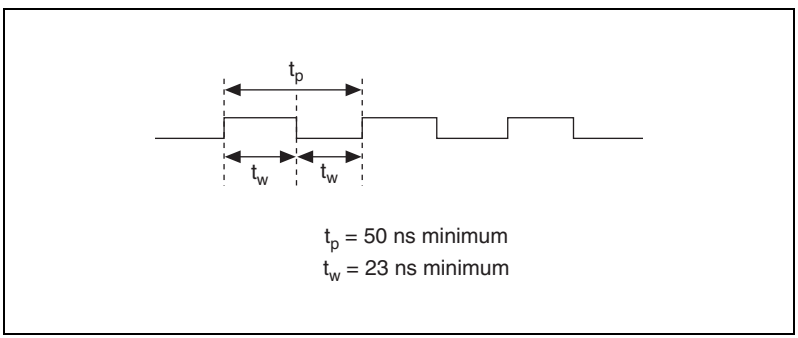



**Figure 2-33.** MasterTimebase Timing Requirements

## AI Hold Complete Event Signal

AI Hold Complete Event (ai/HoldCompleteEvent) is an output-only signal that generates a pulse with the leading edge occurring approximately 50 to 100 ns after an A/D conversion begins. The polarity of this output is software-selectable, but is typically configured so that a low-to-high leading edge can clock external AI multiplexers indicating when the input signal has been sampled and can be removed. This signal has a 400 to 500 ns pulse width and is software-enabled. Figure 2-34 shows the timing for ai/HoldCompleteEvent.

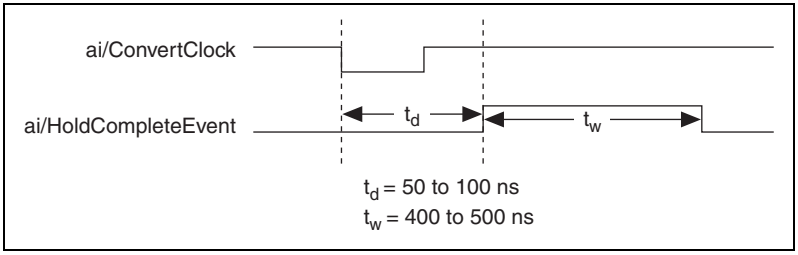



**Figure 2-34.** ai/HoldCompleteEvent Timing

## External Strobe Signal

External Strobe is an output-only signal on the EXT STROBE pin that generates either a single pulse or a sequence of eight pulses in the hardware-strobe mode. An external device can use this signal to latch signals or to trigger events. In the single-pulse mode, software controls the level of External Strobe. A 10 ms and a 1.2 µs clock are available for generating a sequence of eight pulses in the hardware-strobe mode. Figure 2-35 shows the timing for the hardware-strobe mode External Strobe signal.

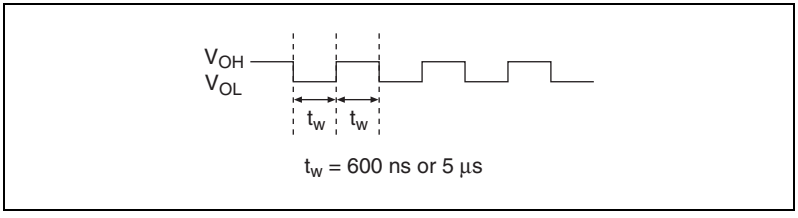



**Figure 2-35.** External Strobe Timing

**Note** External Strobe is used for signal conditioning with SCXI and is not available for use with NI-DAQmx.

# Getting Started with AI Applications in Software

You can use the E Series device in the following analog input applications:

- Single-Point Analog Input
- Finite Analog Input
- Continuous Analog Input

You can perform these applications through DMA, interrupt, or programmed I/O data transfer mechanisms. Some of the applications also use start, reference, and pause triggers.

For more information about programming analog input applications and triggers in software, refer to the *NI-DAQmx Help* or the *LabVIEW 8.x Help*.

# 3

# Analog Output

Figure 3-1 shows the analog output circuitry of E Series devices.

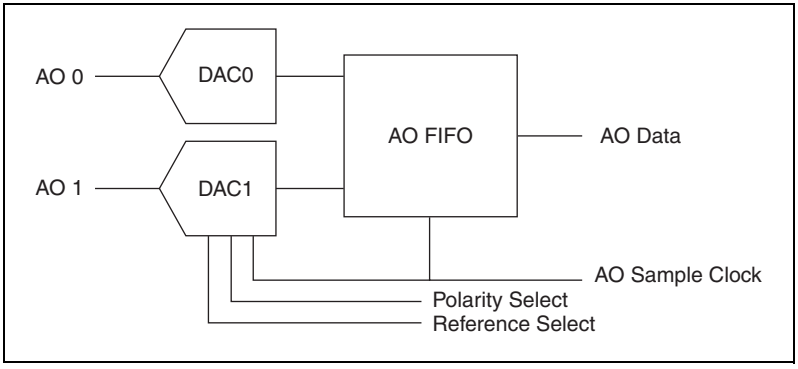



**Figure 3-1.** Analog Output Block Diagram

Many E Series boards have analog output functionality. E Series boards that support analog output have two AO channels that are controlled by a single clock and are capable of waveform generation. Refer to Appendix A, *Device-Specific Information*, for specific information about the capabilities of your device.

## Analog Output Circuitry

### DACs

Digital-to-analog converters (DACs) convert digital codes to analog voltages.

### DAC FIFO

The DAC FIFO enables analog output waveform generation. It is a first-in-first-out (FIFO) memory buffer between the computer and the DACs that allows you to download all the points of a waveform to your board without host computer interaction.

## AO Sample Clock

The DAC reads a sample from the FIFO with every cycle of the AO Sample Clock signal and generates the AO voltage.

## Polarity and Reference Selection

Polarity and reference selection allow you to set the AO range. Refer to Table 3-1 to set the range for your device. Refer to the *Polarity Selection* and the *Reference Selection* sections for more information.

**Table 3-1.** Polarity and Reference Range

| AO Range | Polarity Select | Reference Select |
|---|---|---|
| ±10 V | Bipolar | Internal |
| 0–10 V | Unipolar | Internal |
| ±EXT REF | Bipolar | AO External Reference Signal |
| 0–EXT REF | Unipolar | AO External Reference Signal |

To generate the AO External Reference signal, drive an analog voltage on the AO EXT REF pin.

**Note** Not all E Series devices have every polarity and reference select option. For example, devices such as the NI 6013/6014 and NI 6015/6016 are bipolar only with an internal reference. Refer to the specifications document for your device for more information about range-setting options.

# Reference Selection

**(NI 6020E, NI PXI-6040E, NI 6052E, NI 6062E, NI 6070E/6071E, and PCI-MIO-16E-4 Devices Only)** You can connect each DAC to the device internal reference of 10 V or to the external reference signal connected to the external reference (AO EXT REF) pin on the I/O connector. This signal applied to EXT REF should be within ±11 V. You do not need to configure both channels for the same mode.

# Polarity Selection

**(NI 6020E, NI PXI-6030E, NI PCI-6031E, NI PXI-6040E, NI 6052E, PCI-MIO-16E-4, and PCI-MIO-16XE-10 Devices Only)** With these devices, you can configure each AO channel for either unipolar or bipolar output. All other E Series devices are configured for bipolar output only. A unipolar configuration has a range of 0 to $V_{ref}$ at the analog output. A bipolar configuration has a range of $-V_{ref}$ to $+V_{ref}$ at the analog output. $V_{ref}$ is the voltage reference used by the DACs in the AO circuitry and can be either the +10 V onboard reference or for supported devices, an externally supplied reference within ±11 V. You do not need to configure both channels for the same range.

Selecting a bipolar range for a particular DAC means that any data written to that DAC is interpreted as two's complement format. In two's complement format, data values written to the AO channel can be either positive or negative. If you select unipolar range, data is interpreted in straight binary format. In straight binary mode, data values written to the AO channel range must be positive.

# Reglitch Selection

**(NI 6052E and NI 6070E/6071E Devices Only)** In normal operation, a DAC output glitches whenever it is updated with a new value. The glitch energy differs from code to code and appears as distortion in the frequency spectrum. Each analog output contains a reglitch circuit that generates uniform glitch energy at every code rather than large glitches at the major code transitions. This uniform glitch energy appears as a multiple of the update rate in the frequency spectrum. Notice that this reglitch circuit does not eliminate the glitches; it only makes them more uniform in size. Reglitching is normally disabled at startup and the software can independently enable each channel.

# Minimizing Glitches on the Output Signal

When you use a DAC to generate a waveform, you may observe glitches on the output signal. These glitches are normal; when a DAC switches from one voltage to another, it produces glitches due to released charges. The largest glitches occur when the most significant bit (MSB) of the DACcode switches. You can build a lowpass deglitching filter to remove some of these glitches, depending on the frequency and nature of the output signal. Visit `ni.com/support` for more information about minimizing glitches.

# AO Data Generation Methods

When performing an analog output operation, there are several different data generation methods available. You can either perform software-timed or hardware-timed generations. Hardware-timed generations can be non-buffered or buffered.

## Software-Timed Generations

With a software-timed generation, software controls the rate at which data is generated. Software sends a separate command to the hardware to initiate each DAC conversion. In NI-DAQmx, software-timed generations are referred to as On Demand timing. software-timed generations are also referred to as immediate or static operations. They are typically used for writing a single value out, such as a constant DC voltage.

## Hardware-Timed Generations

With a hardware-timed generation, a digital hardware signal controls the rate of the generation. This signal can be generated internally on your device or provided externally.

Hardware-timed generations have several advantages over software-timed generations:

- The time between samples can be much shorter.
- The timing between samples can be deterministic.
- Hardware-timed generations can use hardware triggering.

Hardware-timed operations can be buffered or non-buffered. A buffer is a temporary storage in computer memory for acquired or to-be-generated samples.

### Buffered

In a buffered generation, data is moved from a PC buffer to the DAQ device onboard FIFO using DMA or interrupts before it is written to the DACs one sample at a time. Buffered generations typically allow for much faster transfer rates than non-buffered generations because data is moved in large blocks, rather than one point at a time. Refer to Chapter 9, *Bus Interface*, for more information on data transfer methods.

One property of buffered I/O operations is the sample mode. The sample mode can be either finite or continuous.

Finite sample mode generation refers to the generation of a specific, predetermined number of data samples. Once the specified number of samples has been written out, the generation stops.

Continuous generation refers to the generation of an unspecified number of samples. Instead of generating a set number of data samples and stopping, a continuous generation continues until you stop the operation. There are several different methods of continuous generation that control what data is written. These methods are regeneration, FIFO regeneration, and non-regeneration modes.

Regeneration is the repetition of the data that is already in the buffer. Standard regeneration is when data from the PC buffer is continually downloaded to the FIFO to be written out. New data can be written to the PC buffer at any time without disrupting the output.

With FIFO regeneration, the entire buffer is downloaded to the FIFO and regenerated from there. Once the data is downloaded, new data cannot be written to the FIFO. To use FIFO regeneration, the entire buffer must fit within the FIFO size. The advantage of using FIFO regeneration is that it does not require communication with the main host memory once the operation is started, thereby preventing any problems that may occur due to excessive bus traffic.

With non-regeneration, old data will not be repeated. New data must be continually written to the buffer. If the program does not write new data to the buffer at a fast enough rate to keep up with the generation, the buffer will underflow and cause an error.

### Non-Buffered

In hardware-timed non-buffered generations, data is written directly to the FIFO on the device. Typically, hardware-timed non-buffered operations are used to write single samples with known time increments between them and good latency.

## Analog Output Triggering

Analog output supports two different triggering actions: start and pause. An analog or digital hardware trigger can initiate these actions. All E Series devices support digital triggering, and some also support analog triggering. Refer to Appendix A, *Device-Specific Information*, to find your device triggering options.

# AO Start Trigger Signal

You can use the AO Start Trigger (ao/StartTrigger) signal to initiate a waveform generation. If you do not use triggers, you begin a generation with a software command.

## Using a Digital Source

To use ao/StartTrigger, specify a source and an edge. The source can be an external signal connected to any PFI or RTSI <0..6> pin. The source can also be one of several internal signal on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW 8.x Help* for more information.

Figure 3-2 shows the timing requirements of the ao/StartTrigger digital source.

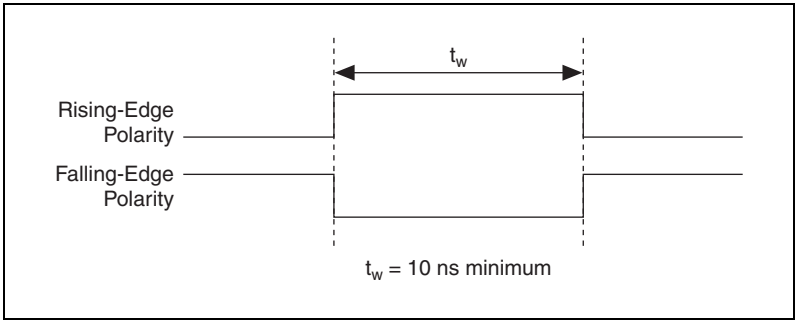



**Figure 3-2.** ao/StartTrigger Digital Source Timing Requirements

## Using an Analog Source

When you use an analog trigger source, the waveform generation begins on the first rising edge of the Analog Comparison Event signal. Refer to Chapter 10, *Triggering*, for more information on analog triggering.

## Outputting the AO Start Trigger Signal

You can configure the PFI 6/AO START TRIG pin to output the ao/StartTrigger signal. The output pin reflects the ao/StartTrigger signal regardless of what signal you specify as its source.

The output is an active high pulse. Figure 3-3 shows the timing behavior of the PFI 6/AO START TRIG pin configured as an output.

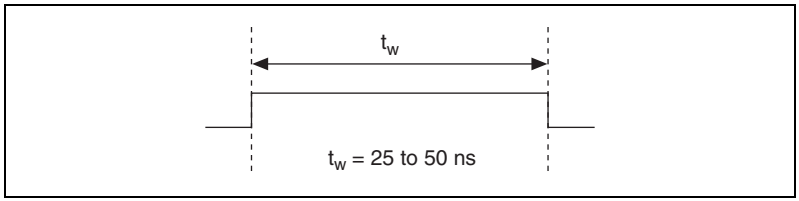



**Figure 3-3.** PFI 6/AO START TRIG Timing Behavior

The PFI 6/AO START TRIG pin is configured as an input by default.

# AO Pause Trigger Signal

You can use the AO Pause trigger signal (ao/PauseTrigger) to mask off samples in a DAQ sequence. That is, when ao/PauseTrigger is active, no samples occur.

The ao/PauseTrigger does not stop a sample that is in progress. The pause does not take effect until the beginning of the next sample. This signal is not available as an output.

## Using a Digital Source

To use ao/PauseTrigger, specify a source and a polarity. The source can be an external signal connected to any PFI or RTSI <0..6> pin. The source can also be one of several other internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW 8.x Help* for more information.

Also, specify whether the samples are paused when ao/PauseTrigger is at a logic high or low level.

## Using an Analog Source

When you use an analog trigger source, the samples are paused when the Analog Comparison Event signal is at a high level. Refer to Chapter 10, *Triggering*, for more information on analog triggering.

# Connecting Analog Output Signals

The AO signals are AO 0, AO 1, and AO GND. AO 0 is the voltage output signal for AO channel 0. AO 1 is the voltage output signal for AO channel 1.

AO GND is the ground reference signal for both AO channels and the external reference signal. Figure 3-4 shows how to make AO connections to the device.

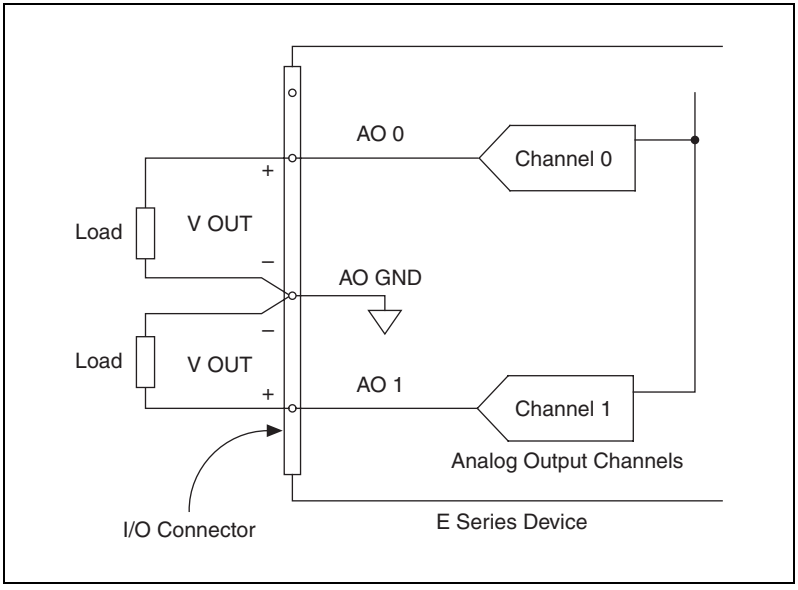



**Figure 3-4.** Analog Output Connections

**Note** Not all E Series devices use the external reference signal. Refer to the specifications document for your device.

# Waveform Generation Timing Signals

There is one AO Sample Clock that causes all AO channels to update simultaneously. Figure 3-5 summarizes the timing and routing options provided by the analog output timing engine.

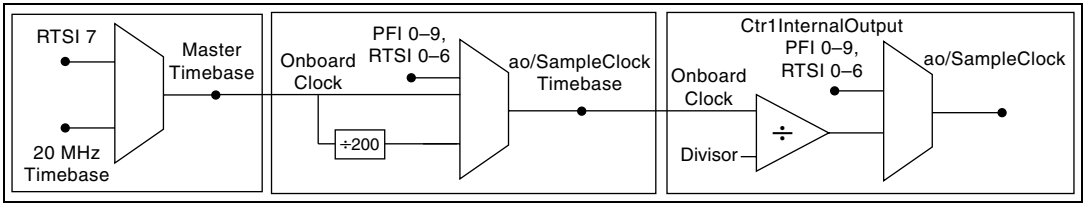



**Figure 3-5.** Analog Output Timing Engine

## AO Start Trigger Signal

You can use the AO Start Trigger (ao/StartTrigger) signal to initiate a waveform generation. If you do not use triggers, you begin a generation with a software command.

### Using a Digital Source

To use ao/StartTrigger, specify a source and an edge. The source can be an external signal connected to any PFI or RTSI <0..6> pin. The source can also be one of several internal signal on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW 8.x Help* for more information.

Figure 3-6 shows the timing requirements of the ao/StartTrigger digital source.

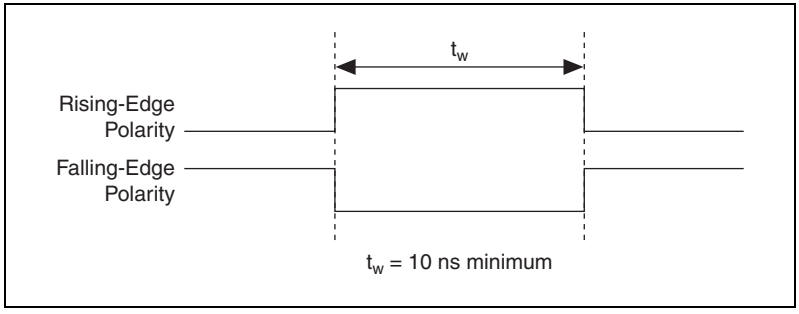



**Figure 3-6.** ao/StartTrigger Digital Source Timing Requirements

## Using an Analog Source

When you use an analog trigger source, the waveform generation begins on the first rising edge of the Analog Comparison Event signal. Refer to Chapter 10, *Triggering*, for more information on analog triggering.

## Outputting the AO Start Trigger Signal

You can configure the PFI 6/AO START TRIG pin to output the ao/StartTrigger signal. The output pin reflects the ao/StartTrigger signal regardless of what signal you specify as its source.

The output is an active high pulse. Figure 3-7 shows the timing behavior of the PFI 6/AO START TRIG pin configured as an output.

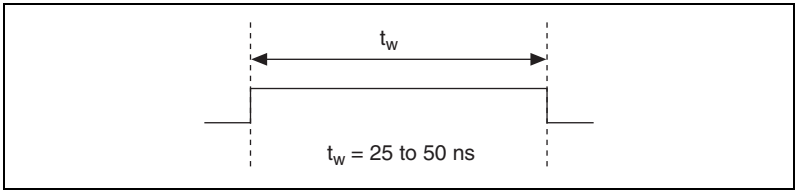



**Figure 3-7.** PFI 6/AO START TRIG Timing Behavior

The PFI 6/AO START TRIG pin is configured as an input by default.

# AO Pause Trigger Signal

You can use the AO Pause trigger signal (ao/PauseTrigger) to mask off samples in a DAQ sequence. That is, when ao/PauseTrigger is active, no samples occur.

The ao/PauseTrigger does not stop a sample that is in progress. The pause does not take effect until the beginning of the next sample. This signal is not available as an output.

## Using a Digital Source

To use ao/Pause Trigger, specify a source and a polarity. The source can be an external signal connected to any PFI or RTSI <0..6> pin. The source can also be one of several other internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW 8.x Help* for more information.

Also, specify whether the samples are paused when ao/PauseTrigger is at a logic high or low level.

### Using an Analog Source

When you use an analog trigger source, the samples are paused when the Analog Comparison Event signal is at a high level. Refer to Chapter 10, *Triggering*, for more information on analog triggering.

## AO Sample Clock Signal

You can use the AO Sample Clock (ao/SampleClock) signal to initiate AO samples. Each sample updates the outputs of all the DACs.

The source of the ao/SampleClock signal can be internal or external. You can specify whether the DAC update begins on the rising edge or falling edge of the ao/SampleClock signal.

### Using an Internal Source

By default, ao/SampleClock is created internally by dividing down the ao/SampleClockTimebase.

Several other internal signals can be routed to the sample clock. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW 8.x Help* for more information.

### Using an External Source

You can use a signal connected to any PFI or RTSI <0..6> pin as the source of ao/SampleClock. Figure 3-8 shows the timing requirements of the ao/SampleClock source.

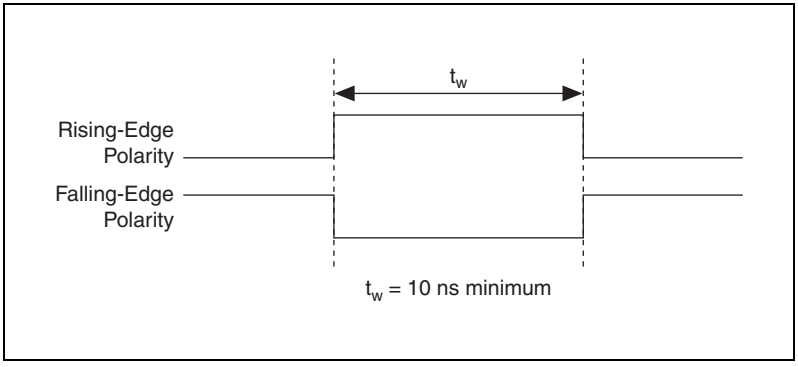



**Figure 3-8.** ao/SampleClock Source Timing Requirements

## Outputting the AO Sample Clock Signal

You can configure the PFI 5/AO SAMP CLK pin to output the ao/SampleClock signal. The output pin reflects the ao/SampleClock signal regardless of what signal you specify as its source.

The output is an active high pulse. Figure 3-9 shows the timing behavior of the PFI 5/AO SAMP CLK pin configured as an output.

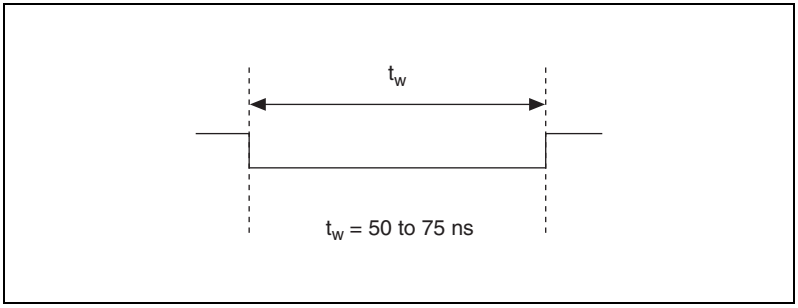



**Figure 3-9.** PFI 5/AO SAMP CLK Timing Behavior

The PFI 5/AO SAMP CLK is configured as an input by default.

## Other Timing Requirements

A counter on your device internally generates ao/SampleClock unless you select some external source. The ao/StartTrigger signal starts this counter. It is stopped automatically by hardware once a finite acquisition completes or manually through software. When using an internally generated ao/SampleClock in NI-DAQmx, you can also specify a configurable delay from the ao/StartTrigger to the first ao/SampleClock pulse. By default, this delay is two ticks of the ao/SampleClockTimebase signal.

Figure 3-10 shows the relationship of the ao/SampleClock signal to the ao/StartTrigger signal.

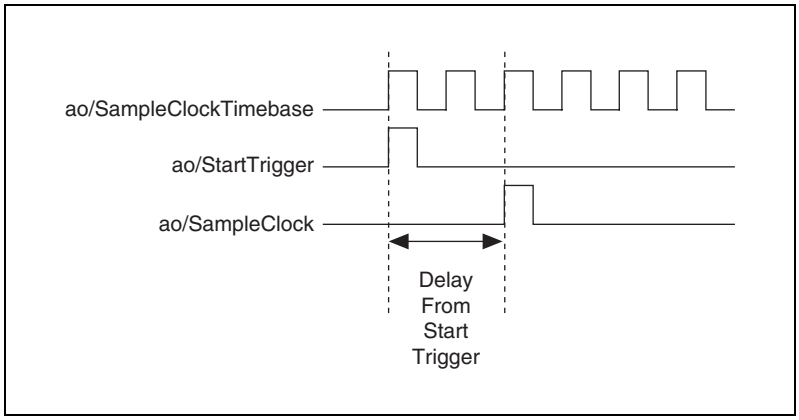



**Figure 3-10.** ao/SampleClock and ao/StartTrigger

## AO Sample Clock Timebase Signal

You can select any PFI or RTSI pin as well as many other internal signals as the AO Sample Clock Timebase (ao/SampleClockTimebase) signal. This signal is not available as an output on the I/O connector. The ao/SampleClockTimebase is divided down to provide the Onboard Clock source for the ao/SampleClock. You specify whether the samples begin on the rising or falling edge of ao/SampleClockTimebase.

You might use the ao/SampleClockTimebase signal if you want to use an external sample clock signal, but need to divide the signal down. If you want to use an external sample clock signal, but do not need to divide the signal, then you should use the ao/SampleClock signal rather than the ao/SampleClockTimebase. If you do not specify an external sample clock timebase, NI-DAQ uses the Onboard Clock.

Figure 3-11 shows the timing requirements for the ao/SampleClockTimebase signal.

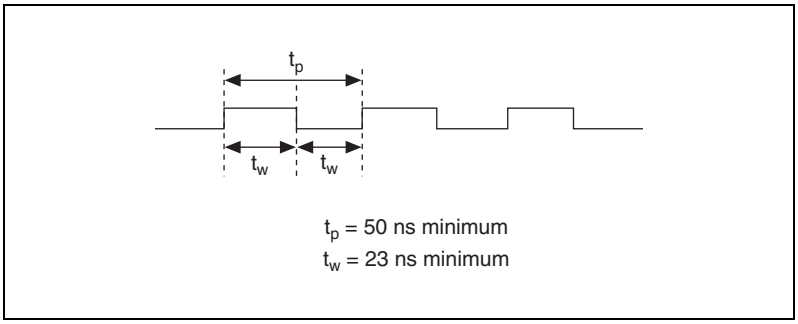



**Figure 3-11.** ao/SampleClockTimebase Signal Timing Requirements

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency.

Unless you select an external source, either the 20MHzTimebase or 100kHzTimebase generates the ao/SampleClockTimebase signal.

## Master Timebase Signal

The Master Timebase (MasterTimebase) signal, or Onboard Clock, is the timebase from which all other internally generated clocks and timebases on the board are derived. It controls the timing for the analog input, analog output, and counter subsystems. It is available as an output on the I/O connector, but you must use one or more counters to do so.

The maximum allowed frequency for the MasterTimebase is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The two possible sources for the MasterTimebase signal are the internal 20MHzTimebase signal or an external signal through RTSI 7. Typically the 20MHzTimebase signal is used as the MasterTimebase unless you wish to synchronize multiple devices, in which case, you should use RTSI 7. Refer to Chapter 8, *Real-Time System Integration Bus (RTSI)*, for more information about which signals are available through RTSI.

Figure 3-12 shows the timing requirements for MasterTimebase.

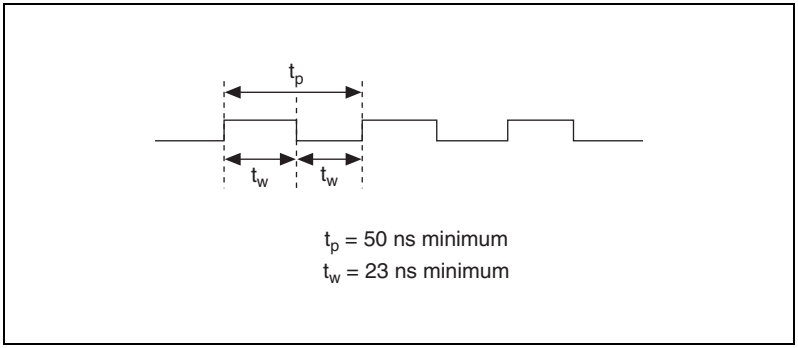



**Figure 3-12.** MasterTimebase Timing Requirements

# Getting Started with AO Applications in Software

You can use the E Series device in the following analog output applications:

- Single-Point Generation
- Finite Generation
- Continuous Generation
- Waveform Generation

You can perform these generations through DMA, interrupt, or programmed I/O data transfer mechanisms. Some of the applications also use start triggers and pause triggers.

**Note** For more information about programming analog output applications and triggers in software, refer to the *NI-DAQmx Help* or the *LabVIEW 8.x Help*.

# 4

# Digital I/O

Figure 4-1 shows the DIO circuitry of the E Series device.

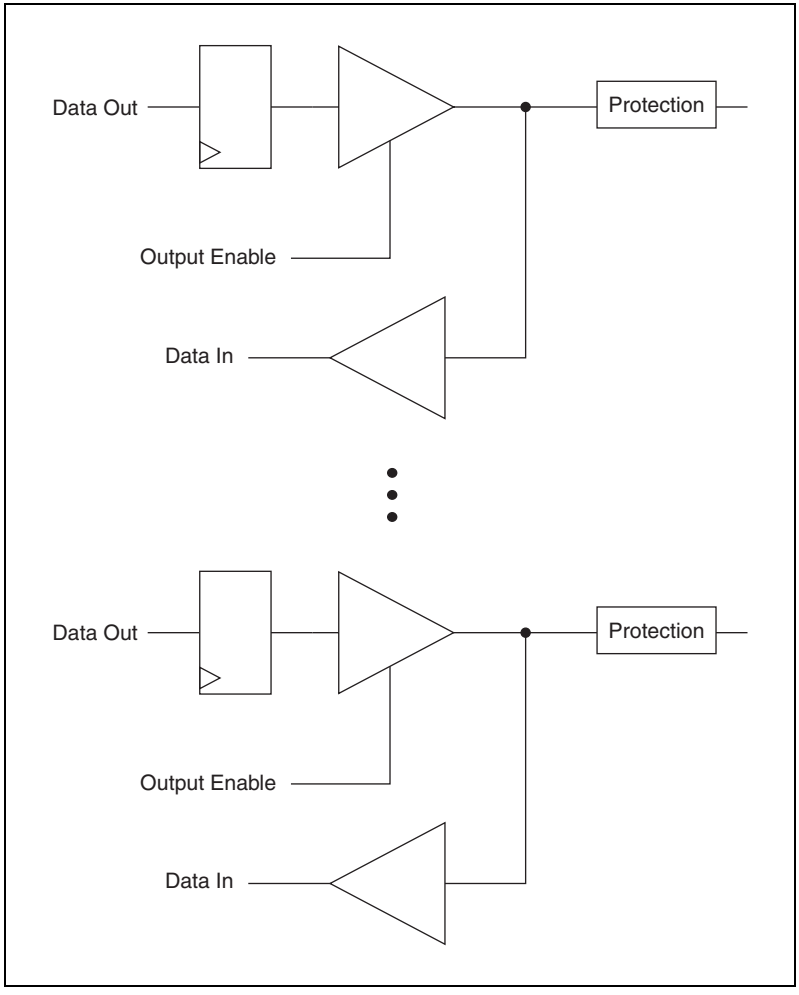



**Figure 4-1.** DIO Circuitry Block Diagram

E Series devices contain eight lines of DIO (P0.<0..7>) for general-purpose use. You can individually configure each line with software for either input

or output. At system startup and reset, the DIO ports are all high-impedance.

The hardware up/down control for general-purpose Counters 0 and 1 are connected onboard to P0.6 and P0.7, respectively. Thus, you can use P0.6 and P0.7 to control the general-purpose counters. The up/down control signals, Counter 0 Up/Down and Counter 1 Up/Down, are input-only and do not affect the operation of the DIO lines. Refer to Chapter 5, *Counters*, for more information on counters.

**(NI 6016 and NI 6025E Devices Only)** The NI 6016 and NI 6025E use an 82C55A programmable peripheral interface to provide additional lines of digital I/O that represent three 8-bit ports. Refer to the *Extended Digital I/O* section for more information.

# Extended Digital I/O

**(NI 6016 and NI 6025E Devices Only)** The NI 6016 and NI 6025E use an 82C55A programmable peripheral interface (PPI) to provide an additional 24 lines of DIO that represent three 8-bit ports: P1, P2, and P3. The 82C55A has three modes of operation: simple I/O (mode 0), strobed I/O (mode 1), and bidirectional I/O (mode 2). In modes 1 and 2, the three ports are divided into two groups: group A and group B. Each group has eight data bits, plus control and status bits from Port 3 (P3). Modes 1 and 2 use handshaking signals from the computer to synchronize data transfers. NI-DAQmx does not currently support mode 2.

The Example Finder contains examples for programming the 82C55A in both Traditional NI-DAQ (Legacy) and NI-DAQmx. To locate the examples, use the keywords `8255` or `handshaking`.

## Port 3 Signal Assignments

**(NI 6016 and NI 6025E Devices Only)** The signals assigned to port 3 depend on how the 82C55A is configured. In mode 0, or no handshaking configuration, port 3 is configured as two 4-bit I/O ports. In modes 1 and 2, or handshaking configuration, port 3 is used for status and handshaking signals with any leftover lines available for general-purpose I/O. Table 4-1 summarizes the port 3 signal assignments for each configuration. You can also use ports 1 and 2 in different modes; Table 4-1 does not show every possible combination.



**Note** Table 4-1 shows both the port 3 signal assignments and the terminology correlation between different documentation sources. The 82C55A terminology refers to the different

82C55A configurations as modes, whereas NI-DAQ, LabWindows/CVI, and LabVIEW documentation refers to them as handshaking and no handshaking.

**Table 4-1.** Configuration Terminology and Signal Assignments

| Configuration Terminology | | Signal Assignments | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **NI 6016 or NI 6025E** | **National Instruments Software** | **P3.7** | **P3.6** | **P3.5** | **P3.4** | **P3.3** | **P3.2** | **P3.1** | **P3.0** |
| Mode 0 (Basic I/O) | No Handshaking | I/O | I/O | I/O | I/O | I/O | I/O | I/O | I/O |
| Mode 1 (Strobed Input) | Handshaking | I/O | I/O | IBF[1] | STB*[1] | INTR[1] | STB*[2] | IBFB[2] | INTR[2] |
| Mode 1 (Strobed Output) | Handshaking | OBF*[1] | ACK*[1] | I/O | I/O | INTR[1] | ACK*[2] | OBF*[2] | INTR[2] |
| Mode 2 (Bidirectional Bus) | Handshaking | OBF*[1] | ACK*[1] | IBF[1] | STB*[1] | INTR[1] | I/O | I/O | I/O |

* Indicates that the signal is active low.

[1] Denotes port 1 handshaking signals.

[2] Denotes port 2 handshaking signals.

# Power-On State

**(NI 6016 and NI 6025E Devices Only)** The NI 6016 and NI 6025E contain bias resistors that control the state of the DIO lines, P1.<0..7>, P2.<0..7>, P3.<0..7>. At power-on, each DIO line is configured as an input and pulled high.

You can change the power-on state of individual lines from pulled high to pulled low by adding your own external resistors.

## Changing DIO Power-On State to Pulled Low

Each DIO line is pulled to $V_{cc}$ (approximately +5 VDC) with a 100 kΩ resistor. To pull a specific line low, add a pull-down resistor ($R_L$) between the line and ground so the maximum value on the line is 0.4 VDC. The DIO lines provide a maximum of 2.5 mA at 3.7 V in the high state. Using the largest possible resistor ensures that you do not use more current than necessary to perform the pull-down task.

Ensure the value of the resistor is not so large that leakage current from the DIO line, along with the current from the 100 kΩ pull-up resistor, drives the

voltage across the pull-down resistor above a TTL-low level of 0.4 VDC. Figure 4-2 shows the DIO configuration for high DIO power-on state.

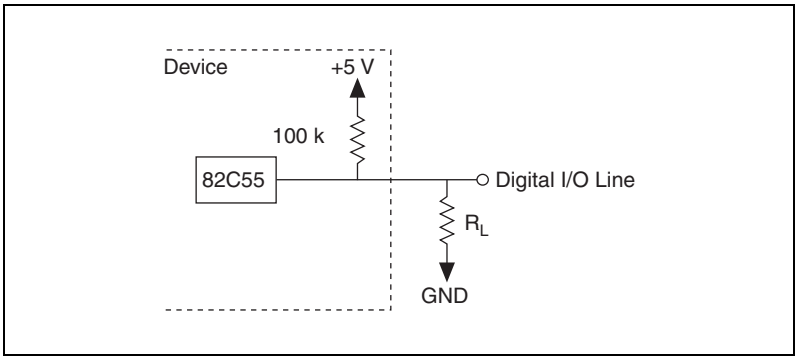



**Figure 4-2.** DIO Configuration for High DIO Power-On State

The following steps show how to calculate the value of $R_L$ needed to achieve a TTL-low power-on state for a single DIO line.

Using the following formula, calculate the largest possible load to maintain a logic low level of 0.4 V and supply the maximum driving current:

$$V = I \times R_L \rightarrow R_L = V/I$$

where:

$$V = 0.4\ V \text{ Voltage across } R_L$$

$I = 46\ \mu A$ (4.6 V across the 100 kΩ pull-up resistor) + 10 µA (10 µA maximum leakage current)

Therefore:

$$R_L = 7.1\ k\Omega\ (0.4\ V/56\ \mu A)$$

This resistor value, 7.1 kΩ, provides a maximum of 0.4 V on the DIO line at power-on. You can substitute smaller resistor values to lower the voltage or to provide a margin for $V_{cc}$ variations and other factors.

## Timing Specifications

**(NI 6016 and NI 6025E Devices Only)** This section lists the timing specifications for handshaking with the P3.<0..7> lines. The handshaking lines STB* and IBF synchronize input transfers. The handshaking lines OBF* and ACK* synchronize output transfers. Table 4-2 describes signals appearing in the handshaking diagrams.

**Table 4-2.** Signal Descriptions

| Name | Type | Description |
|---|---|---|
| STB* | Input | **Strobe input**—A low signal on this handshaking line loads data into the input latch. |
| IBF | Output | **Input buffer full**—A high signal on this handshaking line indicates that data has been loaded into the input latch. A low signal indicates the device is ready for more data. This is an input acknowledge signal. |
| ACK* | Input | **Acknowledge input**—A low signal on this handshaking line indicates that the data written to the port has been accepted. This signal is a response from the external device indicating that it has received the data from your DIO device. |
| OBF* | Output | **Output buffer full**—A low signal on this handshaking line indicates that data has been written to the port. |
| INTR | Output | **Interrupt request**—This signal becomes high when the 82C55A requests service during a data transfer. You must set the appropriate interrupt enable bits to generate this signal. |
| RD* | Internal | **Read**—This signal is the read signal generated from the control lines of the computer I/O expansion bus. |
| WR* | Internal | **Write**—This signal is the write signal generated from the control lines of the computer I/O expansion bus. |
| DATA | Bidirectional | **Data lines at the specified port**—For output mode, this signal indicates the availability of data on the data line. For input mode, this signal indicates when the data on the data lines should be valid. |

# Mode 1 Input Timing

**(NI 6016 and NI 6025E Devices Only)** Figure 4-3 and Table 4-3 show timing specifications for an input transfer in mode 1.

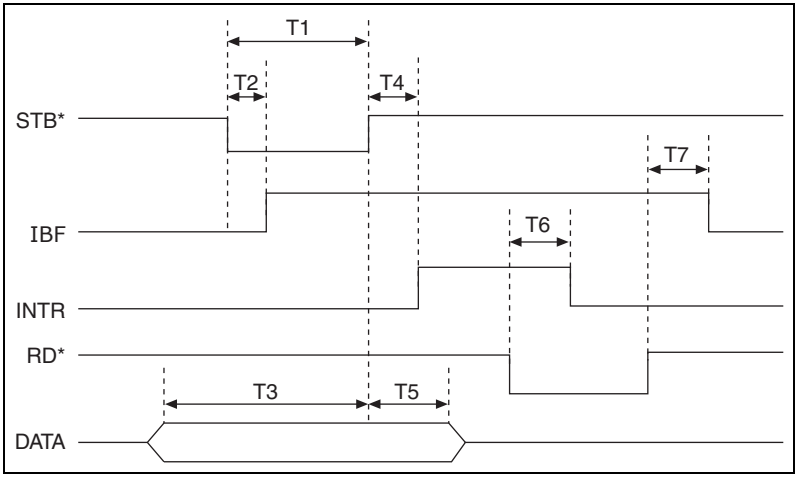



**Figure 4-3.** Input Transfer in Mode 1 Timing Specifications

**Table 4-3.** Input Transfer in Mode 1 Timing Specifications

| Name | Description | Minimum (ns) | Maximum (ns) |
|---|---|---|---|
| T1 | STB* Pulse Width | 100 | — |
| T2 | STB* = 0 to IBF = 1 | — | 150 |
| T3 | Data before STB* = 1 | 20 | — |
| T4 | STB* = 1 to INTR = 1 | — | 150 |
| T5 | Data after STB* = 1 | 50 | — |
| T6 | RD* = 0 to INTR = 0 | — | 200 |
| T7 | STB* Pulse Width | — | 150 |

## Mode 1 Output Timing

**(NI 6016 and NI 6025E Devices Only)** Figure 4-4 and Table 4-4 show timing specifications for an output transfer in mode 1.

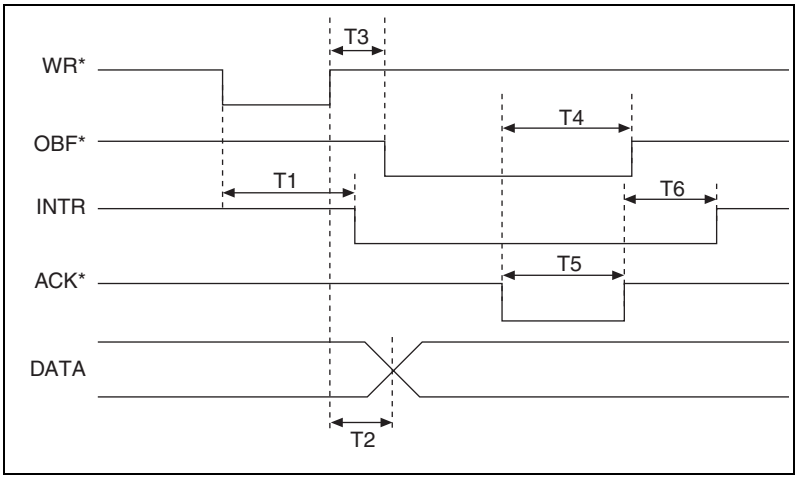



**Figure 4-4.** Output Transfer in Mode 1 Timing Specifications

**Table 4-4.** Output Transfer in Mode 1 Timing Specifications

| Name | Description | Minimum (ns) | Maximum (ns) |
|---|---|---|---|
| T1 | WR* = 0 to INTR = 0 | — | 250 |
| T2 | WR* = 1 to Output | — | 200 |
| T3 | WR* = 1 to OBF* = 0 | — | 150 |
| T4 | ACK* = 0 to OBF* = 1 | — | 150 |
| T5 | ACK* Pulse Width | 100 | — |
| T6 | ACK* = 1 to INTR = 1 | — | 150 |

## Mode 2 Bidirectional Timing

**(NI 6016 and NI 6025E Devices Only)** Figure 4-5 and Table 4-5 show timing specifications for a bidirectional transfer in mode 2.

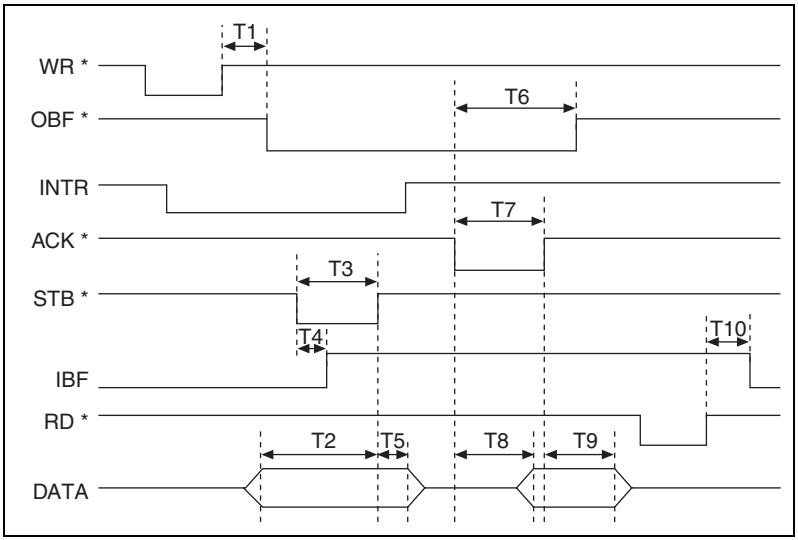



**Figure 4-5.** Bidirectional Transfer Timing Specifications

**Table 4-5.** Bidirectional Transfer Timing Specification

| Name | Description | Minimum (ns) | Maximum (ns) |
|---|---|---|---|
| T1 | WR* = 1 to OBF* = 0 | — | 150 |
| T2 | Data before STB* = 1 | 20 | — |
| T3 | STB* Pulse Width | 100 | — |
| T4 | STB* = 0 to IBF = 1 | — | 150 |
| T5 | Data after STB* = 1 | 50 | — |
| T6 | ACK* = 0 to OBF* = 1 | — | 150 |
| T7 | ACK* Pulse Width | 100 | — |
| T8 | ACK* = 0 to Output | — | 150 |
| T9 | ACK* = 1 to Output Float | 20 | 250 |
| T10 | RD* = 1 to IBF = 0 | — | 150 |

# Power-On States of the PFI and DIO Lines

At system startup and reset, the hardware sets both the PFI and digital lines to high-impedance. This setting means that the device circuitry is not actively driving the output either high or low. However, these lines might have pull-up or pull-down resistors connected to them, as shown in the *I/O Terminal Summary* table in the specifications of each device. These resistors weakly pull the output to either a logic high or logic low state. For example, P0.0 is in the high-impedance state after startup, and the *I/O Terminal Summary* table shows that there is a 50 kΩ pull-up resistor. This pull-up resistor sets the P0.0 pin to a logic high when the output is in a high-impedance state.

**Caution** If you enable a PFI line for output, do *not* connect any external signal source to it. Doing so could damage the device, the computer, and the connected equipment.

# Connecting Digital I/O Signals

All devices have DIO signals P0.<0..7> and D GND. P0.<0..7> are the eight digital lines making up the DIO port, and D GND is the ground-reference signal for the DIO port. You can individually program all lines as inputs or outputs. Figure 4-6 shows P0.<0..3> configured for digital input and P0.<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states such as the state of the switch shown in the Figure 4-6. Digital output applications include sending TTL signals and driving external devices, such as the LED shown in Figure 4-6.

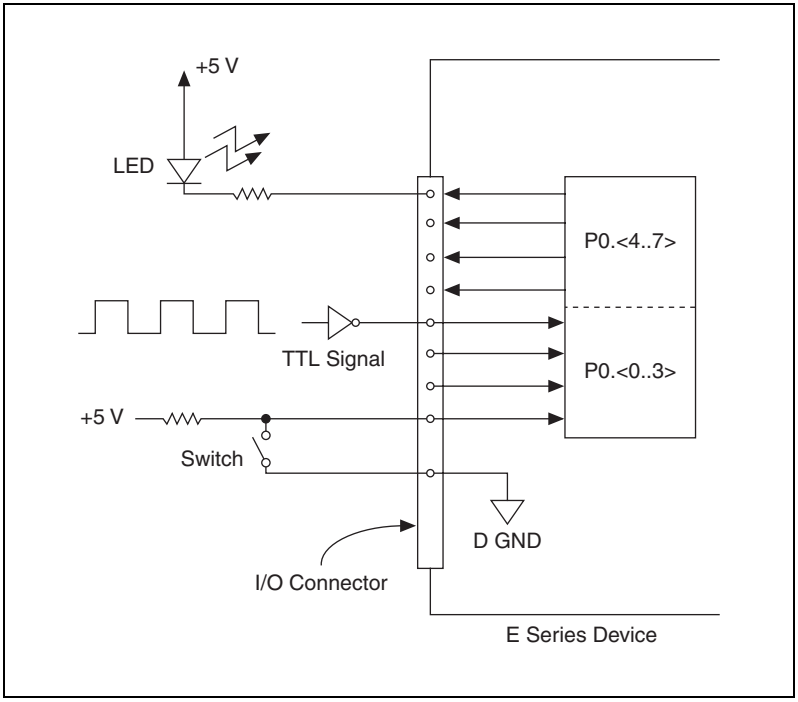



**Figure 4-6.** P0.<0..3> Configured for Digital Input, P0.<4..7> Configured for Digital Output

**Caution** Exceeding the maximum input voltage ratings, which are listed in the *I/O Terminal Summary* table in the specifications document for each E Series family, can damage the DAQ device and the computer. NI is *not* liable for any damage resulting from such signal connections.

# Getting Started with DIO Applications in Software

You can use the E Series device in the following digital I/O applications:

- Static Digital Input
- Static Digital Output
- **(NI 6016 and NI 6025E Devices Only)** Handshaking

**Note** For more information about programming digital I/O applications and triggers in software, refer to the *NI-DAQmx Help* or the *LabVIEW 8.x Help*.

# 5

# Counters

Figure 5-1 shows a counter on the E Series device.

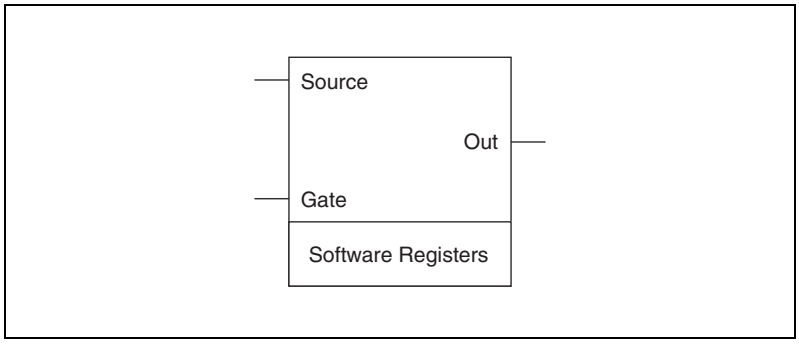



**Figure 5-1.** Counter Block Diagram

Counters 0 and 1 each have two inputs (source and gate), one output, and two software registers, which are used to perform different operations. Counter functionality is built into the *DAQ-STC*.

## Counter Triggering

Counters support two different triggering actions: start and pause. A digital trigger can directly initiate these actions. An analog trigger can indirectly initiate these actions by routing the Analog Comparison Event from a triggered analog input or output task to the counter as a digital trigger.

### Start Trigger

A start trigger begins a finite or continuous pulse generation. Once a continuous generation is initiated, the pulses continue to generate until you stop the operation in software. The specified number of pulses are generated for finite generations unless the retriggerable attribute is used. The retriggerable attribute causes the generation to restart on a subsequent start trigger.

## Pause Trigger

You can use pause triggers in edge counting and continuous pulse generation applications. For edge counting acquisitions, the counter stops counting edges while the external trigger signal is low and resumes when the signal goes high or vice versa. For continuous pulse generations, the counter stops generating pulses while the external trigger signal is low and resumes when the signal goes high or vice versa.

# Counter Timing Signals

Figure 5-2 shows the timing requirements for the gate and source input signals and the timing specifications for the output signals on your device.

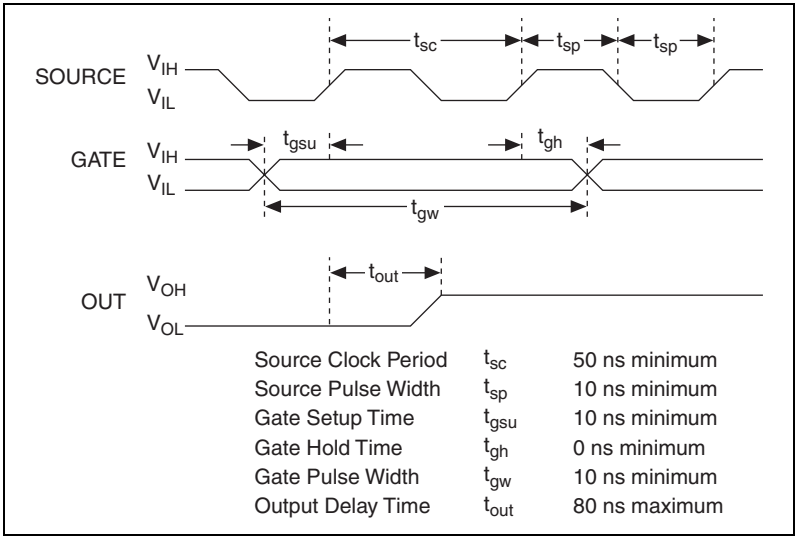



**Figure 5-2.** Counter Timing Signals

The gate and out signal transitions shown above are referenced to the rising edge of the source signal. This timing diagram assumes that the counters are programmed to count rising edges. The same timing diagram, but with the source signal inverted and referenced to the falling edge of the source signal, applies when you program the counter to count falling edges.

The gate input timing parameters are referenced to the signal at the source input or to one of the internally generated signals on your device. Figure 5-2 shows the gate signal referenced to the rising edge of a source signal. The gate must be valid (either high or low) for at least 10 ns before the rising or falling edge of a source signal so the gate can take effect at that

source edge, as shown by $t_{gsu}$ and $t_{gh}$. The gate signal is not required after the active edge of the source signal.

If you use an internal timebase clock, you cannot synchronize the gate signal with the clock. In this case, gates applied close to a source edge take effect either on that source edge or on the next one. This arrangement results in an uncertainty of one source clock period with respect to unsynchronized gating sources.

The output timing parameters are referenced to the signal at the source input or to one of the internally generated clock signals on the device. Figure 5-2 shows the out signal referenced to the rising edge of a source signal. Any out signal state changes occur within 80 ns after the rising or falling edge of the source signal.

For information about the internal routing available on the DAQ-STC counter/timers, refer to *Counter Parts in NI-DAQmx* in the *NI-DAQmx Help or the LabVIEW 8.x Help*.

## Counter 0 Source Signal

You can select any PFI as well as many other internal signals as the Counter 0 Source (Ctr0Source) signal. The Ctr0Source signal is configured in edge-detection mode on either the rising or falling edge. The selected edge of the Ctr0Source signal increments and decrements the counter value depending on the application the counter is performing.

You can export the Ctr0Source signal to the PFI 8/CTR 0 SOURCE pin, even if another PFI is inputting the Ctr0Source signal. This output is set to high-impedance at startup.

Figure 5-3 shows the timing requirements for the Ctr0Source signal.

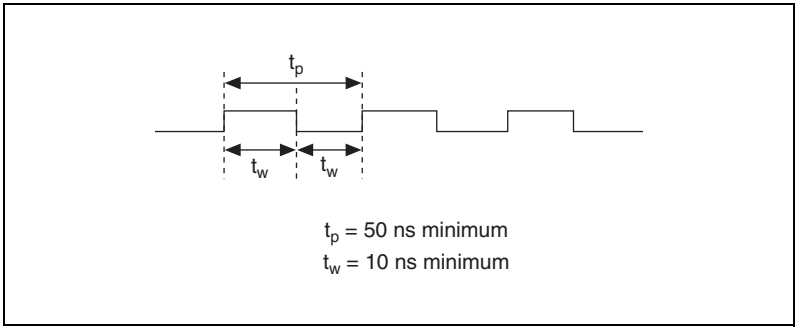



**Figure 5-3.** Ctr0Source Timing Requirements

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency.

For most applications, unless you select an external source, the 20MHzTimebase signal or the 100kHzTimebase signal generates the Ctr0Source signal.

## Counter 0 Gate Signal

You can select any PFI as well as many other internal signals like the Counter 0 Gate (Ctr0Gate) signal. The Ctr0Gate signal is configured in edge-detection or level-detection mode depending on the application performed by the counter. The gate signal can perform many different operations including starting and stopping the counter, generating interrupts, and saving the counter contents.

You can export the gate signal connected to Counter 0 to the PFI 9/CTR 0 GATE pin, even if another PFI is inputting the Ctr0Gate signal. This output is set to high-impedance at startup.

Figure 5-4 shows the timing requirements for the Ctr0Gate signal.

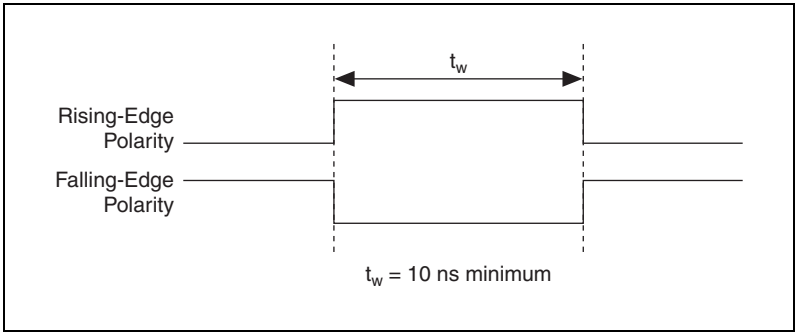



**Figure 5-4.** Ctr0Gate Timing Requirements

## Counter 0 Internal Output Signal

The Counter 0 Internal Output (Ctr0InternalOutput) signal is the output of Counter 0. This signal reflects the terminal count (TC) of Counter 0. The counter generates a terminal count when its count value rolls over. The two software-selectable output options are pulse on TC and toggle output polarity on TC. The output polarity is software-selectable for both options. Figure 5-5 shows the behavior of the Ctr0InternalOutput signal.

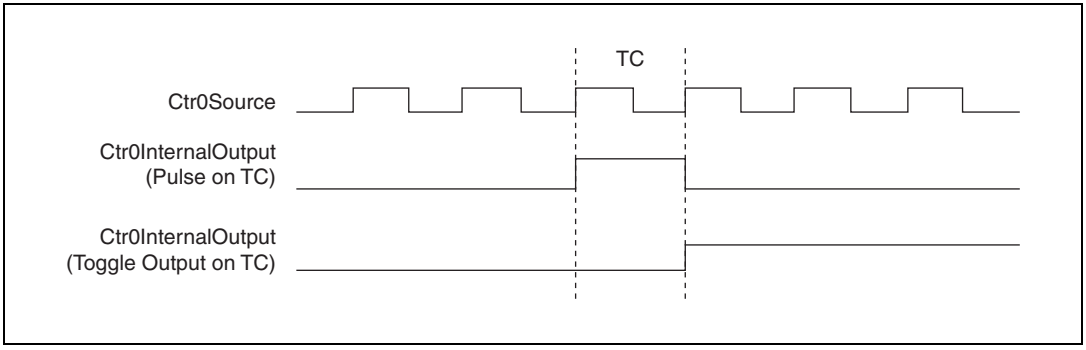



**Figure 5-5.** Ctr0InternalOutput Signal Behavior

You can use Ctr0InternalOutput in the following applications:

- In pulse generation mode, the counter drives Ctr0InternalOutput with the generated pulses. To enable this behavior, software configures the counter to toggle Ctr0InternalOutput on TC.
- Ctr0InternalOutput can control the timing of analog input acquisitions by driving the following signals:
  - ai/SampleClock
  - ai/StartTrigger
  - ai/ConvertClock
- Counter 0 and 1 can be daisy-chained together by routing Ctr0InternalOutput to Ctr1Gate.
- Ctr0InternalOutput can drive any of the RTSI <0..6> signals to control the behavior of other devices in the system.
- Ctr0InternalOutput drives the CTR 0 OUT pin to trigger or control external devices.
- Ctr0InternalOutput can drive other internal signals.

Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW 8.x Help* for more information.

## CTR 0 OUT Pin

When the CTR 0 OUT pin is configured as an output, the Ctr0InternalOutput signal drives the pin. As an input, CTR 0 OUT can drive any of the RTSI <0..6> signals. CTR 0 OUT is set to high-impedance at startup. Figure 5-6 shows the relationship of CTR 0 OUT and Ctr0InternalOutput.

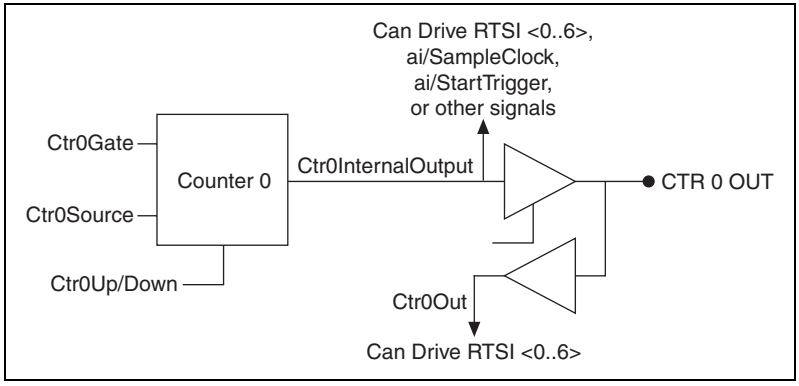



**Figure 5-6.** CTR 0 OUT and Ctr0InternalOutput

## Counter 0 Up/Down Signal

You can externally input this signal on the P0.6 pin, but it is not available as an output on the I/O connector. When you enable externally controlled count direction, Counter 0 counts down when this pin is at a logic low and counts up when it is at a logic high. If you are using an external signal to control the count direction, do not use the P0.6 pin for output. If you do not enable externally controlled count direction, the P0.6 pin is free for general use.

## Counter 1 Source Signal

You can select any PFI as well as many other internal signals as the Counter 1 Source (Ctr1Source) signal. The Ctr1Source signal is configured in edge-detection mode on either rising or falling edge. The selected edge of the Ctr1Source signal increments and decrements the counter value depending on the application the counter is performing.

You can export the Counter 1 signal to the PFI 3/CTR 1 SOURCE pin, even if another PFI is inputting the Ctr1Source signal. This output is set to high-impedance at startup.

Figure 5-7 shows the timing requirements for the Ctr1Source signal.

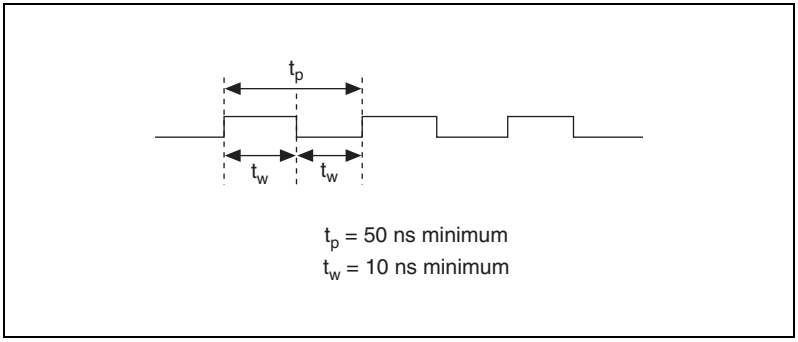



**Figure 5-7.** Ctr1Source Signal Timing Requirements

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency.

For most applications, unless you select an external source, the 20MHzTimebase signal or the 100kHzTimebase signal generates the Ctr1Source signal.

## Counter 1 Gate Signal

You can select any PFI as well as many other internal signals like the Counter 1 Gate (Ctr1Gate) signal. The Ctr1Gate signal is configured in edge-detection or level-detection mode depending on the application performed by the counter. The gate signal can perform many different operations including starting and stopping the counter, generating interrupts, and saving the counter contents.

You can export the gate signal connected to Counter 1 to the PFI 4/CTR 1 GATE pin, even if another PFI is inputting the Ctr1Gate signal. This output is set to high-impedance at startup.

Figure 5-8 shows the timing requirements for the Ctr1Gate signal.

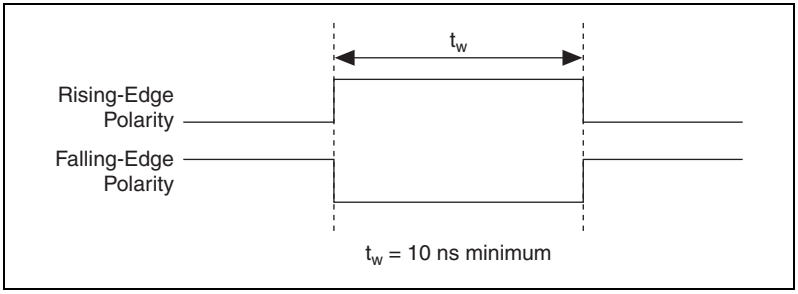



**Figure 5-8.** Ctr1Gate Signal Timing Requirements

## Counter 1 Internal Output Signal

The Counter 1 Internal Output (Ctr1InternalOutput) signal is the output of Counter 1. This signal reflects the terminal count (TC) of Counter 1. The counter generates a terminal count when its count value rolls over. The two software-selectable output options are pulse on TC and toggle output polarity on TC. The output polarity is software-selectable for both options. Figure 5-9 shows the behavior of the Ctr1InternalOutput signal.

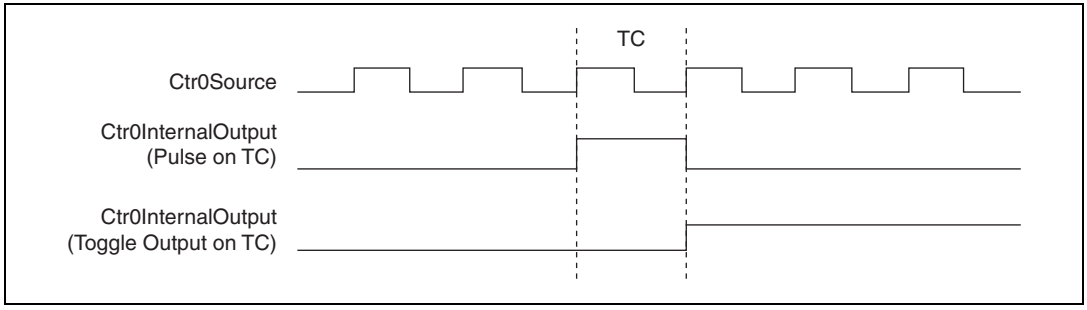



**Figure 5-9.** Ctr1InternalOutput Signal Behavior

You can use Ctr1InternalOutput in the following applications:

- In pulse generation mode, the counter drives Ctr1InternalOutput with the generated pulses. To enable this behavior, software configures the counter to toggle Ctr1InternalOutput on TC.
- Ctr1InternalOutput can control the timing of analog output acquisitions by driving ao/SampleClock.
- Counter 0 and 1 can be daisy-chained together by routing Ctr1InternalOutput to Ctr0Gate.

- Ctr1InternalOutput drives the CTR 1 OUT pin to trigger or control external devices.
- Ctr1InternalOutput can drive other internal signals.

Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW 8.x Help* for more information.

## Counter 1 Up/Down Signal

You can externally input this signal on the P0.7 pin, but it is not available as an output on the I/O connector. When you enable externally controlled count direction, Counter 1 counts down when this pin is at a logic low and counts up when it is at a logic high. If you do not enable externally controlled count direction, the P0.7 pin is free for general use.

## Frequency Output Signal

This signal is available only as an output on the FREQ OUT pin. The frequency generator for the device outputs on the Frequency Output signal. The frequency generator is a 4-bit counter that can divide its input clock by the numbers one through 16. The input clock of the frequency generator is software-selectable from the internal 10 MHz and 100 kHz timebases. The output polarity is software-selectable. This output is set to high-impedance at startup.

## Master Timebase Signal

The Master Timebase (MasterTimebase) signal, or Onboard Clock, is the timebase from which all other internally generated clocks and timebases on the board are derived. It controls the timing for the analog input, analog output, and counter subsystems. It is available as an output on the I/O connector, but you must use one or more counters to do so.

The maximum allowed frequency for the MasterTimebase is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The two possible sources for the MasterTimebase signal are the internal 20MHzTimebase signal or an external signal through RTSI 7. Typically the 20MHzTimebase signal is used as the MasterTimebase unless you wish to synchronize multiple devices, in which case, you should use RTSI 7. Refer to Chapter 8, *Real-Time System Integration Bus (RTSI)*, for more information about which signals are available through RTSI.

Figure 5-10 shows the timing requirements for MasterTimebase.

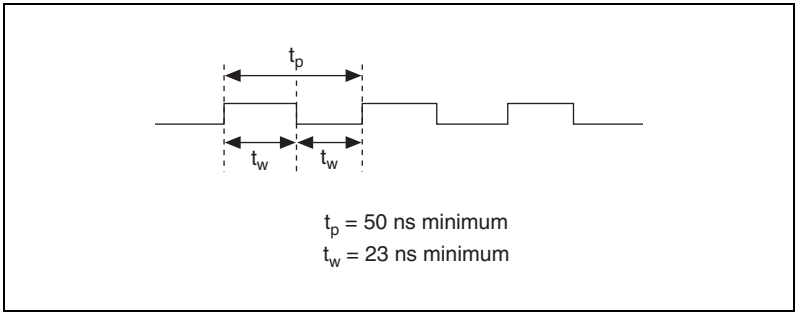



**Figure 5-10.** MasterTimebase Timing Requirements

# Getting Started with Counter Applications in Software

You can use the E Series device in the following counter-based applications.

- Counting Edges
- Frequency Measurement
- Period Measurement
- Pulse Width Measurement
- Semi-Period Measurement
- Pulse Generation

You can perform these measurements through DMA, interrupt, or programmed I/O data transfer mechanisms. The measurements can be finite or continuous in duration. Some of the applications also use start triggers and pause triggers.

**Note** For more information about programming counter applications and triggers in software, refer to the *NI-DAQmx Help* or the *LabVIEW 8.x Help*.

# 6

# Programmable Function Interfaces (PFI)

The 10 Programmable Function Interface (PFI) pins allow timing signals to be routed to and from the I/O connector of a device.

## Inputs

An external timing signal can be input on any PFI pin and multiple timing signals can simultaneously use the same PFI pin. This flexible routing scheme reduces the need to change the physical connections to the I/O connector for different applications. Refer to the *Timing Signal Routing* section of Chapter 7, *Digital Routing*, for more information.

When using the PFI pin as an input, you can individually configure each PFI for edge or level detection and for polarity selection. You can use the polarity selection for any of the timing signals, but the edge or level detection depends upon the particular timing signal being controlled. The detection requirements for each timing signal are listed within the section that discusses that signal.

In edge-detection mode, the minimum pulse width required is 10 ns. This applies for both rising-edge and falling-edge polarity settings. There is no maximum pulse width requirement in edge-detect mode.

In level-detection mode, there are no minimum or maximum pulse width requirements imposed by the PFI signals, but there can be limits imposed by the particular timing signal being controlled.

## Outputs

You can also individually enable each PFI pin to output a specific internal timing signal. For example, if you need the Counter 0 Source signal as an output on the I/O connector, software can turn on the output driver for the PFI 8/CTR 0 SRC pin. This signal, however, cannot be output on any other PFI pin.

Not all timing signals can be output. PFI pins are labeled with the timing signal that can be output on it. For example, PFI 8 is labeled PFI 8/CTR 0 Source. The following timing signals can be output on PFI pins:

- AI Start Trigger Signal
- AI Reference Trigger Signal
- AI Sample Clock Signal
- AI Convert Clock Signal
- AO Start Trigger Signal
- AO Sample Clock Signal
- Counter 0 Source Signal
- Counter 0 Gate Signal
- Counter 1 Source Signal
- Counter 1 Gate Signal

**Caution** Do *not* drive a PFI signal externally when it is configured as an output.

Refer to the *Power-On States of the PFI and DIO Lines* section of Chapter 4, *Digital I/O*, for more information about PFI lines.

# 7

# Digital Routing

The digital routing circuitry manages the flow of data between the bus interface and the acquisition subsystems (analog input circuitry, digital I/O and the counters). The digital routing circuitry uses FIFOs (if present) in each subsystem to ensure efficient data movement.

The digital routing circuitry also routes timing and control signals. The acquisition subsystems use these signals to manage acquisitions. These signals can come from the following:

- Your E Series device
- Other devices in your system through RTSI
- User input through the PFI pins

For a detailed description of which routes are possible on your device, in Measurement & Automation Explorer (MAX), select **Devices and Interfaces**, your device, then select the **Device Routes** tab.

## Timing Signal Routing

The DAQ-STC provides a flexible interface for connecting timing signals to other devices or external circuitry. The E Series devices use the RTSI bus to interconnect timing signals between devices (PCI and PXI buses only) and the PFI pins on the I/O connector to connect the device to external circuitry. These connections enable the device both to control and be controlled by other devices and circuits.

You can control 17 timing signals internal to the DAQ-STC by an external source:

- AI Start Trigger Signal
- AI Reference Trigger Signal
- AI Sample Clock Signal
- AI Convert Clock Signal
- AI Pause Trigger Signal
- AI Sample Clock Timebase Signal

- AO Start Trigger Signal
- AO Sample Clock Signal
- AO Pause Trigger Signal
- AO Sample Clock Timebase Signal
- Counter 0 Source Signal
- Counter 0 Gate Signal
- Counter 0 Up/Down Signal
- Counter 1 Source Signal
- Counter 1 Gate Signal
- Counter 1 Up/Down Signal
- Master Timebase Signal

You also can control these timing signals by signals generated internally to the DAQ-STC, and these selections are fully software-configurable. Figure 7-1 shows an example of the signal routing multiplexer controlling the ai/ConvertClock signal.

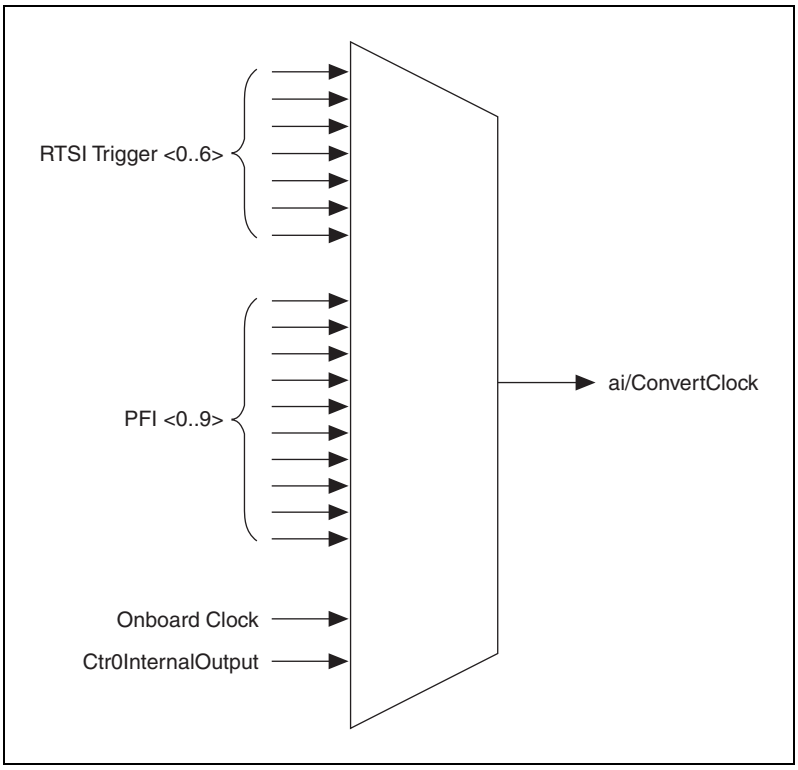



**Figure 7-1.** ai/ConvertClock Signal Routing

Figure 7-1 shows that ai/Convert Clock can be generated from a number of sources, including the external signals RTSI <0..6> (PCI and PXI buses only) and PFI <0..9> and the internal signals, Onboard Clock and Ctr0InternalOutput.

On PCI and PXI devices, many of these timing signals are also available as outputs on the PFI pins.

**Note** The Master Timebase signal can only be accepted as an external signal over RTSI. Refer to the *Device and RTSI Clocks* section of Chapter 8, *Real-Time System Integration Bus (RTSI)*, for information about routing this signal.

# Connecting Timing Signals

**Caution** Exceeding the maximum input voltage ratings, which are listed in the *I/O Terminal Summary* table in the specifications document for each E Series family, can damage the DAQ device and the computer. NI is *not* liable for any damage resulting from such signal connections.

The 10 PFI pins labeled PFI <0..9> route all external control over the timing of the device. These lines serve as connections to virtually all internal timing signals. These PFIs are bidirectional. As outputs they are not programmable and reflect the state of many analog input, waveform generation timing summary and counter timing signals. There are five other dedicated outputs for the remainder of the timing signals. As inputs, the PFI signals are programmable and can control all analog input, waveform generation, and counter timing signals.

All digital timing connections are referenced to D GND. Figure 7-2 shows this reference, and how to connect an external PFI 0 source and an external PFI 2 source to two PFI pins.

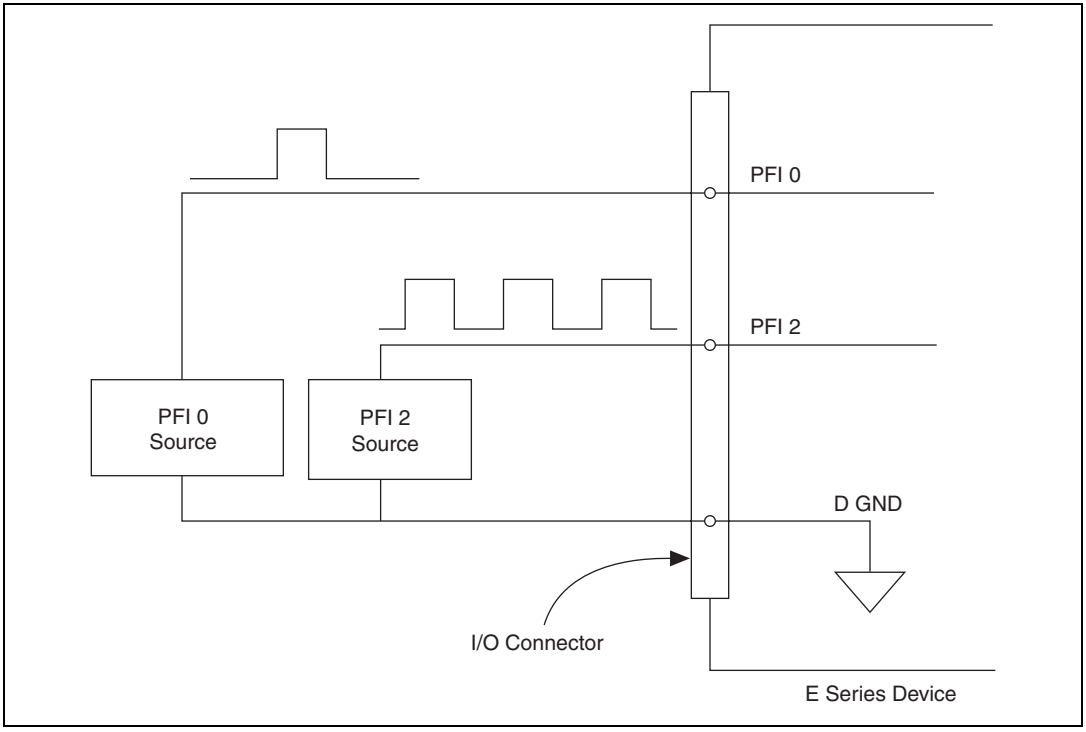



**Figure 7-2.** Connecting Timing Signals

# Routing Signals in Software

Table 7-1 lists the basic functions you can use to route signals.

**Table 7-1.** Functions For Routing Signals.

| Language | Program | Function |
|---|---|---|
| LabVIEW | NI-DAQmx | `DAQmx Export Signal.vi` and `DAQmx Connect Terminals.vi` |
| | Traditional NI-DAQ (Legacy) | `Route Signal.vi` |
| C | NI-DAQmx | `Export_Signal` and `DAQmx_Connect_Terminals` |
| | Traditional NI-DAQ (Legacy) | `Select_Signal` |

**Note** For more information about routing signals in software, refer to the *NI-DAQmx Help* or the *LabVIEW 8.x Help*.

# 8

# Real-Time System Integration Bus (RTSI)

NI-DAQ devices use the Real-Time System Integration (RTSI) bus to easily synchronize several measurement functions to a common trigger or timing event. In a PCI system, the RTSI bus consists of the RTSI bus interface and a ribbon cable. The bus can route timing and trigger signals between several functions on as many as five DAQ devices in the computer. In a PXI system, the RTSI bus consists of the RTSI bus interface and the PXI trigger signals on the PXI backplane. This bus can route timing and trigger signals between several functions on as many as seven DAQ devices in the system. Refer to the KnowledgeBase document, *RTSI Connector Pinout*, for more information.

**Note** DAQCard and DAQPad devices do not use the RTSI bus.

## RTSI Triggers

The seven RTSI trigger lines on the RTSI bus provide a flexible interconnection scheme for any E Series device sharing the RTSI bus. These bidirectional lines can drive or receive any of the timing and triggering signals directly to or from the trigger bus.

### PCI E Series Devices

This signal connection scheme for PCI E Series devices is shown in Figure 8-1.

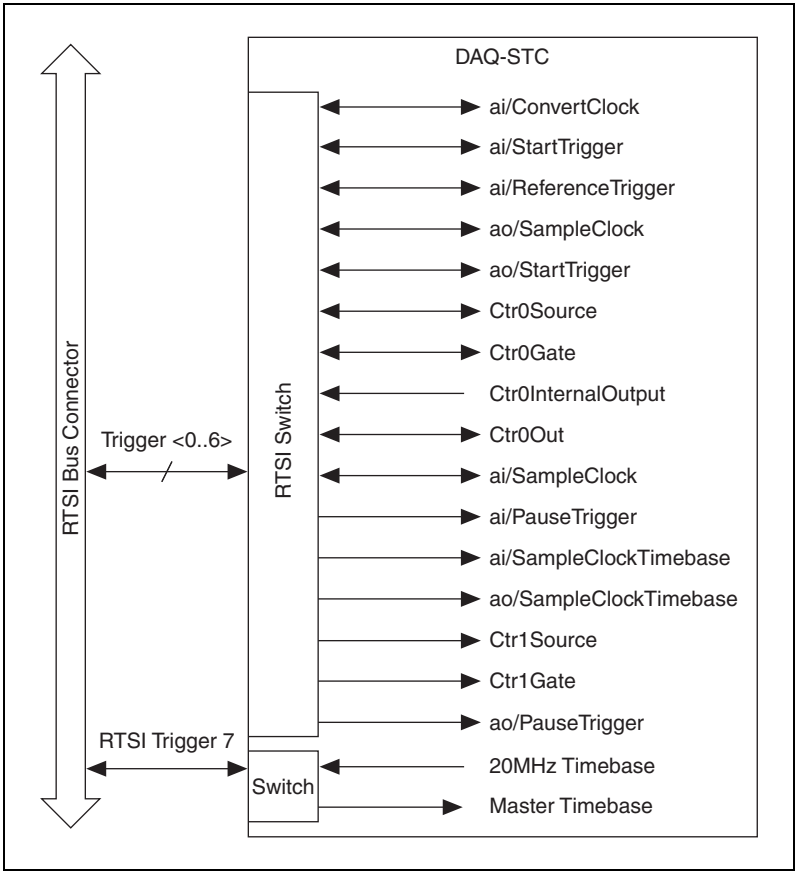



**Figure 8-1.** PCI E Series Signal Connection Scheme

Refer to the *Timing Signal Routing* section of Chapter 7, *Digital Routing*, for a description of the signals shown in Figure 8-1.

**Note** In NI-DAQmx, you can indirectly route timing signals not shown in the above diagrams to RTSI. For a detailed description of which routes are possible on your device, in MAX, select **Devices and Interfaces**, your device, then select the **Device Routes** tab.

## PXI E Series Devices

The RTSI trigger lines connect to other devices through the PXI bus on the PXI backplane. RTSI <0..5> connect to PXI Trigger <0..5>, respectively. This signal connection scheme is shown in Figure 8-2. The RTSI Clock is connected to PXI Trigger 7. In PXI, RTSI 6 connects to the PXI star trigger line, allowing the device to receive triggers from any star trigger controller

plugged into Slot 2 of the chassis. E Series devices can accept timing signals from the PXI star trigger line, but they cannot drive signals onto it. For more information about the star trigger, refer to the *PXI Hardware Specification Revision 2.1*.

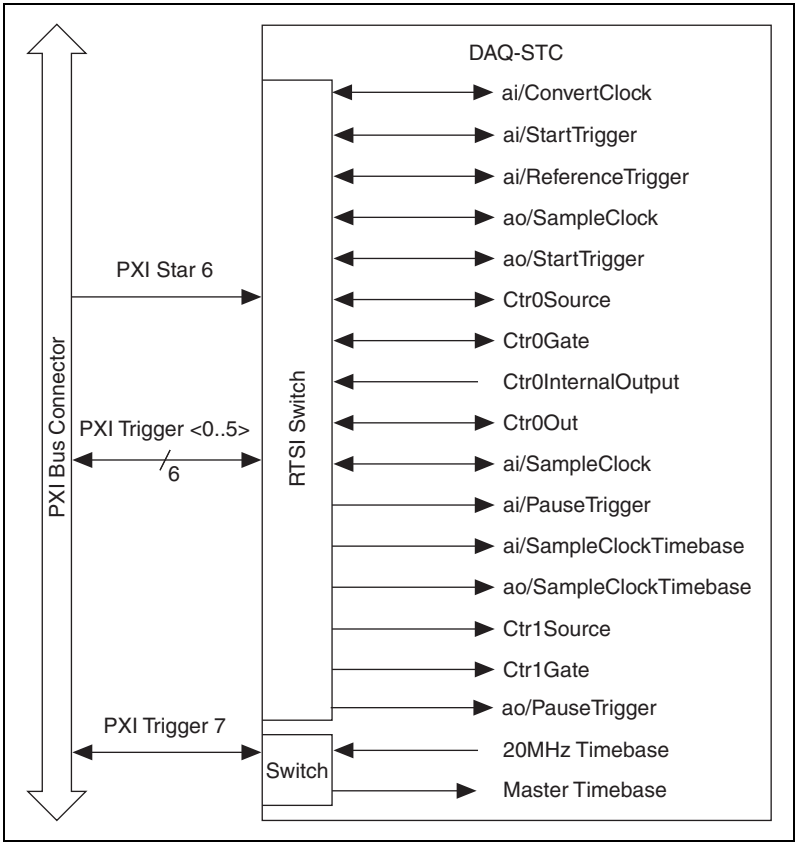



**Figure 8-2.** PXI E Series Signal Connection Scheme

Refer to the *Timing Signal Routing* section of Chapter 7, *Digital Routing*, for a description of the signals shown in Figure 8-2.

**Note** In NI-DAQmx, you can indirectly route timing signals not shown in the above diagrams to RTSI. For a detailed description of which routes are possible on your device, in MAX, select **Devices and Interfaces**, your device, then select the **Device Routes** tab.

# Device and RTSI Clocks

Many E Series device functions require a frequency timebase to generate the necessary timing signals for controlling A/D conversions, DAC updates, or general-purpose signals at the I/O connector. This timebase is also called the Master Timebase or Onboard Clock. Refer to the *Master Timebase Signal* section of Chapter 5, *Counters*, for more information.

Most E Series devices can use either their internal 20 MHz or 100 kHz timebase or a timebase received over the RTSI bus. The timebase can only be routed to or received from RTSI 7, or the RTSI clock. The device directly uses this clock source, whether local or from the RTSI bus, as the primary frequency source. If you configure the device to use the internal timebase, you also can program the device to drive its internal timebase over the RTSI bus to another device that is programmed to receive this timebase signal. The default configuration at startup is to use the internal timebase without driving the RTSI bus timebase signal.

**Note** DAQCard and DAQPad devices do not interface to the RTSI bus.

# Synchronizing Multiple Devices

With the RTSI bus and the routing capabilities of the DAQ-STC, there are several ways to synchronize multiple devices depending on your application. NI recommends that you use a common timebase as the MasterTimebase signal and share any common triggers in the application. One device is designated as the master device and all other devices are designated as slave devices.

The 20MHzTimebase on the master device is the MasterTimebase signal for all devices. The slave devices pull this signal from the master device across the RTSI Trigger 7 line. Slave devices also pull any shared triggers across an available RTSI trigger line from the master device. When you start all of the slave devices before starting the master device, you have successfully synchronized your application across multiple devices.

For more information, refer to *Synchronizing E Series Devices* in the *NI-DAQmx Help* or the *LabVIEW 8.x Help*.

# 9

# Bus Interface

Each E Series device is designed on a complete hardware architecture that is deployed on one of the following platforms:

- PCI
- PXI
- PCMCIA (DAQCard)
- USB (DAQPad)
- IEEE 1394 (DAQPad)

Using NI-DAQ driver software, you have the flexibility to change hardware platforms and operating systems with little or no change to software code.

## MITE and DAQPnP

PCI and PXI E Series devices use the MITE application-specific integrated circuit (ASIC) as a bus master interface to the PCI bus. PCI, PXI, and DAQCard E Series devices are inherently Plug-and-Play (PnP) compatible. On all devices, the operating system automatically assigns the base address of the device. The MITE implements the PCI Local Bus Specification so that the interrupts and base memory addresses are all software-configured.

## Using PXI with CompactPCI

Using PXI-compatible products with standard CompactPCI products is an important feature provided by *PXI Hardware Specification Revision 2.1*. If you use a PXI-compatible plug-in module in a standard CompactPCI chassis, you cannot use PXI-specific functions, but you can still use the basic plug-in device functions. For example, the RTSI bus on a PXI E Series device is available in a PXI chassis, but not in a CompactPCI chassis.

The CompactPCI specification permits vendors to develop sub-buses that coexist with the basic PCI interface on the CompactPCI bus. Compatible operation is not guaranteed between CompactPCI devices with different sub-buses nor between CompactPCI devices with sub-buses and PXI. The

standard implementation for CompactPCI does not include these sub-buses. The PXI E Series device works in any standard CompactPCI chassis adhering to the *PICMG CompactPCI 2.0 R3.0* core specification.

PXI-specific features are implemented on the J2 connector of the CompactPCI bus. The PXI device is compatible with any CompactPCI chassis with a sub-bus that does not drive the lines used by that device. Even if the sub-bus is capable of driving these lines, the PXI device is still compatible as long as those pins on the sub-bus are disabled by default and never enabled.

**Caution** Damage can result if these lines are driven by the sub-bus. NI is *not* liable for any damage resulting from improper signal connections.

# Data Transfer Methods

There are three primary ways to transfer data across the PCI bus: Direct Memory Access (DMA), interrupt request (IRQ), and programmed I/O.

## Direct Memory Access (DMA)

DMA is a method to transfer data between the device and computer memory without the involvement of the CPU. This method makes DMA the fastest available data transfer method. National Instruments uses DMA hardware and software technology to achieve high throughput rates and to increase system utilization. DMA is the default method of data transfer for DAQ devices that support it.

**Note** DAQCard devices do not support DMA.

## Interrupt Request (IRQ)

IRQ transfers rely on the CPU to service data transfer requests. The device notifies the CPU when it is ready to transfer data. The data transfer speed is tightly coupled to the rate at which the CPU can service the interrupt requests. If you are using interrupts to acquire data at a rate faster than the rate the CPU can service the interrupts, your systems may start to freeze.

## Programmed I/O

Programmed I/O is a data transfer mechanism where the user program is responsible for transferring data. Each read or write call in the program initiates the transfer of data. Programmed I/O is typically used in software-timed (on demand) operations.

## Changing Data Transfer Methods between DMA and IRQ

There are a limited number of DMA channels per device. Refer to Appendix A, *Device-Specific Information*, for the specifications document for your device. Each operation (for example, AI, AO, and so on) that requires a DMA channel uses that method until all of the DMA channels are used. Once all of the DMA channels are used, you will get an error if you try to run another operation requesting a DMA channel. If appropriate, you can change one of the operations to use interrupts. For NI-DAQmx, use the **Data Transfer Mechanism** property node. For Traditional NI-DAQ (Legacy), use the **Set DAQ Device Information VI** or function.

# 10

# Triggering

A trigger is a signal that causes a device to perform an action, such as starting an acquisition. You can program your DAQ device to generate triggers on the following:

- A software command
- A condition on an external digital signal
- A condition on an external analog signal

You can also program your DAQ device to perform an action in response to a trigger. This action can affect the following:

- Analog input acquisitions
- Analog output generation
- Counter behavior

**Note** Not all E Series devices support analog triggering. Refer to Appendix A, *Device-Specific Information*, for information about the triggering capabilities of your device.

## Triggering with a Digital Source

Your DAQ device can generate a trigger on a digital signal. You must specify a source and an edge. The digital source can be any of the PFI or RTSI <0..6> signals.

The edge can be either the rising edge or falling edge of the digital signal. A rising edge is a transition from a low logic level to a high logic level. A falling edge is a high-to-low transition.

Figure 10-1 shows a falling-edge trigger.

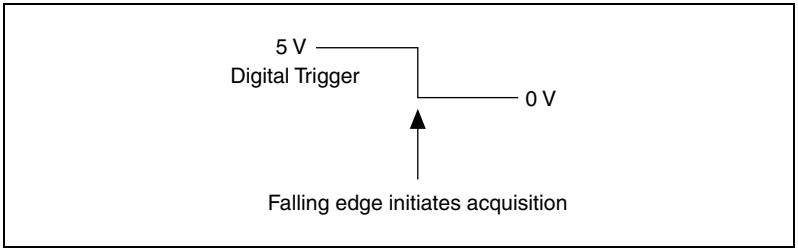



**Figure 10-1.** Falling-Edge Trigger

You can also program your DAQ device to perform an action in response to a trigger from a digital source. This action can affect the following:

- Analog input acquisitions
- Analog output generation
- Counter behavior

# Triggering with an Analog Source

Some E Series devices can generate a trigger on an analog signal. Figure 10-2 shows the analog trigger circuit.

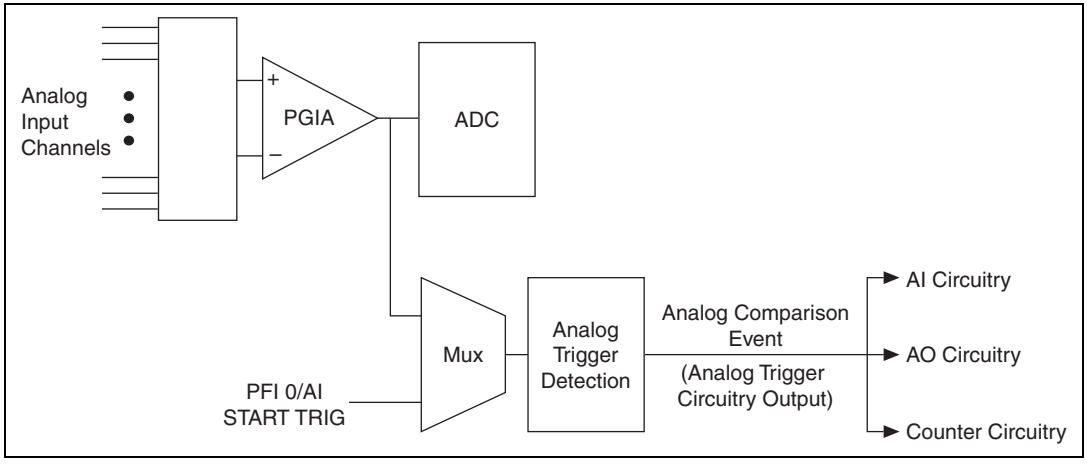



**Figure 10-2.** Analog Trigger Circuit

You must specify a source and an analog trigger type. The source can be either the PFI 0/AI START TRIG pin or an analog input channel. Refer to the *Analog Trigger Types* section for more information.

## PFI 0/AI START TRIG Pin

This pin is an analog input when configured as an analog trigger. Therefore, it is susceptible to crosstalk from adjacent pins, resulting in false triggering when the pin is unconnected. To avoid false triggering, ensure that this pin is connected to a low-impedance signal source (less than 1 kΩ source impedance) if you plan to enable this input using the application software.

## Analog Input Channel

You can select any analog input channel to drive the PGIA. The PGIA amplifies the signal as determined by the input mode and the input polarity and range. The output of the PGIA then drives the analog trigger detection circuit. By using the PGIA, you can trigger on very small voltage changes in the input signal.

When the DAQ device is waiting for an analog trigger with a AI channel as the source, the AI muxes should not route different AI channels to the PGIA. If a different channel is routed to the PGIA, the trigger condition on the desired channel could be missed. The other channels could also generate false triggers.

This behavior places some restrictions on using AI channels as trigger sources. When you use an analog start trigger, the trigger channel must be the first channel in the channel list. When you use an analog reference or pause trigger, and the analog channel is the source of the trigger, there can be only one channel in the channel list. Refer to the *Analog Trigger Accuracy* section for more information.

## Analog Trigger Actions

The output of the Analog Trigger Detection circuit is the Analog Comparison Event signal. In Traditional NI-DAQ (Legacy), this signal is called the Analog Trigger Output Circuitry (ATCOUT). You can program your DAQ device to perform an action in response to the Analog Comparison Event signal. This action can affect the following:

- Analog input acquisitions
- Analog output generation
- Counter behavior

**Note** Refer to the *NI-DAQmx Help* or the *LabVIEW 8.x Help* for more information.

# Analog Trigger Types

You can configure the analog trigger circuitry to different triggering modes. Refer to the *Triggering with an Analog Source* section for more information.

## Level Triggering

You can configure the analog trigger circuitry to detect when the analog signal is below or above a level you specify.

In below-level analog triggering mode, the trigger is generated when the signal value is less than **Level**, as shown in Figure 10-3.

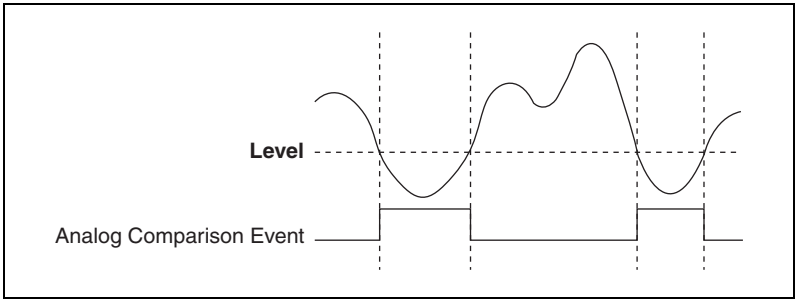



**Figure 10-3.** Below-Level Analog Triggering Mode

In above-level analog triggering mode, the trigger is generated when the signal value is greater than **Level**, as shown in Figure 10-4.

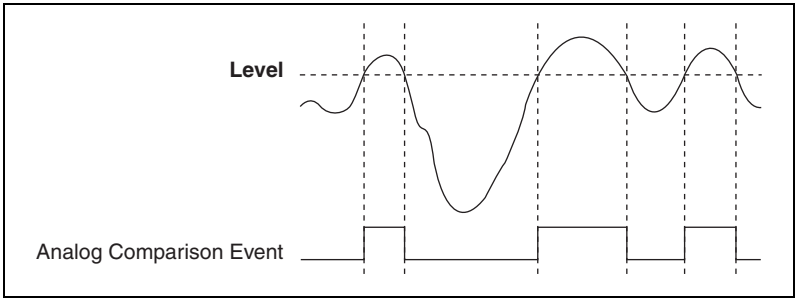



**Figure 10-4.** Above-Level Analog Triggering Mode

## Level Triggering with Hysteresis

Hysteresis adds a programmable window above or below the trigger level that a valid trigger signal must pass through and is often used to reduce false triggering due to noise or jitter in the signal.

When using **Hysteresis** with a rising slope, the trigger asserts when the signal starts below **Level** and then crosses above **Level**. The trigger deasserts when the signal crosses below **Level** minus hysteresis as shown in Figure 10-5.

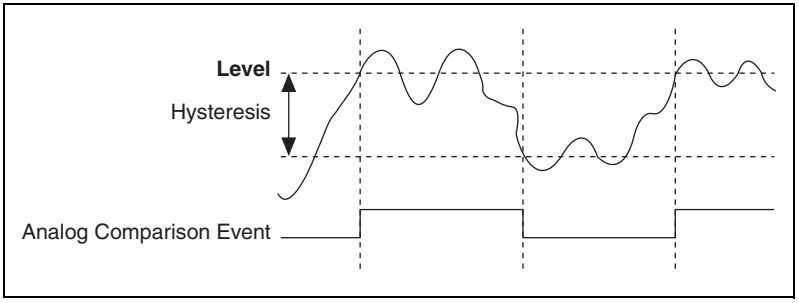



**Figure 10-5.** High Hysteresis

When using **Hysteresis** with a falling slope, the trigger asserts when the signal starts above **Level** and then crosses below **Level**. The trigger deasserts when the signal crosses above **Level** plus hysteresis, as shown in Figure 10-6.

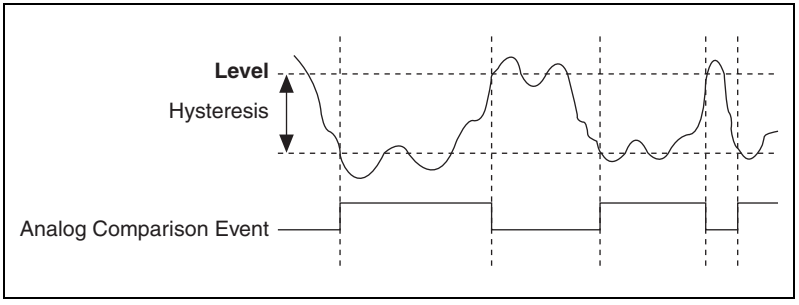



**Figure 10-6.** Low Hysteresis

## Window Triggering

A window trigger occurs when an analog signal either passes into (enters) or passes out of (leaves) a window defined by two voltage levels. Specify the levels by setting the window **Top** value and the window **Bottom** value.

Figure 10-7 demonstrates a trigger that asserts when the signal enters the window.

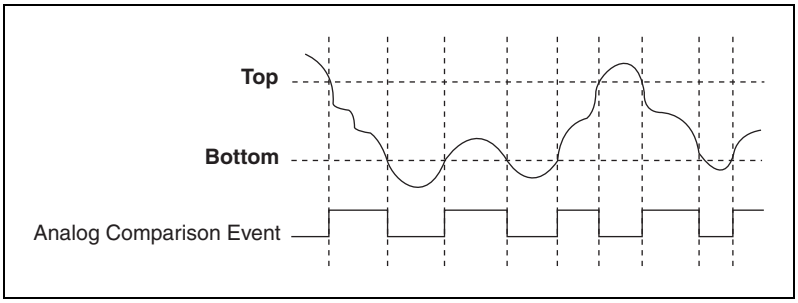



**Figure 10-7.** Window Triggering

# Analog Trigger Accuracy

The analog trigger circuitry compares the voltage of the trigger source to the output of programmable trigger DACs. When you configure the level (or the high and low limits in window trigger mode), the device adjusts the output of the trigger DACs. Refer to the specifications document for your device to find the accuracy and resolution of the analog trigger DACs.

To improve accuracy you can use one of the following methods:

- Use an AI channel (with a small input range) instead of PFI 0/AI START TRIG as your trigger source. The DAQ device does not amplify the PFI 0/AI START TRIG signal. When using an AI channel, the PGIA amplifies the AI channel signal before driving the analog trigger circuitry. If you configure the AI channel to have a small input range, you can trigger on very small voltage changes in the input signal.
- Software-calibrate the analog trigger circuitry. No hardware calibration is provided for the analog trigger circuitry. In addition, the propagation delay from when a valid trigger condition is met to when the analog trigger circuitry emits the Analog Comparison Event may have an impact on your measurements if the trigger signal has a high slew rate. If you find these conditions have a noticeable impact on your measurements, you can perform software calibration on the analog trigger circuitry by configuring your task as normal and applying a known signal for your analog trigger. Comparing the observed results against the expected results, you can calculate the necessary offsets to apply in software to fine-tune the desired triggering behavior.

# A

# Device-Specific Information

This appendix includes device- and family-specific information about the following E Series device families:

- NI 6011E (NI PCI-MIO-16XE-50)
- NI 6013/6014 Family
- NI 6015/6016 Family
- NI 6020E Family
- NI 6023E/6024E/6025E Family
- NI 6030E/6031E/6032E/6033E Family
- NI 6034E/6035E/6036E Family
- NI 6040E Family
- NI 6052E Family
- NI DAQCard-6062E
- NI 6070E/6071E Family

**Note** To obtain documentation for devices not listed here, refer to `ni.com/manuals`.

## NI 6011E (NI PCI-MIO-16XE-50)

The NI 6011E (NI PCI-MIO-16XE-50) is a Plug-and-Play, multifunction analog I/O, DIO, and TIO device for PCI bus computers. The PCI-MIO-16XE-50 features the following:

- 16 AI channels (eight differential) with 16-bit resolution
- Two AO channels with 12-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

Because the PCI-MIO-16XE-50 has no DIP switches, jumpers, or potentiometers, you can easily configure and calibrate it through software.

# NI 6011E (NI PCI-MIO-16XE-50) Dither

You cannot disable dither on the NI 6011E (NI PCI-MIO-16XE-50). The ADC resolution on this device is so fine that the ADC and the PGIA inherently produce almost 0.5 $LSB_{rms}$ of noise. This configuration is equivalent to having a dither circuit that is always enabled.

# NI 6011E (NI PCI-MIO-16XE-50) Block Diagram

Figure A-1 shows a block diagram of the NI 6011E (NI PCI-MIO-16XE-50).

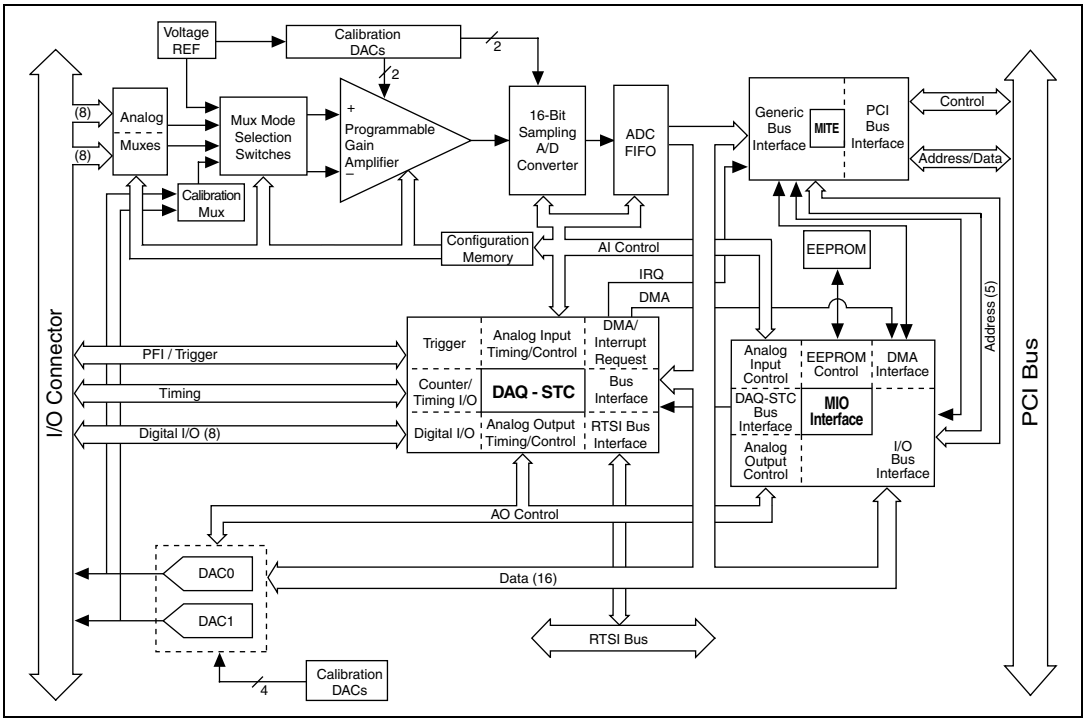



**Figure A-1.** NI 6011E (NI PCI-MIO-16XE-50) Block Diagram

## NI 6011E (NI PCI-MIO-16XE-50) Specifications

Refer to the *NI PCI-MIO-16XE-50 (NI 6011E) Specifications* for more detailed information on the device.

## NI 6011E (NI PCI-MIO-16XE-50) Pinout

Figure A-2 shows the NI 6011E (NI PCI-MIO-16XE-50) device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

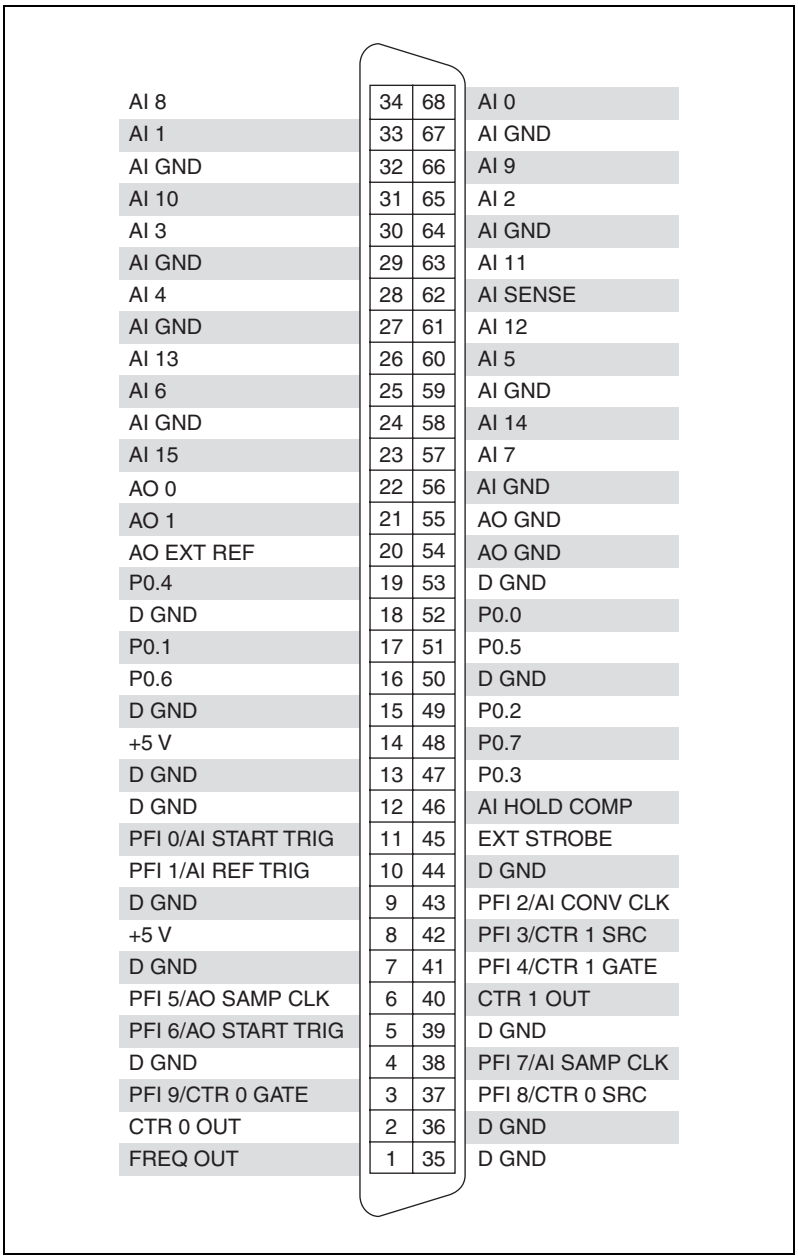



**Figure A-2.** NI 6011E (NI PCI-MIO-16XE-50) Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI 6013/6014 Family

The NI 6013/6014 are basic multifunction AI, AO, DIO, and TIO devices for PCI bus computers.

The NI 6013 features the following:

- 16 AI channels (eight differential) with 16-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

The NI 6014 features the following:

- 16 AI channels (eight differential) with 16-bit resolution
- Two AO channels with 16-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

**Note** The NI 6013/6014 does not support SCXI, RTSI, or referenced single-ended (RSE) AI mode.

# NI 6013/6014 Block Diagram

Figure A-3 shows a block diagram of the NI 6013/6014.

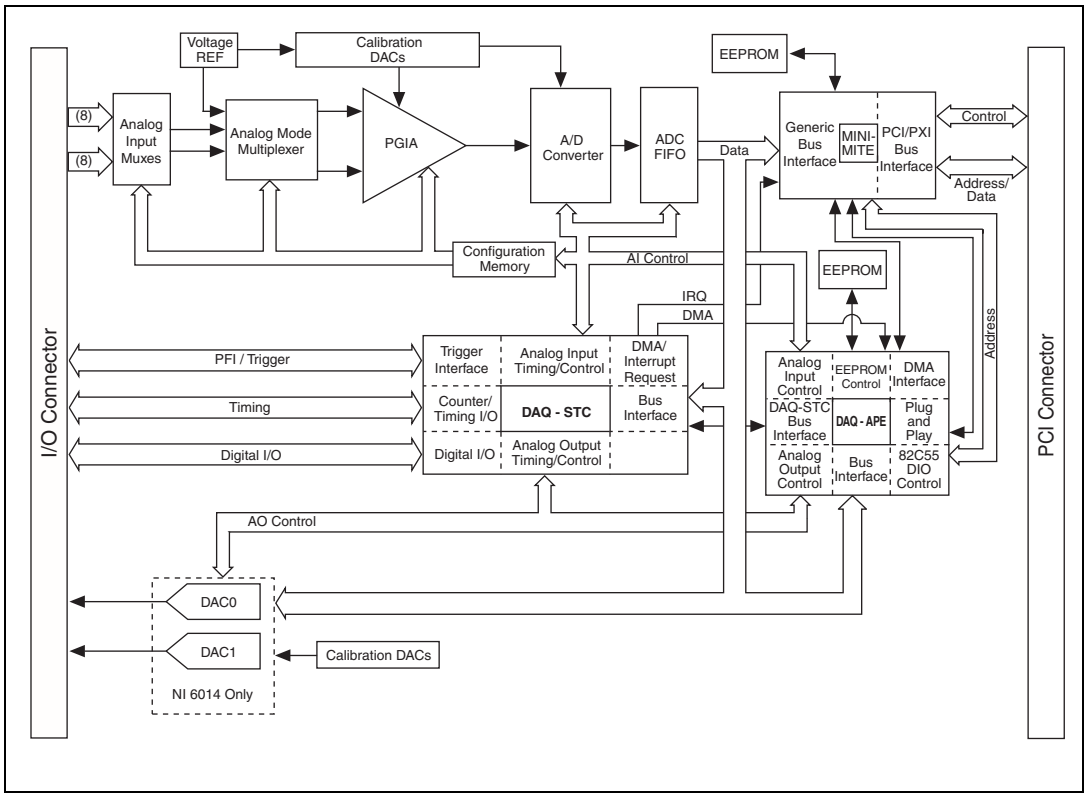



**Figure A-3.** NI 6013/6014 Block Diagram

# NI 6013/6014 Specifications

Refer to the *NI 6013/6014 Family Specifications* for more detailed information on the devices.

# NI 6013 Pinout

Figure A-4 shows the NI 6013 device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

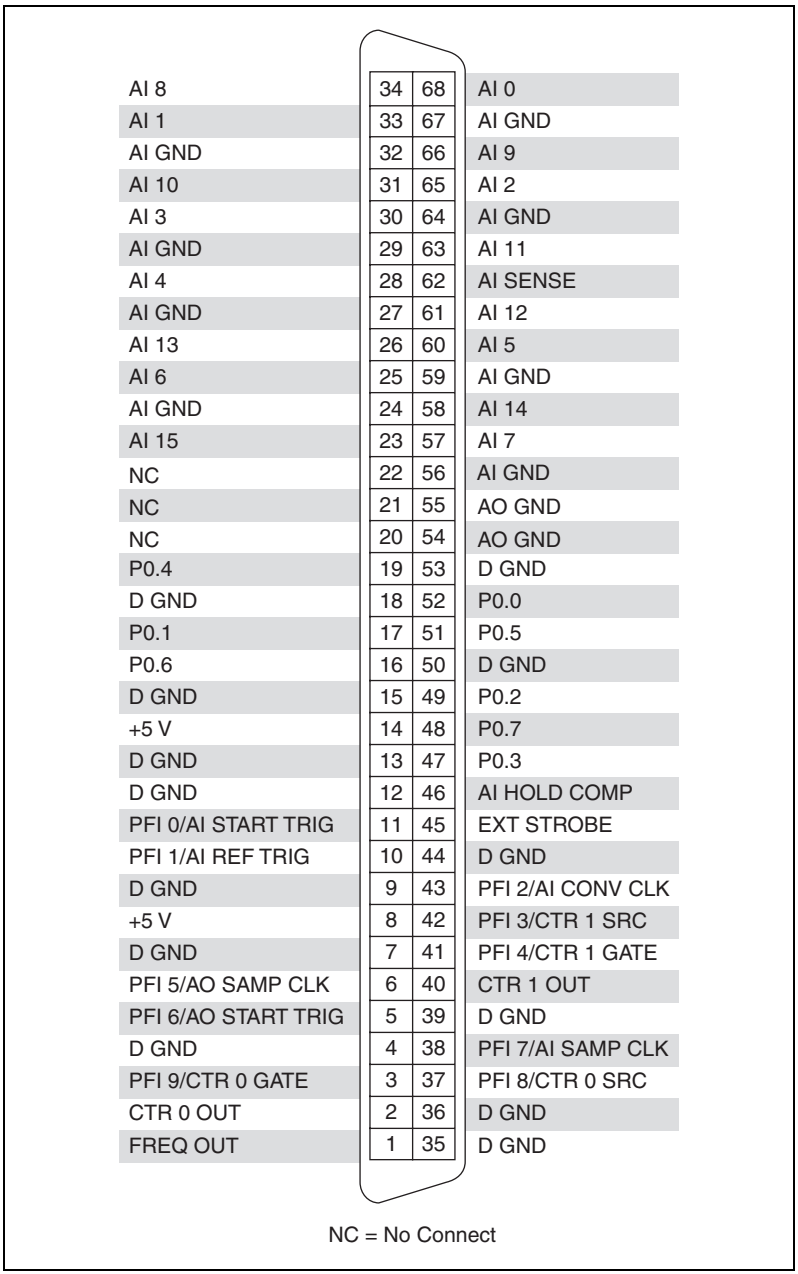



**Figure A-4.** NI 6013 Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI 6014 Pinout

Figure A-5 shows the NI 6014 device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

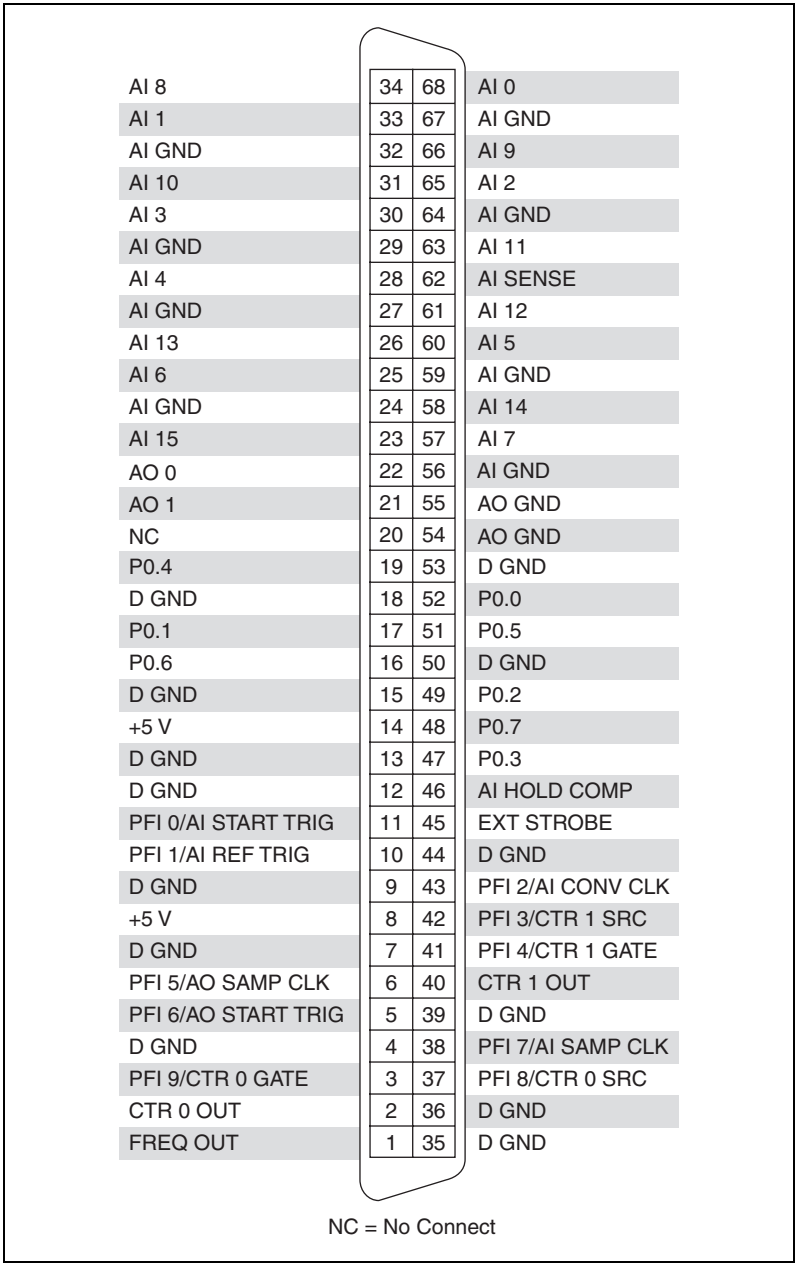



**Figure A-5.** NI 6014 Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI 6015/6016 Family

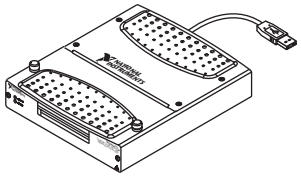
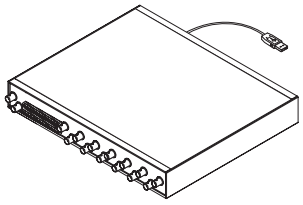
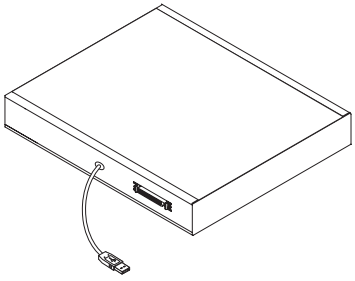
The DAQPad-6015/6016 are Plug-and-Play, USB-compatible multifunction AI, AO, DIO, and TIO devices for USB-compatible computers. The DAQPad-6015/6016 family of devices features the following:

- 16 AI channels (eight differential) with 16-bit resolution
- Two AO channels with 16-bit resolution
- **(DAQPad-6015)** Eight lines of TTL-compatible DIO.
- **(DAQPad-6016)** 32 lines of TTL-compatible DIO.
- Two 24-bit counter/timers for TIO

Because the DAQPad-6015/6016 have no DIP switches, jumpers, or potentiometers, you can easily configure and calibrate them through software.

Table A-1 shows the I/O connectivity and form factors of the DAQPad-6015/6016 devices.

**Table A-1.** NI DAQPad-6015/6016 Versions

| Model | I/O Connector | Form Factor |
|---|---|---|
| DAQPad-6015/6016  | DAQPad-6015:<br>64 screw terminals<br>DAQPad-6016:<br>96 screw terminals<br>Prototyping areas | (8.0 in. × 6.75 in. × 1.4 in.)<br>Stackable<br>Integrated strain relief<br>A removable lid |
| DAQPad-6015 BNC  | Eight AI BNCs<br>Two AO BNCs<br>Four digital BNCs<br>A spring-loaded Combicon connector for other digital signals | (12.1 in. × 10 in. × 1.7 in.)<br>Rack-mountable, stackable |
| DAQPad-6015 mass termination  | 68-pin SCSI-II connector to connect to an SCC system or other accessories | (12.1 in. × 10 in × 1.7 in.)<br>Rack-mountable, stackable |

**Note** The devices in the DAQPad-6015/6016 family do not support SCXI, RTSI, or referenced single-ended (RSE) AI mode.

# DAQPad-6015/6016 Block Diagram

Figure A-6 shows a block diagram of the DAQPad-6015/6016.

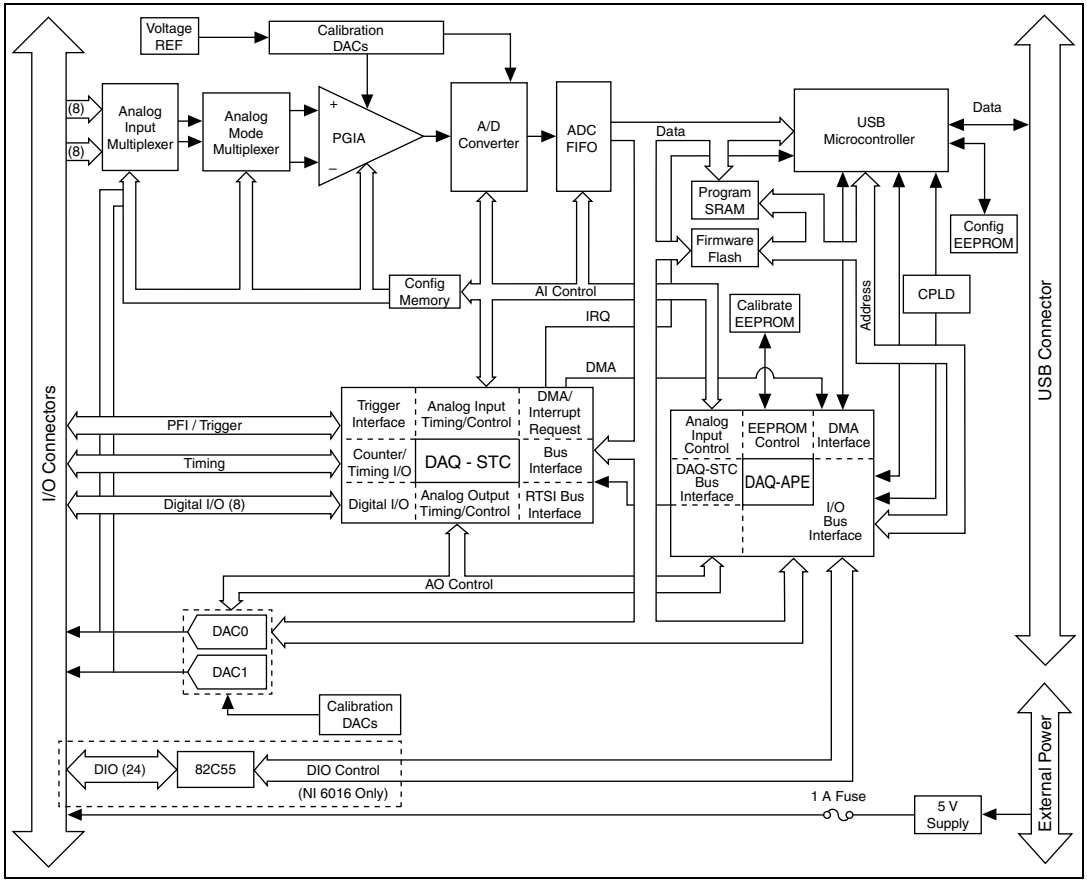



**Figure A-6.** DAQPad-6015/6016 Block Diagram

# Connecting Signals to the NI DAQPad-6015 BNC

## Analog Input

You can use each analog input BNC connector for one differential signal or two single-ended signals.

### Differential Signals

To connect differential signals, determine the type of signal source you are using: a floating signal source or a ground-referenced signal source. Refer to the *Differential Connection Considerations* and *Connecting Analog Input Signals* sections of Chapter 2, *Analog Input*, for more information on connecting analog input signals and differential connection considerations.

To measure a floating signal source, move the switch to the FS position. To measure a ground-referenced signal source, move the switch to the GS position. Figure A-7 shows the source type switch locations on the front panel of the BNC DAQPads.

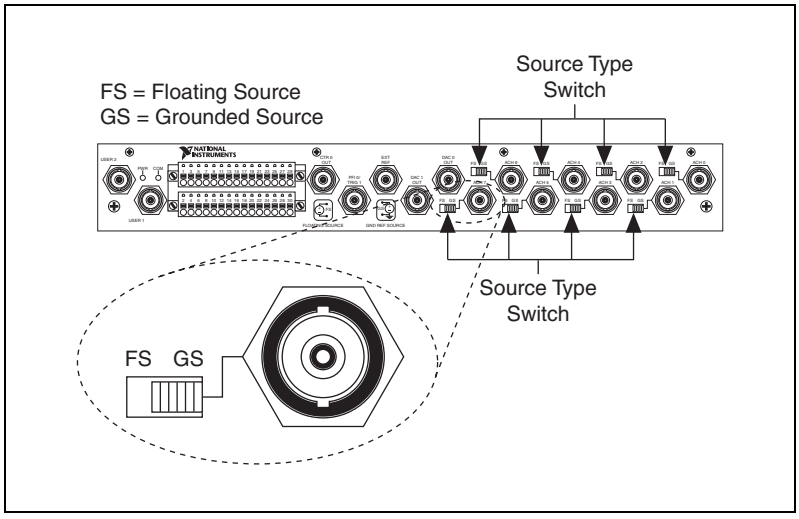



**Figure A-7.** BNC DAQPads Front Panel

Figure A-8 shows the analog input circuitry on BNC DAQPads. When the switch is in the FS position, AI *x* – is grounded through a 0.1 µF capacitor in parallel with a 5 kΩ resistor.

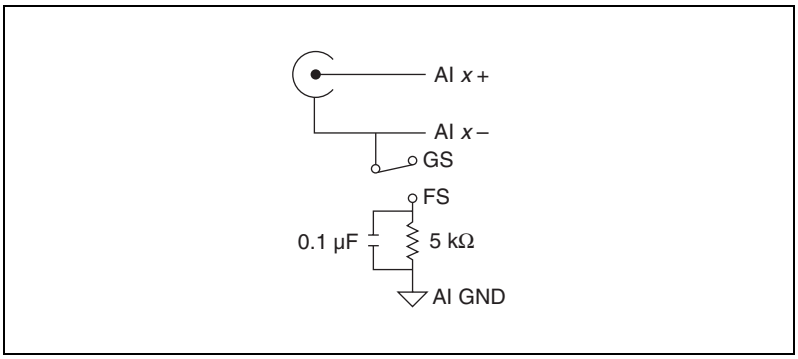



**Figure A-8.** BNC DAQPad Analog Input Circuitry

## Single-Ended Signals

For each BNC connector that you use for two single-ended channels, set the source type switch to the GS position. This setting disconnects the built-in ground reference resistor from the negative terminal of the BNC connector, allowing the connector to be used as a single-ended channel, as shown in Figure A-9.

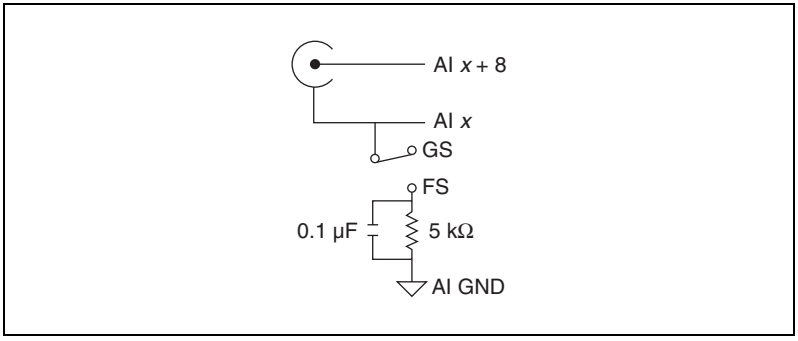



**Figure A-9.** BNC DACPads Single-Ended Connections

When you set the source type to the GS position and software-configure the device for single-ended input, each BNC connector provides access to two single-ended channels, AI *x* and AI *x*+8. For example, the BNC connector labeled AI 0 provides access to single-ended channels AI 0 and AI 8, the BNC connector labeled AI 1 provides access to single-ended channels AI 1 and AI 9, and so on. Up to 16 single-ended channels are available in single-ended measurement modes.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

## Analog Output

You can access analog output signals on the BNC connectors labeled AO 0 and AO 1. Figure A-10 shows the analog output circuitry on BNC DAQPads.

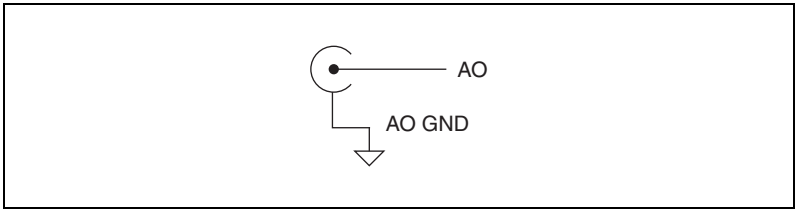



**Figure A-10.** BNC DAQPads Analog Output Circuitry

Refer to the *Connecting Analog Output Signals* section of Chapter 3, *Analog Output*, for more information.

## Counter 0 Out and PFI 0/AI Start Trigger

You can access the Counter 0 Out and PFI 0/AI Start Trigger signals through their respective pins on BNC DAQPads, as shown in Figures A-11 and A-12.

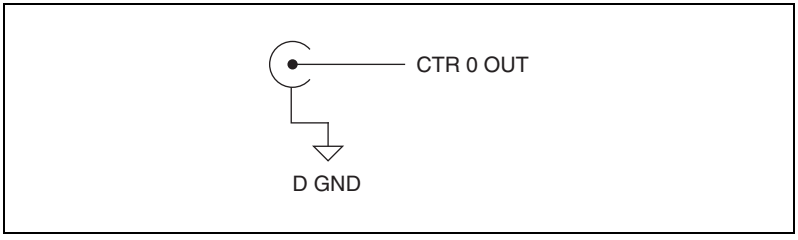



**Figure A-11.** Counter 0 Out

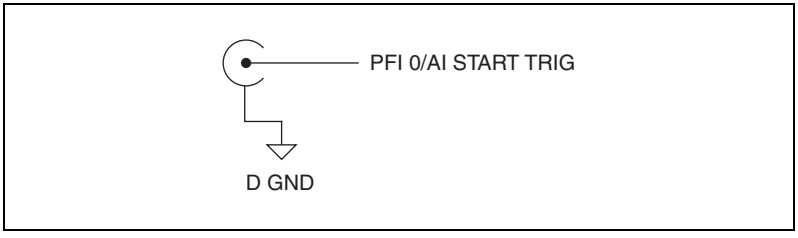



**Figure A-12.** PFI 0/AI Start Trigger

## User <1..2>

The User <1..2> signals connect directly from a screw terminal to a BNC. They allow you to use a BNC connector for a digital or timing I/O signal of your choice. The USER 1 BNC is internally connected to pin 21 and the USER 2 BNC is internally connected to pin 22 on the 30-pin I/O connector. Figure A-13 shows the connection of the User <1..2> BNCs.

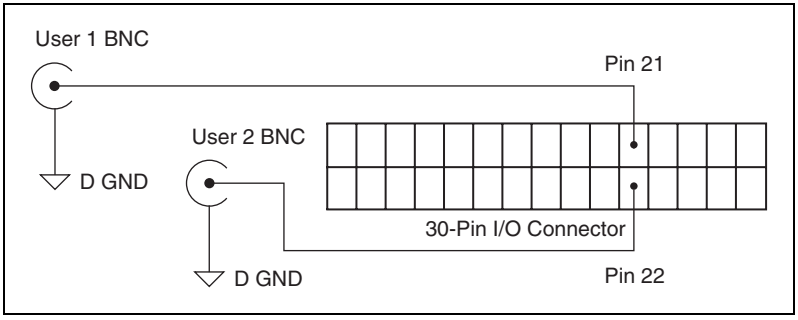



**Figure A-13.** User <1..2> BNC Connection

Figure A-14 shows another example of how to use the User <1..2> BNCs. To access the Ctr1Out signal from a BNC, connect pin 21 (USER 1) to pin 17 (CTR 1 OUT) with a wire.

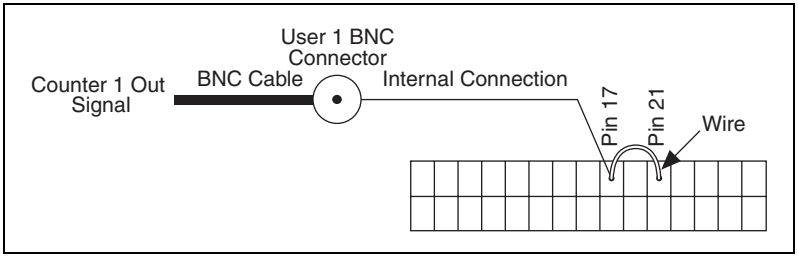



**Figure A-14.** BNC User <1..2> Example

## Other Signals

You can access other signals on BNC DAQPads through a 30-pin Combicon connector.

To connect to one of these signals, use a small screwdriver to press down the orange spring release button at a terminal and insert a wire. Releasing the orange spring release button will lock the wire securely in place.

You can remove the Combicon plugs to assist in connecting wires. Loosening the screws on either side of the two Combicon plugs allows you to detach the Combicon plugs from the BNC DAQPad device, as shown in Figure A-15.

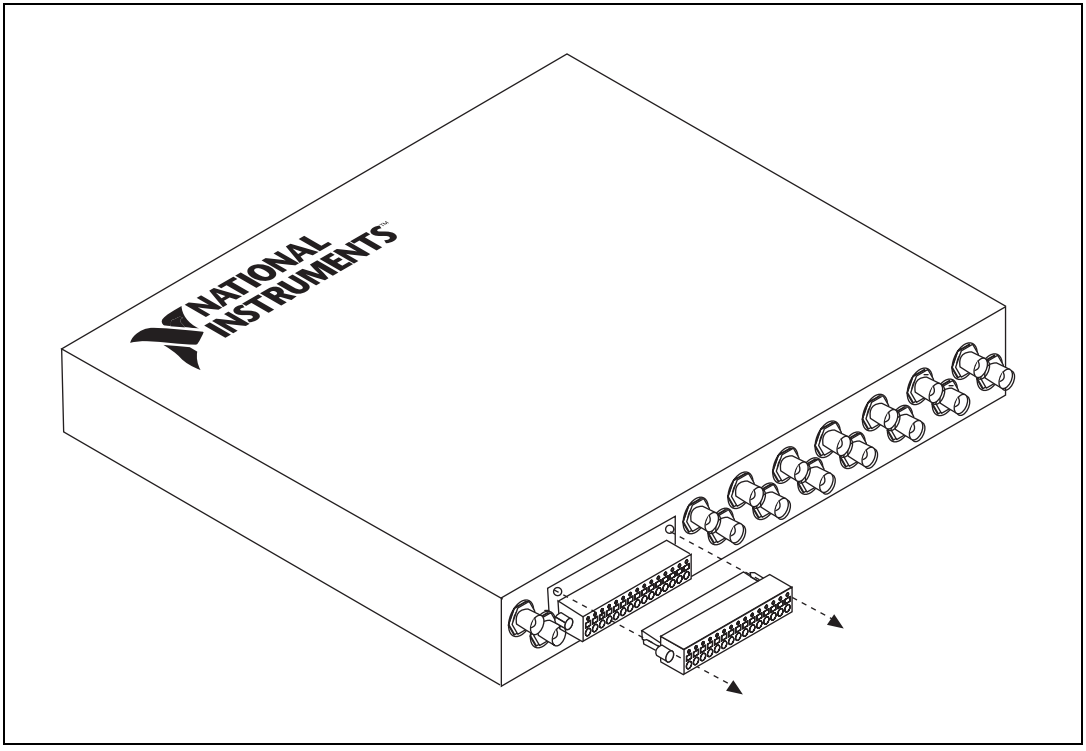



**Figure A-15.** Removing the BNC DAQPad Combicons

## DAQPad-6015/6016 LED Patterns

The DAQPad-6015/6016 devices have two LEDs labeled *ACTIVE* and *READY*. The *ACTIVE* LED indicates activity over the bus. The *READY* LED indicates whether or not the device is configured. The DAQPad-6015 BNC and mass termination devices have a *READY* LED only. Table A-2 shows the behavior of the LEDs.

**Table A-2.** LEDs Behavior

| ACTIVE | READY | DAQPad-6015/6016 State |
|---|---|---|
| Off | Off | The device is not powered. |
| Off | On | The device is configured, but there is no activity over the bus. |
| On | On | The device is configured and there is activity over the bus. |
| Blinking | On | |
| Off | Blinking | The device is not configured and there is no activity over the bus. |
| On | Blinking | The device is not configured, but there is activity over the bus. |
| Blinking | Blinking | |
| Blinking simultaneously | | Both LEDs blinking in the same pattern simultaneously indicates an error state. You must power off and power on your device. |
| Blinking alternately | | If both LEDs blink in the same pattern alternately, contact National Instruments. |

## Replacing the DAQPad-6015/6016 Fuse

The DAQPad-6015/6016 devices have a replaceable F 2 A 250 V (5 × 20 mm) fuse. To remove the fuse from the DAQPad-6015/6016, loosen the four flathead Phillips screws that attach the back lid to the enclosure, and remove the lid as shown in Figure A-16. The fuse is located between the power connector and switch near the back of the device.

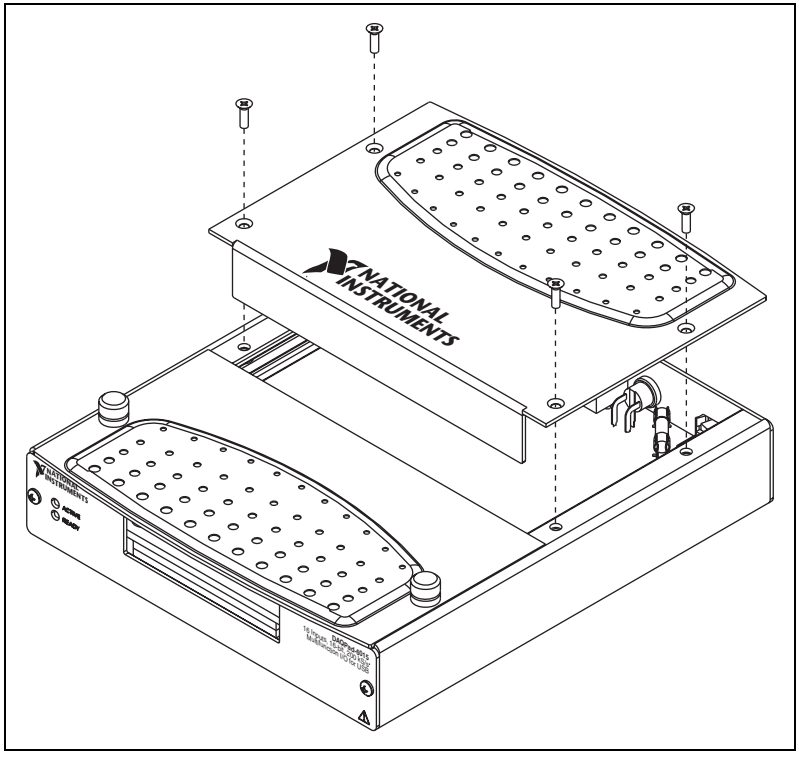



**Figure A-16.** DAQPad-6015/6016 Fuse Removal

To remove the fuse from the DAQPad-6015 BNC or mass termination devices, loosen the eight flathead Phillips screws that attach the lid to the enclosure, and remove the lid. The DAQPad-6015 mass termination device is shown in Figure A-17. The procedure for removing the lid from the DAQPad-6015 BNC is the same.

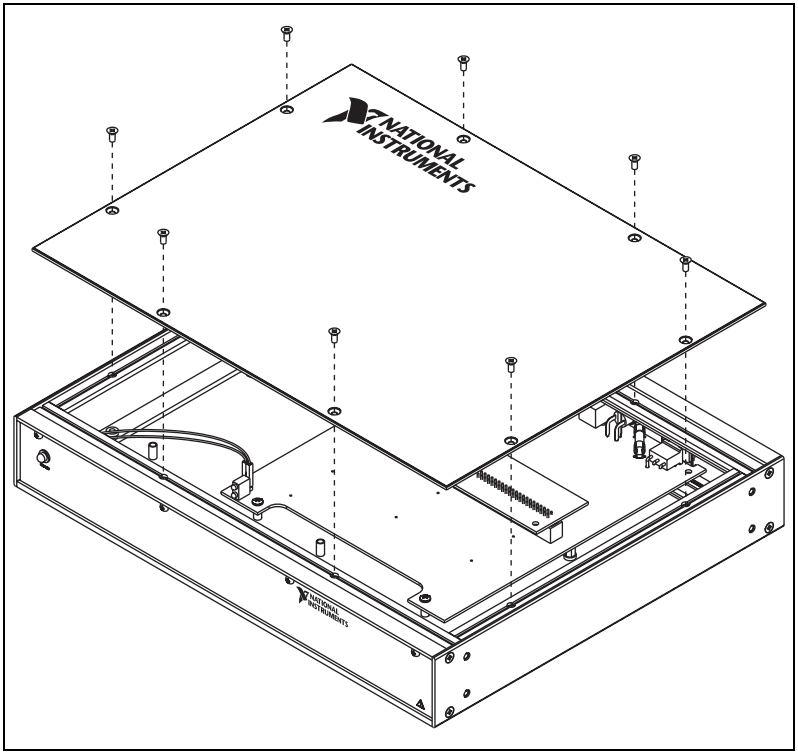



**Figure A-17.** DAQPad-6015 Mass Termination Device

## DAQPad-6015/6016 Specifications

Refer to the *NI DAQPad-6015/6016 Family Specifications* for more detailed information on the devices.

# NI DAQPad-6015 Pinout

Figure A-18 shows the NI DAQPad-6015 device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

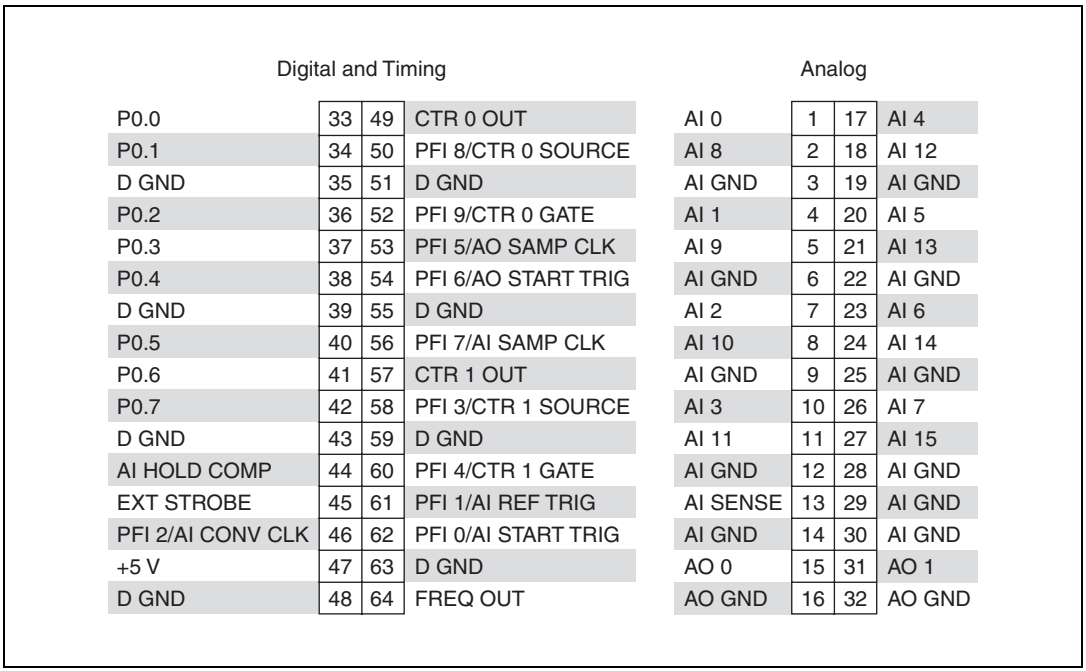



**Figure A-18.** NI DAQPad-6015 Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

## NI DAQPad-6015 BNC Pinout

Figure A-19 shows the NI DAQPad-6015 BNC device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

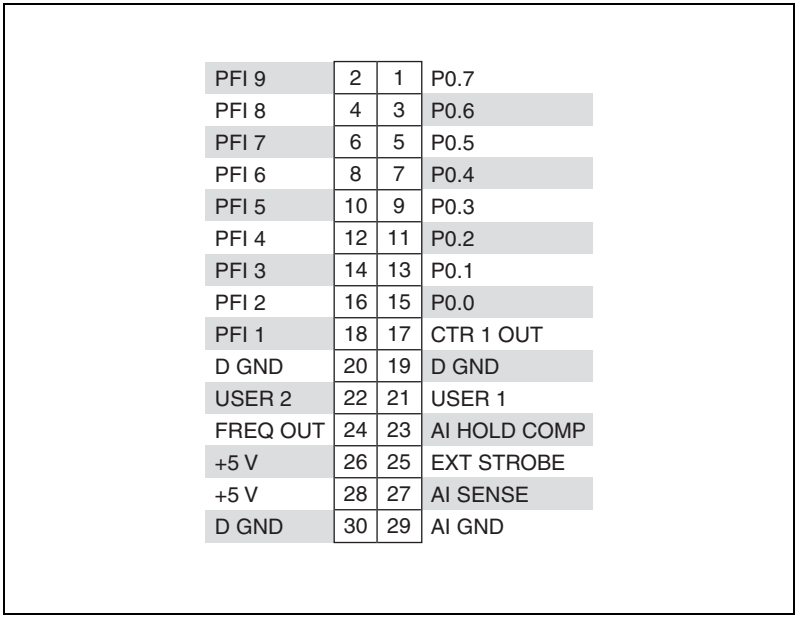



**Figure A-19.** NI DAQPad-6015 BNC Device Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

## NI DAQPad-6015 Mass Termination Pinout

Figure A-20 shows the NI DAQPad-6015 mass termination device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

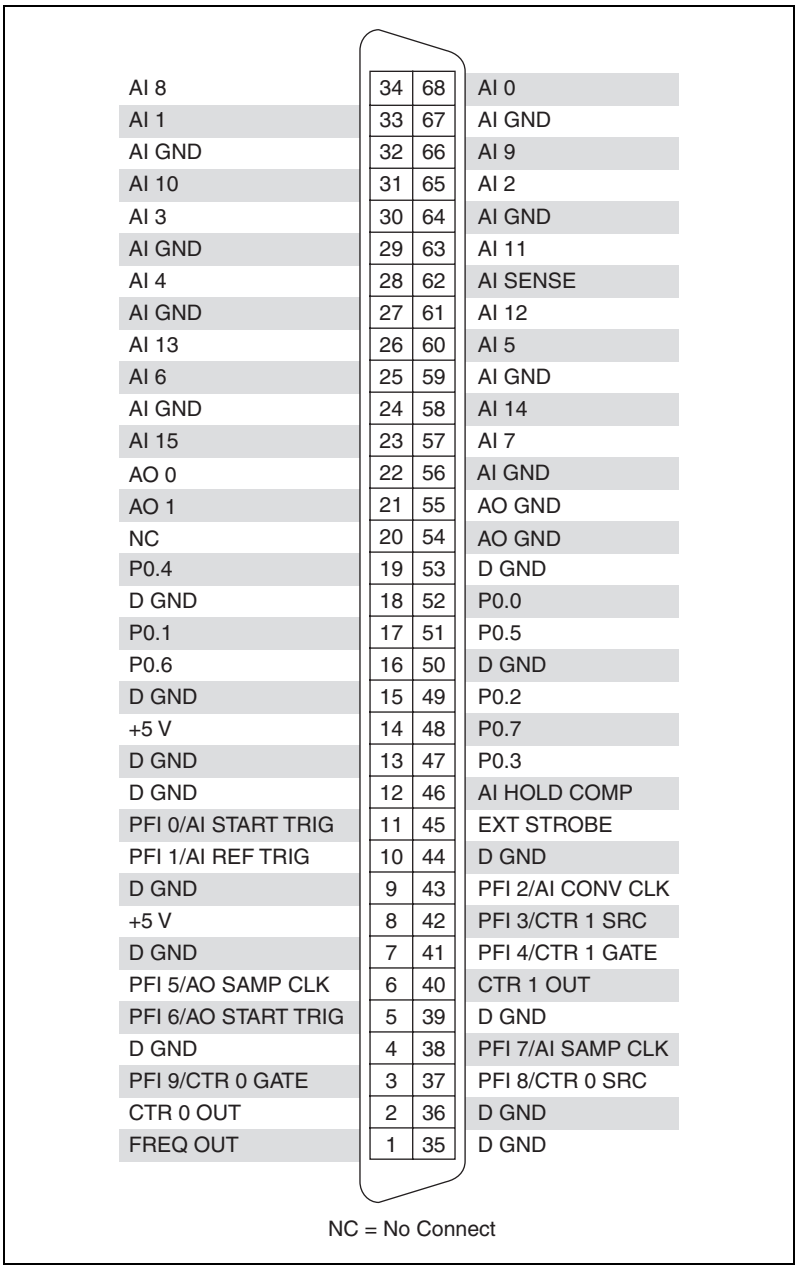


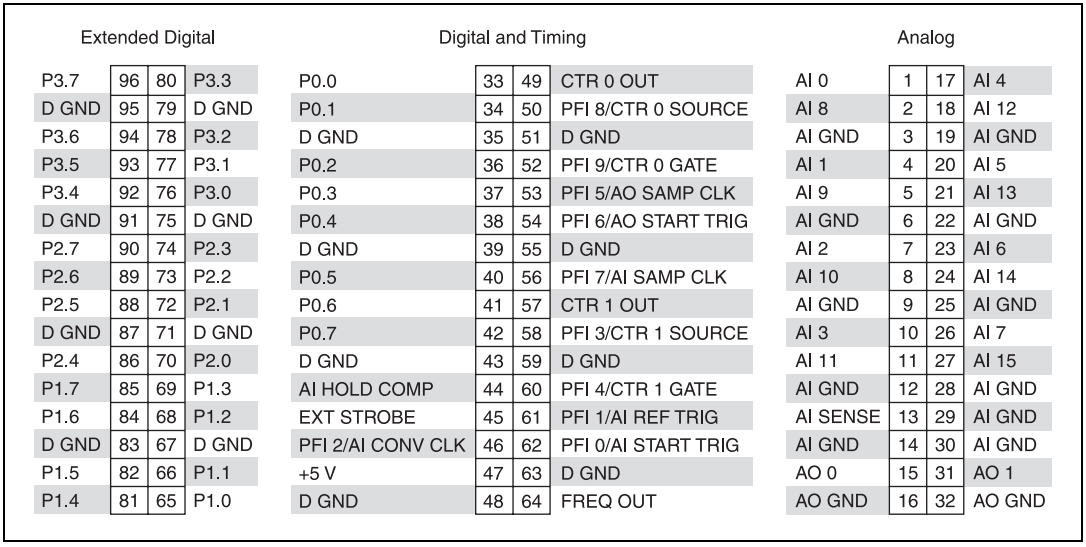

**Figure A-20.** NI DAQPad-6015 Mass Termination Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

## NI DAQPad-6016 Pinout

Figure A-21 shows the NI DAQPad-6016 device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.



| Extended Digital | | | | Digital and Timing | | | | Analog | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| P3.7 | 96 | 80 | P3.3 | P0.0 | 33 | 49 | CTR 0 OUT | AI 0 | 1 | 17 | AI 4 |
| D GND | 95 | 79 | D GND | P0.1 | 34 | 50 | PFI 8/CTR 0 SOURCE | AI 8 | 2 | 18 | AI 12 |
| P3.6 | 94 | 78 | P3.2 | D GND | 35 | 51 | D GND | AI GND | 3 | 19 | AI GND |
| P3.5 | 93 | 77 | P3.1 | P0.2 | 36 | 52 | PFI 9/CTR 0 GATE | AI 1 | 4 | 20 | AI 5 |
| P3.4 | 92 | 76 | P3.0 | P0.3 | 37 | 53 | PFI 5/AO SAMP CLK | AI 9 | 5 | 21 | AI 13 |
| D GND | 91 | 75 | D GND | P0.4 | 38 | 54 | PFI 6/AO START TRIG | AI GND | 6 | 22 | AI GND |
| P2.7 | 90 | 74 | P2.3 | D GND | 39 | 55 | D GND | AI 2 | 7 | 23 | AI 6 |
| P2.6 | 89 | 73 | P2.2 | P0.5 | 40 | 56 | PFI 7/AI SAMP CLK | AI 10 | 8 | 24 | AI 14 |
| P2.5 | 88 | 72 | P2.1 | P0.6 | 41 | 57 | CTR 1 OUT | AI GND | 9 | 25 | AI GND |
| D GND | 87 | 71 | D GND | P0.7 | 42 | 58 | PFI 3/CTR 1 SOURCE | AI 3 | 10 | 26 | AI 7 |
| P2.4 | 86 | 70 | P2.0 | D GND | 43 | 59 | D GND | AI 11 | 11 | 27 | AI 15 |
| P1.7 | 85 | 69 | P1.3 | AI HOLD COMP | 44 | 60 | PFI 4/CTR 1 GATE | AI GND | 12 | 28 | AI GND |
| P1.6 | 84 | 68 | P1.2 | EXT STROBE | 45 | 61 | PFI 1/AI REF TRIG | AI SENSE | 13 | 29 | AI GND |
| D GND | 83 | 67 | D GND | PFI 2/AI CONV CLK | 46 | 62 | PFI 0/AI START TRIG | AI GND | 14 | 30 | AI GND |
| P1.5 | 82 | 66 | P1.1 | +5 V | 47 | 63 | D GND | AO 0 | 15 | 31 | AO 1 |
| P1.4 | 81 | 65 | P1.0 | D GND | 48 | 64 | FREQ OUT | AO GND | 16 | 32 | AO GND |

**Figure A-21.** NI DAQPad-6016 Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI 6020E Family

The DAQPad-6020E is a Plug-and-Play, USB-compatible multifunction AI, AO, DIO, and TIO device for USB-compatible computers. The DAQPad-6020E features the following:

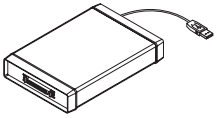
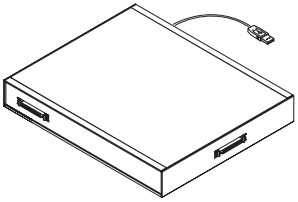
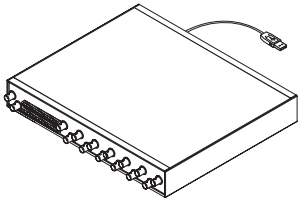
- 16 AI channels (eight differential) with 12-bit resolution
- Two AO channels with 12-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

**Note** The BNC version of the DAQPad-6020E has a 30-pin I/O connector.

Because the DAQPad-6020E has no DIP switches, jumpers, or potentiometers, you can easily configure and calibrate it through software.

There are three versions of the DAQPad-6020E offering different I/O connectivity and form factors. These versions are illustrated in Table A-3.

**Table A-3.** DAQPad-6020E Versions

| Model | I/O Connector | Form Factor |
|---|---|---|
| DAQPad-6020E Half-Size  | 68-pin SCSI-II Male | Half-size box (5.8 in. × 8.4 in. × 1.5 in.) Desktop use |
| DAQPad-6020E Full-Size  | 68-pin SCSI-II Male | Full-size box (12.1 in. × 10 in. × 1.7 in.) Rack-mountable, stackable |
| DAQPad-6020E BNC  | BNC and removable screw terminals | Full-size box (12.1 in. × 10 in. × 1.7 in.) Rack-mountable, stackable |

**Note** The DAQPad-6020E devices are compatible with Traditional NI-DAQ (Legacy) only.

# DAQPad-6020E Block Diagram

Figure A-22 shows a block diagram of the DAQPad-6020E.

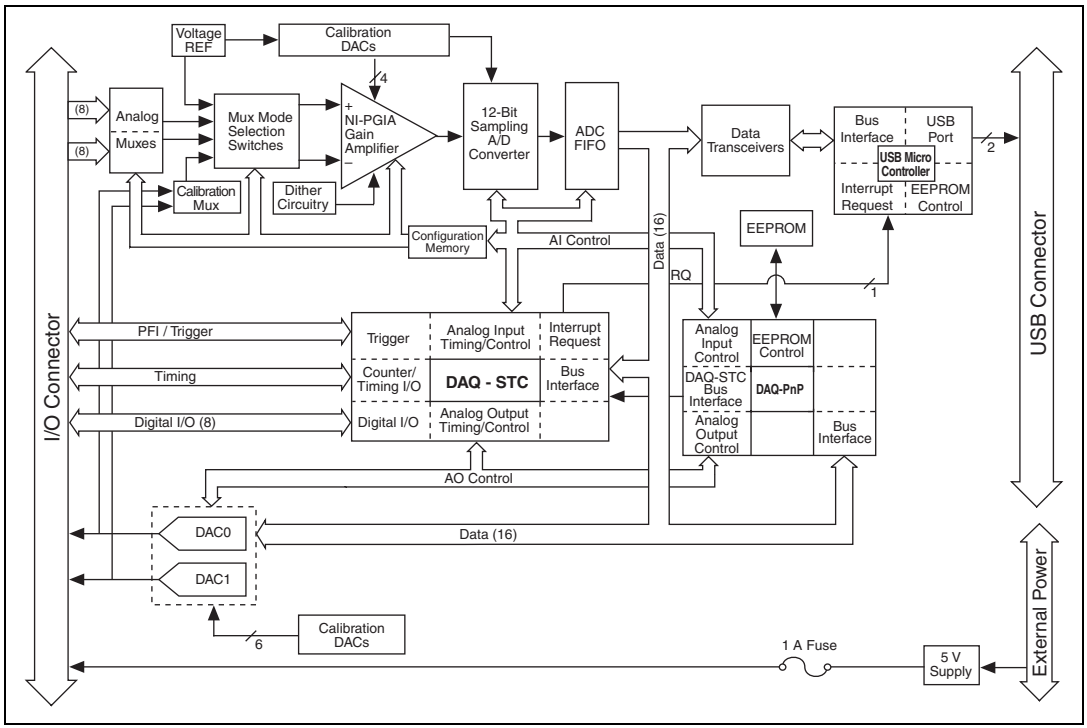



**Figure A-22.** DAQPad-6020E Block Diagram

# Connecting Signals to the DAQPad-6020E BNC

## Analog Input

You can use each analog input BNC connector for one differential signal or two single-ended signals.

### Differential Signals

To connect differential signals, determine the type of signal source you are using: a floating signal source or a ground-referenced signal source. Refer to the *Differential Connection Considerations* and *Connecting Analog Input Signals* sections of Chapter 2, *Analog Input*, for more information.

To measure a floating signal source, move the switch to the FS position. To measure a ground-referenced signal source, move the switch to the GS

position. Figure A-23 shows the source type switch locations on the front panel of the BNC DAQPads.

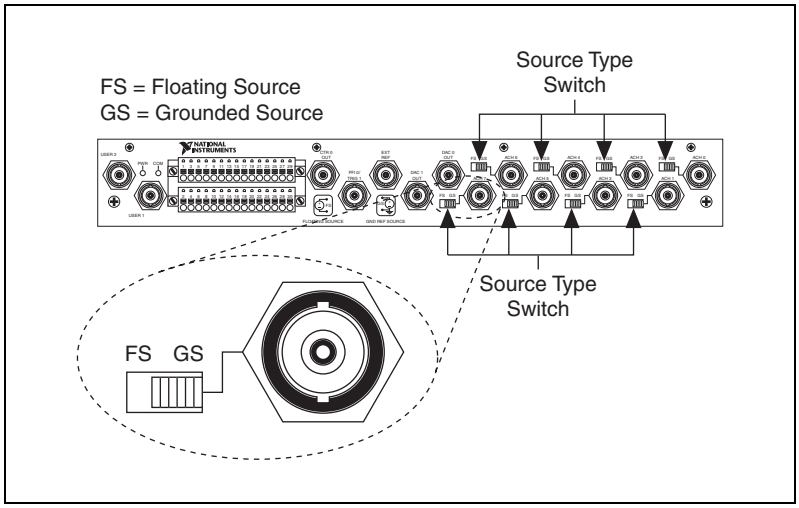



**Figure A-23.** BNC DAQPad Front Panel

Figure A-24 shows the analog input circuitry on BNC DAQPads. When the switch is in the FS position, AI *x* – is grounded through a 0.1 µF capacitor in parallel with a 5 kΩ resistor.

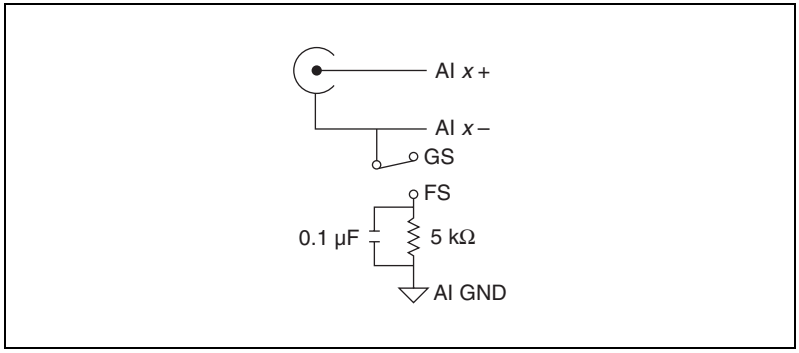



**Figure A-24.** BNC DAQPads Analog Input Circuitry

### Single-Ended Signals

For each BNC connector that you use for two single-ended channels, set the source type switch to the GS position. This setting disconnects the built-in ground reference resistor from the negative terminal of the BNC connector, allowing the connector to be used as a single-ended channel, as shown in Figure A-25.

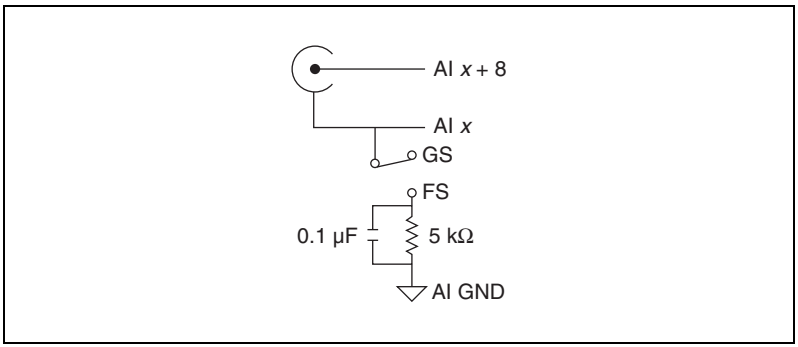



**Figure A-25.** BNC Single-Ended Signals

When you set the source type to the GS position and software-configure the device for single-ended input, each BNC connector provides access to two single-ended channels, AI *x* and AI *x*+8. For example, the BNC connector labeled AI 0 provides access to single-ended channels AI 0 and AI 8, the BNC connector labeled AI 1 provides access to single-ended channels AI 1 and AI 9, and so on. Up to 16 single-ended channels are available in single-ended measurement modes.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

## Analog Output

You can access analog output signals on the BNC connectors labeled AO 0 and AO 1. Figure A-26 shows the analog output circuitry on BNC DAQPads.

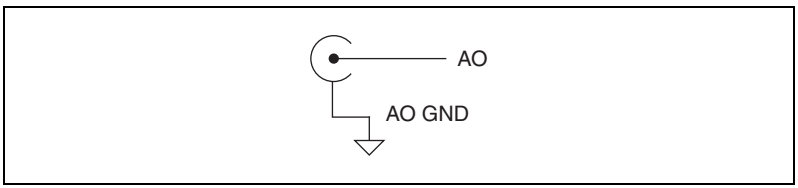



**Figure A-26.** Analog Output

Refer to the *Connecting Analog Output Signals* section of Chapter 3, *Analog Output*, for more information.

## AO External Reference

The AO EXT REF input controls the voltage range of analog output signals. Figure A-27 shows circuitry of the AO EXT REF on BNC DAQPads.

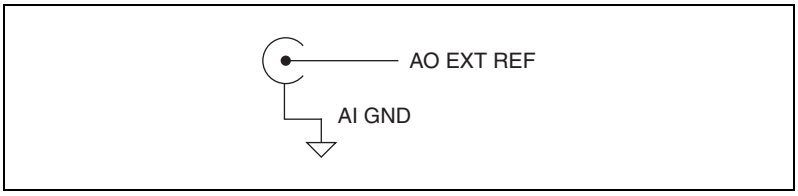



**Figure A-27.** AO EXT REF

Refer to the *Reference Selection* section of Chapter 3, *Analog Output*, for more information.

## Counter 0 Out and PFI 0/AI Start Trigger

You can access the Counter 0 Out and PFI 0/AI Start Trigger signals through their respective pins on BNC DAQPads, as shown in the Figure A-28 and Figure A-29.

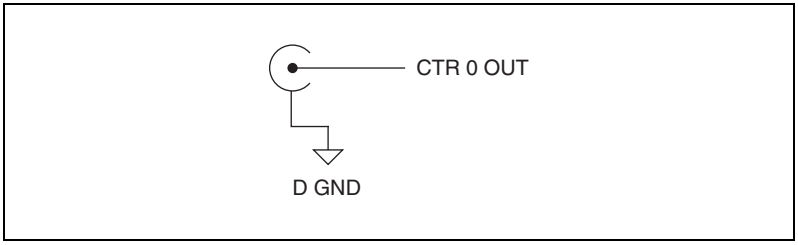



**Figure A-28.** Counter 0 Out

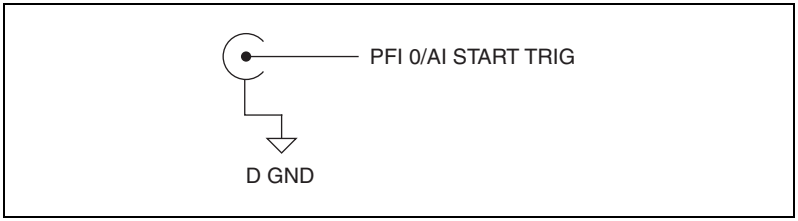



**Figure A-29.** PFI 0/AI Start Trigger

## User <1..2>

The User <1..2> signals connect directly from a screw terminal to a BNC. They allow you to use a BNC connector for a digital or timing I/O signal of your choice. The USER 1 BNC is internally connected to pin 21 and the USER 2 BNC is internally connected to pin 22 on the 30-pin I/O connector. Figure A-30 shows the connection of the User <1..2> BNCs.

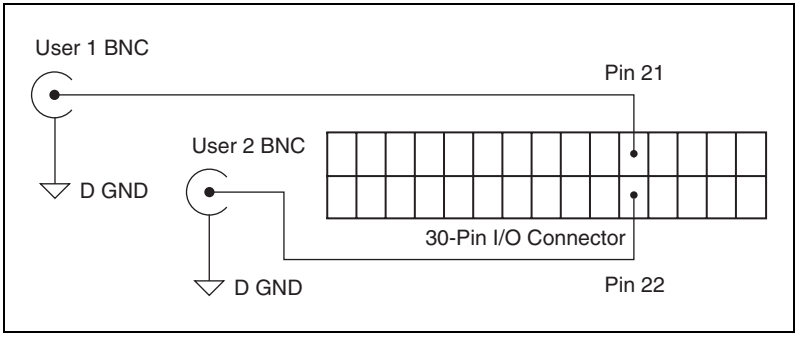



**Figure A-30.** BNC User <1..2> Connection

Figure A-31 shows another example of how to use the User <1..2> BNCs. To access the Ctr1Out signal from a BNC, connect pin 21 (USER 1) to pin 17 (CTR 1 OUT) with a wire.

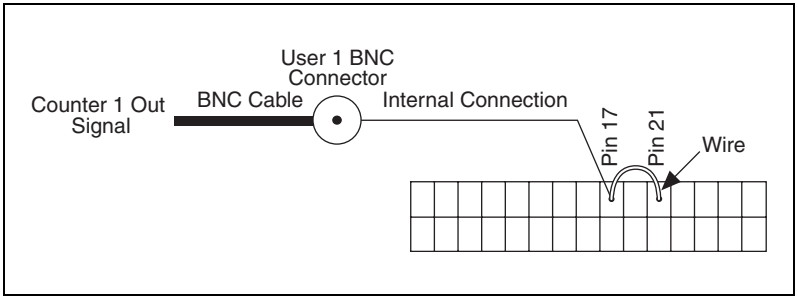



**Figure A-31.** BNC User <1..2> Example

## Other Signals

You can access other signals on BNC DAQPads through a 30-pin Combicon connector.

To connect to one of these signals, use a small screwdriver to press down the orange spring release button at a terminal and insert a wire. Releasing the orange spring release button will lock the wire securely in place.

You can remove the Combicon plugs to assist in connecting wires. Loosening the screws on either side of the two Combicon plugs allows you to detach the Combicon plugs from the BNC DAQPad device, as shown in Figure A-32.

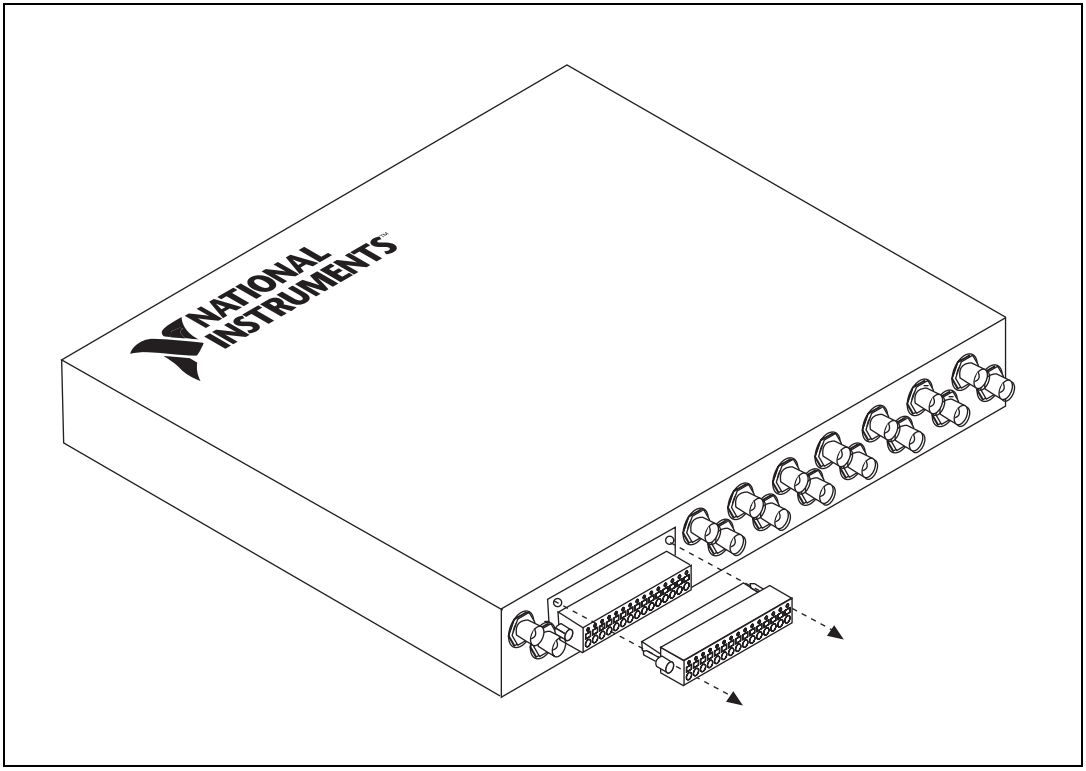



**Figure A-32.** Removing the BNC DAQPad Device Combicons

## DAQPad-6020E LED Patterns

The DAQPad-6020E has an LED on the front panel. Refer to Table A-4 for descriptions of each LED state.

**Table A-4.** DAQPad-6020E LEDs

| LED | DAQPad-6020E State |
|---|---|
| On | The device is configured. |
| Dim | — |
| Off | The device turns off or goes into the low-power, suspend mode when the computer is powered down. |
| 1 blink | The device is recognized but not configured. |
| 2 blinks | The device displays this pattern if the host computer detects the DAQPad but cannot configure it. This problem arises if NI-DAQ is not properly installed, or there are no system resources available. |
| 4 blinks | If this pattern is displayed, contact National Instruments. |

## DAQPad-6020E Specifications

Refer to the *NI DAQPad-6020E Family Specifications* for more detailed information on the devices.

## NI DAQPad-6020E Pinout

Figure A-33 shows the NI DAQPad-6020E device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

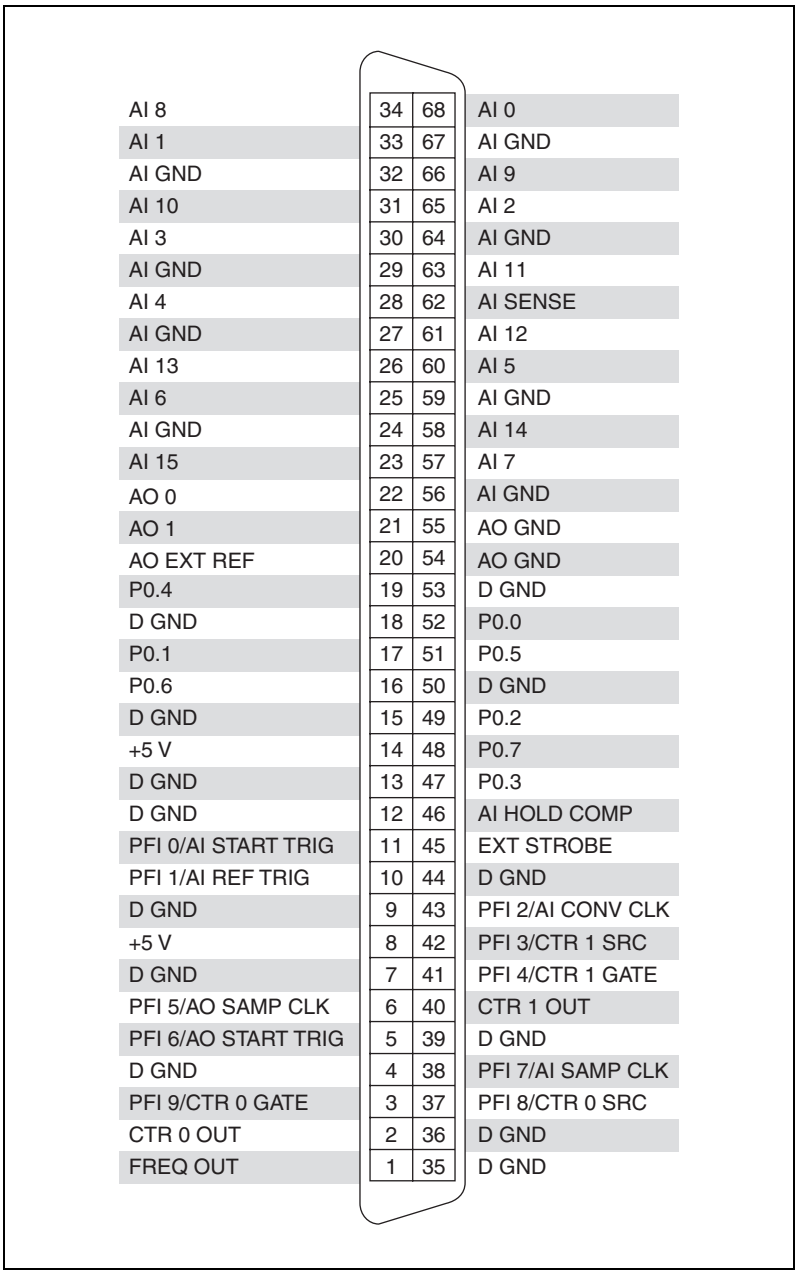



**Figure A-33.** NI DAQPad-6020E Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI DAQPad-6020E BNC Pinout

Figure A-34 shows the NI DAQPad-6020E BNC device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

| | | | |
|---|---|---|---|
| PFI 9 | 2 | 1 | P0.7 |
| PFI 8 | 4 | 3 | P0.6 |
| PFI 7 | 6 | 5 | P0.5 |
| PFI 6 | 8 | 7 | P0.4 |
| PFI 5 | 10 | 9 | P0.3 |
| PFI 4 | 12 | 11 | P0.2 |
| PFI 3 | 14 | 13 | P0.1 |
| PFI 2 | 16 | 15 | P0.0 |
| PFI 1 | 18 | 17 | CTR 1 OUT |
| D GND | 20 | 19 | D GND |
| USER 2 | 22 | 21 | USER 1 |
| FREQ OUT | 24 | 23 | AI HOLD COMP |
| +5 V | 26 | 25 | EXT STROBE |
| +5 V | 28 | 27 | AI SENSE |
| D GND | 30 | 29 | AI GND |

**Figure A-34.** NI DAQPad-6020E BNC Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI 6023E/6024E/6025E Family

The NI 6023E/6024E/6025E are high-performance multifunction AI, AO, DIO, and TIO devices for PCI, PXI, PCMCIA, and CompactPCI bus computers.

The NI 6023E features the following:

- 16 AI channels (eight differential) with 12-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

The NI 6024E features the following:

- 16 AI channels (eight differential) with 12-bit resolution
- Two AO channels with 12-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

The NI 6025E features the following:

- 16 AI channels (eight differential) with 12-bit resolution
- Two AO channels with 12-bit resolution
- 32 DIO lines
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 100-pin extended DIO connector

For more information about the DIO lines on the NI 6025E, refer to the *Extended Digital I/O* section of Chapter 4, *Digital I/O*.

# NI 6023E/6024E/6025E Block Diagrams

Figure A-35 shows a block diagram of the NI PCI-6023E/6024E/6025E and the NI PXI-6025E.

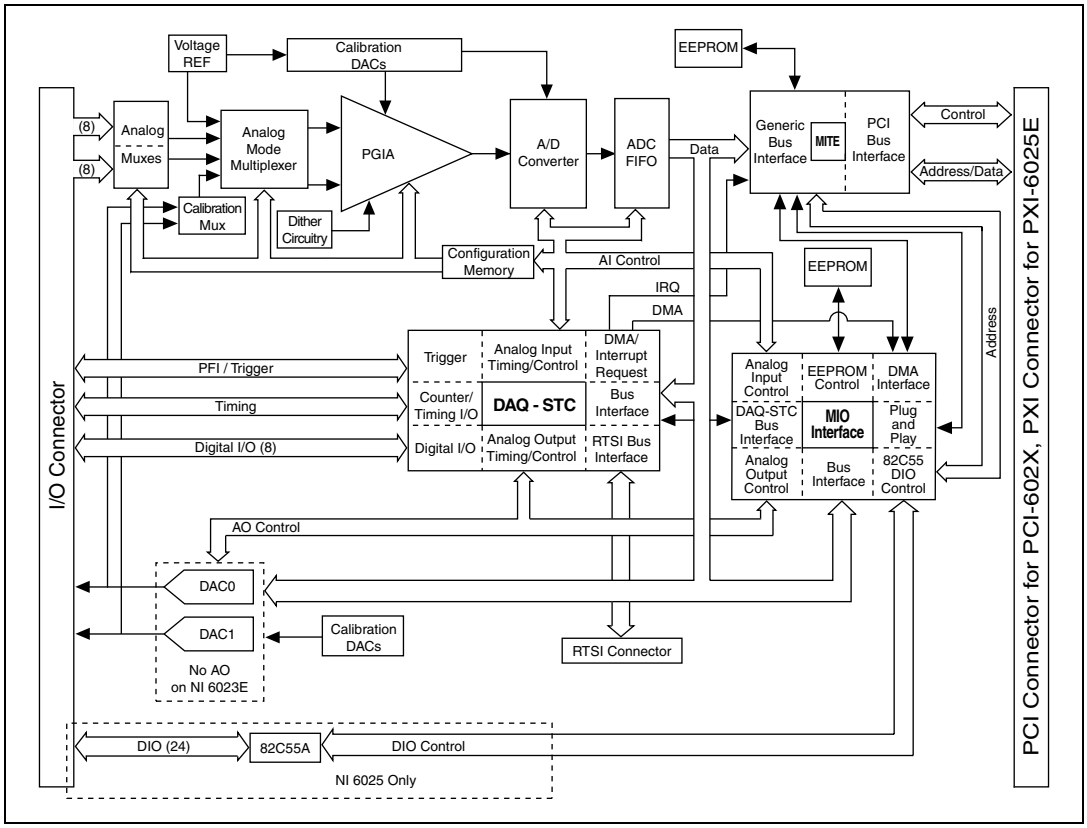



**Figure A-35.** NI PCI-6023E/6024E/6025E and NI PXI-6025E Block Diagram

Figure A-36 shows the block diagram of the DAQCard-6024E.

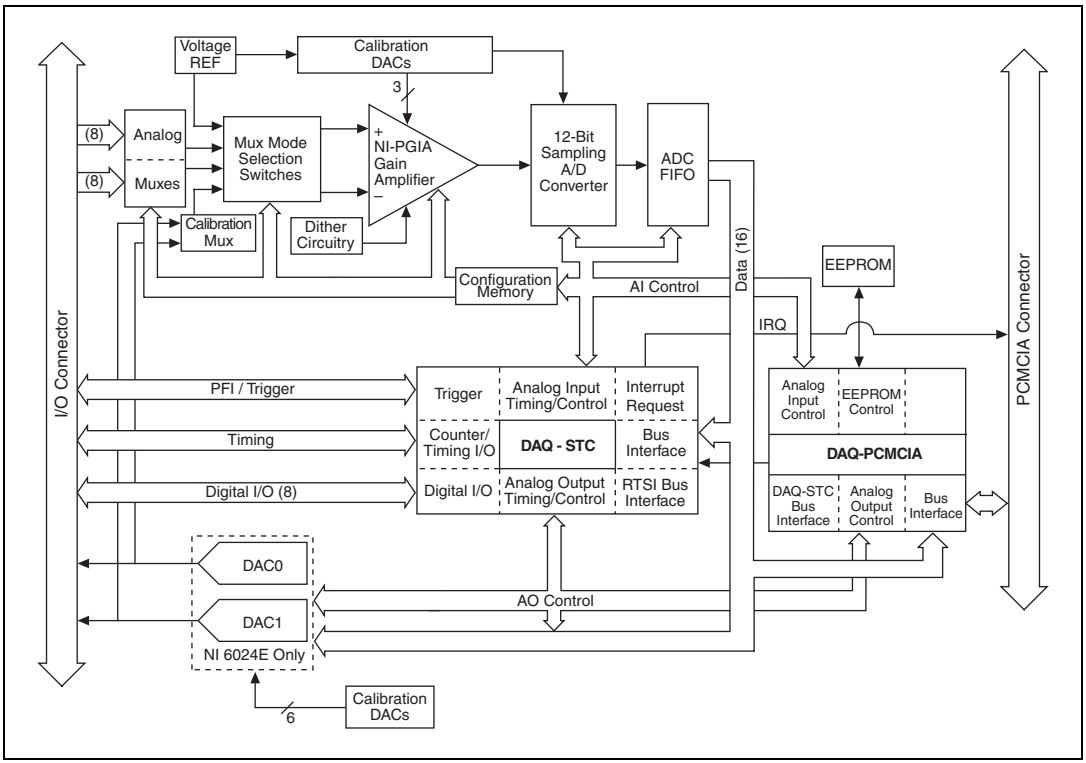



**Figure A-36.** DAQCard-6024E Block Diagram

## NI 6023E/6024E/6025E Specifications

Refer to the *NI 6023E/6024E/6025E Family Specifications* for more detailed information on the devices.

## NI 6023E Pinout

Figure A-37 shows the NI 6023E device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.




**Figure A-37.** NI 6023E Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI 6024E Pinout

Figure A-38 shows the NI 6024E device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

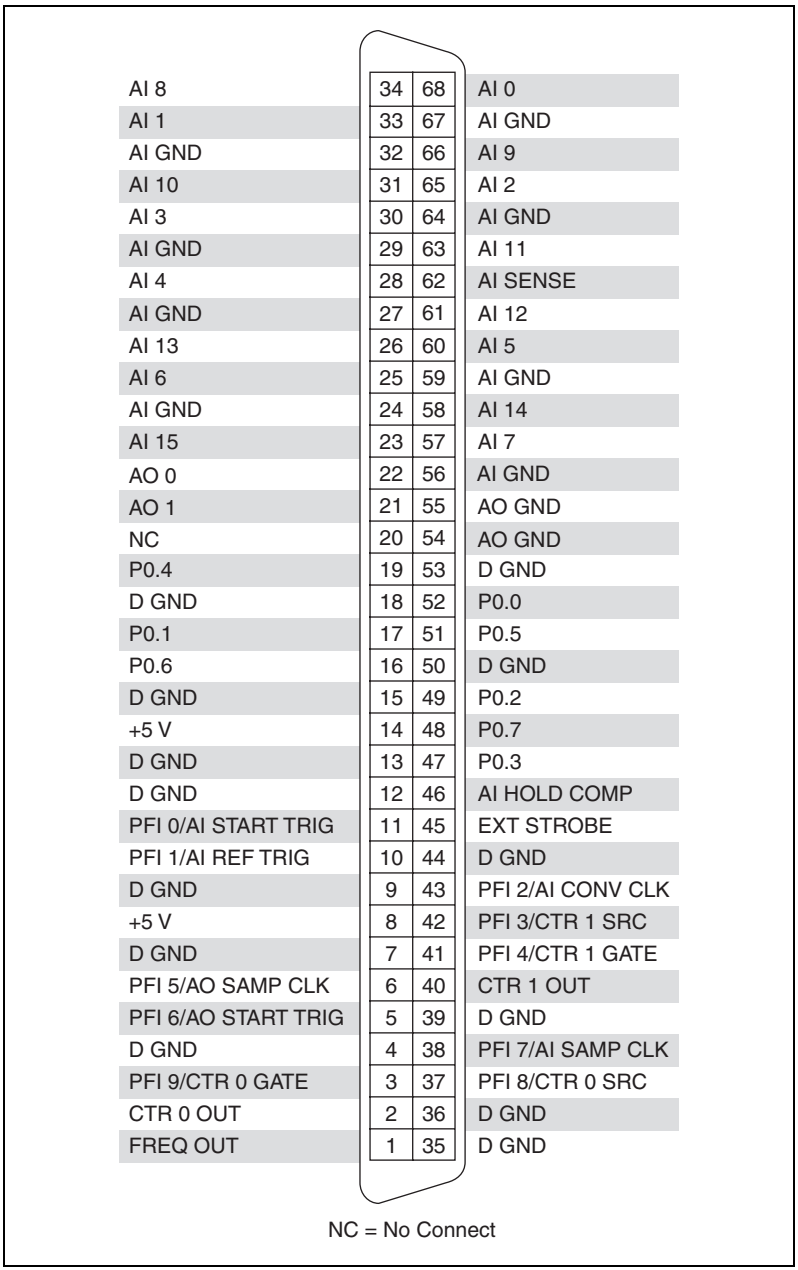



**Figure A-38.** NI 6024E Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI 6025E Pinout

Figure A-39 shows the NI 6025E device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

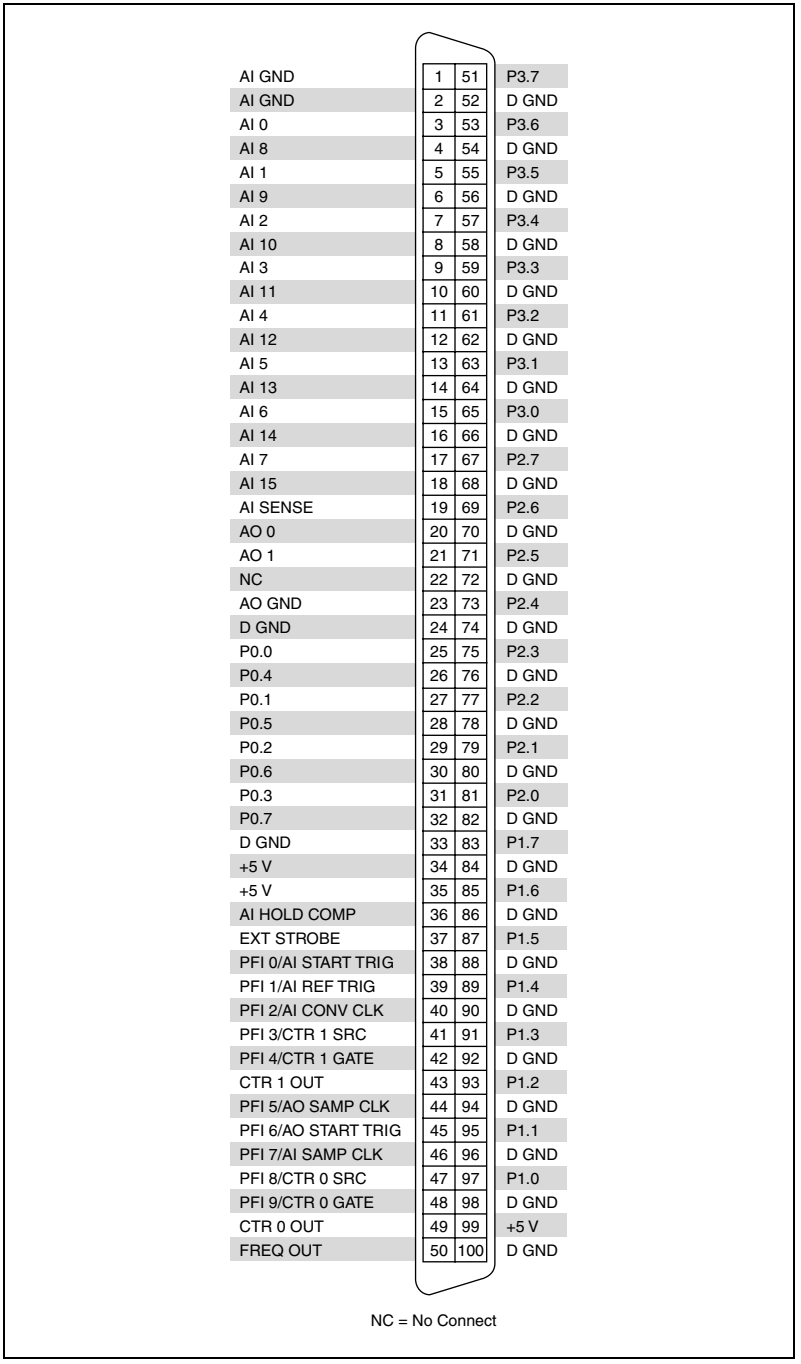



**Figure A-39.** NI 6025E Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI 6030E/6031E/6032E/6033E Family

The NI 6030E/6031E/6032E/6033E are Plug-and-Play, multifunction AI, AO, DIO, and TIO devices for PCI bus computers.

The NI 6030E features the following:

- 16 AI channels (eight differential) with 16-bit resolution
- Two AO channels with 16-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

The NI 6031E features the following:

- 64 AI channels (32 differential) with 16-bit resolution
- Two AO channels with 16-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 100-pin extended AI connector

The NI 6032E features the following:

- 16 AI channels (eight differential) with 16-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

The NI 6033E features the following:

- 64 AI channels (32 differential) with 16-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 100-pin extended AI connector

Because the NI 6030E/6031E/6032E/6033E devices have no DIP switches, jumpers, or potentiometers, you can easily configure and calibrate them through software.

# NI 6030E/6031E/6032E/6033E Dither

You cannot disable dither on the NI 6030E/6031E/6032E/6033E. The ADC resolution is so fine that the ADC and the PGIA inherently produce almost 0.5 $LSB_{rms}$ of noise. This configuration is equivalent to having a dither circuit that is always enabled.

# NI 6030E/6031E/6032E/6033E Block Diagrams

Figure A-40 shows a block diagram of the NI 6030E/6031E.

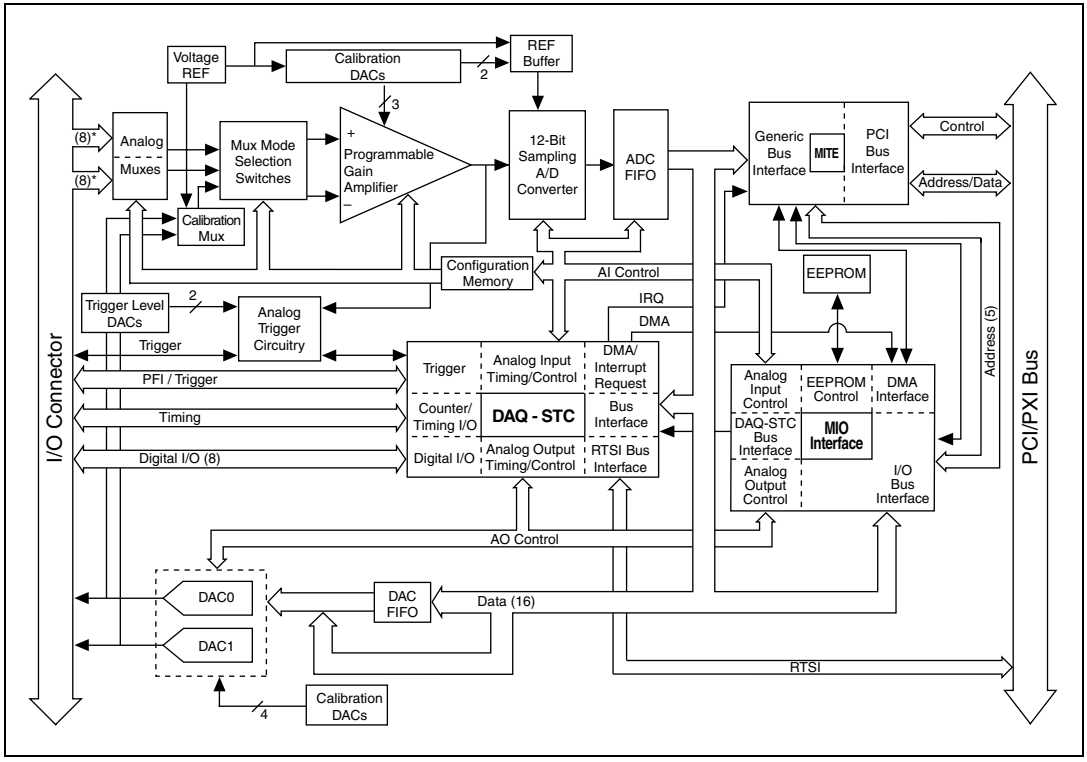



**Figure A-40.** NI 6030E/6031E Block Diagram

Figure A-41 shows a block diagram of the NI 6032E/6033E.

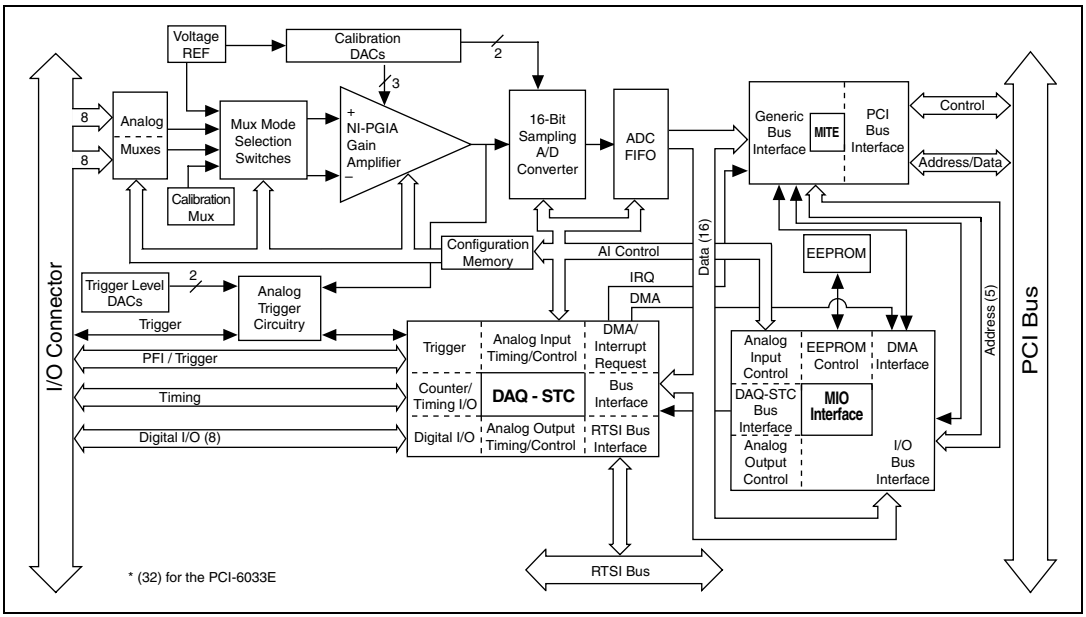



**Figure A-41.** NI 6032E/6033E Block Diagram

## NI 6030E/6031E/6032E/6033E Specifications

Refer to the *NI 6030E/6031E/6032E/6033E Family Specifications* for more detailed information on the devices.

## NI 6030E Pinout

Figure A-42 shows the NI 6030E device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

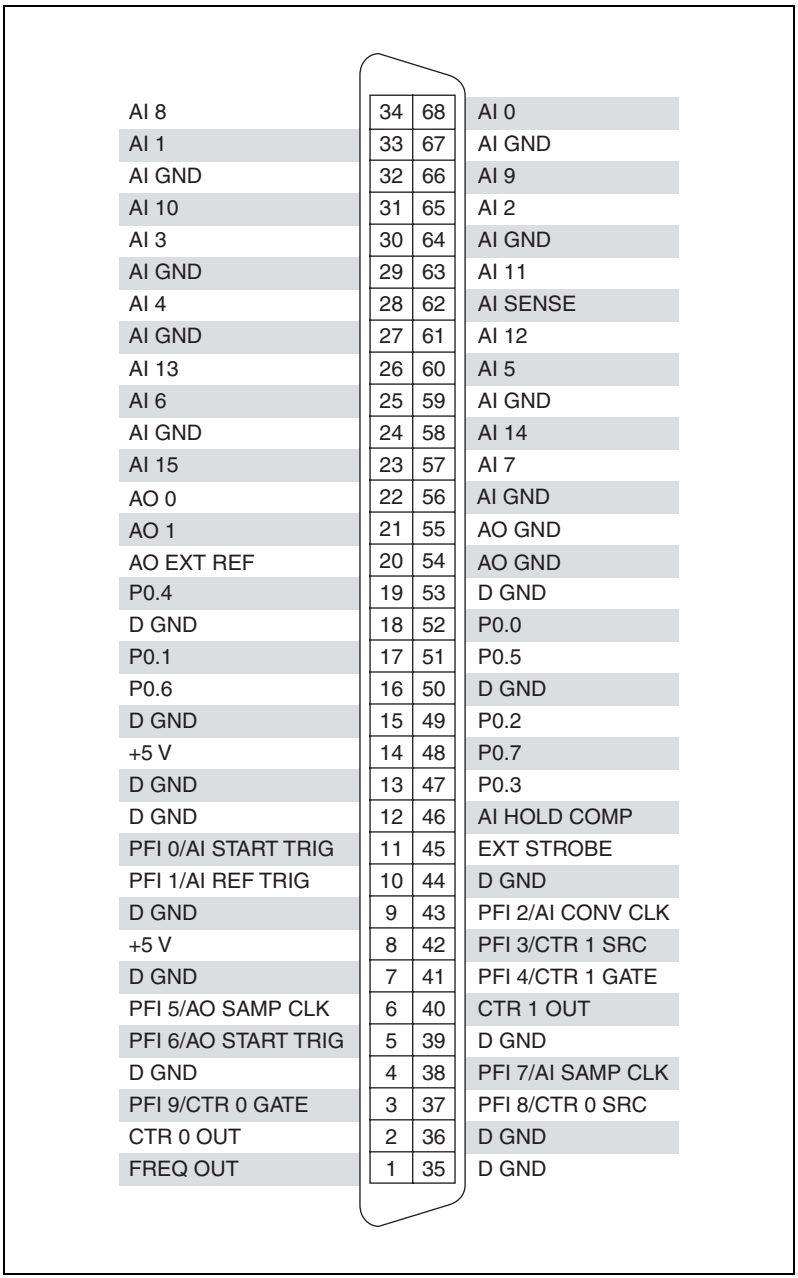



**Figure A-42.** NI 6030E Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI PCI-MIO-16XE-10 (NI 6030E) Pinout

Figure A-43 shows the PCI-MIO-16XE-10 (NI 6030E) device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

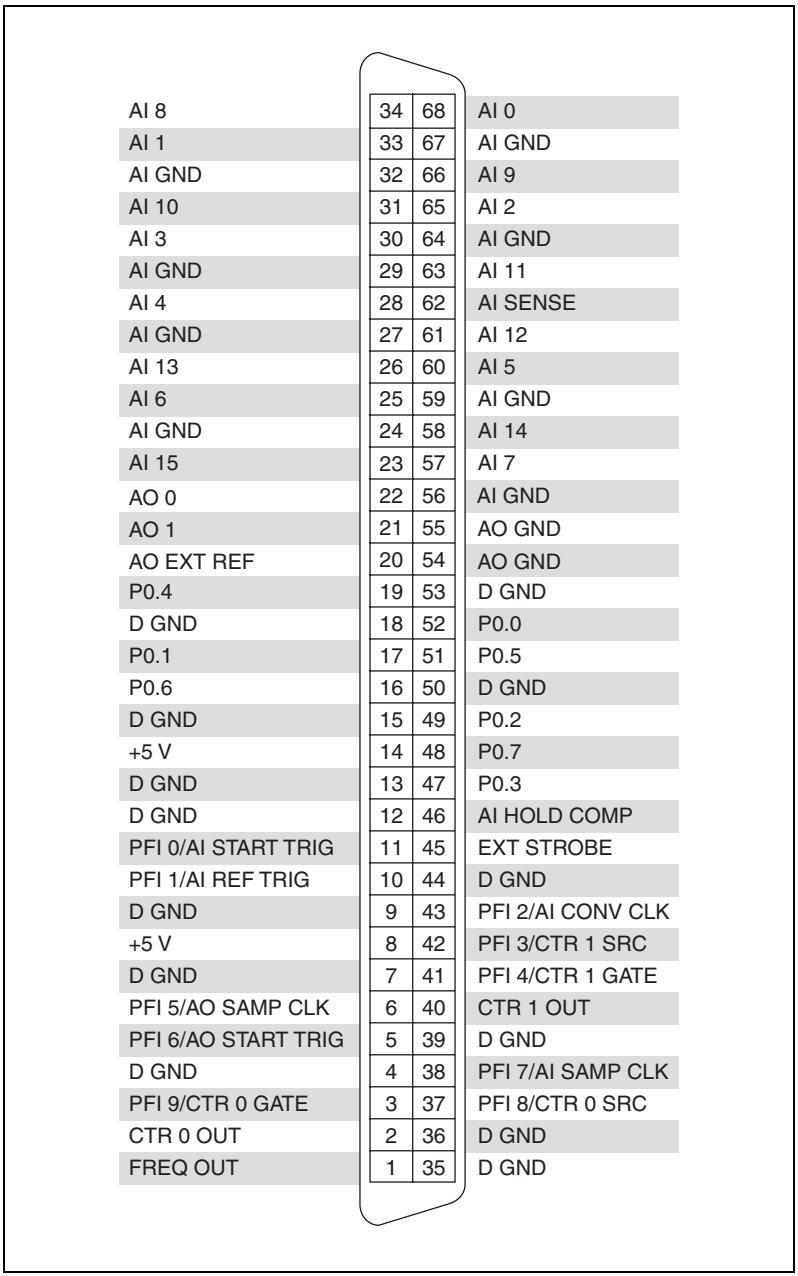



**Figure A-43.** NI PCI-MIO-16XE-10 (NI 6030E) Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI 6031E Pinout

Figure A-44 shows the NI 6031E device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

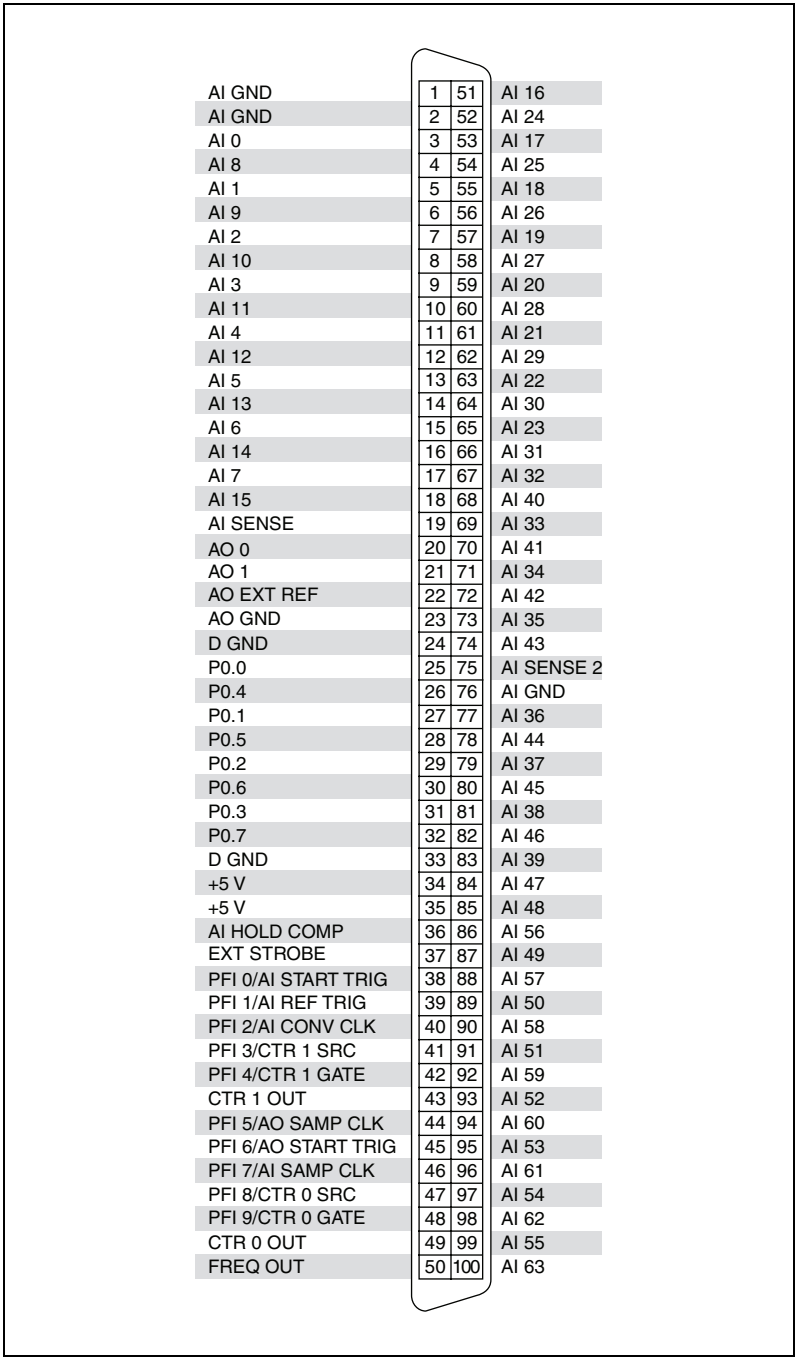



**Figure A-44.** NI 6031E Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

## NI 6032E Pinout

Figure A-45 shows the NI 6032E device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.




**Figure A-45.** NI 6032E Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section in Chapter 1, *DAQ System Overview*.

# NI 6033E Pinout

Figure A-46 shows the NI 6033E device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

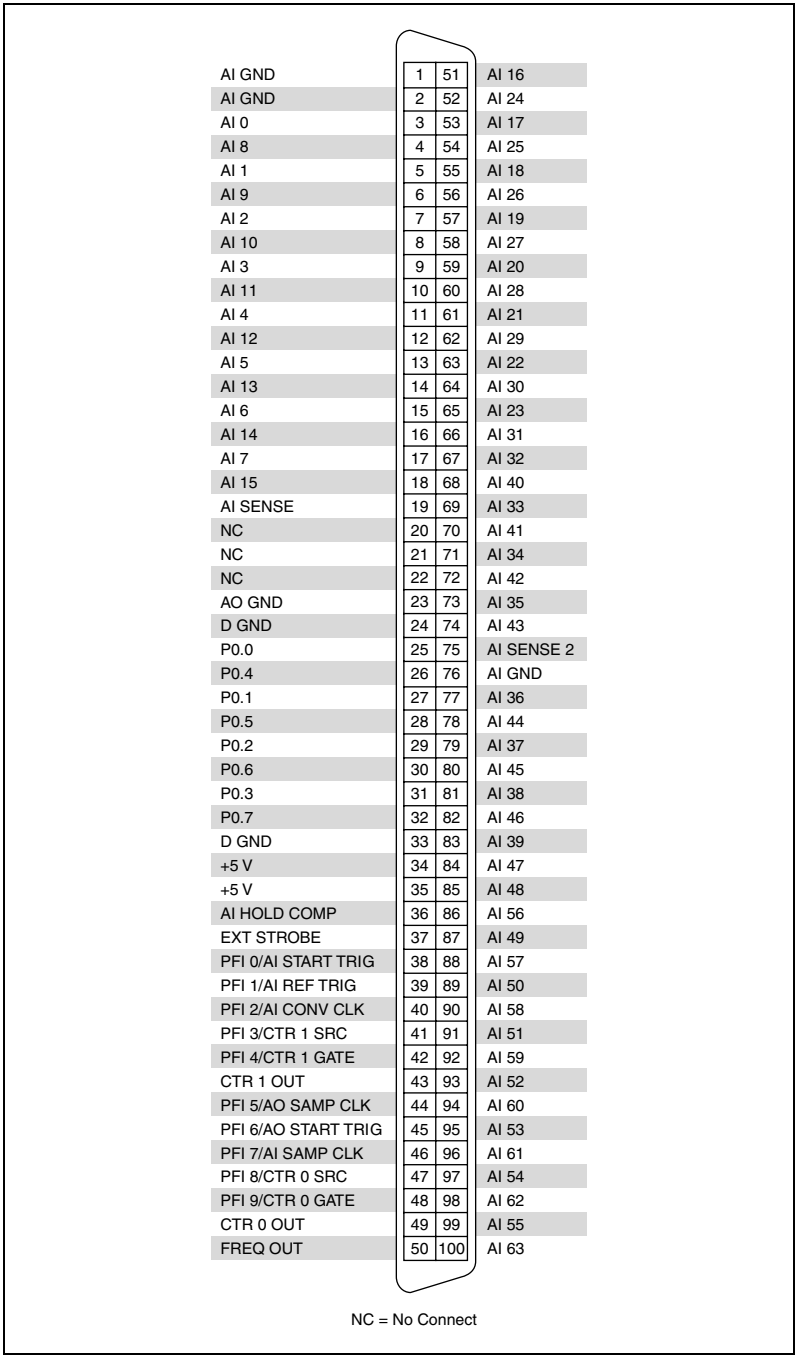



**Figure A-46.** NI 6033E Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI 6034E/6035E/6036E Family

The NI 6034E/6035E/6036E are Plug-and-Play, multifunction AI, AO, DIO, and TIO devices.

The NI 6034E features the following:

- 16 AI channels (eight differential) with 16-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

The NI 6035E features the following:

- 16 AI channels (eight differential) with 16-bit resolution
- Two AO channels with 12-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

The NI 6036E features the following:

- 16 AI channels (eight differential) with 16-bit resolution
- Two AO channels with 16-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

Because the NI 6034E/6035E/6036E devices have no DIP switches, jumpers, or potentiometers, you can easily configure and calibrate them through software.

The DAQCard-6036E is a low-power AI, AO, DIO, and TIO card for computers equipped with a Type II PC Card slot. The low power consumption of the DAQCard-6036E makes this card ideal for use in portable computers and makes portable data acquisition practical.

# NI 6034E/6035E/6036E Block Diagrams

Figure A-47 shows the block diagram of the NI PCI-6034E/6035E/6036E.

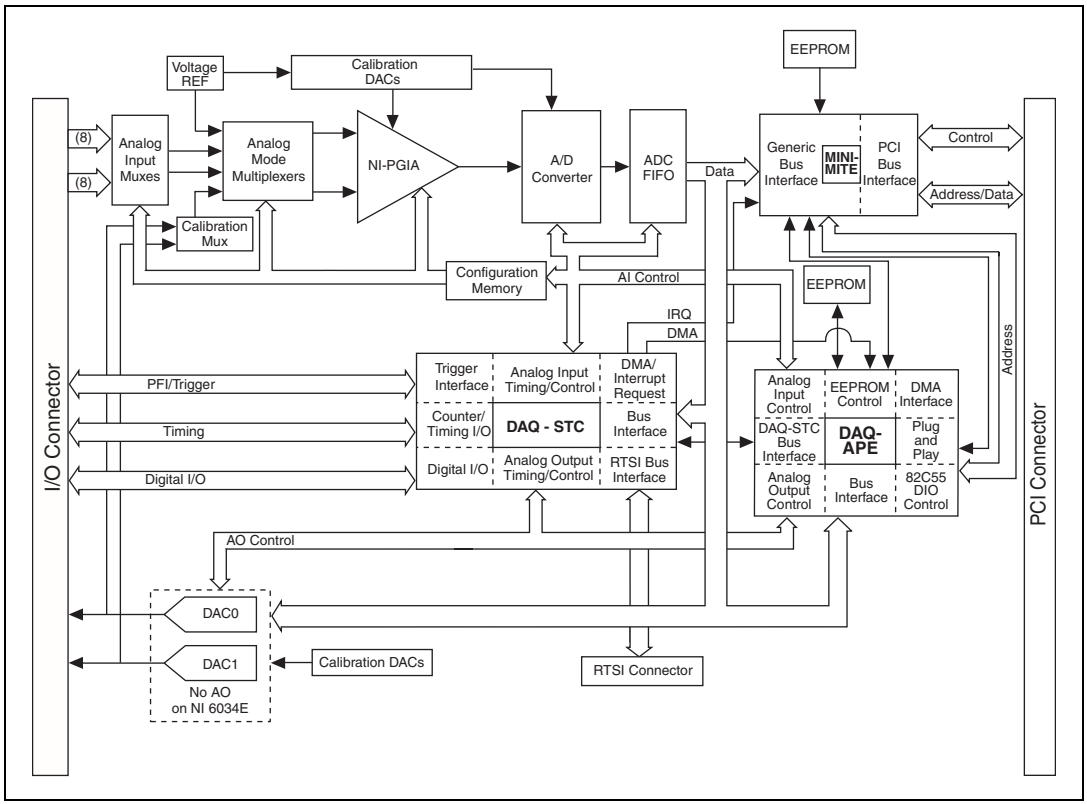



**Figure A-47.** NI PCI-6034E/6035E/6036E Block Diagram

Figure A-48 shows the block diagram of the DAQCard-6036E.

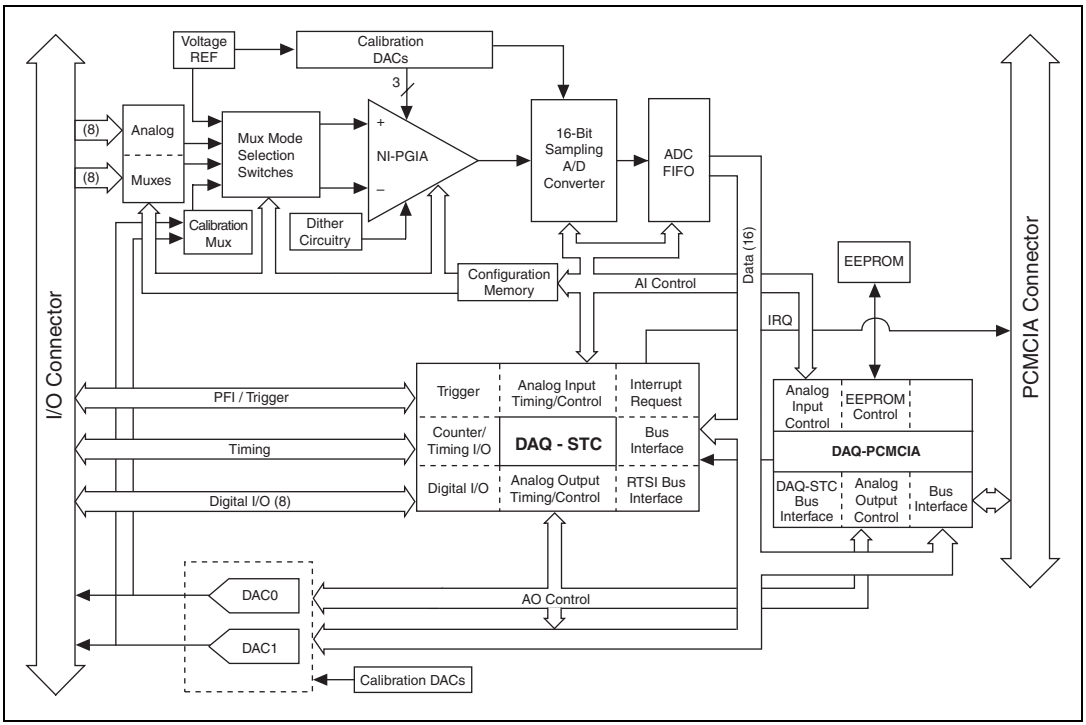



**Figure A-48.** DAQCard-6036E Block Diagram

## NI 6034E/6035E/6036E Specifications

Refer to the *NI 6034E/6035E/6036E Family Specifications* for more detailed information on the devices.

## NI 6034E Pinout

Figure A-49 shows the NI 6034E device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.




**Figure A-49.** NI 6034E Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI 6035E Pinout

Figure A-50 shows the NI 6035E device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

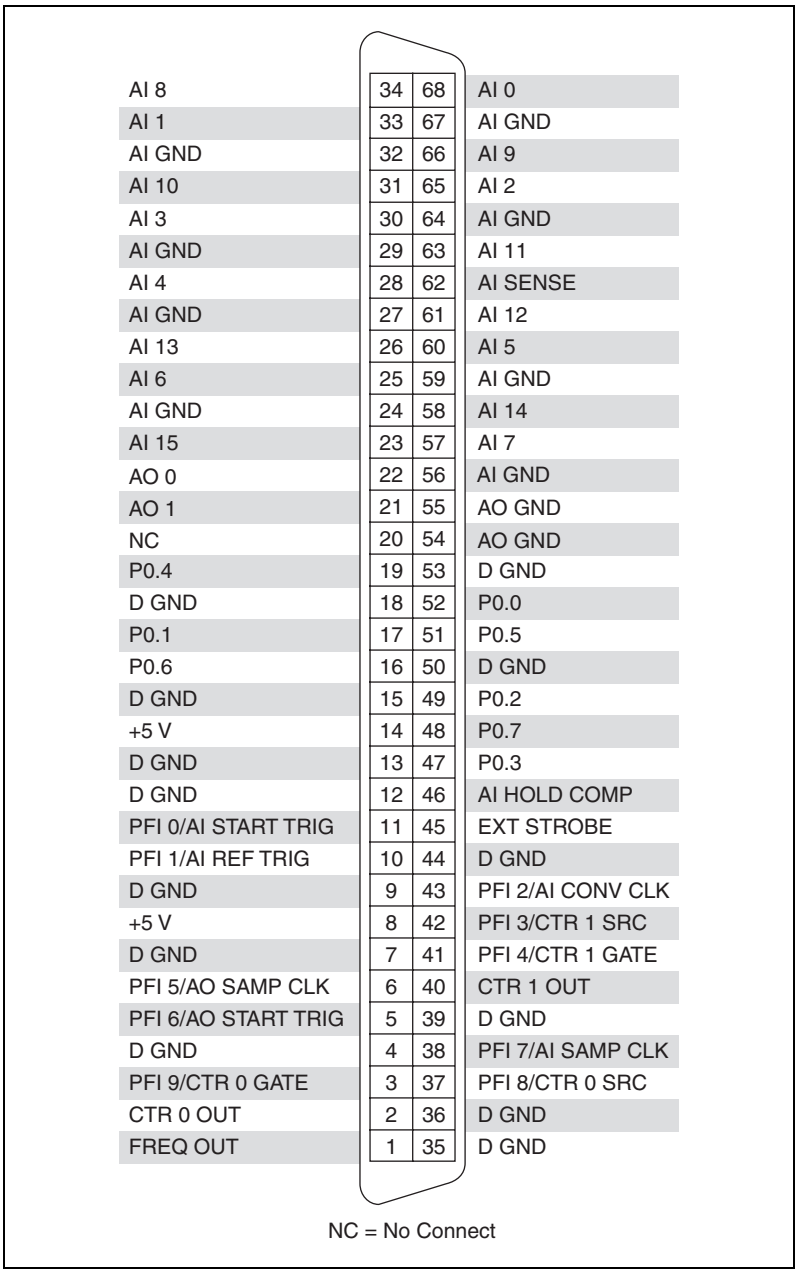



**Figure A-50.** NI 6035E Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI 6036E Pinout

Figure A-51 shows the NI 6036E device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

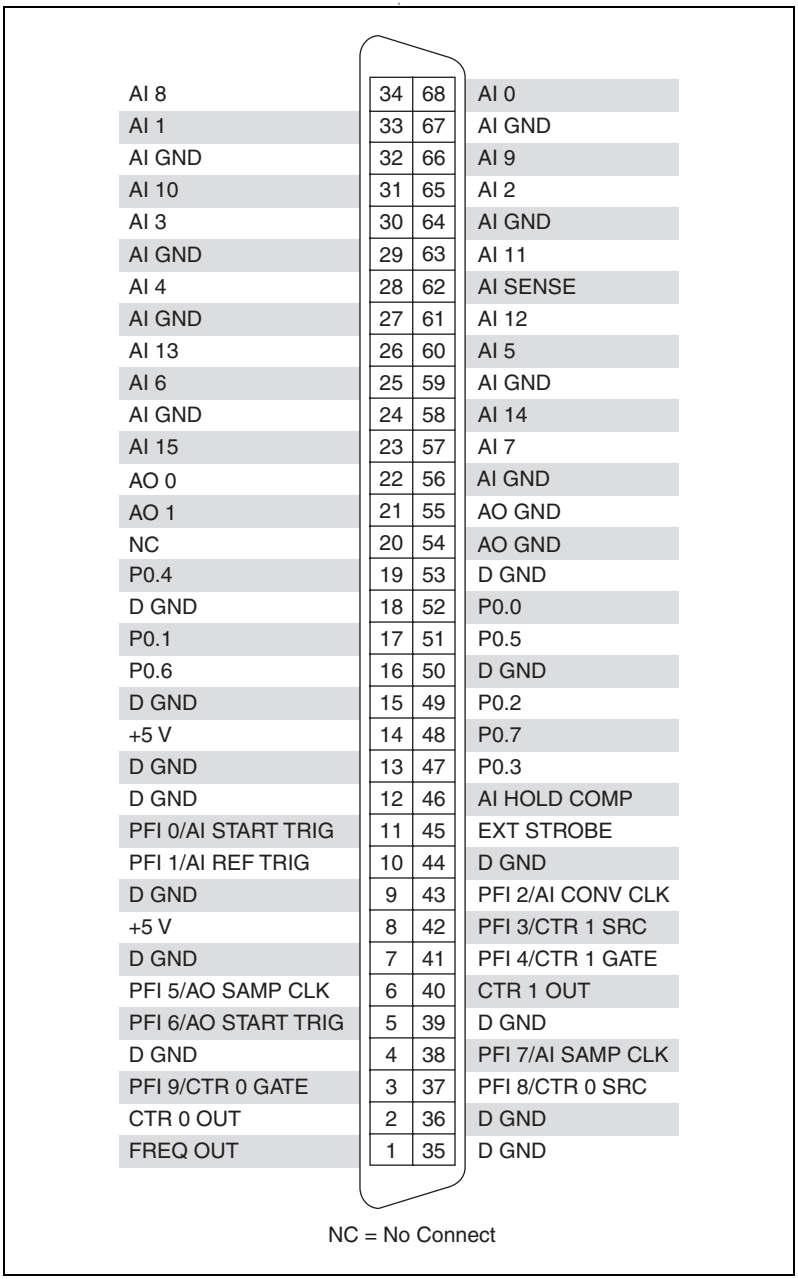



**Figure A-51.** NI 6036E Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI 6040E Family

## NI PXI-6040E

The NI PXI-6040E is a Plug-and-Play, multifunction AI, AO, DIO, and TIO device.

The NI PXI-6040E features the following:

- 16 AI channels (eight differential) with 12-bit resolution
- Two AO channels with 12-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

Because the NI 6040E for PXI has no DIP switches, jumpers, or potentiometers, you can easily configure and calibrate it through software.

### NI PXI-6040E Block Diagram

Figure A-52 shows a block diagram of the NI PXI-6040E.

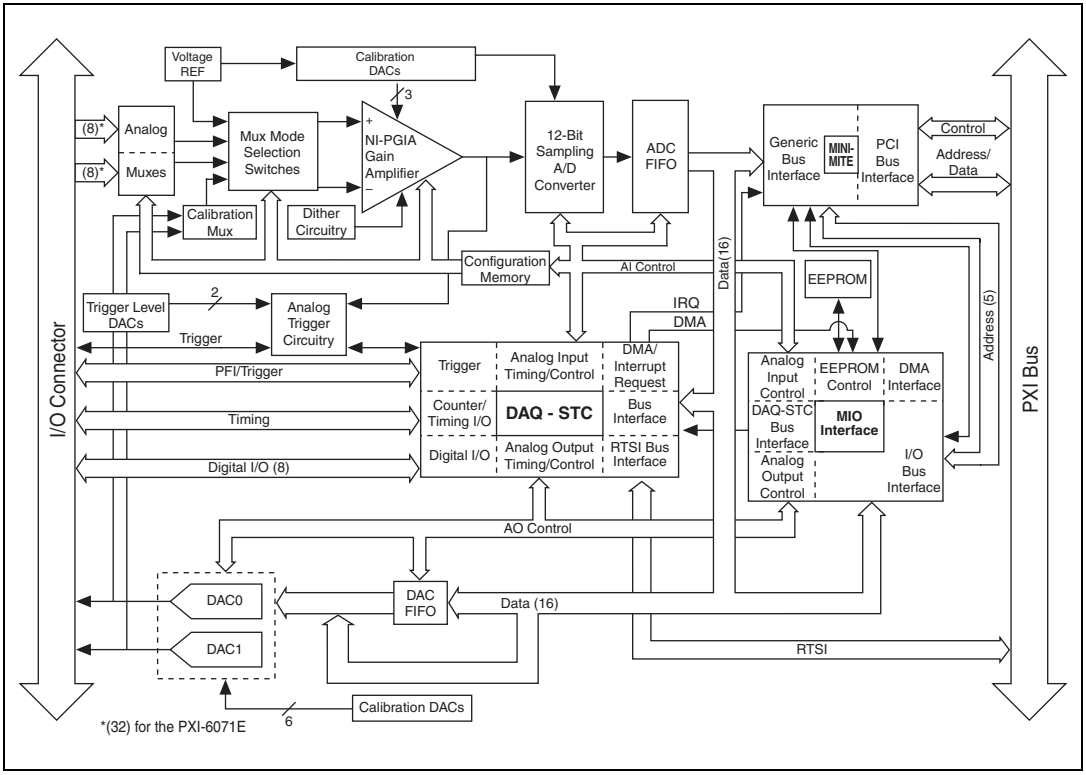



**Figure A-52.** NI PXI-6040E Block Diagram

## NI 6040E Pinout

Figure A-53 shows the NI 6040E device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

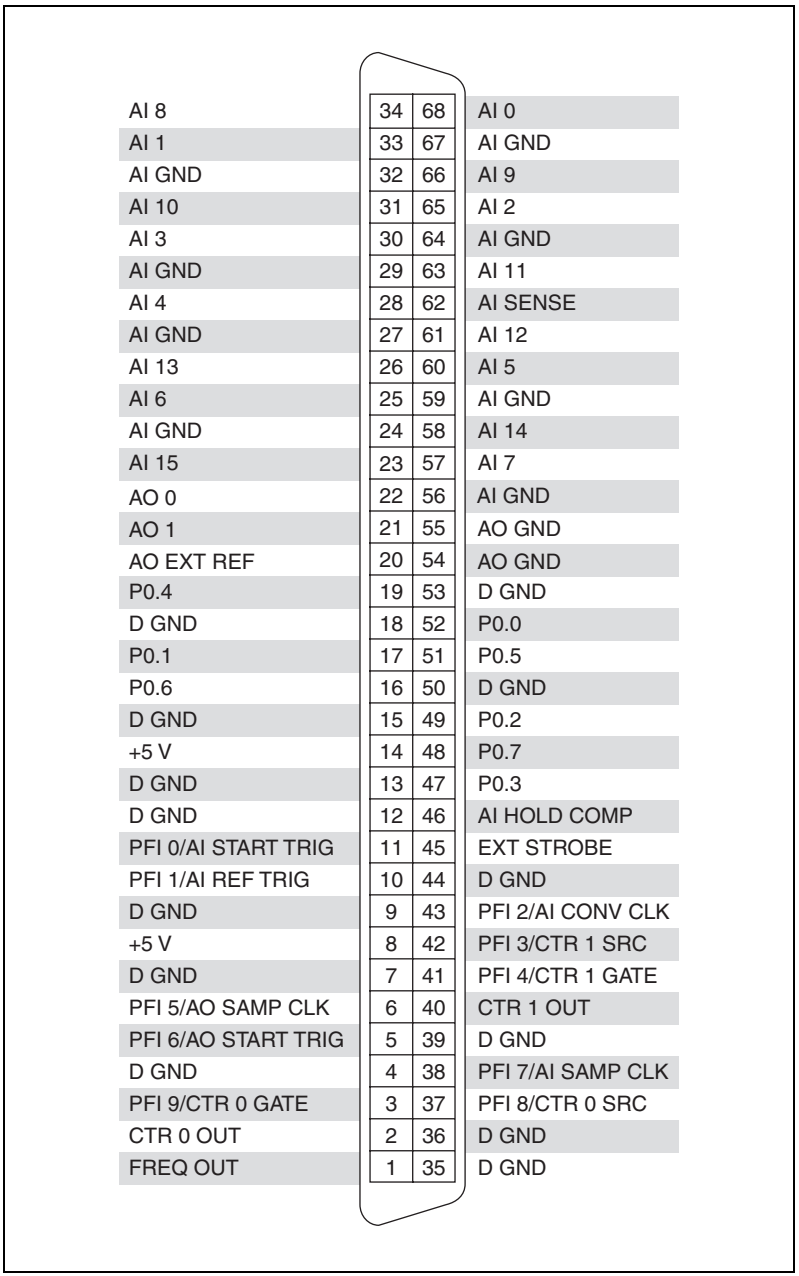



**Figure A-53.** NI 6040E Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# PCI-MIO-16E-4

The PCI-MIO-16E-4 is a Plug-and-Play, multifunction AI, AO, DIO, and TIO device for PCI bus computers.

The PCI-MIO-16E-4 features the following:

- 16 AI channels (eight differential) with 16-bit resolution
- Two AO channels with 12-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

Because the PCI-MIO-16E-4 has no DIP switches, jumpers, or potentiometers, you can easily configure and calibrate it through software.

# PCI-MIO-16E-4 Block Diagram

Figure A-54 shows a block diagram of the PCI-MIO-16E-4.

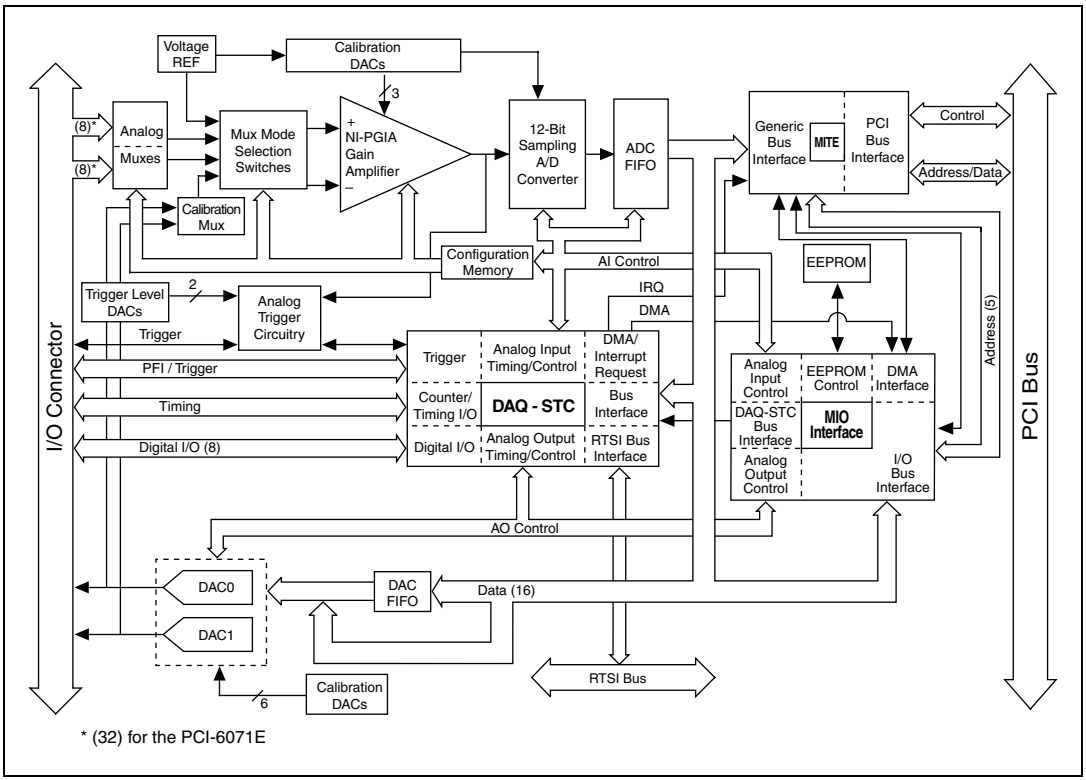



**Figure A-54.** PCI-MIO-16E-4 Block Diagram

# NI PCI-MIO-16E-4 (NI 6040E) Pinout

Figure A-55 shows the PCI-MIO-16E-4 (NI 6040E) device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

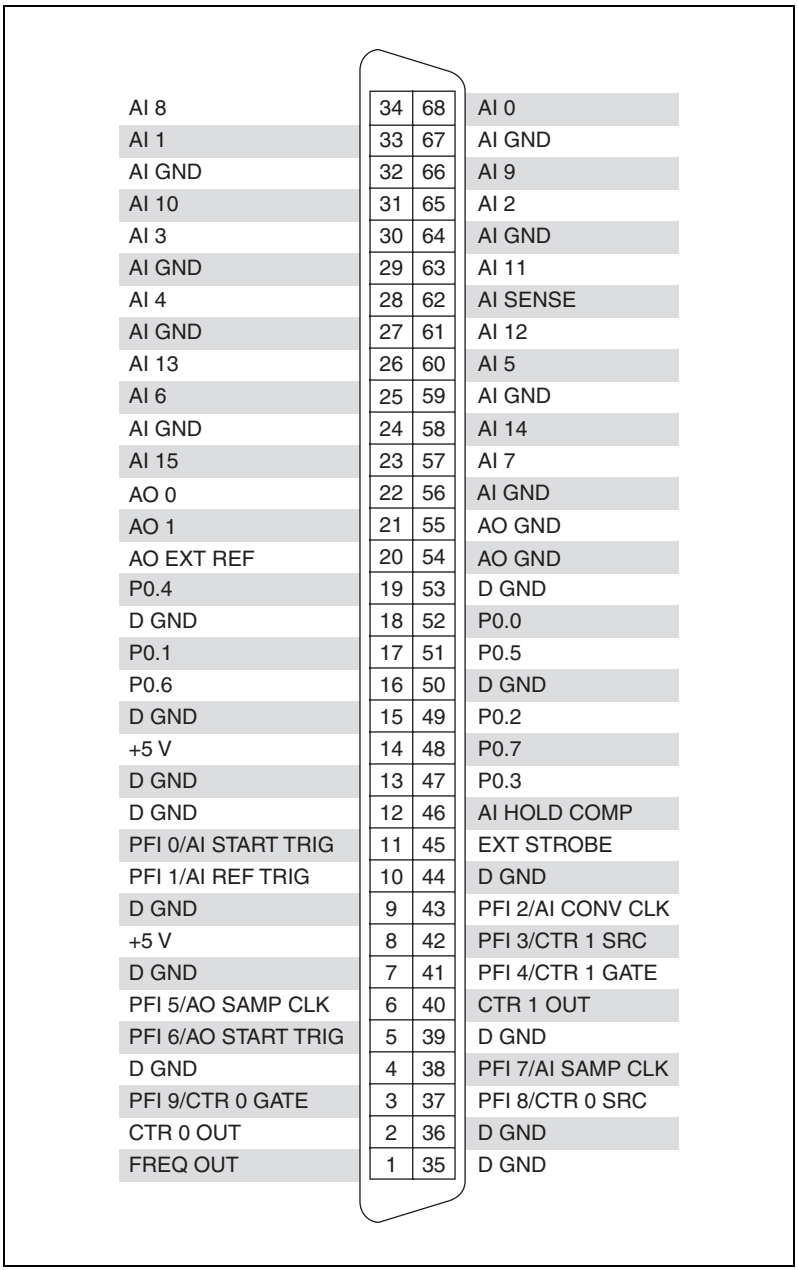



**Figure A-55.** NI PCI-MIO-16E-4 (NI 6040E) Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

## NI 6040E Family Specifications

Refer to the *NI 6040E Family Specifications* for more detailed information on the devices.

# NI 6052E Family

## DAQPad-6052E

The DAQPad-6052E is a Plug-and-Play, multifunction AI, AO, DIO, and TIO device.

The DAQPad-6052E features the following:

- 16 AI channels (eight differential) with 16-bit resolution
- Two AO channels with 16-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector



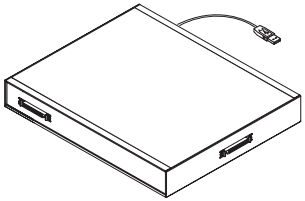
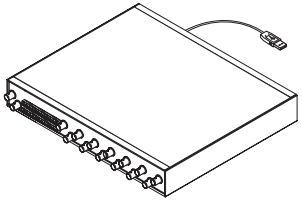
**Note** The BNC version of the DAQPad-6052E has a 30-pin I/O connector.

The NI DAQPad-6052E for 1394 is a high-performance, switchless, jumperless, hot-pluggable DAQ device. The 1394 interface automatically handles the assignment of all host resources and allows you to install the device without powering off the computer. You can plug up to 64 National Instruments DAQ devices into a single computer using 1394, although you will run out of bus bandwidth if all devices operate at full rate. The NI DAQPad-6052E for 1394 provides up to 250 V of DC functional isolation from the computer.

The NI DAQPad-6052E for 1394 has an onboard watchdog timer that continuously resets the device until the device successfully enumerates with the host operating system and the device driver initiates transactions to the device. To avoid continuous resets, make sure the device and host computer are powered on, the 1394 cable is attached to the host computer, and the device drivers are installed.

There are two versions of the NI DAQPad-6052E. Table A-5 illustrates the different I/O connectivity and form factors of each version.

**Table A-5.** NI DAQPad-6052E Versions

| Model | I/O Connector | Form Factor |
|---|---|---|
| DAQPad-6052E  | 68-pin SCSI-II male | Full-size box<br>(12.1 in. × 10 in. × 1.7 in.)<br>Rack-mountable, stackable |
| DAQPad-6052E BNC  | BNC and removable screw terminals | Full-size box<br>(12.1 in. × 10 in. × 1.7 in.)<br>Rack-mountable, stackable |

# DAQPad-6052E Block Diagram

Figure A-56 shows a block diagram of the DAQPad-6052E.

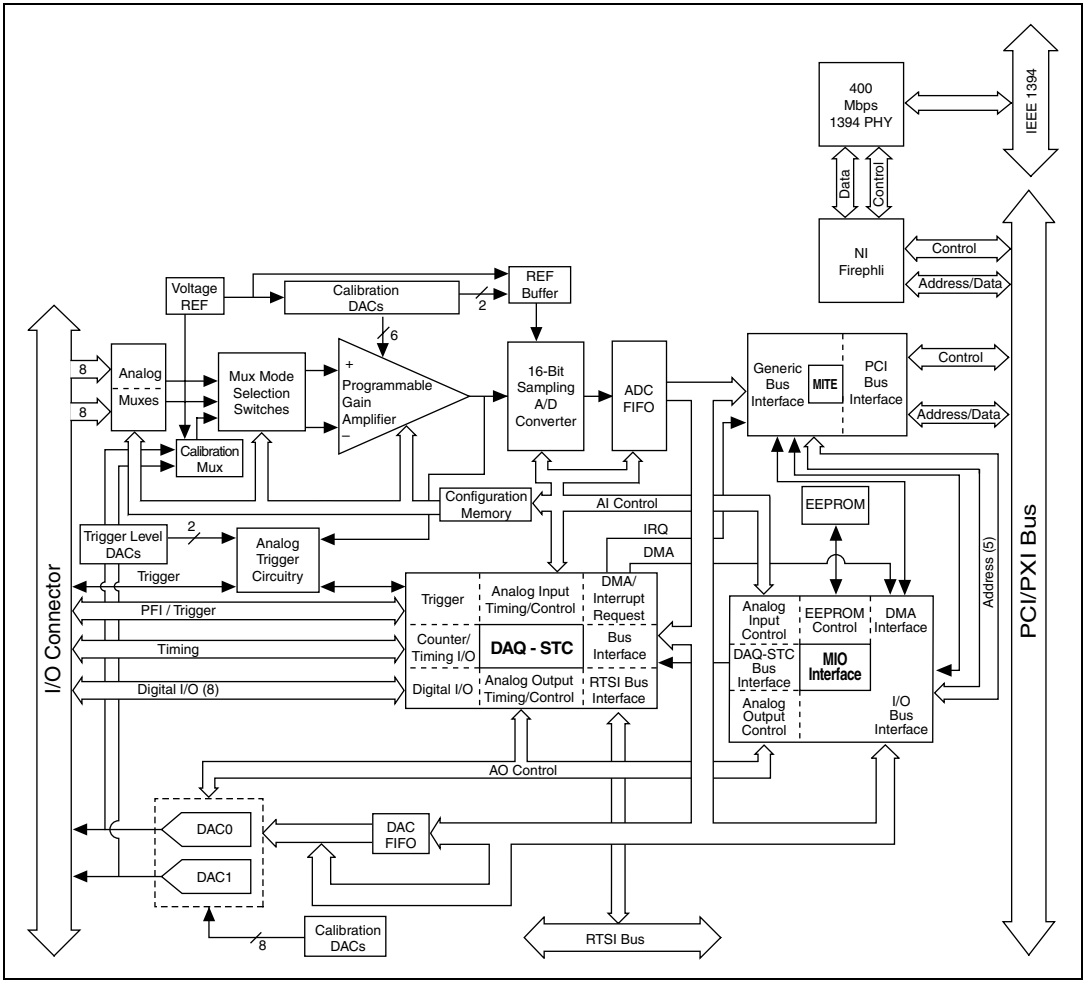



**Figure A-56.** DAQPad-6052E Block Diagram

# Connecting Signals to the DAQPad-6052E BNC

## Analog Input

You can use each analog input BNC connector for one differential signal or two single-ended signals.

### Differential Signals

To connect differential signals, determine the type of signal source you are using: a floating signal source or a ground-referenced signal source. Refer to the *Differential Connection Considerations* and *Connecting Analog Input Signals* sections of Chapter 2, *Analog Input*, for more information on AI signals.

To measure a floating signal source, move the switch to the FS position. To measure a ground-referenced signal source, move the switch to the GS position. Figure A-57 shows the source type switch locations on the front panel of the BNC DAQPads.

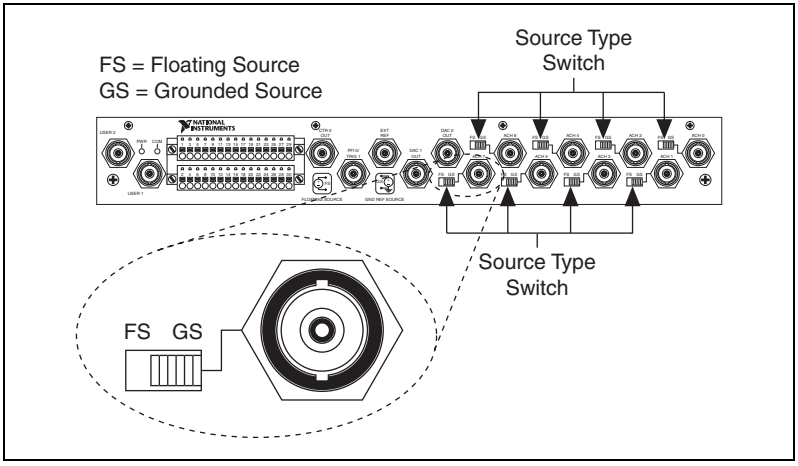



**Figure A-57.** BNC DAQPad Front Panel

Figure A-58 shows the analog input circuitry on BNC DAQPads. When the switch is in the FS position, AI *x* – is grounded through a 0.1 µF capacitor in parallel with a 5 kΩ resistor.

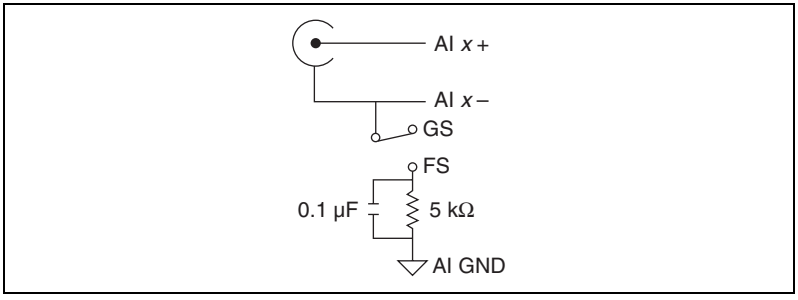



**Figure A-58.** Analog Input Circuitry

### Single-Ended Signals

For each BNC connector that you use for two single-ended channels, set the source type switch to the GS position. This setting disconnects the built-in ground reference resistor from the negative terminal of the BNC connector, allowing the connector to be used as a single-ended channel, as shown in Figure A-59.

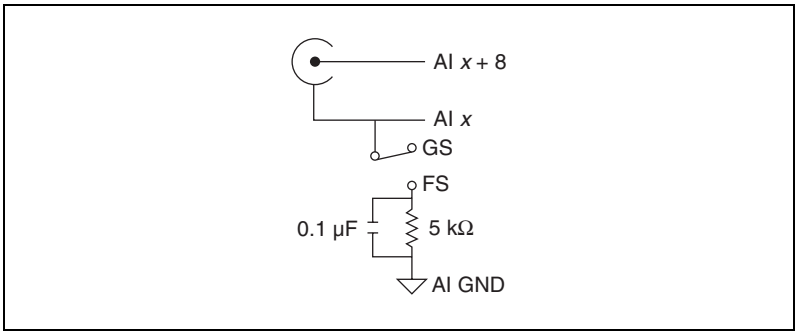



**Figure A-59.** Single-Ended Signals

When you set the source type to the GS position and software-configure the device for single-ended input, each BNC connector provides access to two single-ended channels, AI *x* and AI *x*+8. For example, the BNC connector labeled AI 0 provides access to single-ended channels AI 0 and AI 8, the BNC connector labeled AI 1 provides access to single-ended channels AI 1 and AI 9, and so on. Up to 16 single-ended channels are available in single-ended measurement modes.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

## Analog Output

You can access analog output signals on the BNC connectors labeled AO 0 and AO 1. Figure A-60 shows the analog output circuitry on BNC DAQPads.

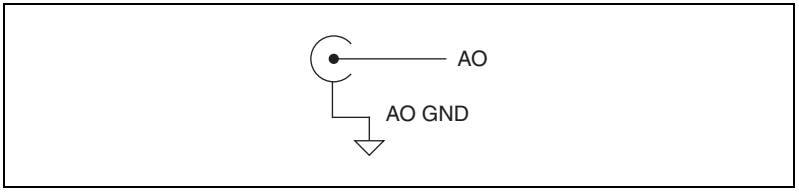



**Figure A-60.** Analog Output Circuitry

Refer to the *Connecting Analog Output Signals* section of Chapter 3, *Analog Output*, for more information.

## AO External Reference

The AO EXT REF input controls the voltage range of analog output signals. Figure A-61 shows circuitry of the AO EXT REF on BNC DAQPads.




**Figure A-61.** AO EXT REF

Refer to the *Reference Selection* section of Chapter 3, *Analog Output,* for more information.

## Counter 0 Out and PFI 0/AI Start Trigger

You can access the Counter 0 Out and PFI 0/AI Start Trigger signals through their respective pins on BNC DAQPads, as shown in Figure A-62 and Figure A-63. Refer to the *Counter 0 Internal Output Signal* section of Chapter 5, *Counters*, for more information on counter signals. Refer to Chapter 6, *Programmable Function Interfaces (PFI)*, for more information on programmable function interface signals. Refer to the *AI Start Trigger Signal* section of Chapter 2, *Analog Input*, for more information.

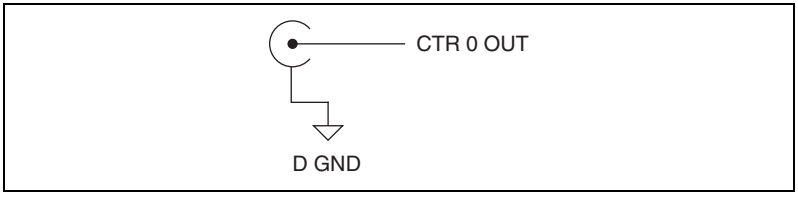



**Figure A-62.** Counter 0 Out

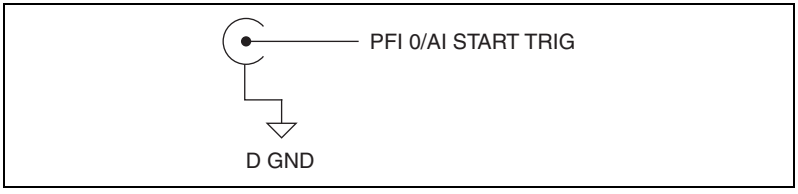



**Figure A-63.** PFI 0/AI Start Trigger

## User <1..2>

The User <1..2> signals connect directly from a screw terminal to a BNC. They allow you to use a BNC connector for a digital or timing I/O signal of your choice. The USER 1 BNC is internally connected to pin 21 and the USER 2 BNC is internally connected to pin 22 on the 30-pin I/O connector. Figure A-64 shows the connection of the User <1..2> BNCs.

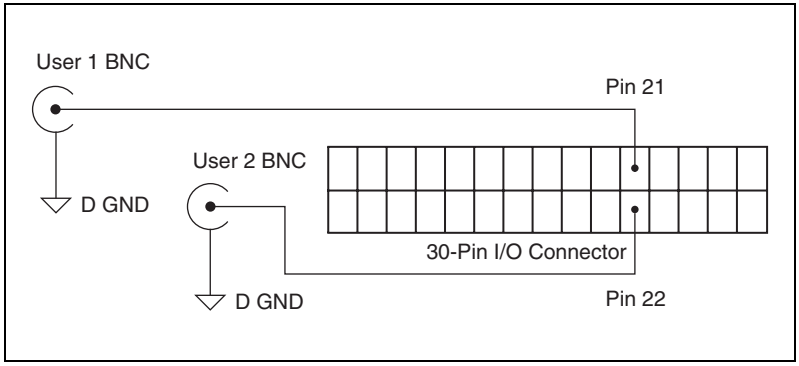



**Figure A-64.** User <1..2> BNCs

Figure A-65 shows another example of how to use the User <1..2> BNCs. To access the Ctr1Out signal from a BNC, connect pin 21 (USER 1) to pin 17 (CTR 1 OUT) with a wire.

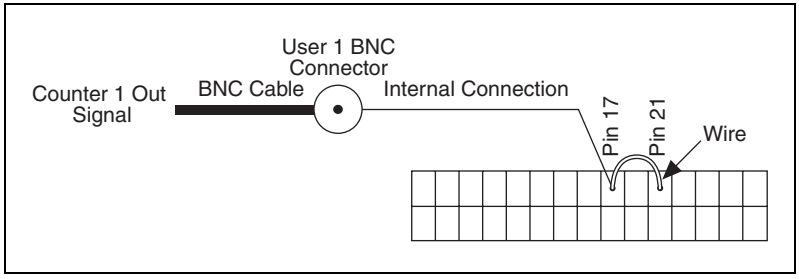



**Figure A-65.** User <1..2> BNC Example

## Other Signals

You can access other signals on BNC DAQPads through a 30-pin Combicon connector.

To connect to one of these signals, use a small screwdriver to press down the orange spring release button at a terminal and insert a wire. Releasing the orange spring release button will lock the wire securely in place.

You can remove the Combicon plugs to assist in connecting wires. Loosening the screws on either side of the two Combicon plugs allows you to detach the Combicon plugs from the BNC DAQPad device, as shown in Figure A-66

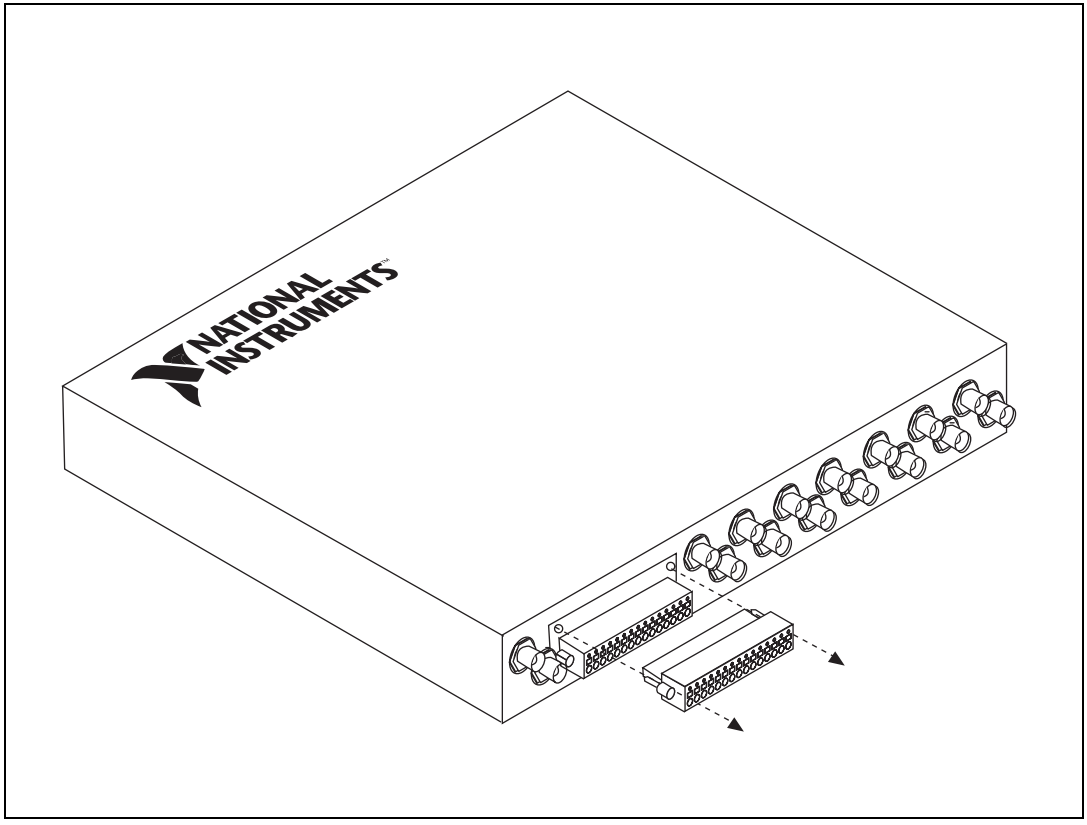



**Figure A-66.** Removing the BNC Combicon

## DAQPad-6052E LED Patterns

The DAQPad-6052E has an LED on its front panel. Refer to Table A-6 for descriptions of each LED state.

**Table A-6.** DAQPad-6052E LEDs

| LED | DAQPad-6052E State |
|---|---|
| On | The device is receiving power and is connected to an active 1394 port. |
| Dim | The device is receiving power but is not connected to an active 1394 port. |
| Off | No power is being provided to the device. |
| 1 blink | — |
| 2 blinks | |
| 4 blinks | |

## NI DAQPad-6052E Pinout

Figure A-70 shows the NI DAQPad-6052E device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5 in Chapter 1 for the Traditional NI-DAQ (Legacy) signal names.

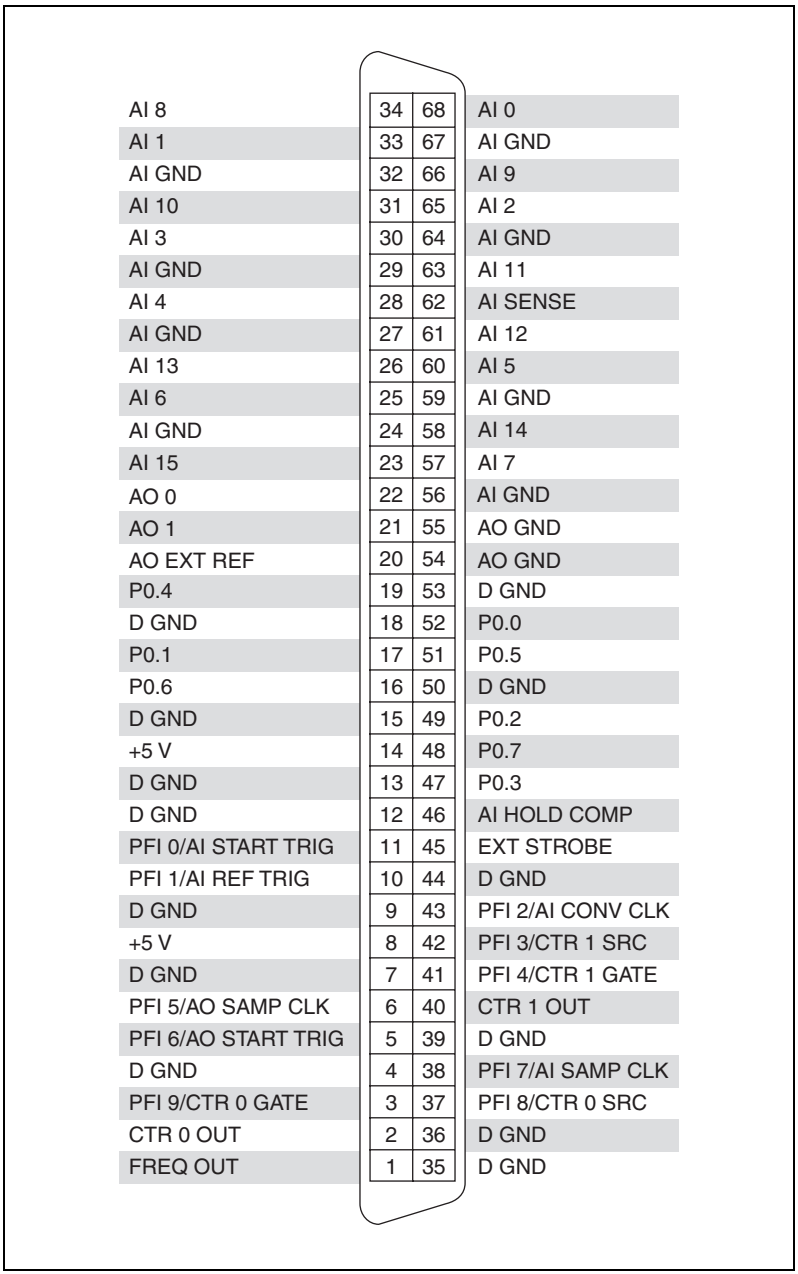



**Figure A-67.** NI DAQPad-6052E Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

## NI DAQPad-6052E BNC Pinout

Figure A-68 shows the NI DAQPad-6052E BNC device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

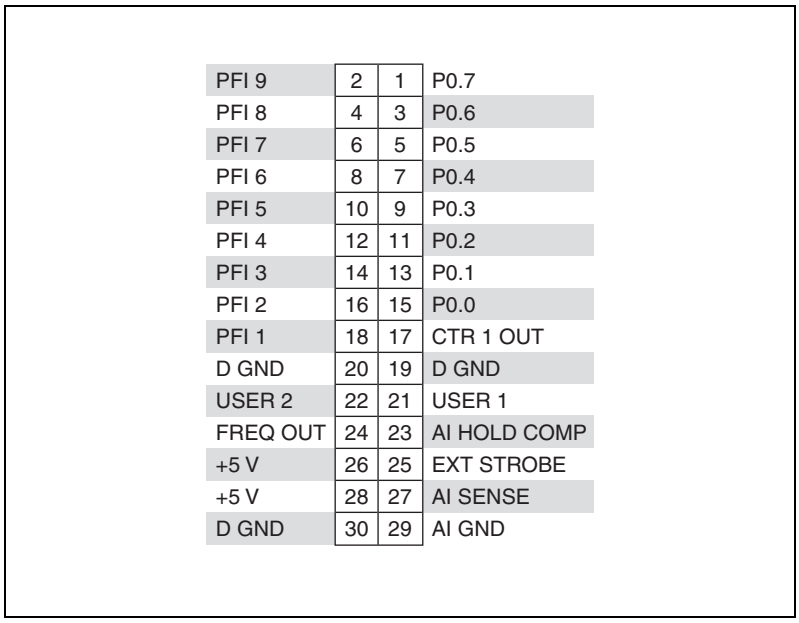



**Figure A-68.** NI DAQPad-6052E BNC Device Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI PCI/PXI-6052E

The NI PCI/PXI-6052E are Plug-and-Play, multifunction AI, AO, DIO, and TIO devices.

The NI PCI/PXI-6052E feature the following:

- 16 AI channels (eight differential) with 16-bit resolution
- Two AO channels with 16-bit resolution
- Eight lines of TTL-compatible DIO

- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

Because the NI 6052E devices have no DIP switches, jumpers, or potentiometers, you can easily configure and calibrate them through software.

## NI PCI/PXI-6052E Block Diagram

Figure A-69 shows a block diagram of the NI PCI/PXI-6052E.

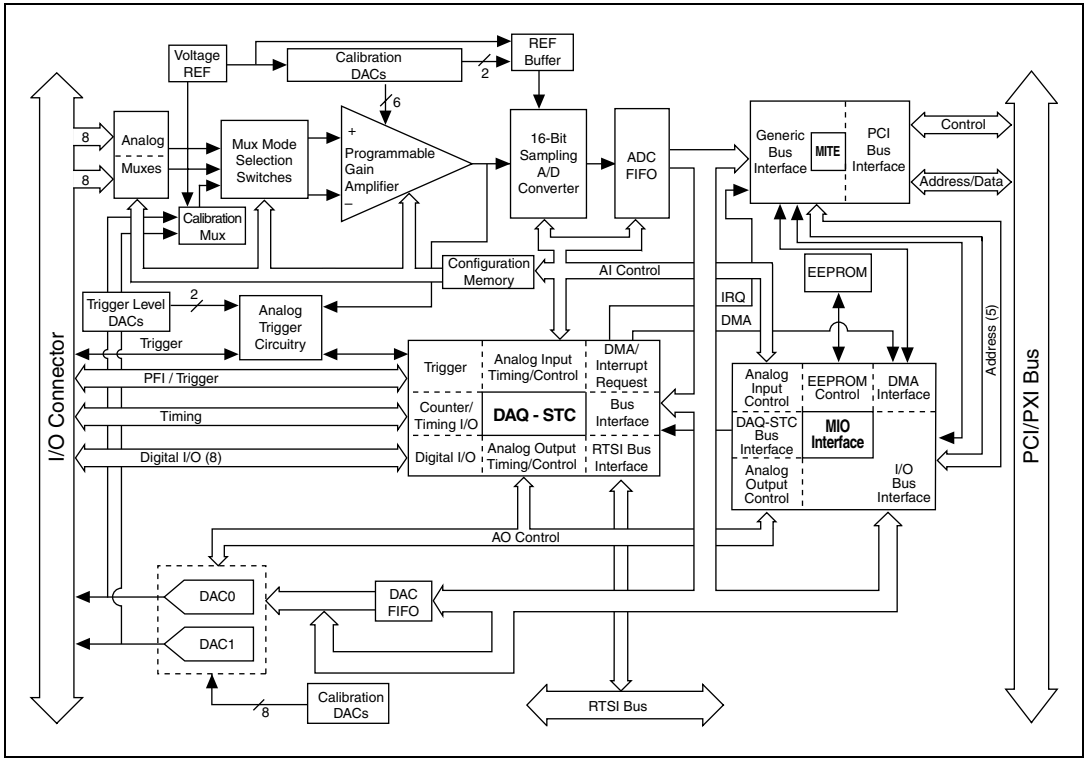



**Figure A-69.** NI PCI/PXI-6052E Block Diagram

## NI PCI/PXI-6052E Pinout

Figure A-70 shows the NI PCI/PXI-6052E device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5 in Chapter 1 for the Traditional NI-DAQ (Legacy) signal names.

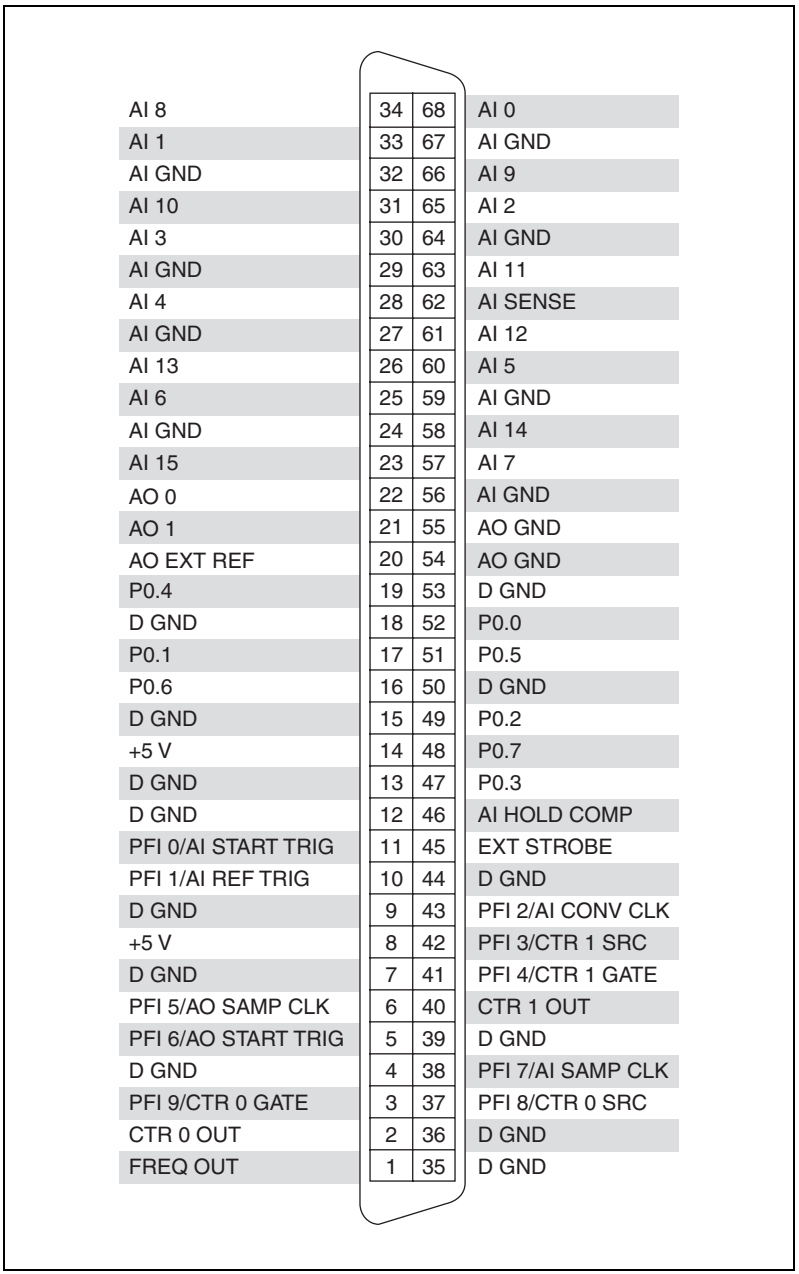



**Figure A-70.** NI PCI/PXI-6052E Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

## NI 6052E Family Specifications

Refer to the *NI 6052E Family Specifications* for more detailed information on the devices.

# NI DAQCard-6062E

The DAQCard-6062E is a multifunction AI, AO, DIO, and TIO DAQ device for computers equipped with Type II PCMCIA slots.

The DAQCard-6062E features the following:

- 16 AI channels (eight differential) with 12-bit resolution
- Two AO channels with 12-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

Because the DAQCard-6062E does not have DIP switches, jumpers, or potentiometers, you can easily configure and calibrate it through software.

## DAQCard-6062E Block Diagram

Figure A-71 shows a block diagram for the DAQCard-6062E.

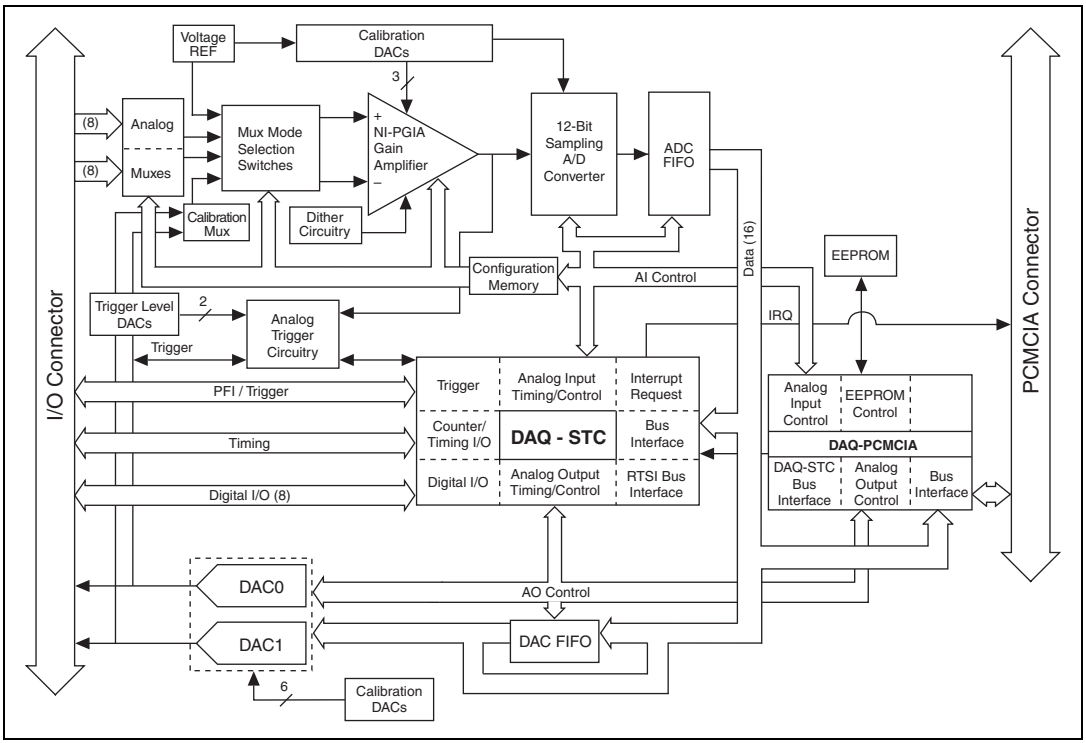



**Figure A-71.** DAQCard-6062E Block Diagram

## DAQCard-6062E Specifications

Refer to the *NI DAQCard-6062E Family Specifications* for more detailed information on the device.

## NI DAQCard-6062E Pinout

Figure A-72 shows the NI 6062E device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

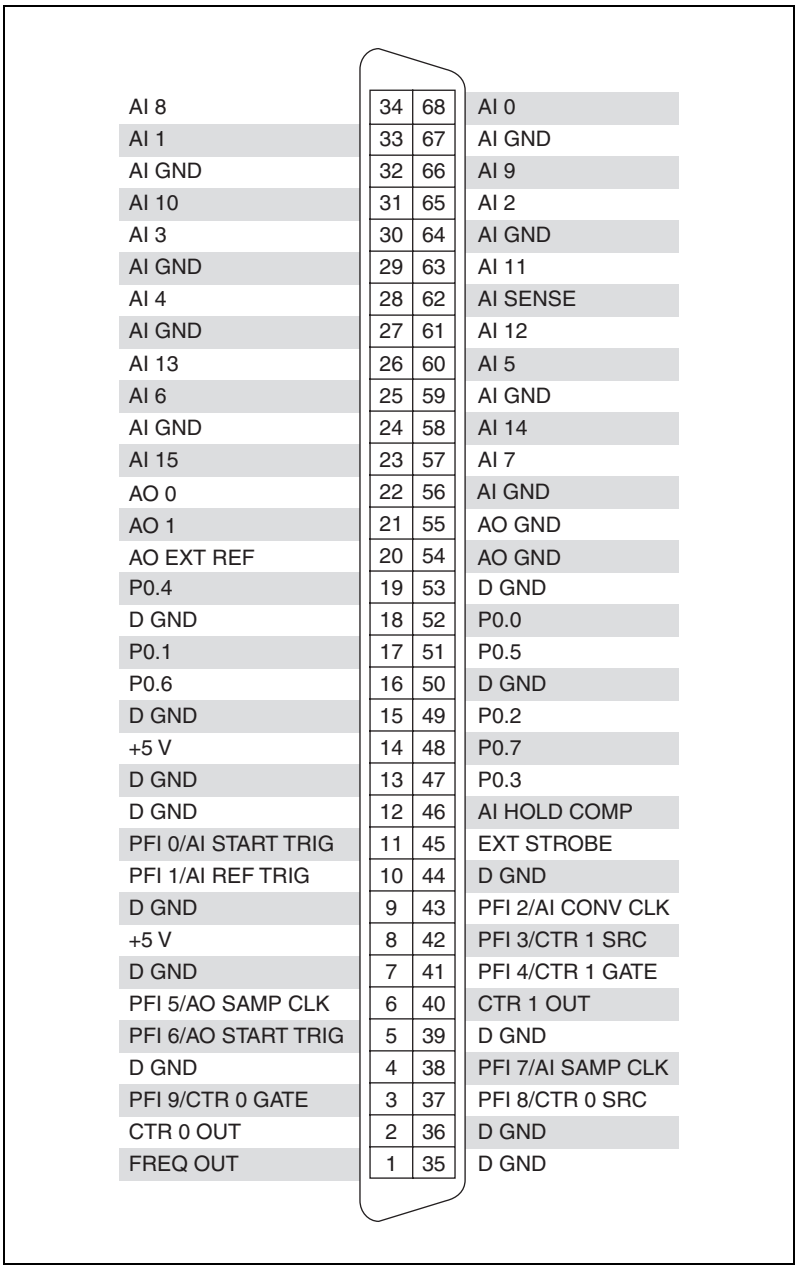



**Figure A-72.** NI 6062E Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI 6070E/6071E Family

## DAQPad-6070E

The DAQPad-6070E is a Plug-and-Play, multifunction AI, AO, DIO, and TIO device.

The DAQPad-6070E features the following:

- 16 AI channels (eight differential) with 12-bit resolution
- Two AO channels with 12-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

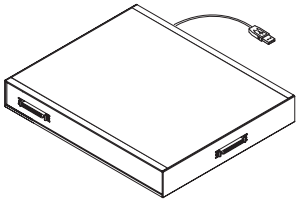
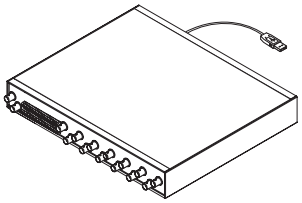
**Note** The BNC version of the DAQPad-6070E has a 30-pin I/O connector.

The DAQPad-6070E is a switchless, jumperless, hot-pluggable DAQ device for 1394. The 1394 interface automatically handles the assignment of all host resources, so you can install the device without powering off the computer. You can connect up to 64 DAQ devices to a single computer using 1394, although you will run out of bus bandwidth if all devices operate at full rate. The DAQPad-6070E provides up to 250 V of DC functional isolation from the PC.

The NI DAQPad-6070E has an onboard watchdog timer that continuously resets the device until the device successfully enumerates with the host operating system and the device driver initiates transactions to the device. To avoid continuous resets, make sure the device and host computer are powered on, the 1394 cable is attached to the host computer, and the device drivers are installed.

There are two versions of the DAQPad-6070E: the DAQPad-6070E with a 68-pin SCSI male I/O connector and the DAQPad-6070E with BNC and removable screw terminal connectors. Table A-7 illustrates the different I/O connectivity and form factors of each version.

**Table A-7.** NI DAQPad-6070E Versions

| DAQ Device | I/O Connector | Form Factor |
|---|---|---|
| DAQPad-6070E  | 68-pin SCSI-II male | Full-size box<br>(12.1 in. × 10 in. × 1.7 in.)<br>Rack-mountable, stackable |
| DAQPad-6070E BNC  | BNC and removable screw terminals | Full-size box<br>(12.1 in. × 10 in. × 1.7 in.)<br>Rack-mountable, stackable |

# DAQPad-6070E Block Diagram

Figure A-73 shows the block diagram of the DAQPad-6070E.

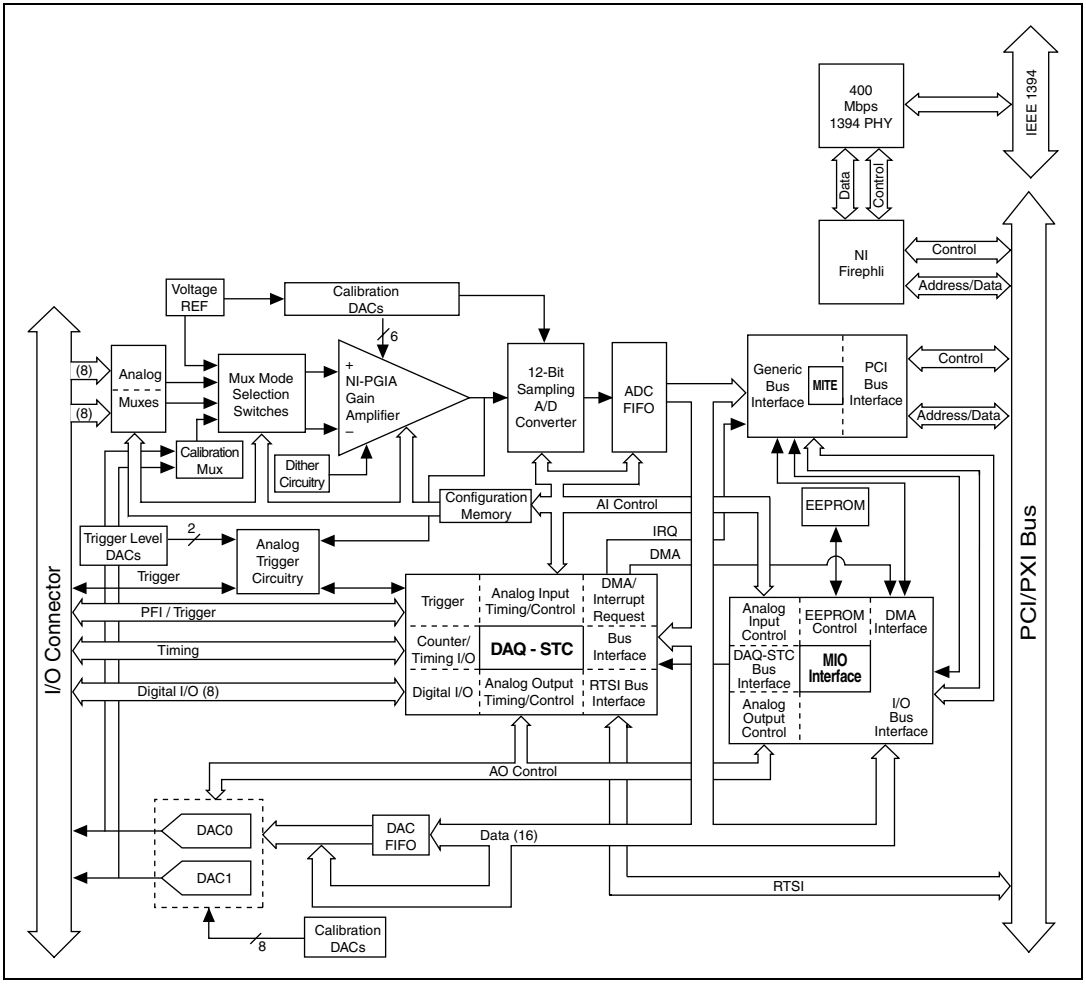



**Figure A-73.** DAQPad-6070E Block Diagram

# Connecting Signals to the NI DAQPad-6070E

## Analog Input

You can use each analog input BNC connector for one differential signal or two single-ended signals.

### Differential Signals

To connect differential signals, determine the type of signal source you are using: a floating signal source or a ground-referenced signal source. Refer to the *Differential Connection Considerations* and *Connecting Analog Input Signals* sections of Chapter 2, *Analog Input*, for more information.

To measure a floating signal source, move the switch to the FS position. To measure a ground-referenced signal source, move the switch to the GS position. Figure A-74 shows the source type switch locations on the front panel of the BNC DAQPads.

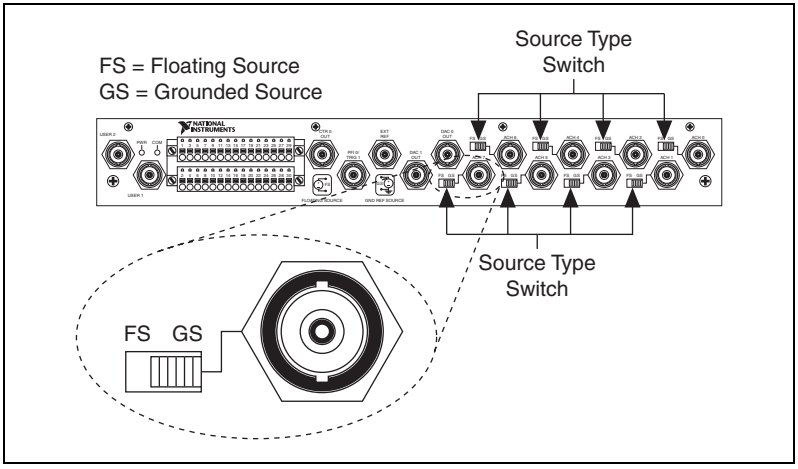



**Figure A-74.** BNC DAQPad Front Panel

Figure A-75 shows the analog input circuitry on BNC DAQPads. When the switch is in the FS position, AI *x* – is grounded through a 0.1 µF capacitor in parallel with a 5 kΩ resistor.

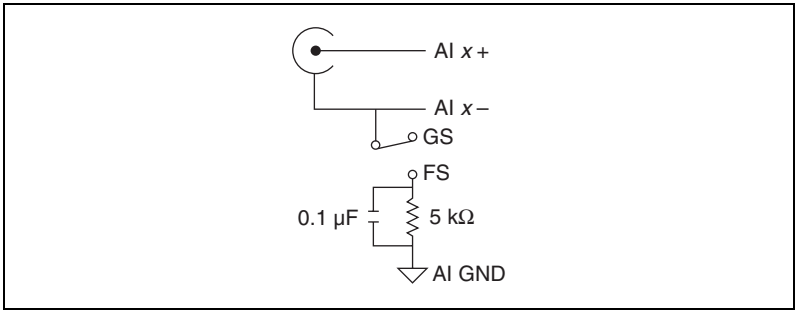



**Figure A-75.** Analog Input Circuitry

### Single-Ended Signals

For each BNC connector that you use for two single-ended channels, set the source type switch to the GS position. This setting disconnects the built-in ground reference resistor from the negative terminal of the BNC connector, allowing the connector to be used as a single-ended channel, as shown in Figure A-76.

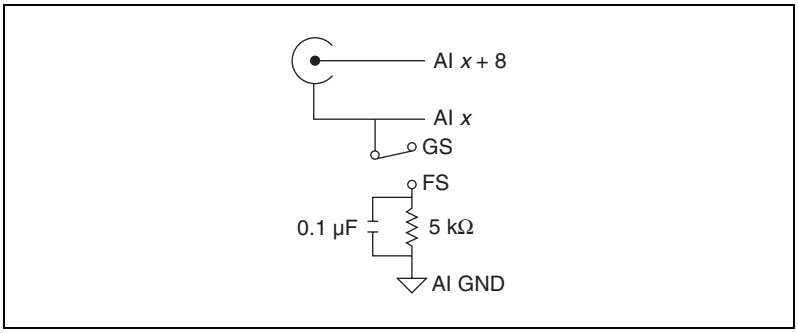



**Figure A-76.** Single-Ended Channel

When you set the source type to the GS position and software-configure the device for single-ended input, each BNC connector provides access to two single-ended channels, AI *x* and AI *x*+8. For example, the BNC connector labeled AI 0 provides access to single-ended channels AI 0 and AI 8, the BNC connector labeled AI 1 provides access to single-ended channels AI 1 and AI 9, and so on. Up to 16 single-ended channels are available in single-ended measurement modes.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

## Analog Output

You can access analog output signals on the BNC connectors labeled AO 0 and AO 1. Figure A-77 shows the analog output circuitry on BNC DAQPads.

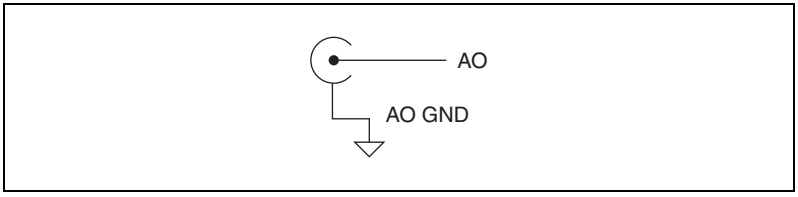



**Figure A-77.** Analog Output

Refer to the *Connecting Analog Output Signals* section of Chapter 3, *Analog Output*, for more information.

## AO External Reference

The AO EXT REF input controls the voltage range of analog output signals. Figure A-78 shows circuitry of the AO EXT REF on BNC DAQPads.




**Figure A-78.** AO EXT REF

Refer to the *Reference Selection* section of Chapter 3, *Analog Output*, for more information.

## Counter 0 Out and PFI 0/AI Start Trigger

You can access the Counter 0 Out and PFI 0/AI Start Trigger signals through their respective pins on BNC DAQPads, as shown in Figure A-79 and Figure A-80.

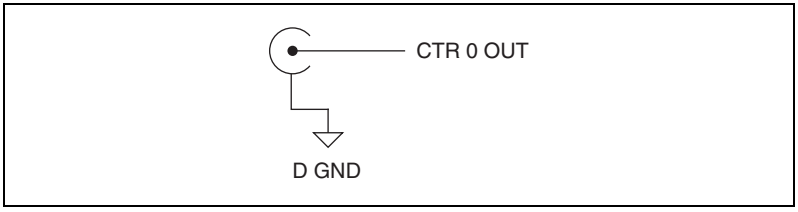



**Figure A-79.** Counter 0 Out

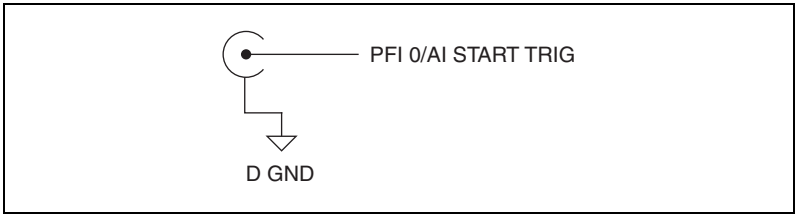



**Figure A-80.** PFI 0/AI Start Trigger

## User <1..2>

The User <1..2> signals connect directly from a screw terminal to a BNC. They allow you to use a BNC connector for a digital or timing I/O signal of your choice. The USER 1 BNC is internally connected to pin 21 and the USER 2 BNC is internally connected to pin 22 on the 30-pin I/O connector. Figure A-81 shows the connection of the User <1..2> BNCs.

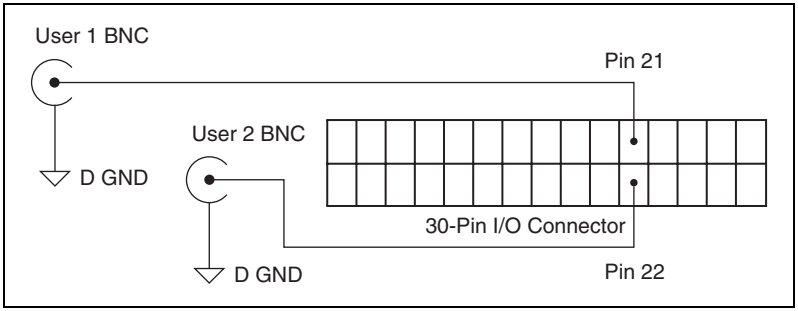



**Figure A-81.** User <1..2> BNCs

Figure A-82 shows another example of how to use the User <1..2> BNCs. To access the Ctr1Out signal from a BNC, connect pin 21 (USER 1) to pin 17 (CTR 1 OUT) with a wire.

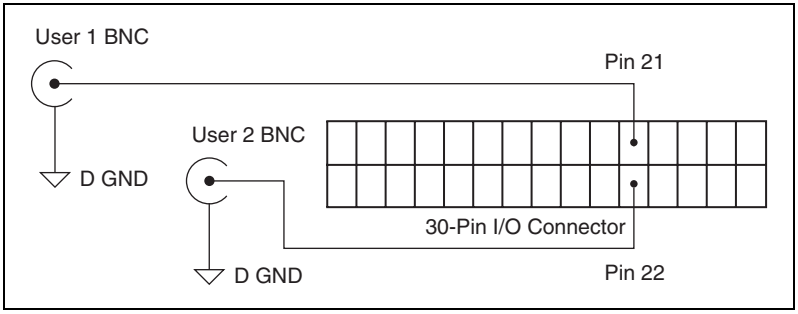



**Figure A-82.** User <1..2> BNC Example

## Other Signals

You can access other signals on BNC DAQPads through a 30-pin Combicon connector.

To connect to one of these signals, use a small screwdriver to press down the orange spring release button at a terminal and insert a wire. Releasing the orange spring release button will lock the wire securely in place.

You can remove the Combicon plugs to assist in connecting wires. Loosening the screws on either side of the two Combicon plugs allows you to detach the Combicon plugs from the BNC DAQPad device, as shown in Figure A-83.

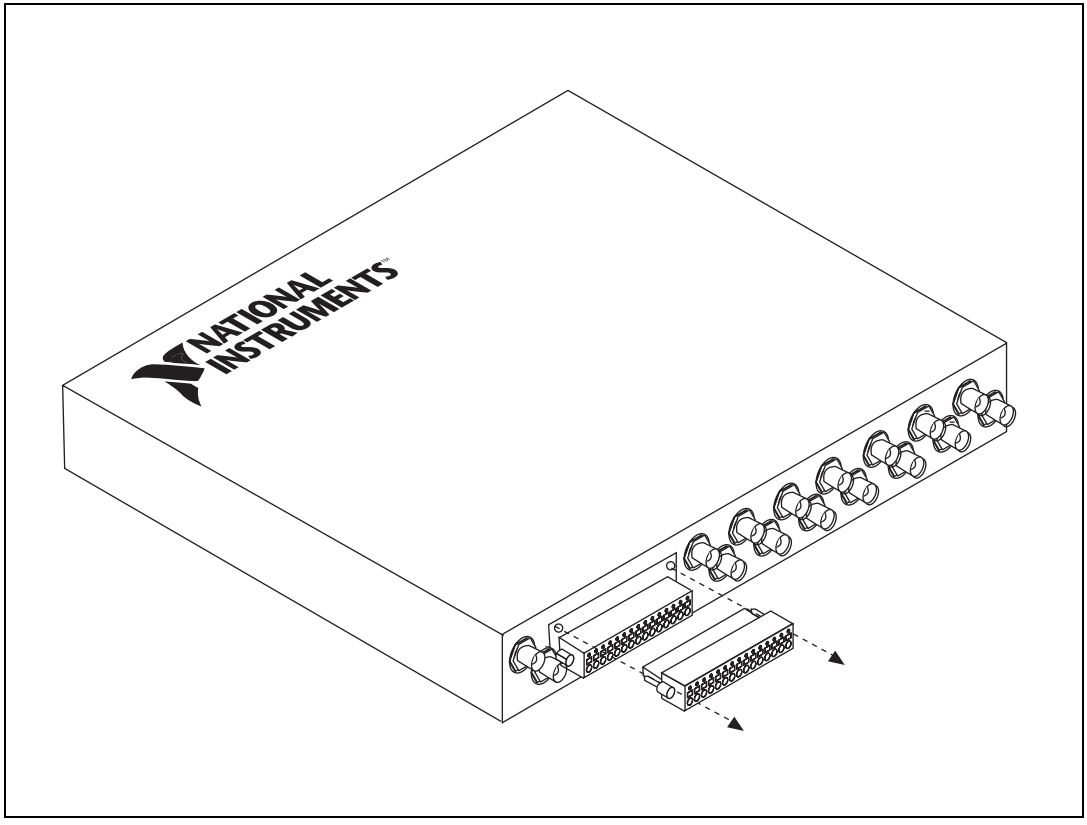



**Figure A-83.** Removing the BNC Combicon

## DAQPad-6070E LED Patterns

The DAQPad-6070E has an LED on its front panel. Refer to Table A-8 for descriptions of each LED state.

**Table A-8.** DAQPad-6070E LEDs

| LED | DAQPad-6070E State |
|---|---|
| On | The device is receiving power and is connected to an active 1394 port. |
| Dim | The device is receiving power but is not connected to an active 1394 port. |
| Off | No power is being provided to the device. |
| 1 blink | — |
| 2 blinks | |
| 4 blinks | |

## NI DAQPad-6070E BNC Pinout

Figure A-84 shows the NI DAQPad-6070E BNC device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

| | | | |
|---|---|---|---|
| PFI 9 | 2 | 1 | P0.7 |
| PFI 8 | 4 | 3 | P0.6 |
| PFI 7 | 6 | 5 | P0.5 |
| PFI 6 | 8 | 7 | P0.4 |
| PFI 5 | 10 | 9 | P0.3 |
| PFI 4 | 12 | 11 | P0.2 |
| PFI 3 | 14 | 13 | P0.1 |
| PFI 2 | 16 | 15 | P0.0 |
| PFI 1 | 18 | 17 | CTR 1 OUT |
| D GND | 20 | 19 | D GND |
| USER 2 | 22 | 21 | USER 1 |
| FREQ OUT | 24 | 23 | AI HOLD COMP |
| +5 V | 26 | 25 | EXT STROBE |
| +5 V | 28 | 27 | AI SENSE |
| D GND | 30 | 29 | AI GND |

**Figure A-84.** NI DAQPad-6070E BNC Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

## NI PCI/PXI-6070E and NI PCI-6071E

The NI 6070E/6071E are Plug-and-Play, multifunction AI, AO, DIO, and TIO devices.

The NI 6070E features the following:

- 16 AI channels (eight differential) with 12-bit resolution
- Two AO channels with 12-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

The NI 6071E features the following:

- 64 AI channels (32 differential) with 12-bit resolution
- Two AO channels with 12-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 100-pin extended AI connector

Because the NI 6070E/6071E have no DIP switches, jumpers, or potentiometers, you can easily configure and calibrate them through software.

## NI 6070E/6071E Block Diagram

Figure A-85 shows a block diagram of the NI PCI/PXI-6070E and NI PCI-6071E.

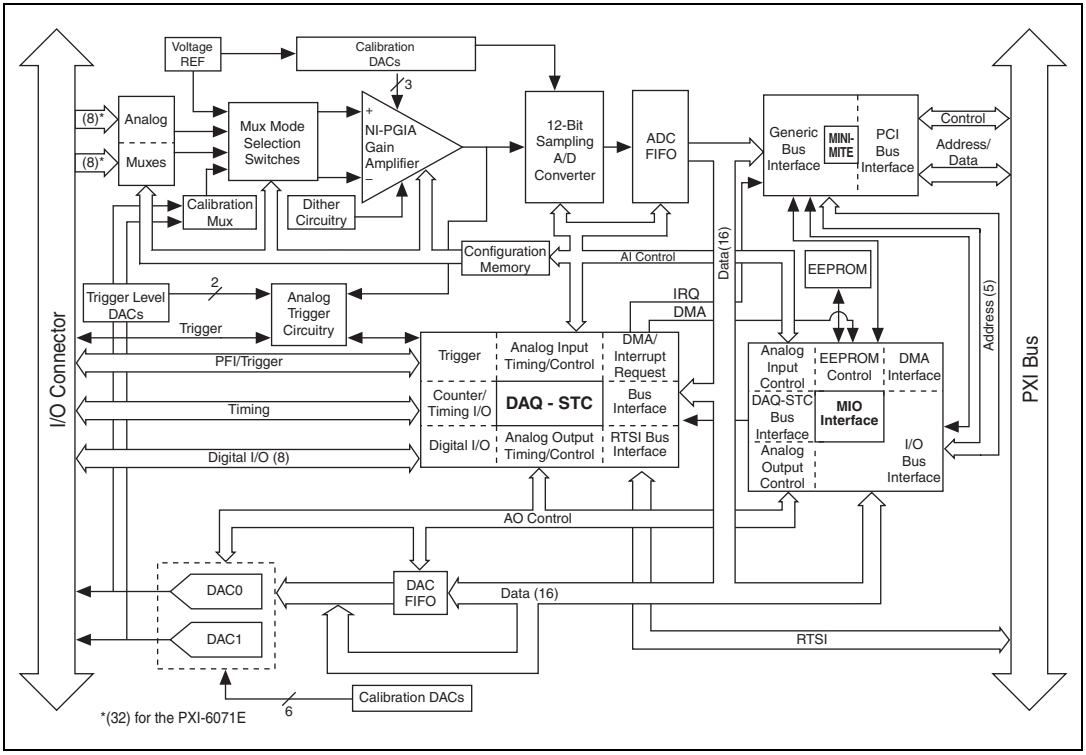



**Figure A-85.** NI 6070E/6071E Block Diagram

## NI PCI/PXI-6070E Pinout

Figure A-86 shows the NI 6070E device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

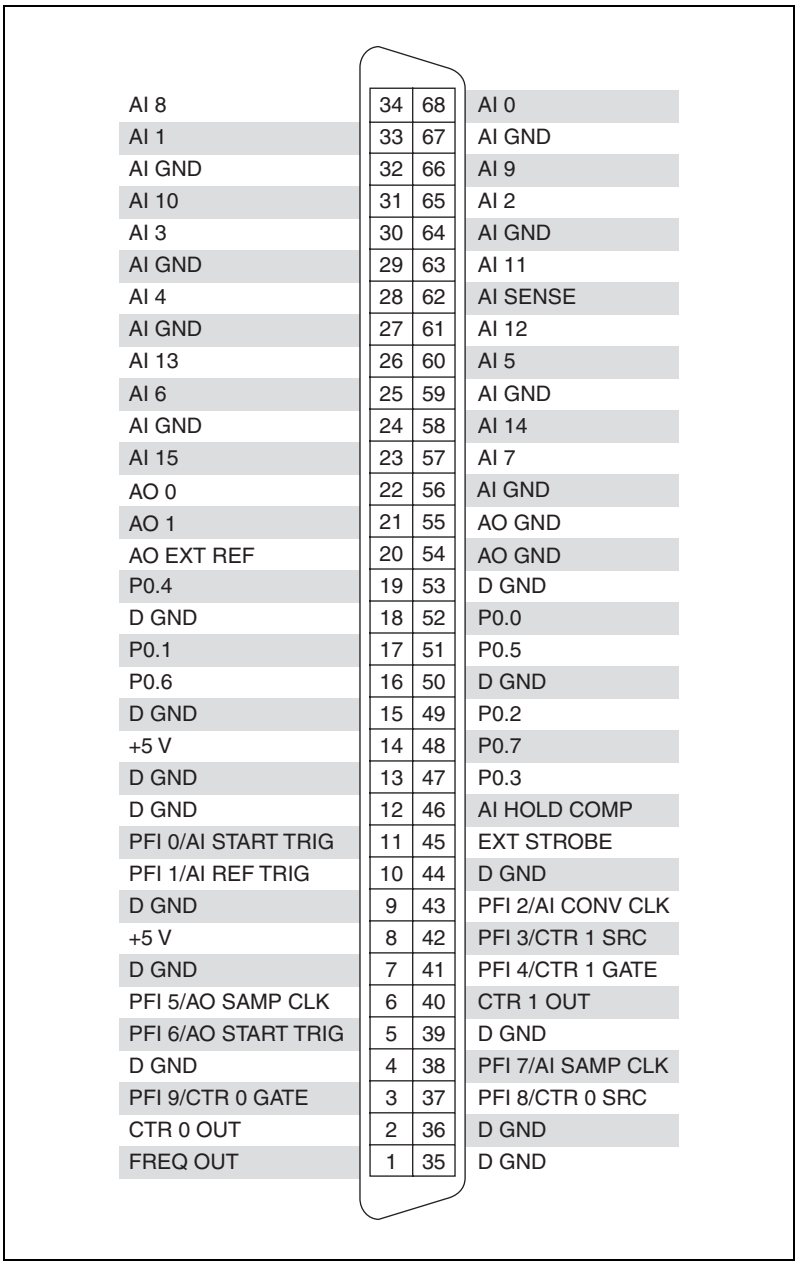



**Figure A-86.** NI PCI/PXI-6070E Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

## NI PCI-6071E Pinout

Figure A-87 shows the NI 6071E device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

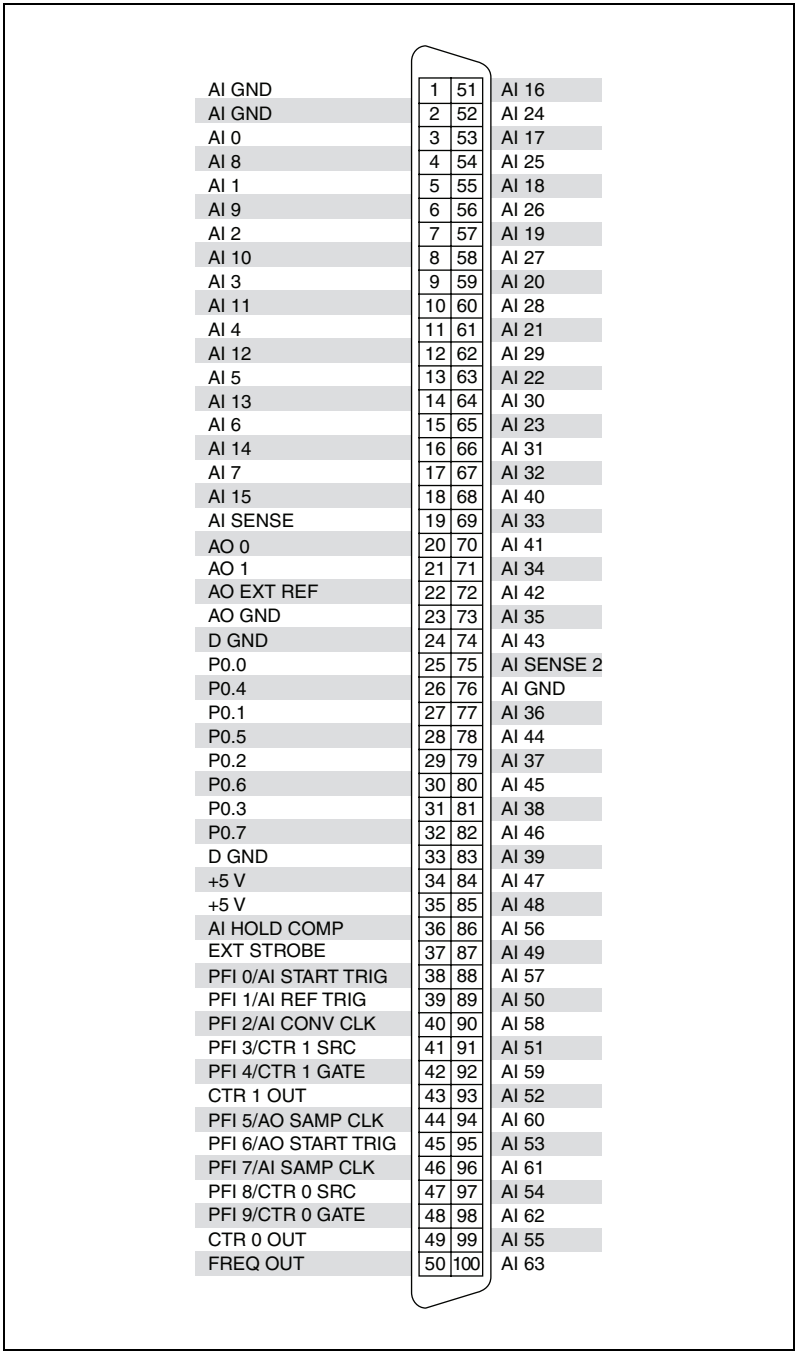



**Figure A-87.** NI PCI-6071E Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

## PCI-MIO-16E-1

The PCI-MIO-16E-1 is a Plug-and-Play, multifunction AI, AO, DIO, and TIO device for PCI bus computers.

The PCI-MIO-16E-1 features the following:

- 16 AI channels (eight differential) with 12-bit resolution
- Two AO channels with 12-bit resolution
- Eight lines of TTL-compatible DIO
- Two 24-bit counter/timers for TIO
- A 68-pin I/O connector

Because the PCI-MIO-16E-1 has no DIP switches, jumpers, or potentiometers, you can easily configure and calibrate it through software.

# PCI-MIO-16E-1 Block Diagram

Figure A-88 shows a block diagram of the PCI-MIO-16E-1.

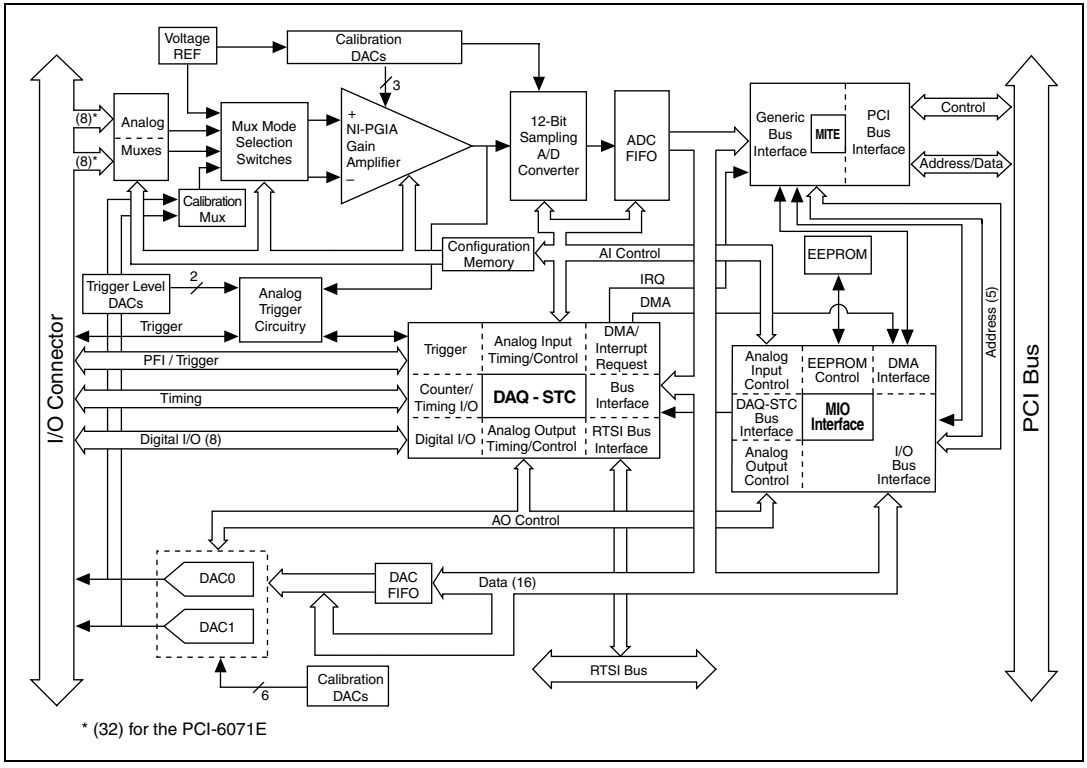



**Figure A-88.** PCI-MIO-16E-1 Block Diagram

# NI PCI-MIO-16E-1 (NI 6070E) Pinout

Figure A-89 shows the PCI-MIO-16E-1 (NI 6070E) device pinout.

**Note** Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an E Series device in Traditional NI-DAQ (Legacy), refer to Table 1-5, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

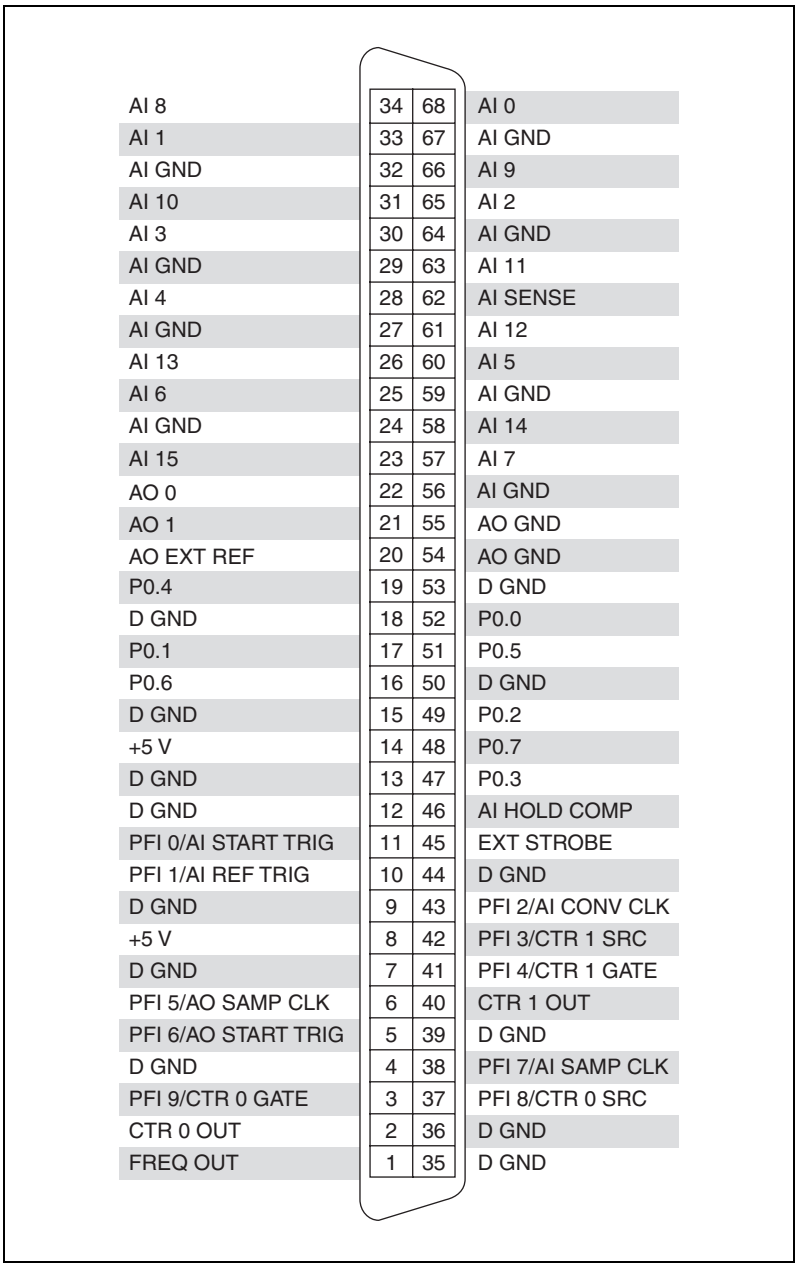



**Figure A-89.** NI PCI-MIO-16E-1 (NI 6070E) Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 1, *DAQ System Overview*.

# NI 6070E/6071E Specifications

Refer to the *NI 6070E/6071E Family Specifications* for more detailed information on the devices.

# B

# I/O Connector Pinouts

Table  corresponds each E Series device to the associated I/O connector pinouts for that device and compatible accessories.

**Table B-1.** E Series I/O Connector Pinouts

| E Series Device | Typical Cable | Accessory |
|---|---|---|
| NI 6013 | SH6868EP | Refer to Figure A-4. |
| | SH6850 | Refer to Figure B-4. |
| NI 6014 | SH6868EP | Refer to Figure A-5. |
| | SH6850 | Refer to Figure B-4. |
| NI DAQPad-6015 | — | — |
| NI DAQPad-6015 BNC | — | — |
| NI DAQPad-6015 Mass Termination | — | — |
| NI DAQPad-6016 | — | — |
| NI DAQPad-6020E | SH6868EP | Refer to Figure A-33. |
| | SH6850 | Refer to Figure B-4. |
| NI DAQPad-6020E BNC | — | — |
| NI 6023E | SH6868EP | Refer to Figure A-37. |
| | SH6850 | Refer to Figure B-4. |
| NI 6024E | SH6868EP | Refer to Figure A-38. |
| | SH6850 | Refer to Figure B-4. |
| NI 6025E | SH1006868 | Refer to Figure B-2. |
| | SH100100 | Refer to Figure A-39. |
| | R1005050 | Refer to Figure B-3. |

**Table B-1.** E Series I/O Connector Pinouts (Continued)

| E Series Device | Typical Cable | Accessory |
|---|---|---|
| NI 6030E | SH6868EP | Refer to Figure A-42. |
| | SH6850 | Refer to Figure B-4. |
| NI 6031E | SH1006868 | Refer to Figure B-1. |
| | SH100100 | Refer to Figure A-44. |
| | R1005050 | Refer to Figure B-3. |
| NI 6032E | SH6868EP | Refer to Figure A-45. |
| | SH6850 | Refer to Figure B-4. |
| NI 6033E | SH1006868 | Refer to Figure B-1. |
| | SH100100 | Refer to Figure A-46. |
| | R1005050 | Refer to Figure B-3. |
| NI 6034E | SH6868EP | Refer to Figure A-49. |
| | SH6850 | Refer to Figure B-4. |
| NI 6035E | SH6868EP | Refer to Figure A-50. |
| | SH6850 | Refer to Figure B-4. |
| NI 6036E | SH6868EP | Refer to Figure A-51. |
| | SH6850 | Refer to Figure B-4. |
| NI 6040E | SH6868EP | Refer to Figure A-53. |
| | SH6850 | Refer to Figure B-4. |
| NI 6052E | SH6868EP | Refer to Figure A-70. |
| | SH6850 | Refer to Figure B-4. |
| NI DAQPad-6052E BNC | — | — |
| NI 6062E | SH6868EP | Refer to Figure A-72. |
| | SH6850 | Refer to Figure B-4. |
| NI PCI/PXI-6070E | SH6868EP | Refer to Figure A-86. |
| | SH6850 | Refer to Figure B-4. |
| NI DAQPad-6070E BNC | — | — |

**Table B-1.** E Series I/O Connector Pinouts (Continued)

| E Series Device | Typical Cable | Accessory |
|---|---|---|
| NI PCI-6071E | SH1006868 | Refer to Figure B-1. |
| | SH100100 | Refer to Figure A-87. |
| | R1005050 | Refer to Figure B-3. |
| NI PCI-MIO-16E-1 (NI 6070E) | SH6868EP | Refer to Figure A-88. |
| | SH6850 | Refer to Figure B-4. |
| NI PCI-MIO-16E-4 (NI 6040E) | SH6868EP | Refer to Figure A-55. |
| | SH6850 | Refer to Figure B-4. |
| NI PCI-MIO-16XE-10 (NI 6030E) | SH6868EP | Refer to Figure A-43. |
| | SH6850 | Refer to Figure B-4. |
| NI PCI-MIO-16XE-50 (NI 6011E) | SH6868EP | Refer to Figure A-2. |
| | SH6850 | Refer to Figure B-4. |

# 100-68-68-Pin

## 100-68-68-Pin Extended AI I/O Connector Pinout

When you use an NI 6031E/6033E/6071E with an SH1006868 cable, the I/O signals appear on two 68-pin connectors. Figure B-1 shows the pinouts of the two connectors.

## 100-68-68-Pin Extended DIO I/O Connector Pinout

When you use an NI 6025E with an SH1006868 cable, the I/O signals appear on two 68-pin connectors. Figure B-2 shows the pinouts of the two connectors.




**Figure B-1.** 100-68-68-Pin Extended AI I/O Connector Pinout




**Figure B-2.** 100-68-68-Pin Extended DIO I/O Connector Pinout

# 100-50-50-Pin

## 100-50-50-Pin Extended AI I/O Connector Pinout

When you use the NI 6025E with an R1005050 cable assembly, the signals appear on two 50-pin connectors. Figure B-3 shows the pinouts of the 50-pin connectors.

# 100-50-50-Pin Extended DIO I/O Connector Pinout

When you use the NI 6025E with an R1005050 cable assembly, the signals appear on two 50-pin connectors. Figure B-3 shows the pinouts of the 50-pin connectors.

| Positions 1–50 Connector | | | | Positions 51–100 Connector | | | |
|---|---|---|---|---|---|---|---|
| AI GND | 1 | 2 | AI GND | P3.7 | 1 | 2 | D GND |
| AI 0 | 3 | 4 | AI 8 | P3.6 | 3 | 4 | D GND |
| AI 1 | 5 | 6 | AI 9 | P3.5 | 5 | 6 | D GND |
| AI 2 | 7 | 8 | AI 10 | P3.4 | 7 | 8 | D GND |
| AI 3 | 9 | 10 | AI 11 | P3.3 | 9 | 10 | D GND |
| AI 4 | 11 | 12 | AI 12 | P3.2 | 11 | 12 | D GND |
| AI 5 | 13 | 14 | AI 13 | P3.1 | 13 | 14 | D GND |
| AI 6 | 15 | 16 | AI 14 | P3.0 | 15 | 16 | D GND |
| AI 7 | 17 | 18 | AI 15 | P2.7 | 17 | 18 | D GND |
| AI SENSE | 19 | 20 | AO 0[1] | P2.6 | 19 | 20 | D GND |
| AO 1[1] | 21 | 22 | AO EXT REF[1] | P2.5 | 21 | 22 | D GND |
| AO GND[1] | 23 | 24 | D GND | P2.4 | 23 | 24 | D GND |
| P0.0 | 25 | 26 | P0.4 | P2.3 | 25 | 26 | D GND |
| P0.1 | 27 | 28 | P0.5 | P2.2 | 27 | 28 | D GND |
| P0.2 | 29 | 30 | P0.6 | P2.1 | 29 | 30 | D GND |
| P0.3 | 31 | 32 | P0.7 | P2.0 | 31 | 32 | D GND |
| D GND | 33 | 34 | +5 V | P1.7 | 33 | 34 | D GND |
| +5 V | 35 | 36 | AI HOLD COMP | P1.6 | 35 | 36 | D GND |
| EXT STROBE | 37 | 38 | PFI 0/AI START TRIG | P1.5 | 37 | 38 | D GND |
| PFI 1/AI REF TRIG | 39 | 40 | PFI 2/AI CONV CLK | P1.4 | 39 | 40 | D GND |
| PFI 3/CTR 1 SRC | 41 | 42 | PFI 4/CTR 1 GATE | P1.3 | 41 | 42 | D GND |
| CTR 1 OUT | 43 | 44 | PFI 5/AI SAMP CLK | P1.2 | 43 | 44 | D GND |
| PFI 6/AO START TRIG | 45 | 46 | PFI 7/AI SAMP CLK | P1.1 | 45 | 46 | D GND |
| PFI 8/CTR 0 SRC | 47 | 48 | PFI 9/CTR 0 GATE | P1.0 | 47 | 48 | D GND |
| CTR 0 OUT | 49 | 50 | FREQ OUT | +5 V | 49 | 50 | D GND |

[1] No connects appear on pins 20 through 23 of devices that do not support AO or use an external reference.

**Figure B-3.** 100-50-50-Pin Extended DIO I/O Connector Pinout

# 50-Pin MIO I/O Connector Pinout

Figure B-4 shows the 50-pin I/O connector that is available when you use the R6850 or SH6850 cable assemblies with 68-pin E Series devices.

| | | | |
|---|---|---|---|
| AI GND | 1 | 2 | AI GND |
| AI 0 | 3 | 4 | AI 8 |
| AI 1 | 5 | 6 | AI 9 |
| AI 2 | 7 | 8 | AI 10 |
| AI 3 | 9 | 10 | AI 11 |
| AI 4 | 11 | 12 | AI 12 |
| AI 5 | 13 | 14 | AI 13 |
| AI 6 | 15 | 16 | AI 14 |
| AI 7 | 17 | 18 | AI 15 |
| AI SENSE | 19 | 20 | AO 0[1] |
| AO 1[1] | 21 | 22 | AO EXT REF[1] |
| AO GND[1] | 23 | 24 | D GND |
| P0.0 | 25 | 26 | P0.4 |
| P0.1 | 27 | 28 | P0.5 |
| P0.2 | 29 | 30 | P0.6 |
| P0.3 | 31 | 32 | P0.7 |
| D GND | 33 | 34 | +5 V |
| +5 V | 35 | 36 | AI HOLD COMP |
| EXT STROBE | 37 | 38 | PFI 0/AI START TRIG |
| PFI 1/AI REF TRIG | 39 | 40 | PFI 2/AI CONV CLK |
| PFI 3/CTR 1 SRC | 41 | 42 | PFI 4/CTR 1 GATE |
| CTR 1 OUT | 43 | 44 | PFI 5/AI SAMP CLK |
| PFI 6/AO START TRIG | 45 | 46 | PFI 7/AI SAMP CLK |
| PFI 8/CTR 0 SRC | 47 | 48 | PFI 9/CTR 0 GATE |
| CTR 0 OUT | 49 | 50 | FREQ OUT |

[1] No connects appear on pins 20 through 23 of devices that do not support AO or use an external reference.

**Figure B-4.** 50-Pin MIO I/O Connector Pinout

# C

# Troubleshooting

This appendix contains some common questions about E Series devices. If your questions are not answered here, refer to the National Instruments KnowledgeBase at `ni.com`. It contains thousands of documents that answer frequently asked questions about NI products.

## Analog Input

**I am seeing crosstalk or ghost voltages when sampling multiple channels. What does this mean?**

You may be experiencing a phenomenon called *charge injection*, which occurs when you sample a series of high-output impedance sources with a multiplexer. Multiplexers contain switches, usually made of switched capacitors. When a channel, for example AI 0, is selected in a multiplexer, those capacitors accumulate charge. When the next channel, for example AI 1, is selected, the accumulated current (or charge) leaks backward through that channel. If the output impedance of the source connected to AI 1 is high enough, the resulting reading can somewhat reflect the voltage trends in AI 0. To circumvent this problem, use a voltage follower that has operational amplifiers (op-amps) with unity gain for each high-impedance source before connecting to an E Series device. Otherwise, you must decrease the sample rate for each channel.

Another common cause of channel crosstalk is due to sampling among multiple channels at various gains. In this situation, the settling times can increase. For more information about charge injection and sampling channels at different gains, refer to the *Multichannel Scanning Considerations* section of Chapter 2, *Analog Input.*

**I am using my device in differential analog input mode and I have connected a differential input signal, but my readings are random and drift rapidly. What is wrong?**

In DIFF mode, if the readings from the DAQ device are random and drift rapidly, you should check the ground-reference connections. The signal can be referenced to a level that is considered floating with reference to the device ground reference. Even if you are in DIFF mode, you must still

reference the signal to the same ground level as the device reference. There are various methods of achieving this reference while maintaining a high common-mode Rejection Ratio (CMRR). These methods are outlined in the *Connecting Analog Input Signals* section of Chapter 2, *Analog Input*.

AI GND is an AI common signal that routes directly to the ground connection point on the devices. You can use this signal if you need a general analog ground connection point to the device. Refer to the *Differential Connection Considerations* section of Chapter 2, *Analog Input*, for more information.

**How can I use the AI Sample Clock and AI Convert Clock signals on an E Series device to sample the AI channel(s)?**

E Series devices use the ai/SampleClock and ai/ConvertClock signals to perform interval sampling. As Figure C-1 shows, ai/SampleClock controls the sample period, which is determined by the following equation:

1/sample period = sample rate

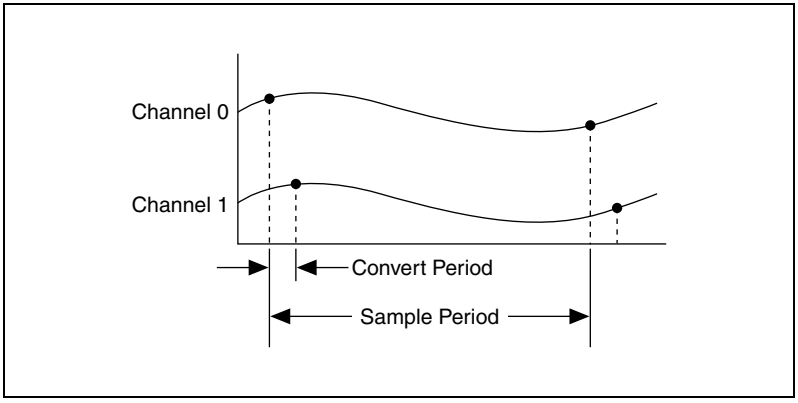



**Figure C-1.** Interval Sample

The ai/ConvertClock signal controls the convert period, which is determined by the following equation:

1/convert period = convert rate

This method allows multiple channels to be sampled relatively quickly in relationship to the overall scan rate, providing a nearly simultaneous effect with a fixed delay between channels.

# Register-Level Programming Information



**Caution** NI is *not* liable for any damage or injury that results from register-level programming the E Series devices.

Refer to `ni.com/manuals` for register-level programming manuals that are available for E Series devices.

The National Instruments Measurement Hardware DDK provides development tools and a register-level programming interface for NI data acquisition hardware. The NI Measurement Hardware DDK provides access to the full register map of each device and offers examples for completing common measurement and control functions. The Measurement Hardware DDK works with E Series multifunction, analog output, digital I/O, and counter/timer I/O devices. Refer to `ni.com` for more information.



**Note** Register-level programming documentation is *not* available for every E Series device.

# D

# Technical Support and Professional Services

Visit the following sections of the National Instruments Web site at ni.com for technical support and professional services:

- **Support**—Online technical support resources at ni.com/support include the following:
  - **Self-Help Resources**—For answers and solutions, visit the award-winning National Instruments Web site for software drivers and updates, a searchable KnowledgeBase, product manuals, step-by-step troubleshooting wizards, thousands of example programs, tutorials, application notes, instrument drivers, and so on.
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    For information about other technical support options in your area, visit ni.com/services or contact your local office at ni.com/contact.
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- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, National Instruments Alliance Partner members can help. To learn more, call your local NI office or visit ni.com/alliance.
- **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electronic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting ni.com/certification.

- **Calibration Certificate**—If your product supports calibration, you can obtain the calibration certificate for your product at `ni.com/calibration`.

If you searched `ni.com` and could not find the answers you need, contact your local office or NI corporate headquarters. Phone numbers for our worldwide offices are listed at the front of this manual. You also can visit the Worldwide Offices section of `ni.com/niglobal` to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

# Glossary

| Symbol | Prefix | Value |
|---|---|---|
| p | pico | $10^{-12}$ |
| n | nano | $10^{-9}$ |
| μ | micro | $10^{-6}$ |
| m | milli | $10^{-3}$ |
| k | kilo | $10^{3}$ |
| M | mega | $10^{6}$ |
| G | giga | $10^{9}$ |
| T | tera | $10^{12}$ |

## Symbols

| | |
|---|---|
| % | Percent. |
| + | Positive of, or plus. |
| / | Per. |
| ° | Degree. |
| Ω | Ohm. |

## A

| | |
|---|---|
| A | Amperes—the unit of electric current. |
| AC | Alternating current. |
| ADE | Application development environment. |
| AI | Analog input. Analog input channel signal. |
| AI GND | Analog input ground signal. |

| | |
|---|---|
| AI SENSE | Analog input sense signal. |
| AO | Analog output. |
| AO 0 | Analog channel 0 output signal. |
| AO 1 | Analog channel 1 output signal. |
| AO GND | Analog output ground signal. |

## B

| | |
|---|---|
| bipolar | A signal range that includes both positive and negative values (for example, −5 to +5 V). |

## C

| | |
|---|---|
| channel | Physical—a terminal or pin at which you can measure or generate an analog or digital signal. A single physical channel can include more than one terminal, as in the case of a differential analog input channel or a digital port of eight lines. The name used for a counter physical channel is an exception because that physical channel name is not the name of the terminal where the counter measures or generates the digital signal.<br><br>Virtual—a collection of property settings that can include a name, a physical channel, input terminal connections, the type of measurement or generation, and scaling information. You can define NI-DAQmx virtual channels outside a task (global) or inside a task (local). Configuring virtual channels is optional in Traditional NI-DAQ (Legacy) and earlier versions, but is integral to every measurement you take in NI-DAQmx. In Traditional NI-DAQ (Legacy), you configure virtual channels in MAX. In NI-DAQmx, you can configure virtual channels either in MAX or in a program, and you can configure channels as part of a task or separately.<br><br>Switch—a switch channel represents any connection point on a switch. It may be made up of one or more signal wires (commonly one, two, or four), depending on the switch topology. A virtual channel cannot be created with a switch channel. Switch channels may be used only in the NI-DAQmx Switch functions and VIs. |
| channel rate | Reciprocal of the interchannel delay. |

| | |
|---|---|
| CMOS | Complementary metal-oxide semiconductor. |
| counter/timer | A circuit that counts external pulses or clock pulses (timing). |

## D

| | |
|---|---|
| DAC | Digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current. |
| DAQ | *See* data acquisition (DAQ). |
| DAQ device | A device that acquires or generates data and can contain multiple channels and conversion devices. DAQ devices include plug-in devices, PCMCIA cards, and DAQPad devices, which connect to a computer USB or 1394 (FireWire®) port. SCXI modules are considered DAQ devices. |
| data acquisition (DAQ) | Acquiring and measuring analog or digital electrical signals from sensors, transducers, and test probes or fixtures. Generating analog or digital electrical signals. |
| DC | Direct current—although the term speaks of current, many different types of DC measurements are made, including DC Voltage, DC current, and DC power. |
| device | An instrument or controller you can access as a single entity that controls or monitors real-world I/O points. A device often is connected to a host computer through some type of communication network. *See also* DAQ device and measurement device. |
| DIO | Digital input/output. |
| driver | Software unique to the device or type of device, and includes the set of commands the device accepts. |

## F

| | |
|---|---|
| ft | Feet. |

## H

| | |
|---|---|
| hysteresis | Lag between making a change and the effect of the change. |

## I

| | |
|---|---|
| interchannel delay | Amount of time that passes between sampling consecutive channels. The interchannel delay must be short enough to allow sampling of all the channels in the channel list, within the scan interval. The greater the interchannel delay, the more time the PGIA is allowed to settle before the next channel is sampled. The interchannel delay is regulated by the AI CONV signal. |

## L

| | |
|---|---|
| LED | Light-Emitting Diode—a semiconductor light source. |

## M

| | |
|---|---|
| m | Meter. |
| measurement device | DAQ devices such as the E Series multifunction I/O (MIO) devices, SCXI signal conditioning modules, and switch modules. |
| module | A board assembly and its associated mechanical parts, front panel, optional shields, and so on. A module contains everything required to occupy one or more slots in a mainframe. SCXI and PXI devices are modules. |

## N

| | |
|---|---|
| NI | National Instruments. |
| NI-DAQ | Driver software included with all NI measurement devices. NI-DAQ is an extensive library of VIs and functions you can call from an application development environment (ADE), such as LabVIEW, to program all the features of an NI measurement device, such as configuring, acquiring and generating data from, and sending data to the device. Includes two NI-DAQ drivers—Traditional NI-DAQ (Legacy) and NI-DAQmx—each with its own API, hardware configuration, and software configuration. |

| | |
|---|---|
| NI-DAQmx | The latest NI-DAQ driver with new VIs, functions, and development tools for controlling measurement devices. The advantages of NI-DAQmx over earlier versions of NI-DAQ include the DAQ Assistant for configuring channels and measurement tasks for your device for use in LabVIEW, LabWindows/CVI, and Measurement Studio; increased performance such as faster single-point analog I/O; and a simpler API for creating DAQ applications using fewer functions and VIs than earlier versions of NI-DAQ. |
| NRSE | Non-Referenced Single-Ended mode—all measurements are made with respect to a common (NRSE) measurement system reference, but the voltage at this reference can vary with respect to the measurement system ground. |

## O

| | |
|---|---|
| OEM | Original Equipment Manufacturer. |
| offset | The unwanted DC voltage due to amplifier offset voltages added to a signal. |

## P

| | |
|---|---|
| PCI | Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It offers a theoretical maximum transfer rate of 132 Mbytes/s. |
| PGIA | Programmable gain instrumentation amplifier. |
| physical channel | *See* channel. |
| PXI | PCI eXtensions for Instrumentation—PXI is an open specification that builds off the CompactPCI specification by adding instrumentation-specific features. |

## R

| | |
|---|---|
| RSE | Referenced single-ended mode—all measurements are made with respect to a common reference measurement system or a ground. Also called a grounded measurement system. |

| | |
|---|---|
| RTSI | Real-Time System Integration—the National Instruments timing bus that connects DAQ devices directly, by means of connectors on top of the devices, for precise synchronization of functions. |

## S

| | |
|---|---|
| s | Seconds. |
| S | Samples. |
| S/s | Samples per second—Used to express the rate at which a digitizer or D/A converter or DAQ device samples an analog signal. |
| scan interval | Controls how often a scan is initialized; is regulated by the AI Sample Clock signal. |
| scan rate | Reciprocal of the scan interval. |
| SCXI | Signal Conditioning eXtensions for Instrumentation—the National Instruments product line for conditioning low-level signals within an external chassis near sensors so that only high-level signals are sent to DAQ devices in the noisy PC environment. SCXI is an open standard available for all vendors. |
| sensor | A device that responds to a physical stimulus (heat, light, sound, pressure, motion, flow, and so on) and produces a corresponding electrical signal. |
| signal conditioning | The manipulation of signals to prepare them for digitizing. |

## T

| | |
|---|---|
| task | NI-DAQmx—a collection of one or more channels, timing, and triggering and other properties that apply to the task itself. Conceptually, a task represents a measurement or generation you want to perform. |
| terminal count | The highest value of a counter. |
| $t_{gh}$ | Gate hold time. |
| $t_{gsu}$ | Gate setup time. |
| $t_{gw}$ | Gate pulse width. |

| | |
|---|---|
| $t_{out}$ | Output delay time. |
| Traditional NI-DAQ (Legacy) | An upgrade to the earlier version of NI-DAQ. Traditional NI-DAQ (Legacy) has the same VIs and functions and works the same way as NI-DAQ 6.9.*x*. You can use both Traditional NI-DAQ (Legacy) and NI-DAQmx on the same computer, which is not possible with NI-DAQ 6.9.*x*. |
| transducer | *See* sensor. |
| $t_{sc}$ | Source clock period. |
| $t_{sp}$ | Source pulse width. |
| TTL | Transistor-transistor logic—a digital circuit composed of bipolar transistors wired in a certain manner. A typical medium-speed digital technology. Nominal TTL logic levels are 0 and 5 V. |

## V

| | |
|---|---|
| V | Volts. |
| $V_{cm}$ | Common-mode voltage. |
| $V_g$ | Ground loop voltage. |
| $V_{IH}$ | Volts, input high. |
| $V_{IL}$ | Volts, input low. |
| $V_{in}$ | Volts in. |
| virtual channel | *See* channel. |
| $V_m$ | Measured voltage. |
| $V_{OH}$ | Volts, output high. |
| $V_{OL}$ | Volts, output low. |
| Vs | Signal source voltage. |

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